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Hardware Logic for the Selection and Analysis of Events Observed in Charpak-Chamber and Counter Experiments

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Summary:

The general organisation of a system using standard integrated circuits in simple configurations is described. Emphasis is given to the use of shift registers for sequential pattern recognition operations.

1. INTRODUCTION

Data handling for accelerator experiments have improved substantially during the last few years. Usually a set of counters is connected to a fast electronic system which "triggers" devices like spark chambers giving detailed information of an event. All the data are then transferred to an "on-line" computer which performs logic and mathematical operations and eventually stores data and results on a permanent medium (like tapes). The rate of events is limited by the spark-chambers, by the computer capabilities and by the permanent storage system.

The use of proportional wire chambers makes it possible at present to obtain a much higher rate of events from the apparatus. The computer and the storage systems however, have not been substantially improved. In order to take full advantage of the capabilities of proportional wire chambers it is necessary that the events (which may include huge amounts of background) undergo some preliminary analysis in a faster electronic system interposed between the detector and the computer.

In the present note we give some examples of fast ($\sim$ 1/2 μs) and medium ($\sim$ 100 μs) speed electronic devices which may be used for such "pre-computer" analysis of events. It will be shown that many specific geometrical criteria for the selection of events and for the rejection of background can be taken into account. Another interesting feature of these devices is that they can performe at high speed operations for which conventional computers are not particularly well prepared.

The possibility of a hardware preanalysis of the events is closely related to the geometrical configuration of the wire-chambers and counters used in the experiment. Therefore all circuits must be discussed in connection with concrete wire configurations.

In the following sections we illustrate several cases of electronic logic with examples which are familiar to us. There is no aim of completeness in this.

2. PARALLEL AND SEQUENTIAL LOGIC

Logical requirements between wires and counters can always be expressed in terms of AND, OR and INVERT operations associated with some timing conditions. This can be done in a straightforward way by connecting all wires and counters (data lines) directly to the logical circuits associated to them. All circuits work simultaneously and an eventual acceptance condition for an event is obtained in the shortest time allowed by the propagation delays. This is what is generally indicated as fast parallel logic.

The size and cost of such a system will grow with the number of data lines, in strong dependence on the complexity of the wanted logical operation. A simple example is the determination of both the angle (θ) and origin (z) of tractes in a system of two wire chambers and a segment "source". In the sketch shown in Fig. 1a there will be 10 possible values of z and for each of them 5 possible values of θ. In parallel logic the fast determination of z and θ will require 10x5 coincidence circuits: The product of the number of intervals of the two resulting variables determines the number of identical circuits of the system. It is a bidimensional problem. In the following sections we will discuss cases with hundreds of channels per dimension and even with a larger number of dimensions. It is practically impossible to construct such systems using the technology available at present. As a rule, we will only consider as candidates for parallel logic, systems which can be considered as "unidimensional", in which only one output variable is requested. In the case of Fig. 1a we may either look for z or for θ; the other one should be known a-priori.

A different approach to the problem consists in applying the coincidence condition in sequence to all the data inputs using only one logical circuit. A reduction in the number of dimensions is obtained by spending a much longer time to obtain the result. The sequential interrogation of all concerned input channels can be performed by different means (gate combinations etc). In Section 4. we describe a method in which the whole array of data is shifted through the single logic circuit. The position at which the logical condition is satisfied is obtained from the number of "shifting steps" performed. In some cases the shift operation can be easily understood and corresponds to translations and rotations of the event. In the example of Fig. 1a we obtain a reduction to one dimension by means of a translation of the event along the z axis. Only 10 Θ-coindicendes are needed to identify a track as it is shown in Fig. 1b. The z coordinate is given by the number of translation steps needed to obtain the Θ-coincidence.

The system can even be reduced to dimension zero introducing a rotation. This consists in shifting the upper wires twice as fast as the lower. This is a rotation of an eventual "track" around a fixed z-point. We now need only one coincidence circuit as it is shown in Fig. 1c. Both, z and Θ are obtained counting the number of translation- and rotation-steps needed to obtain a positive answer from the single logical circuit.

In section 3.1. we will see that the definition of directions can not be done using simple coincidences, as it was assumed in the example of Fig. 1. Therefore economy considerations will be of great importance.

3. FAST TRIGGER CIRCUITS

3.1 Telescope Arrangements

The definition of directions by means of telescopic arrangements ("tracks" of charged particles) is of interest in many experiments. The size of the source of tracks and the smallest component of the telescope define a certain acceptance. The telescope in itself must have a somewhat higher angular acceptance if losses at the borders should be avoided. As a result, adjacent telescope may overlap in certain regions. These are well known techniques used for counter hodoscopes. The effect of multiple scattering and the eventual curvature of the tracks in a magnetic field is taken into account by increasing the acceptance angle.

In Fig. 2 (a, b and c) we show some examples of telescope arrangements together with the required circuits. More complicated telescopes can be constructed for curved tracks or for tracks not originating in the source region (scattering or decay). Some examples will be given in Section 4.

As it was already shown in Section 2. telescopes for the determination of angles can be used in parallel, building many identical circuits, or in sequence, applying some shifting technique and using a single telescope circuit.

3.2 Angular Selection

The AND-function between two groups of telescopes defines a correlation which can be used for event selection purposes. The fundamental circuits (for a symmetric case) on a circle are shown in Fig. 3. Each sector represents a group of telescopes in "OR"-connection. The output C means that there was at least one track in each one of the sectors. The sketched example is a kind of rough collinearity test.

In order to perform the test over the whole circle one must repeat the same diagram in convenient angular positions. In Fig. 4 we show an example in which 6 pairs of 120°-sectors cover the whole circle. The OR-function of the 6 outputs has some particular properties:

a) events in which all tracks are concentrated in a single 30°-sector will never give a positive output;

b) events which can not be covered completely with a 60°-sector will always provide a positive answer;

c) events giving a positive answer have at least two tracks;

d) events not included in category a) or b) are detected with variable efficiency.
This type of circuit will be discussed in connection with background rejection criteria in Section 5.

A simple symmetry condition can be checked extending the sectors to 180° (momentum conservation). There must be at least one track on each half circle. If such a condition should be checked at many different orientations it can be done rotating the event in a sequential logic system.

3.3 Majority Coincidences, Counting

The problem consists in determining the number of logical "1"-s present in a long array of data. The obvious solution consists in counting them. This is a sequential operation requiring quite a long time. A parallel digital solution would consist in a kind of encoder which would use a pyramide-system of adders. This may be too complicated or slow for some applications.

An analog circuit which accepts many digital input lines and provides within $\sim$ 50 ns an answer regarding the number of "1"-s can be built attaching a precision current generator to each input line and sending the resulting total current into an operational amplifier as is shown in Fig. 5. The output of the ampli-

fier must be compared with fixed D.C. levels or sent into a window discriminator in order to obtain the numerical informations required. For a reliable and stable circuit the accuracy is limited to ∿ 10 output channels when ∿ 200 input lines are interrogated[1]. This type of circuit can be very useful for selection purposes.

Some interesting logical condition can be applied to the input lines of the described "counter", i.e. the requirement that contiguous "1"-s should be counted as only one (cluster counting). A simple circuit for this operation is shown in Fig. 6. It must be noticed that there is an anticoincidence in this circuit and therefore timing considerations are essential.

3.4 Timing Problems

The input signals for the fast trigger logic are not perfectly synchronized, mainly due to the time jitter of the proportional wires. Further uncertainties are added by the integrated circuits used. Careful timing is therefore of greatest importance.

All circuits described in Sections 3.1 and 3.3 are of the "coincidence"-type (DC-coupled) and therefore standard overlapping criteria can be applied. The element with best time resolution (in general a plastic scintillator) should dominate and must be overlapped by the other signals arriving to the AND gates. These coincidence circuits give the fastest logical information about the events and their outputs can be combined to form a timing strobe for slower analog and anticoincidence circuits such as those described in Section 3.3. We will call this timing strobe the "pre-trigger". In general the pre-trigger will correspond to a very low level logical requirement, as for instance: "at least one track" (= OR-function of all direction telescopes). The rate of such a low-level pre-trigger is an essential information to

establish whether the whole logic system is overcrowded (too high input-rates from the apparatus). Using normal integrated circuits the pre-trigger can be obtained within a few hundred nanoseconds (part of this delay is due to the overlapping problems arising from the use of proportional wire chambers). The rest of the trigger information (mainly analog counters strobed by the pre-trigger) can be checked within another few hundred nanoseconds in order to establish whether the event can be accepted. For rejected events (and most of the pre-trigger must be rejected) the total dead-time is of the order of 1/2 microsecond. This means that a rate of $\sim 10^5$ pre-trigger per second is still tolerable (5 % loss).

Apart from strobing all trigger functions we have found it practical to perform several other operations with the pre-trigger pulse. It is used to set the master flip-flop for the "busy"-condition of the system. Rejection (or end) of an event consists simply in presetting this master flip-flop. Since the pre-trigger strobes all other functions, the "busy"-condition needs only to be applied to itself.

Also the memorization of all input-data (Charpak-Chamber wires and counters) is strobed by the pre-trigger. The rate at which this happens is still compatible with economic memory fli-flops and there are several interesting advantages when compared to a memorization with the "final" lower rate trigger:

a) as long as the pre-trigger condition is not changed the timing of the memorization process is kept constant;

b) the final trigger condition can be arbitrarily changed (see also the last observation of this Section);

c) the prompt arrival of the pre-trigger allows the use of the shortest delay for the wire chamber signals; This reduces the dead-time per wire and simplifies the construction of the delay ONE-SHOTS (200 ns are possible);

d) the static outputs of the data flip-flops can be used for fast trigger operations.

The final trigger obtained from the fast parallel logic in $\sim$ 1/2 μs starts the next step in the analysis of the event. It may also be used as trigger for spark chambers or similar devices. However, if no such devices must be triggered, there is no compulsory limit for further logical operations and it is interesting to notice that the time needed for each event to be sent to the next analysis needs not to be constant. In the example of Section 3, Fig. 10, a diagram is shown which illustrates the trigger operations.

4. SEQUENTIAL SHIFTING TECHNIQUE

4.1 Principle of Operation and its Arithmetic Equivalent

In the very moment an event is to be sent to the "sequential" logic, all the original data and, for convenience, also the information obtained in the fast analysis, should be available in a flip flop memory. The first step consists in transferring a part of or all the information into special registers able to perform the operations required for the sequential logic. (In some special cases the same memory flip-flops of the fast logic may be used as such registers.)

We will discuss here operations which can be performed using shift-registers. These are cheap and compact commercial circuits with very high reliability. An array of binary data can be accepted in ∿ 20 ns by these registers using the parallel inputs of the single flip-flops. Furthermore the full array can be shifted forwards or backwards at a rate exceeding 10 MHz. The parallel outputs are available to perform logical operations in the time between two shifts. This corresponds to the logic discussed in Section 2.

The procedure is equivalent to the sequential use of subroutines in a computer. For example: a "direction look-up" or "coincidence" subroutine would be fed with the measured coordinates in a loop in which at every turn the input data are incremented by one interval. The operation of adding one to all coordinates is equivalent to the "shift-one" order in our sequential logic. The "shift-all" operation requires less than 100 ns to be done, the "add one to all" takes at least a hundred times more time in the computer. In many cases the equivalent to the subroutine is a fast parallel logic requiring ∿100 ns for its execution. This gives further time advantages with respect to the computer.

In a hardware shifting system the data can be compared simultaneously with several different wired configurations. New configurations can be added in a later stage. Counting and memorization processes are performed at the same time.

An interesting development would consist in establishing the "pattern" (with which comparison is made at each shift) by means of external levels defined by switches or by a computer. For simplicity we will assume for the following considerations that the "patterns" are made of fixed wired OR-AND-OR combinations similar to thosealready used in fast parallel logic.

4.2 Unidimensional Applications

The definition of directions which was already shown in fast parallel logic can be performed shifting an event seen in cylindrical chambers[2] around its axis, i.e. turning it. The one-direction-coincidence telescope needs to be wired only once. In the case of curved or scattered tracks several differently shaped directions can still be wired and recognized. In one turn of such a system the number of tracks of each wanted shape can be counted and eventually each one recorded. Wires with signals can be simultaneously counted without difficulty. Defined angles can be easily recognized by wiring two directions at convenient points. Coplanarity or non-coplanarity can be defined.

Another interesting operation which can be performed in a single rotation is the registration of all data in a compact buffer memory. This works as a derandonizer for fast sequential block transfer to a computer.

Particularly interesting is the recognition of decay products of instable particles like $K^{o} \rightarrow 2\pi$ or $\Lambda^{o} \rightarrow P + \pi^{-}$. These particles do not necessarily come from the source and would not be seen by the fast direction logic. The rotating device compares the data with their characteristic decay patterns.

Some wiring examples are given in Fig. 7.

4.3. Spatial Reconstruction, Ambiguity Resolution

For this section we will consider a system of wire chambers or hodoscopes which provides three coordinates of the crossing point of a particle through a surface. Three Charpak-chambers with wires at different angle can provide such information. One can also read out the negative electrode divided in stripes[3] as it is shown in Fig. 8. A similar geometry can be obtained on cylindrical surfaces. Each "crossing point" is then given by one wire and two symmetrically located stripes. The stripes are treated as wires from the point of view of storage and shifting.

In a plane chamber the coordinate along the wire (Z) can be determined as a threefold coincidence between a wire and two stripes as it is shown in Fig. 9. The eventual ambiguity due to the presence of other tracks is removed. Since the wiring for all possible Z coordinates on all wires is quite complicated it will be convenient to make it only once and to shift wires and the corresponding stripes through the system. When an activiated wire is found the Z-coordinate is present at the output of the threefold coincidences. The number can be easily coded if necessary. One must notice that the stripes and wires must be either the same number or a multiple of each other in order to make simultaneous shifting possible.

Now we introduce a second shifting operation which constists in shifting the top stripes to the left and the lower stripes to the right. This movement is equivalent to a TRANSLATION of the whole even along the Z-axis. Any logic combination made on the Z outputs (like directions) can be checked with the event moving along Z. Obviously we could have used stripes or wires at 90° which would allow equivalent operations with simple Z-shifts, but ambiguities would not be solved.

Let us now go to a system of several chambers. The translation can be used to find the Θ-angle and simultaneously the origin of tracks as was already shown in Fig. 1. All these considerations can be applied to cylindrical wire chambers with stripes (the practical advantage of inclined stripes is not only the ambiguity resolution but also the fact that all stripes and wires are read-out at the ends of the cylinders). The sequence of operations to get ϕ,Θ and Z is then

a) rotate the whole system until a wire coincidence is found (number of shifts = ϕ-angle);

b) translate the event until a full wire-stripes-coincidence is found. The number of translation-shifts gives the Z-coordinate of the origin of the track; the Θ-angle should be wired and there is one output for each possible Θ-interval.

The ϕ,Θ,Z combinations can be memorized for later use in software analysis. This information is very useful even if several different combinations are found for a single track (wire or stripe clusters etc) or in the case of crossing tracks and background.

If the origin of tracks is known (point source) the translation is not necessary and the coincidence of wires (ϕ-angle) should correspond to a coincidence of stripes giving the Θ-angle.

The cylindrical chambers which were assumed for these last considerations must be built taking into account some geometrical restrictions. This becomes clear when we consider the definition of directions in plane chambers, as was shown in Fig. 2b. The crossing points of our diagonal stripes have the same problems. Simple relations of stripes- and chamber-spacing must be requested.

5. EXAMPLE OF A COMBINED SYSTEM

Fig. 10 shows how the data can be analysed in successive stages of increasing accuracy. The indicated time limitations are imposed by the type of integrated circuits used. This simplified diagram emphasises the logical interconnections which, in a real system will be geometrically distributed in a very different way.

The functions performed in each section of the logic depend on the type of events to be selected. Background rejection can be a very different problem in each experiment.

In Fig. 11 we show a very simple set-up composed of 2 cylindrical Charpak-chambers[2] with negative electrodes divided in transversal stripes[3]. The events expected in this set-up are sketched in Fig. 12. The possibilities of a hardware logic of very modest dimensions are shown in Fig. 13. The main parts of this electronic system have already been tested[4]. It is considered as a prototype for similar devices to be used in storage ring experiments.

Substantial progress is expected in this field in the near future. More circuits must be designed and tested and additional external controls must be added.

ACKNOWLEDGEMENTS

We like to thank many of our collegues for enlightening discussions, in particular Drs. S. Prünster, V. Valente and R. Visentin. We enjoyed the collaboration with Messrs. Heinsch, Kratzart, Neff, Nicoletti, Schultz and Sommer in building and testing several of the devices given as examples in this report.

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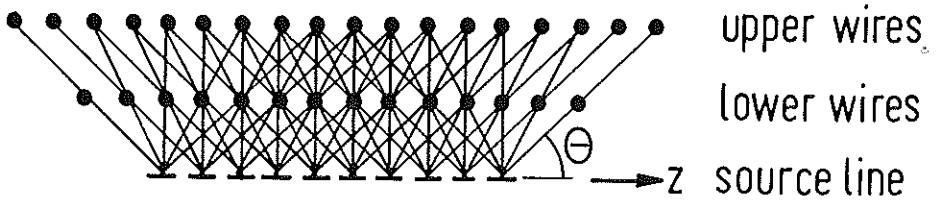
(1) N. Neff, circuit built at group F56 of DESY

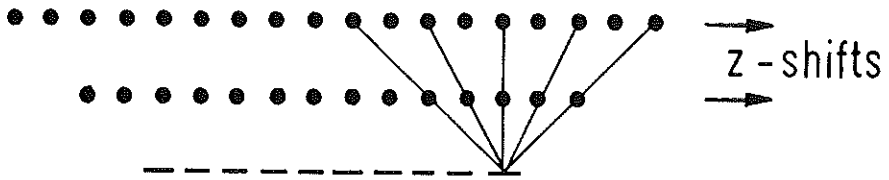
(2) J. Heinsch, Diplomarbeit, Hamburg, to be published

(3) G. Fischer and I. Plch, CERN Preprint Nov. 1971
S. Prünster, DESY, private communication

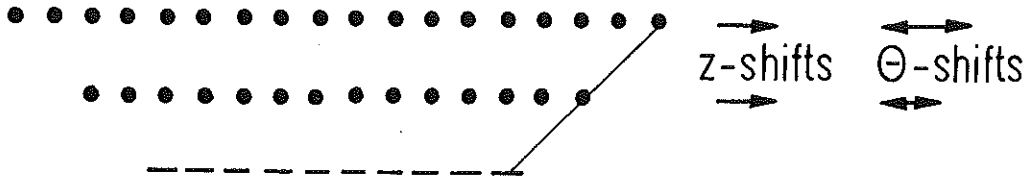
(4) K. Sommer, Diplomarbeit, Hamburg, to be published



a) Bidimensional logic : 50 circuits

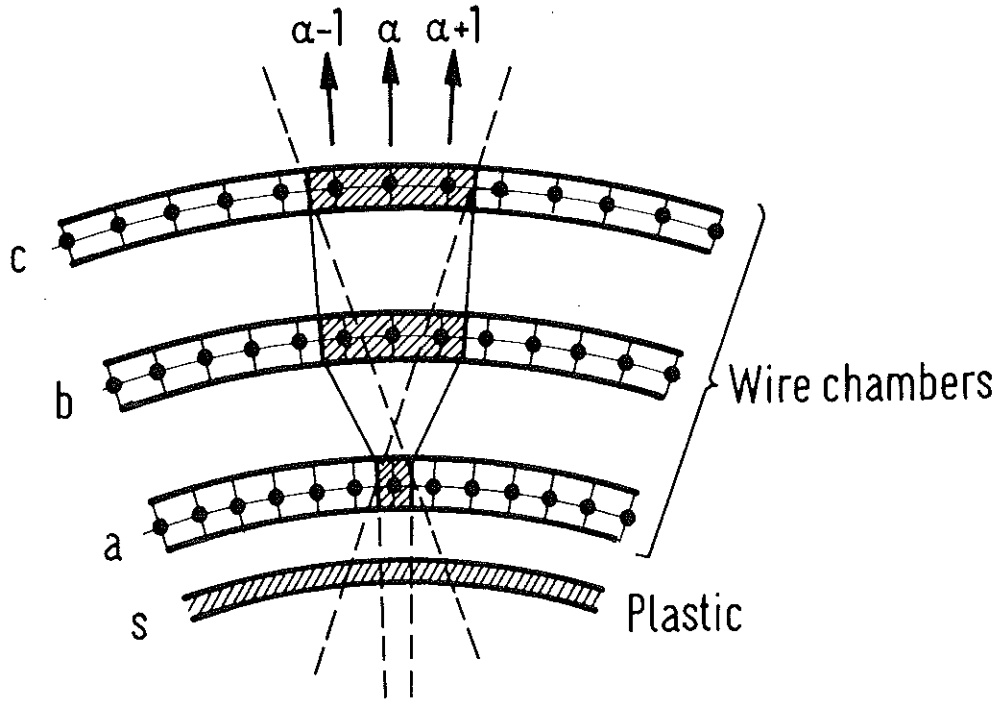


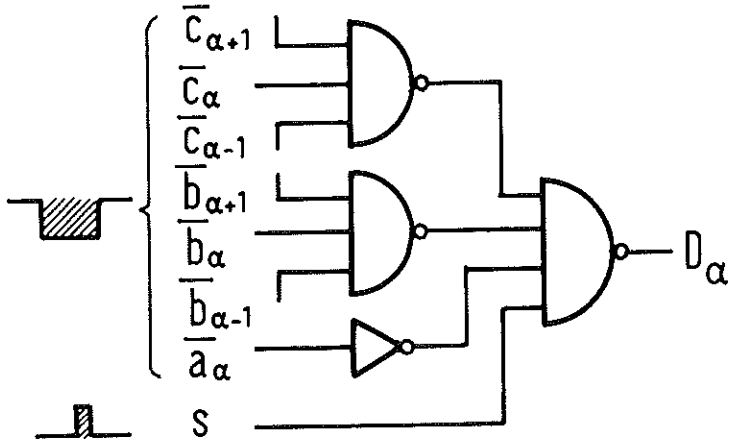
b) Undimensional logic : 5 circuits



c) Zero-dimensional logic: 1 circuit

Fig.1 Parallel and sequential determination of Θ and z.
Each full line corresponds to a coincidence circuit.





$$D_\alpha = s \cdot a_\alpha \, (b_{\alpha-1} + b_\alpha + b_{\alpha+1}) \cdot (c_{\alpha-1} + c_\alpha + c_{\alpha+1})$$

(circuit shown in NAND-logic)

Fig. 2a

Example of a telescope for the direction D made with three cylindrical Charpak chambers and one plastic scintillator.

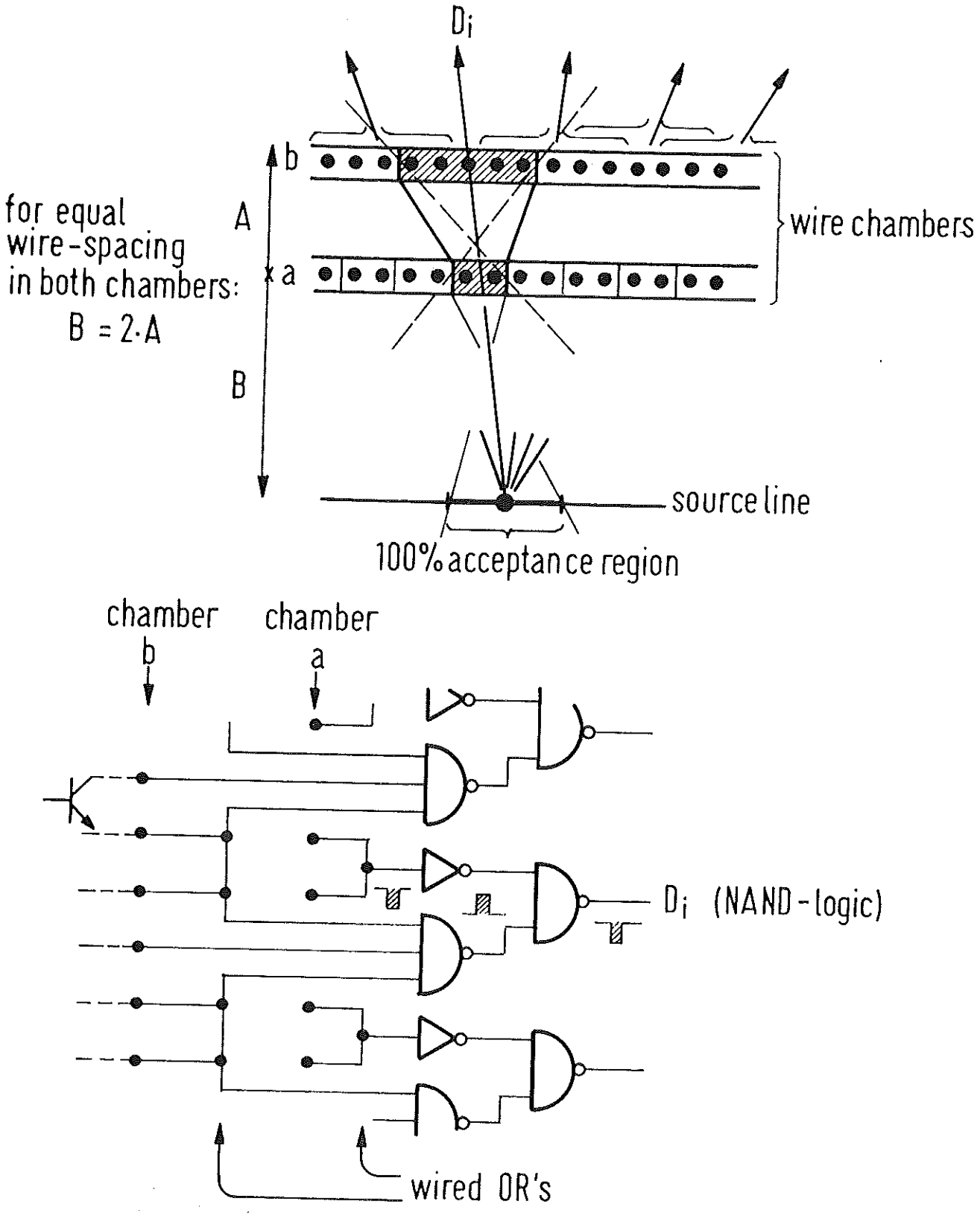
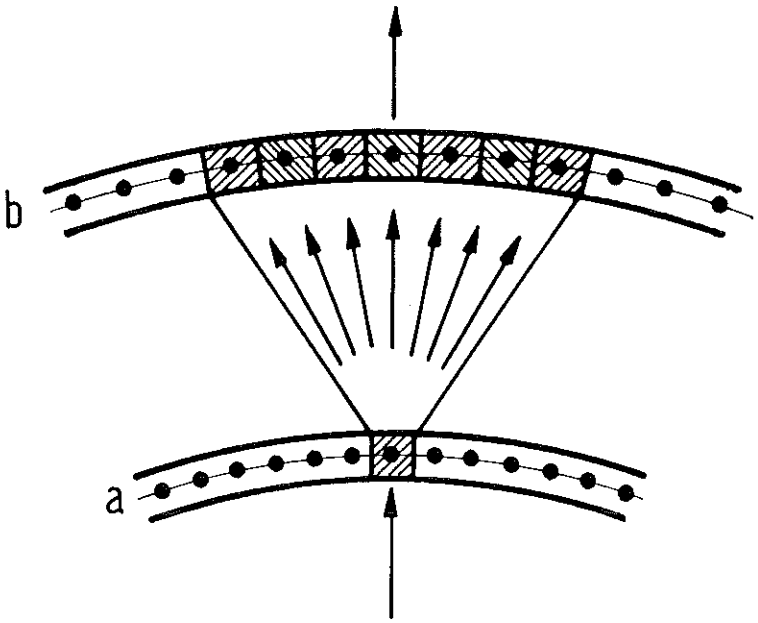


Fig. 2b

Example of a telescope for flat chambers. A system of 48 such telescopes is working at ADONE.



Circuit for "variable" telescope, NAND - logic

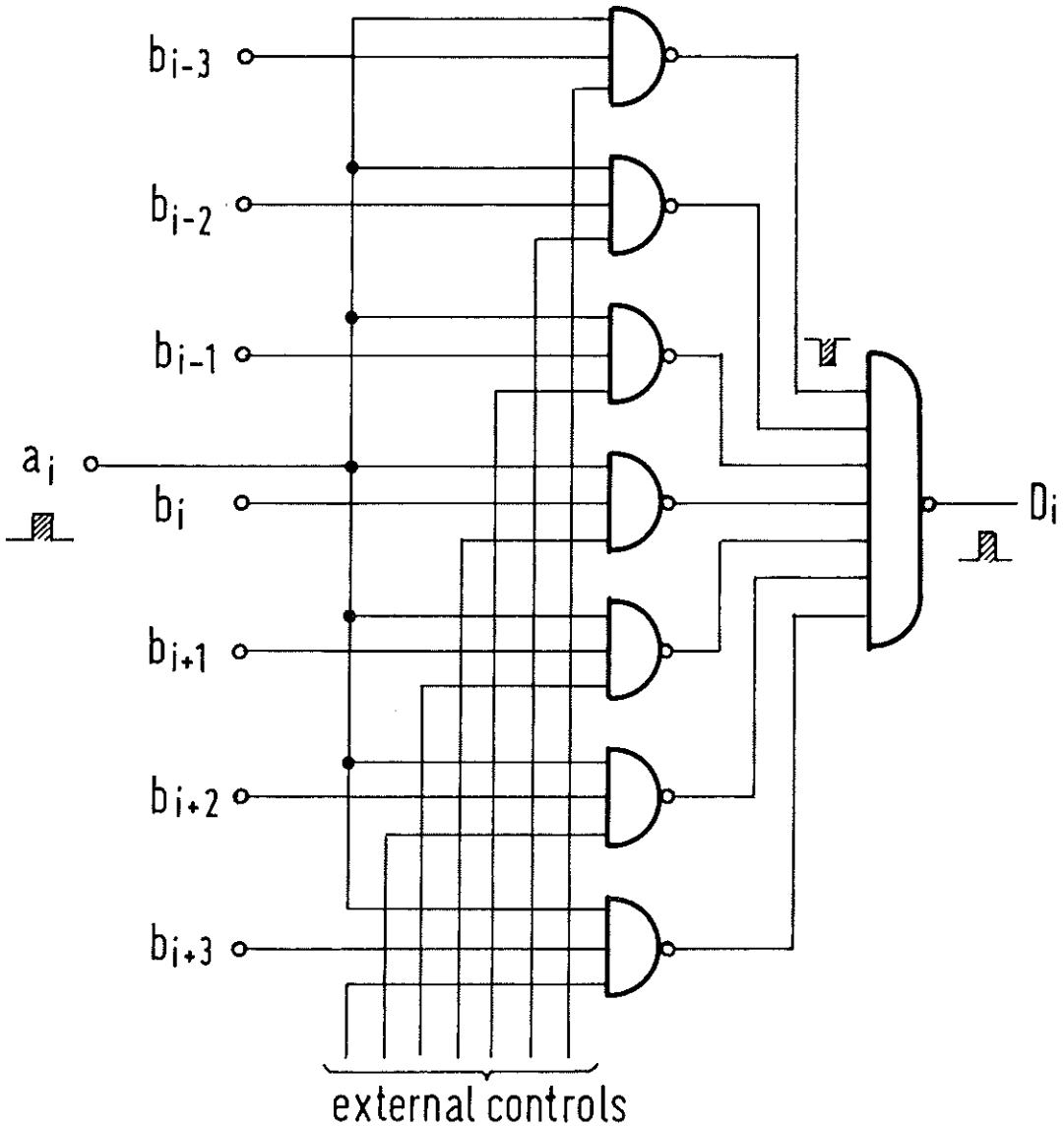
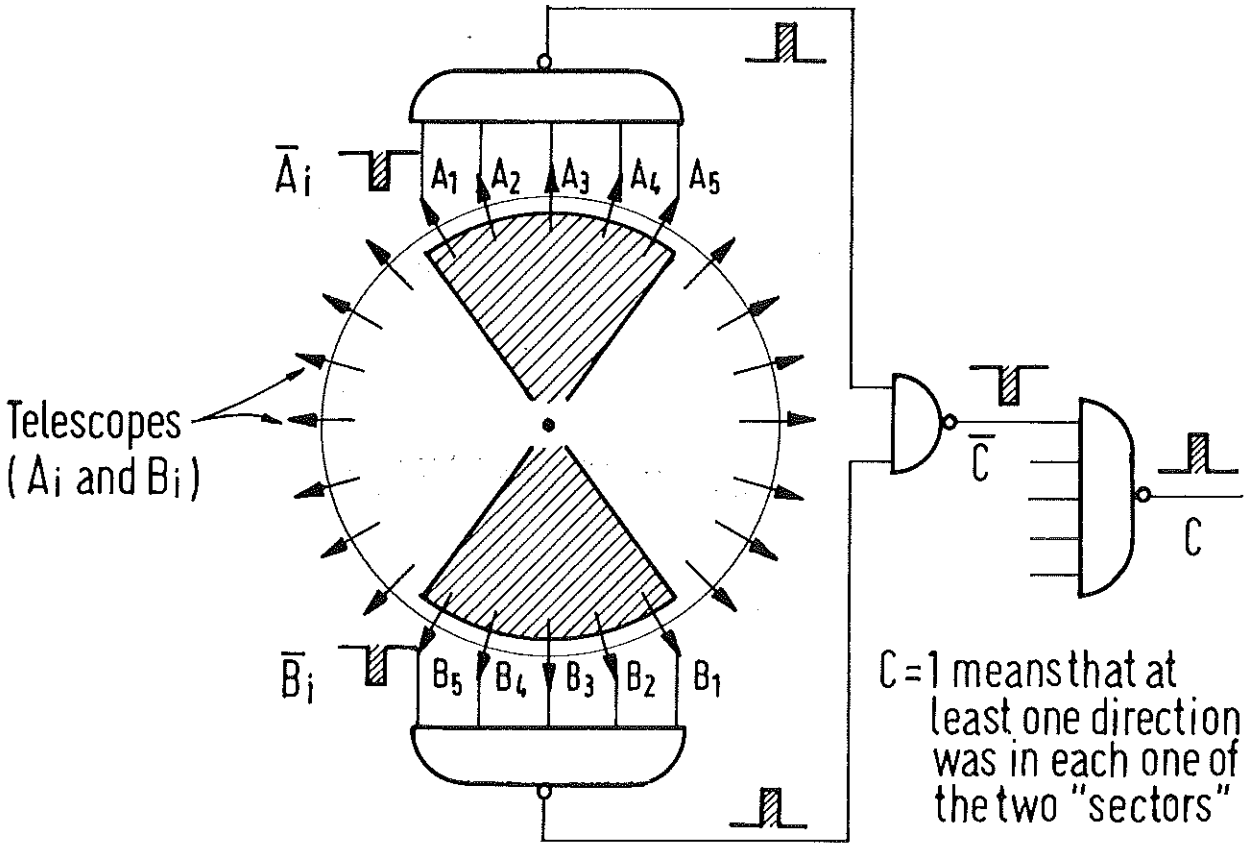


Fig.2c

A system in wich the acceptance of the telescopes can be externally controlled (7 intervals)



The "OR-AND-OR" logic performed with NAND Circuits

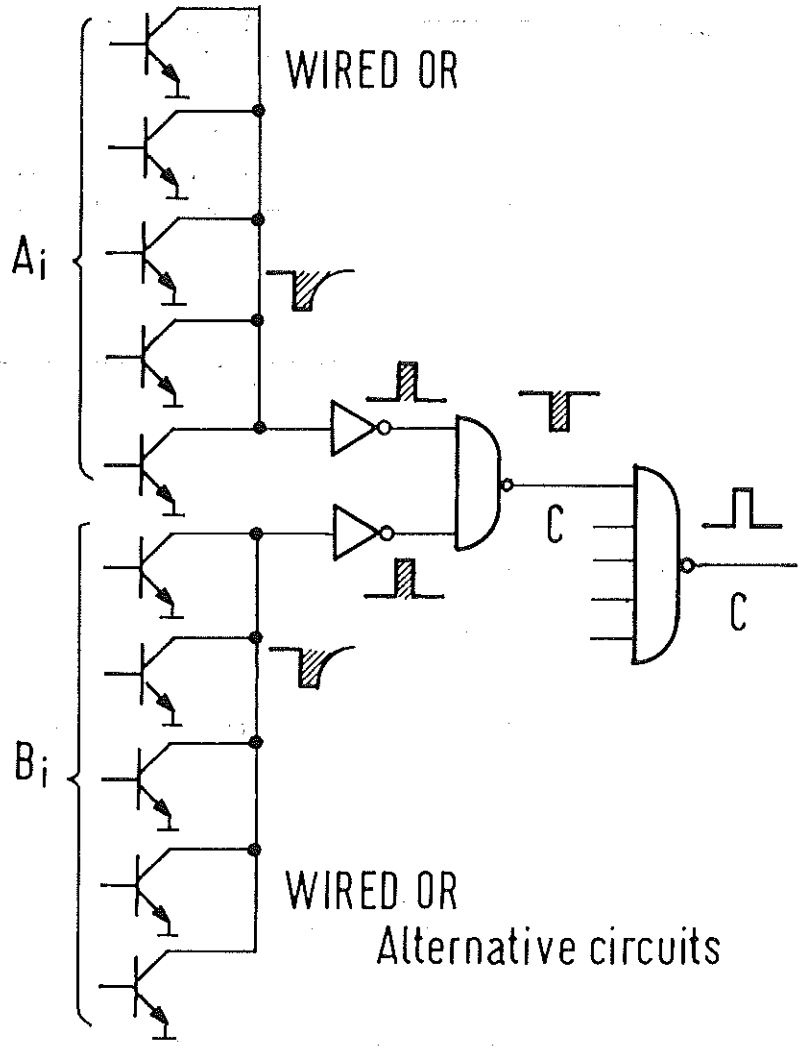


Fig. 3
Principle of circuits for angular correlation

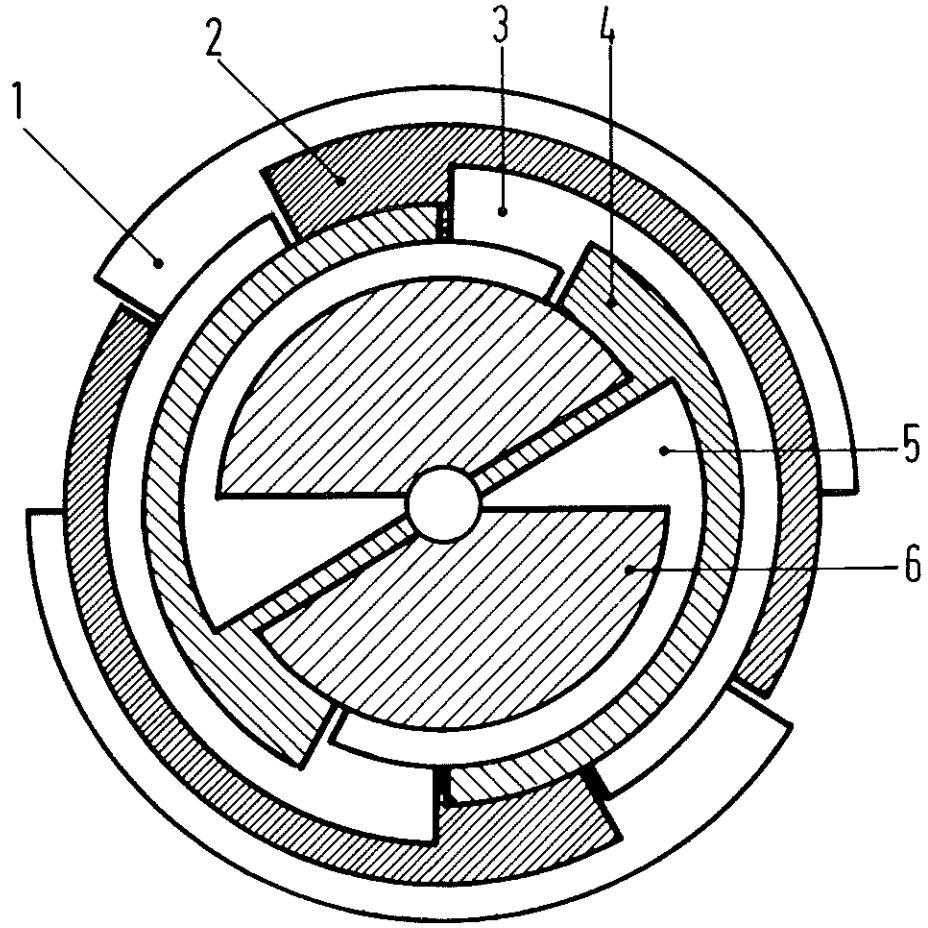


Fig.4

Combination of 6 correlation circuits (Fig.3), each of them covering two 120°-sectors.

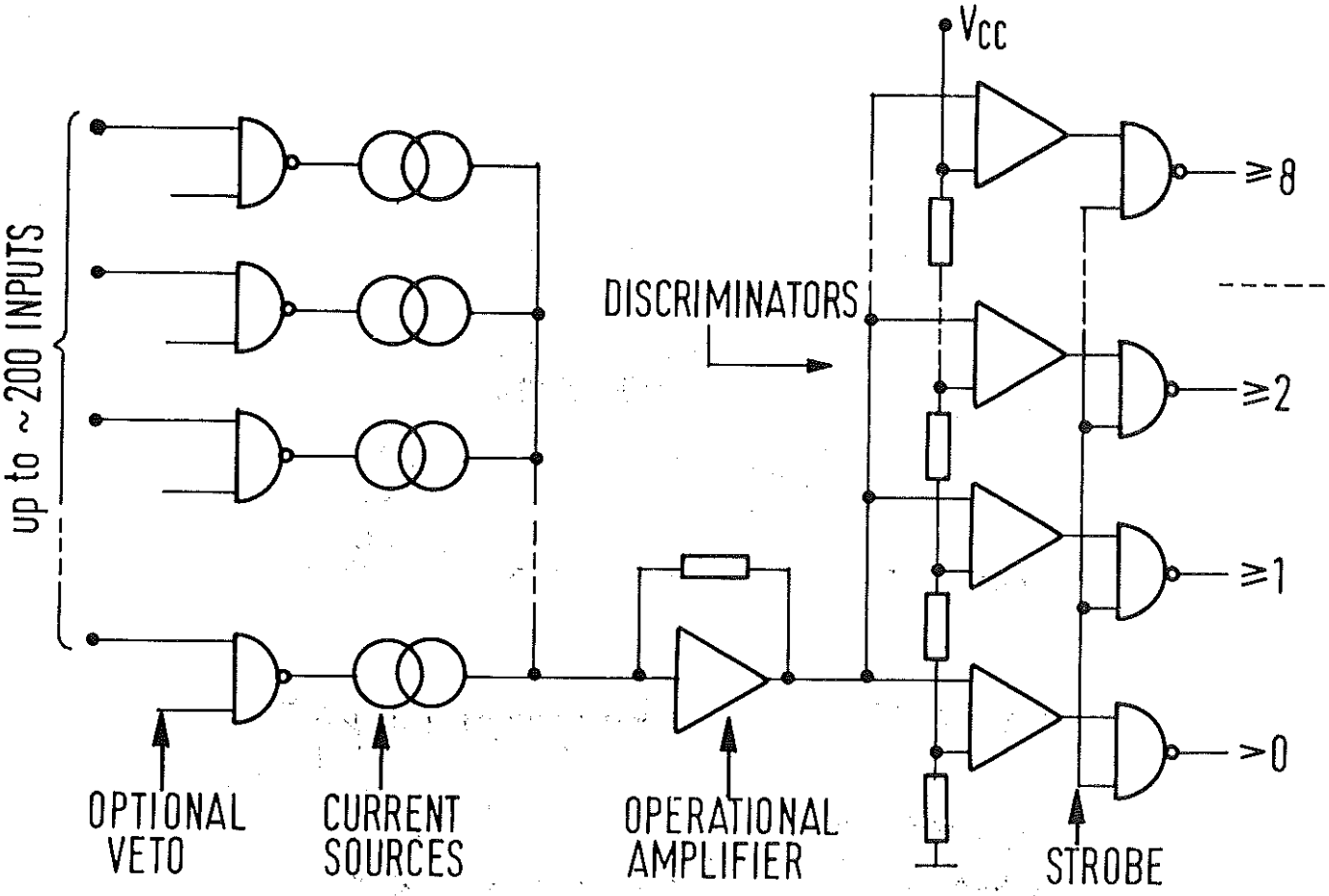
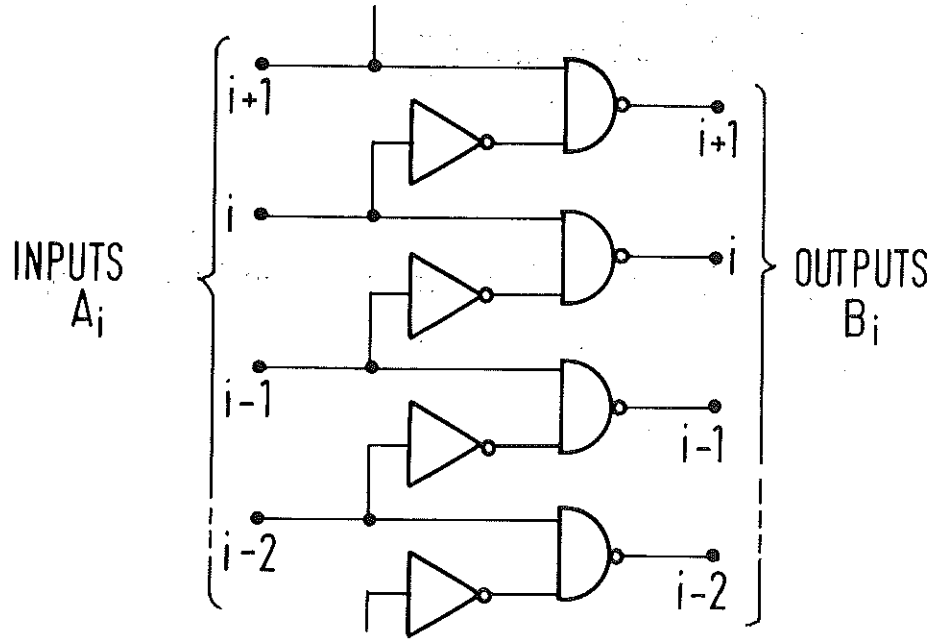


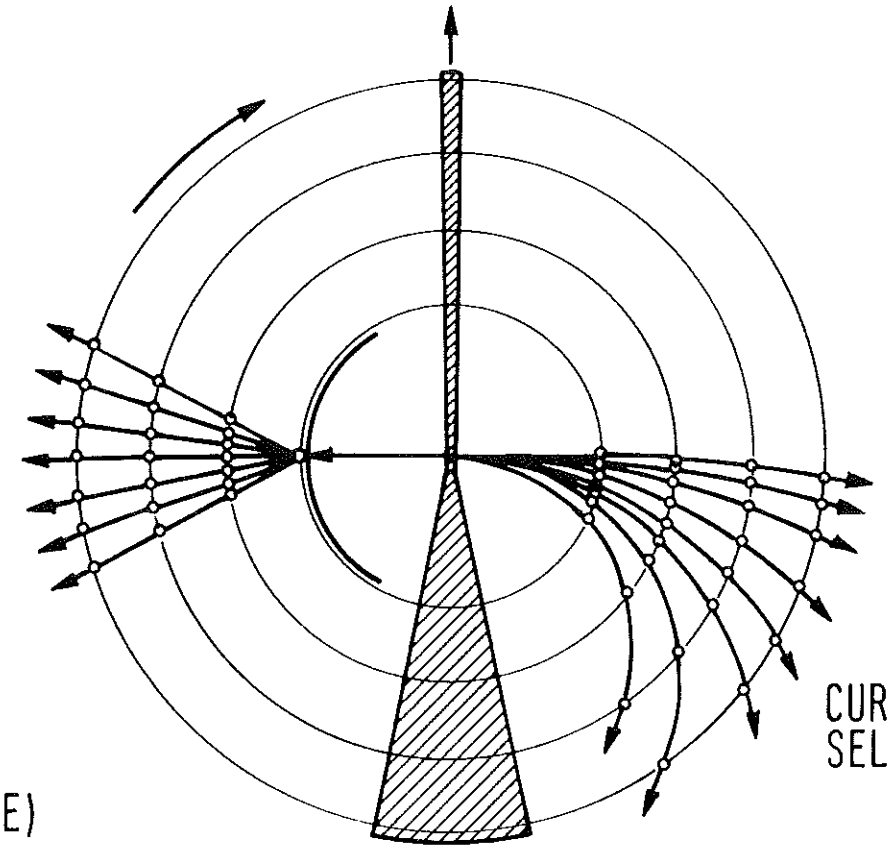
Fig.5 A possible circuit for a majority coincidence or fast "counter".



A_i	A_{i-1}	B_i
0	0	1
0	1	1
1	0	0
1	1	1

Fig.6

Cluster Condensation



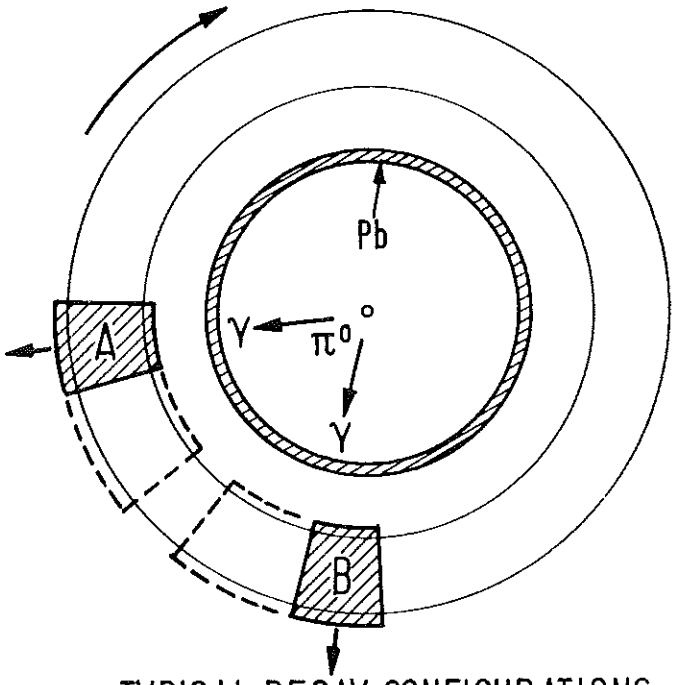
MULTIPLE SCATTERING IN A WALL (NO CURVATURE)

CURVATURE SELECTION

COPLANARITY SELECTION

The "event" is rotated 360° and compared with fixed, wired configurations, like those sketched in the Figures.

Similar configurations can be made for flat chamber systems.



TYPICAL DECAY CONFIGURATIONS (ONLY IN ONE PROJECTION)

Fig.7

Examples of pattern comparison in sequential logic

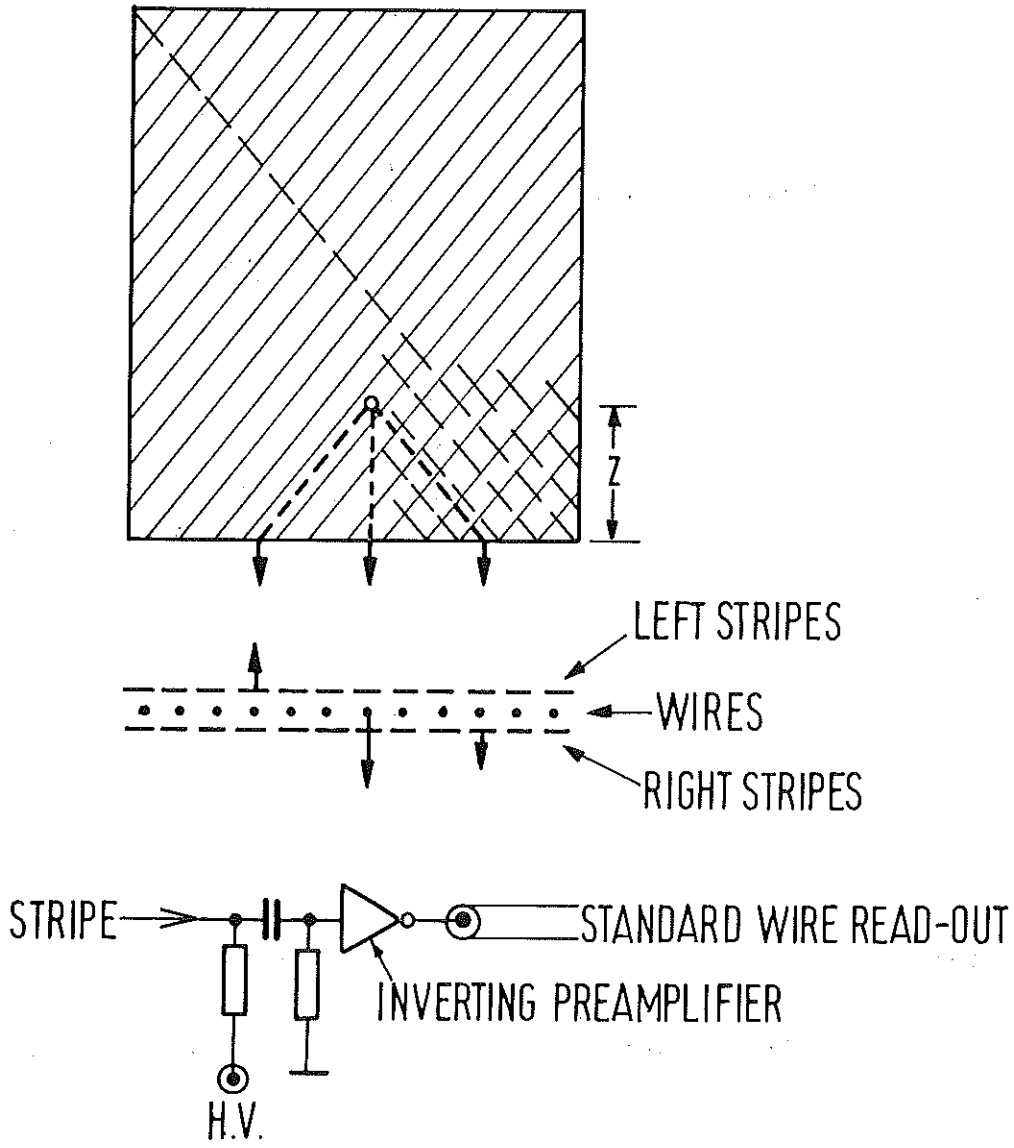


Fig.8
Charpak-chamber with negative electrode read-out.

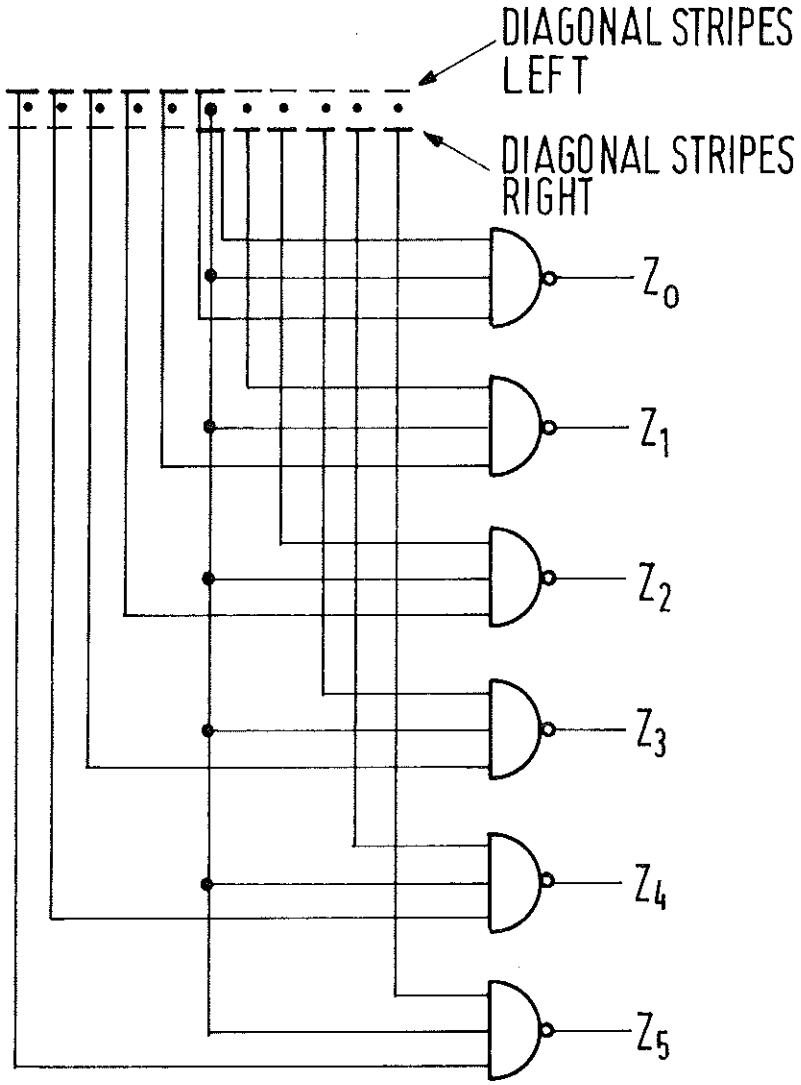


Fig.9

Circuits for the coordinate along one wire

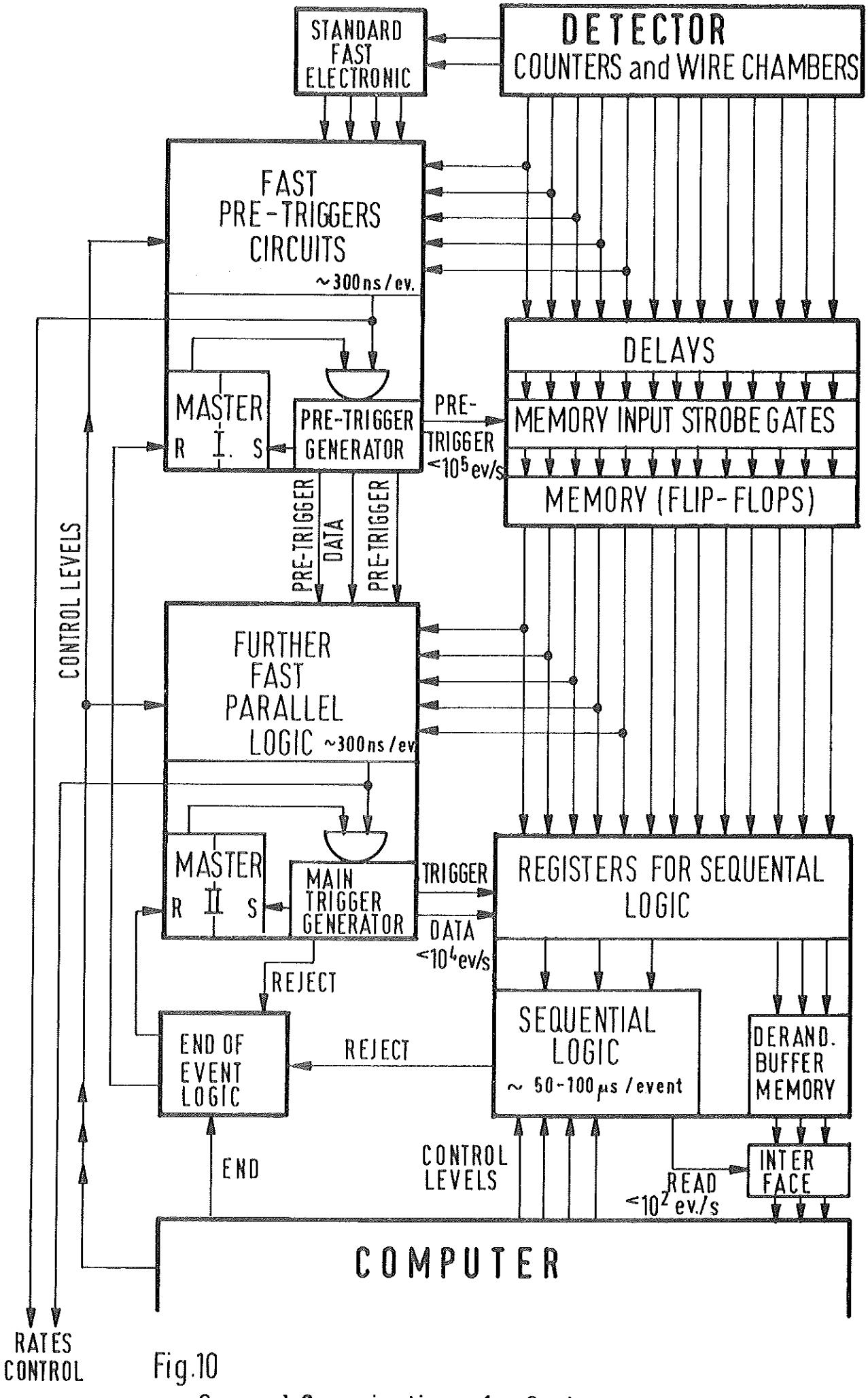


Fig.10

General Organisation of a System

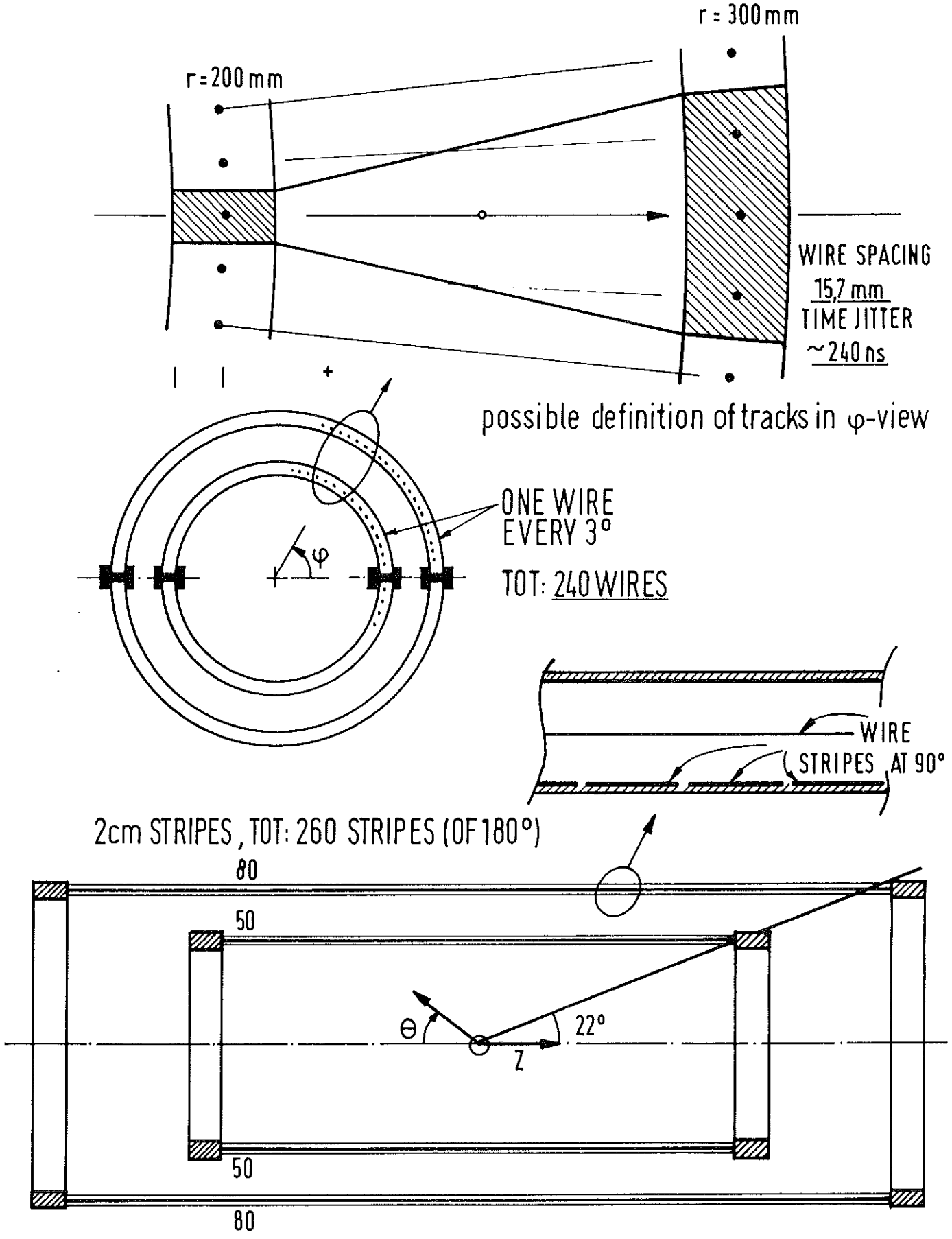
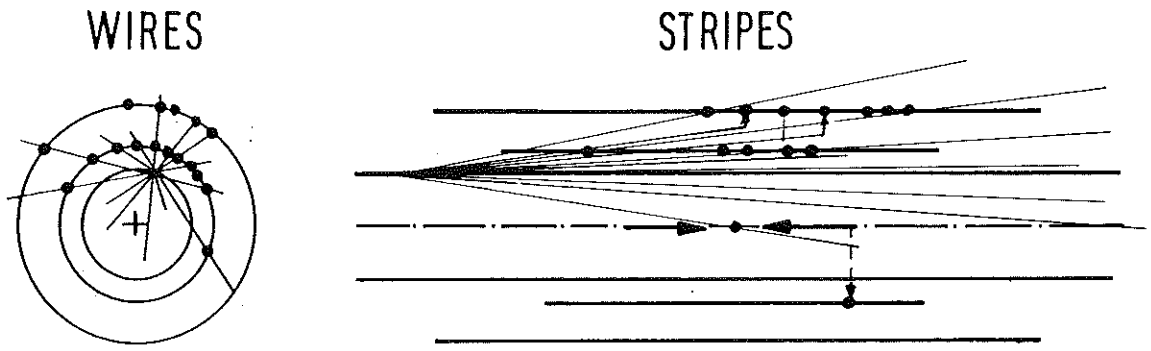
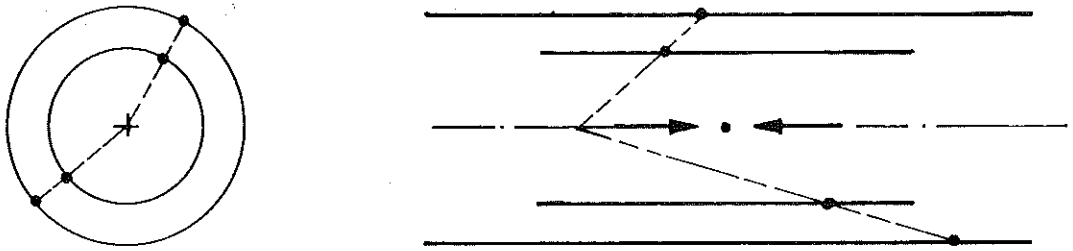


Fig.11

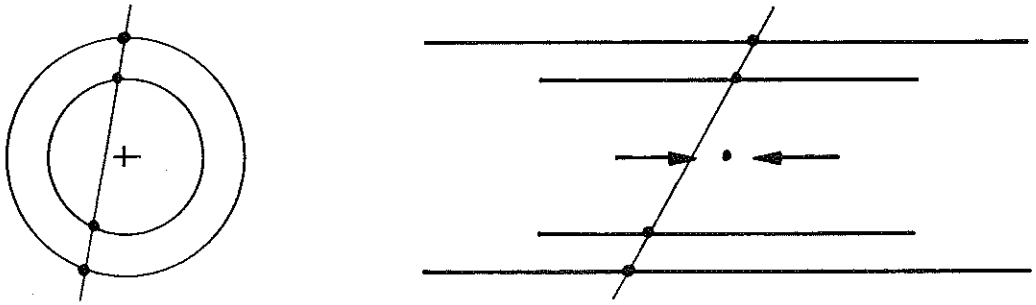
A simple cylindrical set-up using 500 amplifier.



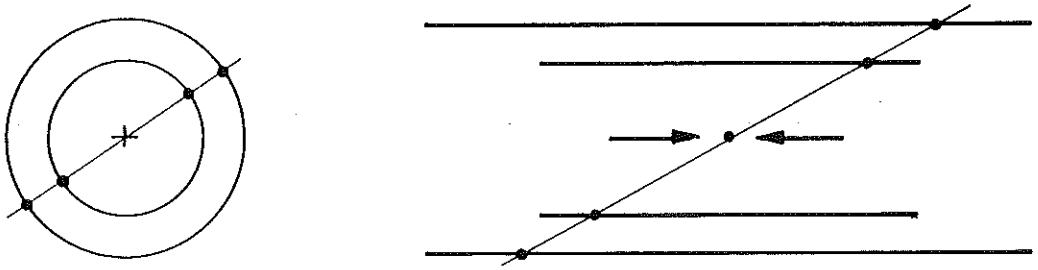
a) shower orginated in the vacuum tube



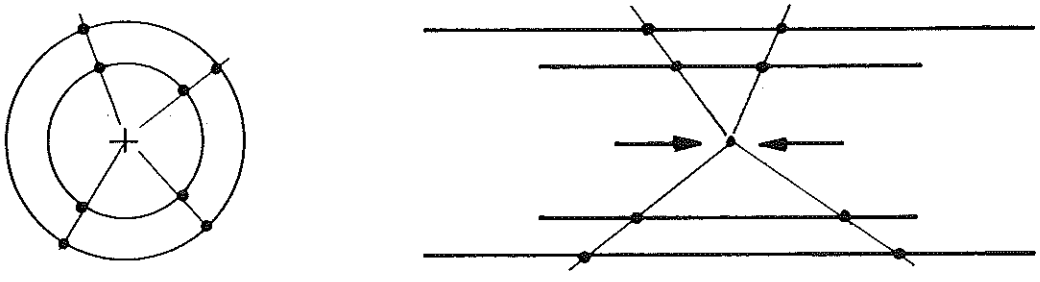
b) beam-gas interaction



c) cosmic ray background



d) coplanar and colinear beam-beam interaction



e) multibody beam-beam event

Fig.12
Some expected storage ring events and background

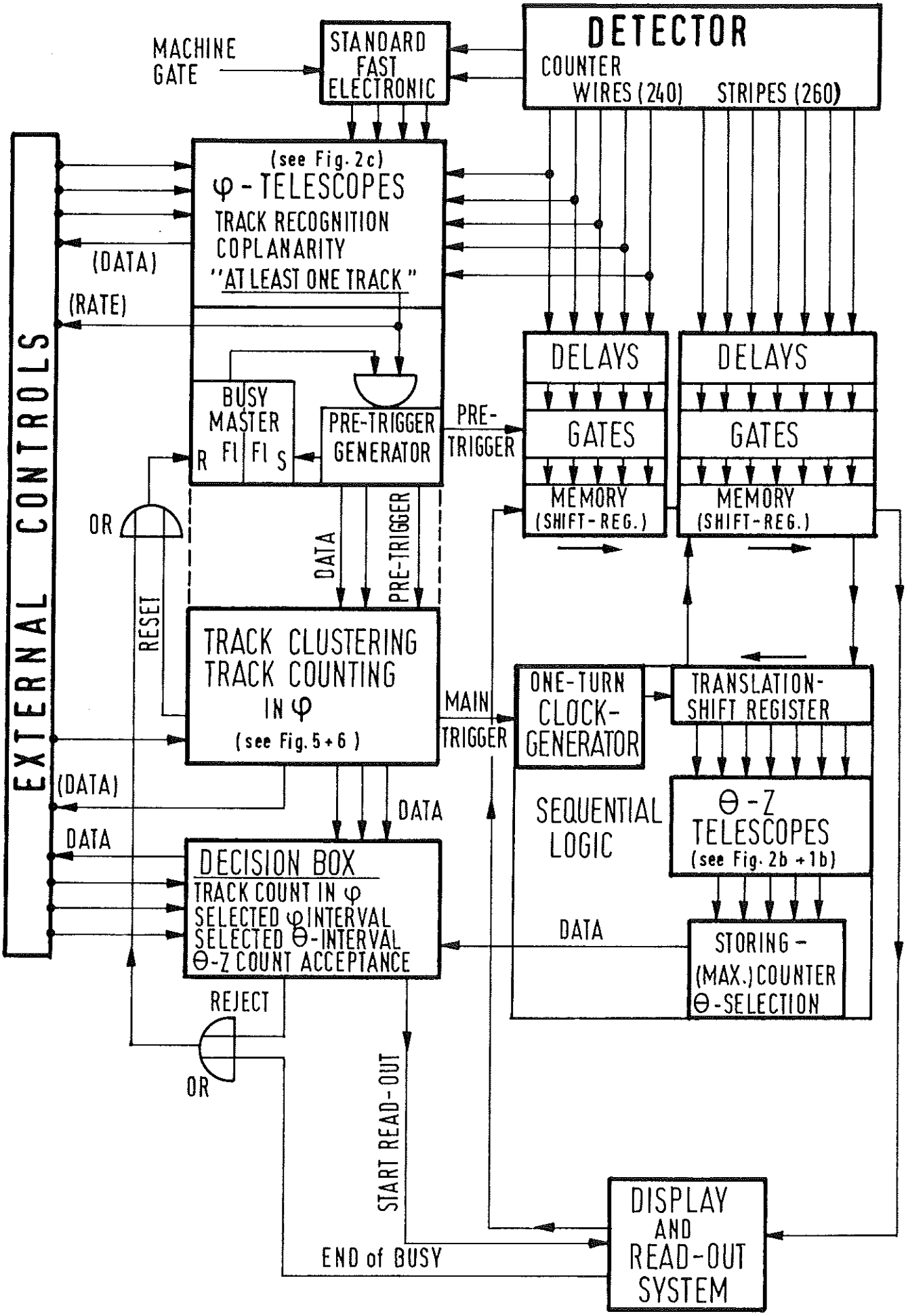


Fig. 13
A small trigger logic system