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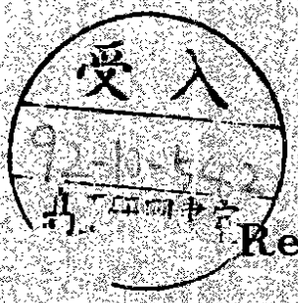

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Abstract

The readout of the ~ 12400 photomultipliers of the ZEUS high resolution calorimeter at HERA has to meet the following specifications:

- dynamic range of ~100,000:1,
- calibration accuracy ~0.2%,
- timing accuracy <1 ns,
- dead time free analog storage for about 5μs at the 10.4 MHz bunch crossing frequency of HERA,
- radiation tolerance up to ≥100 Gy.

The central building block of the readout are two integrated circuits in standard CMOS: the switched capacitor analog pipeline and the switched capacitor analog buffer–multiplexer. This paper describes the performance of the pipeline and problems which have shown up in detailed long time tests prior to installation in ZEUS. The required redesign and first test measurements for the improved pipelines are presented. Due to the schedule of HERA the original pipelines have been installed into ZEUS for the first year running; their exchange is planned for the winter shutdown 1992/93.

Introduction

The high luminosity operation of HERA with a time of 96 ns between collisions and the small cross sections of physics events require an efficient and deadtimeless first level trigger. During this time the event data have to be stored so that they are available for higher trigger levels and off–line storage.

For the readout of the high resolution depleted uranium–scintillator calorimeter of the ZEUS experiment at HERA an analog pipeline system using the switched capacitor technique is being used. The calorimeter is of the sampling type. It is segmented into a tower structure where each tower is read out by two wavelength shifters collecting the light onto two photomultipliers. The anode signal of each photomultiplier is split four fold to provide

- a measurement of the radioactivity induced current for gain calibration,
- a high and a low gain energy scale to cover the full range of the HERA collider,
- a trigger signal for the first level trigger system.

The signals for the energy measurements are shaped to deliver a signal of about 100 ns rise and fall time and a peak amplitude proportional to the charge from the photomultiplier. The output of the shaper is sampled by the analog pipeline with a frequency of 10.4 MHz, the HERA collision rate. From the samples of the shaped signals at several points in time the

charge and time of the photomultiplier pulse is reconstructed. The decision time for the first level has been defined to be 5 μs resulting in a length of the analog pipeline of 58 cells.

In order to reduce noise problems and cable costs, the readout electronics is mounted directly on the calorimeter with a minimum distance of 1 m to the beam. The radiation dose expected in these areas is estimated to be 10 Gy/year of ionizing radiation.

The analog pipeline has been designed by the Fraunhofer Institute IMS at Duisburg using a standard 3 μm CMOS technology with 3.5 μm minimum NMOS gate length, 40 nm gate oxide, and a metal over n^+–implantation capacitor with 70 nm oxide. Each chip contains 4 pipeline channels with 3 common control signals: clock, a read/write signal, and a reset of the feedback capacitor of the output operational amplifier. Each individual pipeline contains 58 storage capacitors of 1 pF each. They are addressed through a CMOS shift register operating at 10.4 MHz for writing and 0.75 MHz for reading. A detailed description of the pipeline system can be found in ref. 1 to 3.

Performance

Table 1 gives the performance achieved by the pipeline. Essentially all of the required specifications have been met. In the following we discuss problems which have been found in detailed test measurements.

Table 1

Input signal	–3.5 to +3 V
Signal to noise	~8000:1
Cell matching(gain)	0.3% to 1%
Nonlinearity	0.05%(input –3 to +2 V)
Input time constant	~5 ns
Cell–cell switching jitter	~0.2 ns
Max. write frequency	~15 MHz

Radiation hardness

Irradiation tests on MOS transistors and pipeline chips have shown that the CMOS process used will not tolerate more than a few 10 Gy. After a dose of 20 Gy the power supply currents of the pipelines increased by factors two to five heating up the chip. The pipelines were used for installation nevertheless. This appeared to be acceptable, since only a small part of the electronics had to be mounted in areas where doses of 10 Gy/year are expected. The affected chips would have to be exchanged from time to time.

Aging

At the burn–in tests of the final electronics after continous operation for 5 months, a degradation in the performance of the pipelines was discovered: the range of duty cycle of the write clock over which the pipeline operates changed with elapsed time of operation. In addition chips from different production lots a wide spread of duty cycle range. At that moment, 6 months before the first cosmic test run of the ZEUS detector, it was decided to select the

chips according to duty cycle, modify the readout of the electronics to allow for different clock duty cycles in different regions of the calorimeter, and to start a program to find the cause of the problems and cure them. Having understood the problems of the pipeline chips it was decided to redesign it with the aim of a higher radiation tolerance and a larger safety margin of operating conditions . A new prototype was designed at Nevis with the goal to produce prototypes at ORBIT, Sunnyvale, Cal.; and a redesign was also started at IMS and DESY with the aim of series production at IMS.

Improvements and Redesign

Radiation hardness

Ionizing radiation causes quasi–immobile positive charges in the gate and field oxide which shift the threshold voltages of MOS transistors and field transistors to lower values. In particular, the shift of the threshold voltage of the field oxide can lead to a conducting path between neighbouring active n^+–structures and within single standard NMOS transistors. For our investigation NMOS transistors, which have been produced together with the pipeline chips, have been irradiated using a Cs137 source. In addition to the expected shift of the threshold voltage large leakage currents appear already at a few 10 Gy for the NMOS transistors for negative V_{GS}. They increase rapidly with dose. After about 350 Gy the leakage current is of the same order as the on–current, and the transistor is dead (fig.1). The leakage current can be attributed to parasitic transistors which are turned on when the silicon underneath the junction of field and gate oxide is inverted by the ionizing radiation (see fig.2). These leakage currents are the cause for the increase of supply currents. Detailed studies on the performance of the buffer–multilpexer chip after irradiation have supported this conclusion (ref. 4).

Techniques to provide better isolation are p^+–guardrings around active n^+–regions with much higher doping than the normal field region and extension of the thin gate oxide (TOE) over the guardrings (ref.5 and fig.2). The TOE introduces additional gate substrate capacitances which have to be taken into account in the design.

With these improvements in the design, the next limitations are expected to be the effects due to the threshold voltage shifts of the actual transistors. They are strongly technology dependent, but the technologies offered by the two founderies should allow a radiation tolerance up to about 500 Gy.

Voltage Hardening

In order to achieve the stringent specifications of the pipeline with respect to speed, linearity and dynamic range a gate length for NMOS transistors of 3.5 μm and power supply voltages of ± 5 V were chosen in accordance with the design rules of the technology employed. It however turned out that standard transistors of that gate length cannot withstand voltages of 10 V without avalanching. In the design no NMOS transistor in the stationary state has to hold the full supply voltage: the transistors in the operational amplifiers are biased in the linear region; the current of the NMOS transistors in the digital part is always limited by the accompanying PMOS transistor in CMOS inverters. But nevertheless, NMOS transistors will be stressed during transitions when being clocked. Depending on details like the rise time of gate signals and the layout, the transistor can shortly operate in the avalanche region. This

will result in hot electron injection into the gate oxide and will lead eventually to an increase of threshold voltage and a decrease of transconductance (ref. 6). Both effects will reduce the speed of the transistor. Actually, one particular transistor of the clock circuit is under such conditions because of the slow rise time of the gate signal. Measurements on chips operating at 10 MHz using an e–beam tester have shown this reduction of speed in the input circuit for used chips.

Techniques to prevent or reduce hot electron effects are Lightly Doped Drain (LDD) and Extended Drain (ED) (ref. 7 and fig. 3a,b). Both techniques aim for a reduction of the electric field at the drain. This is obtained by introducing a region of lower implantation dose between the gate region and the contact region of the drain.

The ED technique requires an extra mask and thus can be implemented only where needed. LDD affects all NMOS transistors both on the drain and source side since it is applied in an additional technological step without extra mask. For both techniques an increase of the safe operating voltage of about 2 V is expected. Because of the added low dose implantation at the drain the transconductance of the LDD and ED transistors decreases by around 10 to 15% resulting in a reduction of speed.

Both radiation hardening via TOE and voltage hardening via ED or LDD will degrade the speed which has to be taken into account in the redesign.

Redesign

The redesign of the chips had to be done in the geometrical layout of the existing version; in particular, the package and the pin layout have to remain the same. The original layout used a 3 μm technology. By applying 2 μm design rules for the redesign the necessary space for the improvements could be found.

All NMOS structures– transistors and wells – have been surrounded by p^+–guardrings, and the TOE has been applied to all NMOS transistors for radiation hardening. All NMOS transistors in the digital part have been laid out in either LDD or ED version.

The redesign was checked by simulations using SPICE and BONSAI, a simulation program optimized to the technology of IMS. The simulations showed that the performance of the pipeline could be improved considerably by

- increasing the bias current in the input comparator for the digital signals,
- optimising the 'two–phase circuit' which provides the non–overlapping clock for the CMOS shift register and its fanout to the four independent pipelines.

The increase of the bias current in the comparator from 30 to 100 μA improves the rise time thus reducing the stress on the output transistors; at the same time it reduces the delay through the circuit as well as its sensitivity to technological variations of transistor parameters. The bias current is defined by an off–chip current source which defines the control voltage of the current mirror. In this way the dependence of the current on transistor parameters is further reduced.

The original two–phase circuit had been laid out in a very conservative way: four inverters were used as delays to ensure a non–overlapping clock. In the simulations the resulting clock signals show a strong dependence on the duty cycle of the input signal, leaving only 25 ns of duty cycle range. This is in good agreement with measurements. The optimized version uses

no extra delay beyond the NAND–gates (fig. 4). Simulations show that this solution still provides safe non–overlapping clock signals. The inverters between the two–phase circuit and the bus for the clock signals of the individual pipeline have been optimized in drive capability for the high capacitive load of the long shift register. Minor changes which lead to a reduction of the capacitive load of the clock busses were included as well.

Simulations of the redesigned pipeline gave the following results:

- operation at 10.4 MHz leaves a duty cycle range of 70 ns; the delay between the clock input and the actual sampling time is reduced to from 55 ns to 35 ns;
- with clock signals of 50% duty cycle the chip should operate at 25 MHz.

The expected changes of threshold voltage and transconductance due to irradiation have been simulated as well. They do not influence strongly the performance of the pipeline.

First results on prototypes

The redesigned layout has been sent to two places for manufacturing, ORBIT and IMS. Both use guardrings and TOE. For voltage hardening ORBIT uses LDD, and IMS uses ED. The storage capacitors are laid out in double poly with about 75 nm oxide at ORBIT, and in poly over n^+–implantation with about 40 nm oxide at IMS.

Prototypes from ORBIT have already been delivered, and first tests have been performed on test transistors and pipelines. The chips have been produced in standard CMOS and in LDD version to allow for comparison between the two technologies. Test structures exist in standard MOS, LDD and ED versions.

The NMOS transistors in LDD and ED version show the expected increase of safe operating voltage of about 2 V (fig. 5a,b). The transconductance is reduced by about 10%. The threshold voltage of the NMOS transistors changes by about 3 V after receiving a dose of 4000 Gy in the on–biased version, but no parasitic conducting transistors appear. With V_{GS} pulsed with 19 kHz between 0 and +10 V with 50% duty cycle the voltage shift reduces to 1.6 V. The corresponding values for the PMOS transistors are 1.3 and 0.9 V, respectively. The following results have been obtained from measurements on a few chips done in standard CMOS:

- variation of pedestals over a pipeline about 1 mV, excluding the cells at the end of the pipeline which have around 10 mV deviation from the mean,
- variation of gain less than 0.5% over a pipeline,
- variation of pedestal from chip to chip less than 5 mV (was up to 30 mV for original chips),
- variation of the gain from chip to chip less than 1%,
- variation of the delay between clock and sampling from chip to chip about 0.4 ns (was about 3 ns for original chips),
- duty cycle range of 53 ns at 10.4 MHz (was about 25 ns for original chips); from this range one can deduce a maximum write frequency of about 23 MHz (was about 15 MHz).

Measurements on chips done in LDD show a duty cycle range of 45 ns. The other parameters are about the same.

Chips in standard CMOS have been irradiated up to 4000 Gy with a Cs137 source. During irradiation the standard cycle of WRITE, READ and RESET as during data taking was applied. Up to 1000 Gy no changes in performance could be measured. Beyond that dose the linearity starts to degrade, and the gain and pedestals start changing. At 4000 Gy the pipeline still functions. The gain has changed by about 3%, the pedestals have shifted by 30 mV, and the linearity shows deviations of several mV from a straight line fit where 0.5 mV are required. The supply currents have increased by about 50%. No change in the duty cycle range and no measurable increase in noise was observed.

First test results from IMS show for ED transistors an increase of over 2 V in the safe operating voltage as expected (fig. 6a,b). A first on–wafer measurement has shown that the pipeline functions.

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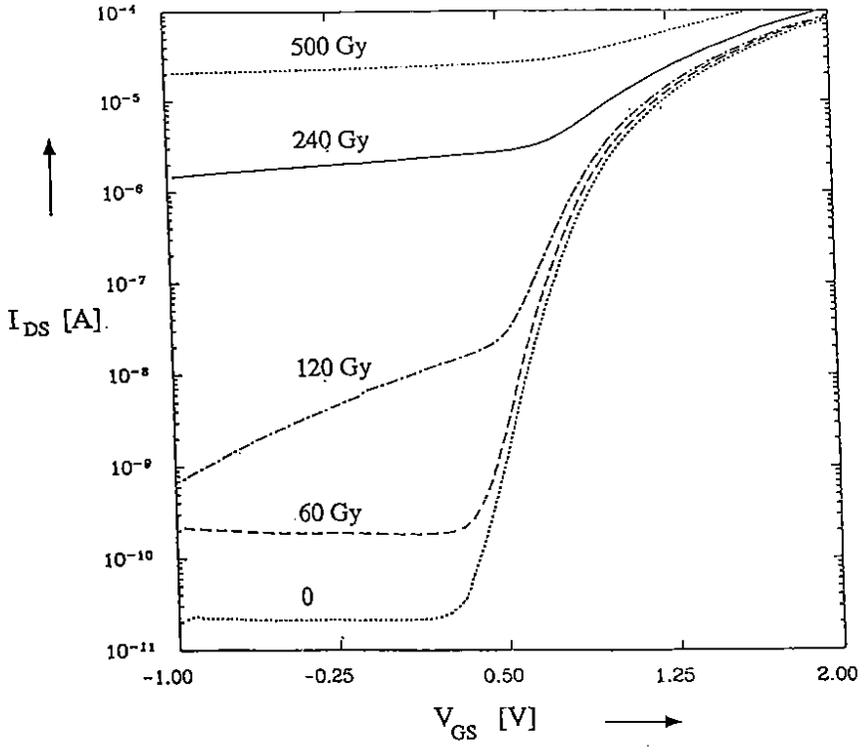

Fig.1 I_{DS} vs. V_{GS} for a NMOS transistor (W/L=60/20) with received dose as parameter

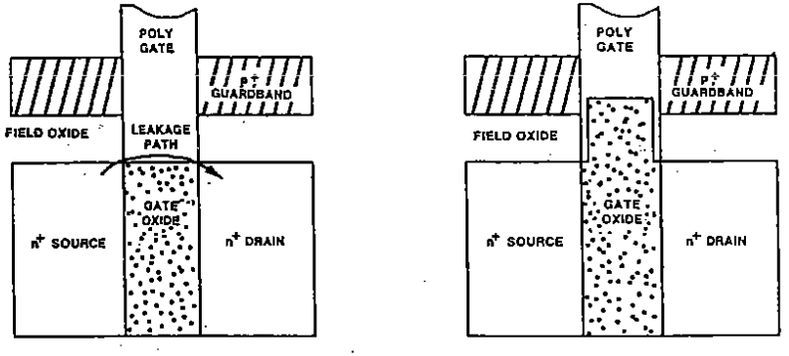

Fig.2 possible leakage path after irradiation
and a method to prevent the leakage path – thin oxide extension – (from ref. 5)

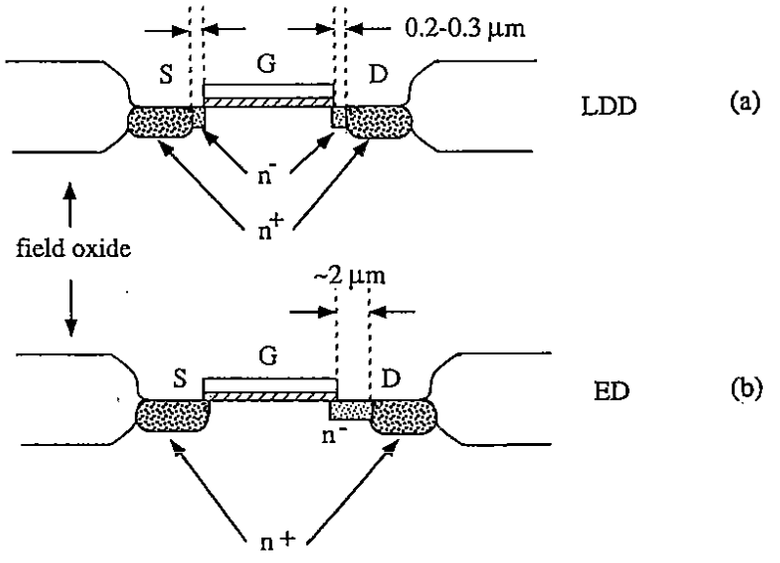

Fig.3 Illustration of NMOS transistors employing
a) LDD technique
b) ED technique

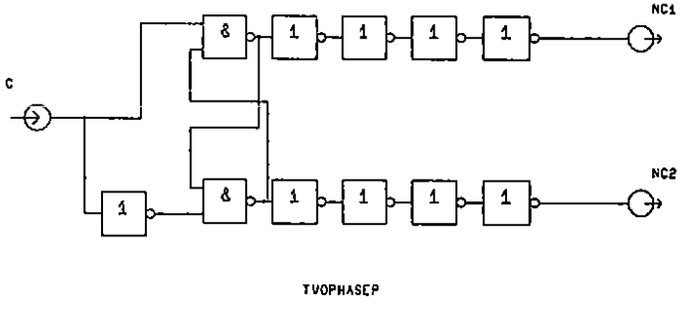

Fig.4 Two-phase circuit for the non-overlapping clock.
In the original layout the feedback to the NAND–gates was connected to the outputs NC1, NC2

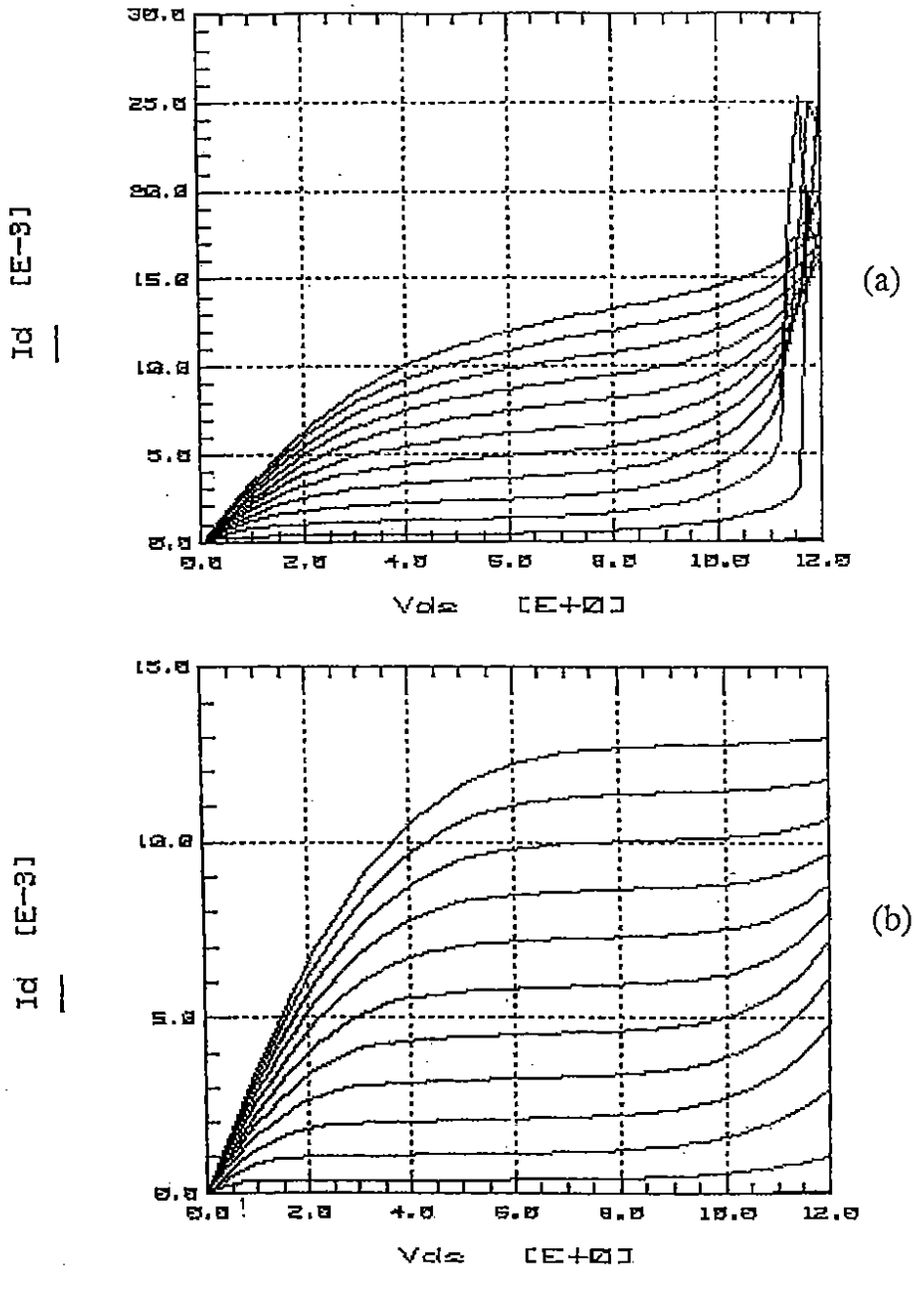

Fig.5 Characteristics of a NMOS transistor (W/L=40/4) from ORBIT
a) standard layout
b) LDD layout

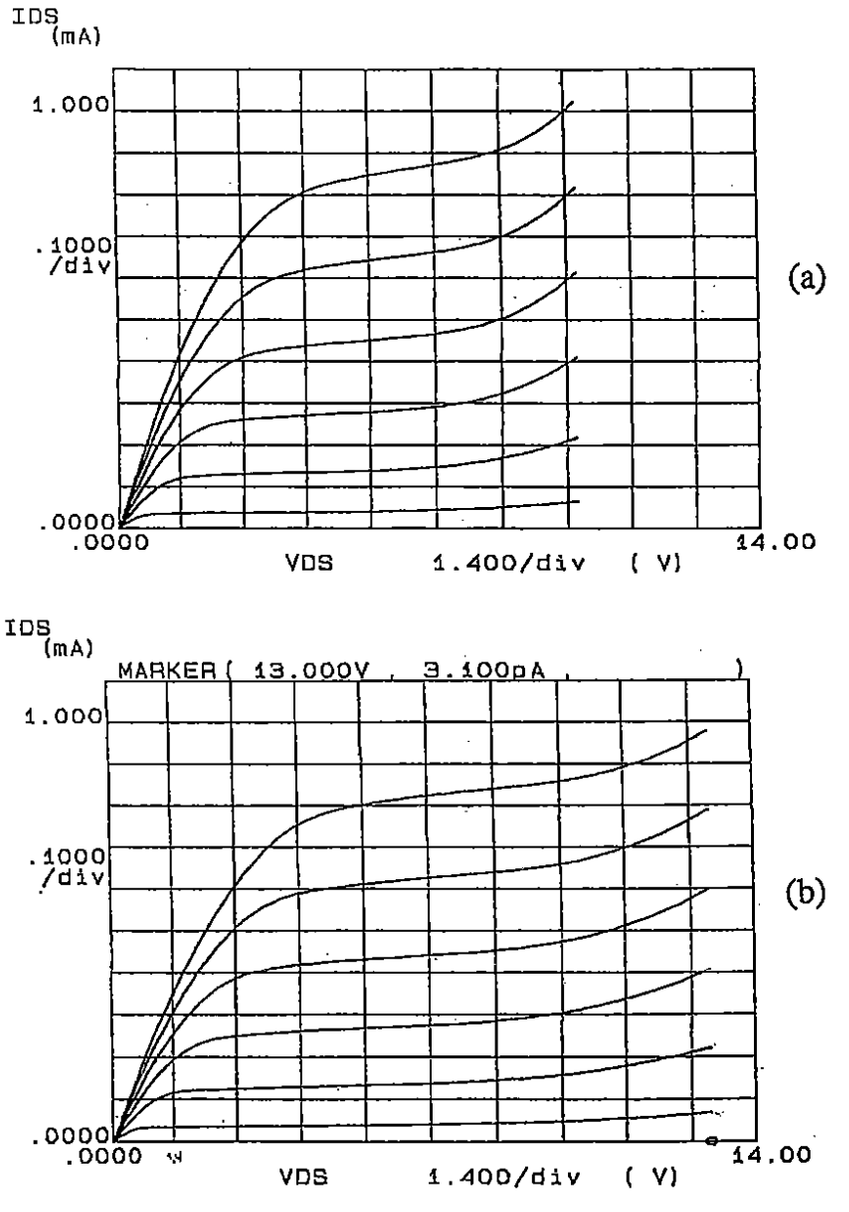

Fig.6 Characteristics of a NMOS transistor (W/L=4/4) from IMS
a) standard layout
b) ED layout