The LPS Trigger System

F.Benotto[2], M.Bollito[1], M.Costa[2], P.Isoardi[1]
H.Larsen[3], T.Massam[3], C.Nemoz[3], E.Pernigotti[1]
R.Sacchi[1], A.Staiano[2], P.P.Trapani[1], A.Zampieri[2]

University of Torino[1] , INFN Torino[2]
INFN Bologna[3]

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1 Introduction

The Leading Proton Spectrometer (LPS) [15] has been equipped with microstrip silicon detectors specially designed to trigger events with high values of $x_L = \frac{|\vec{p}'_p|}{|\vec{p}_p|} \geq 0.95$ where $|\vec{p}'_p|$ and $|\vec{p}_p|$ are respectively the momenta of outgoing and incoming protons. The LPS First Level Trigger can provide a clear tag for very high momentum protons in a kinematical region never explored before.
In the following we will discuss the physics motivation in tagging very forward protons and present a detailed description of the detector design, the front end electronics, the readout electronics, the Montecarlo simulation (ZGANA [27]) and some preliminary results from 1995 data taking.

2 Physics at High x_L

There is a large class of events in which the proton emerges intact with high longitudinal momentum and is well separated in polar angle θ from the particles of the hadronic final state. We refer to this class of events generally as produced by *diffractive* processes, both in photoproduction ($Q^2 \sim 0$) and in DIS. Various models have been proposed to describe the production mechanism of diffractive events. For all models, the x_L value of the scattered proton is very strongly peaked at $x_L = 1$, and the p_t distribution is peaked at $\sim 200 - 300\ MeV$.
As an example see Fig. 1 where the x_L and p_T distributions have been generated with the DIPSI Montecarlo simulation program [14], based on the model of Ryskin et al. [12], [13].
The model used in the LPSFLT DIS trigger efficiency simulation (see Section 8) has been developed by Nikolaev and Zakharov [8]-[11], and implemented in `ZDIS` [7].
The model describes diffractive events in terms of the exchange of a colorless object, generally called *pomeron*, between the photon and the proton (see Fig. 3). The

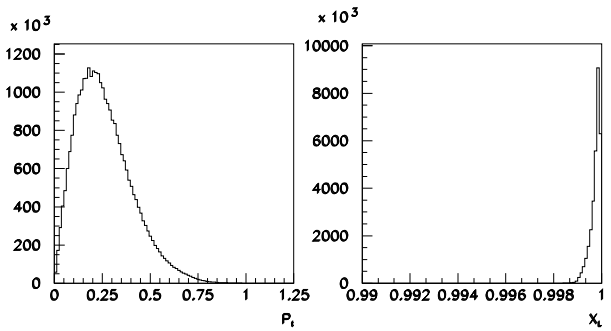

Figure 1: x_L and p_t distributions in the Ryskin Model

topology of the event, as seen in ZEUS, is an energy deposition in the central detector, and a fast forward proton [2]. The x_L and p_T distributions for these events are shown in Fig. 2.

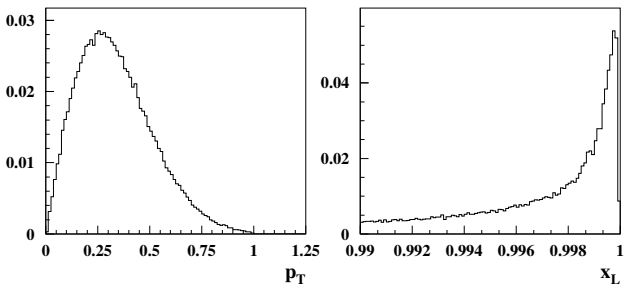

Figure 2: x_L and p_t distributions in the Nikolaev-Zackarov Model

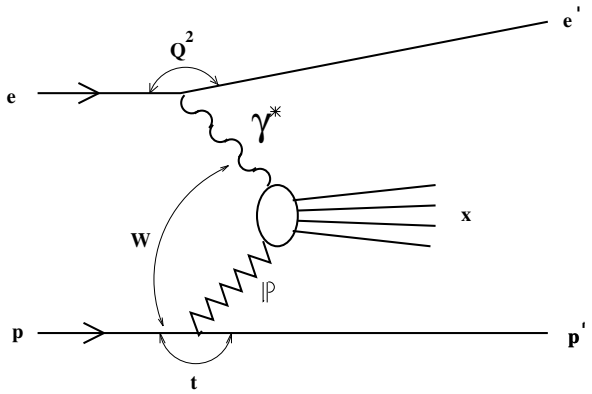

Figure 3: Photon-$\mathbb{P}$Interaction

The model predicts that $10 - 15\%$ of the total deep inelastic events is diffractive.

3 Trigger Detectors

3.1 Design of the Trigger Detectors

We have derived the design of the trigger detectors by completing the following steps (see also [15],[16],[17]):

- Simulate the LPS geometry with `GEANT`, including some dummy trigger detectors with the same geometrical acceptance as the LPS planes;
- Generate proton tracks with $x_L = 1$ and track them through the spectrometer;
- Find track correlations between hits in different stations;
- Determine the trigger acceptance as a function of the geometrical dimensions of the trigger planes and of the trigger detector pitch;
- Define optimum for location, dimensions and pitch of the trigger detectors.

The simulation program has been written within the `GEANT` framework, and included in `MOZART`. The LPS simulation describes the full beam transport line from the interaction point to the last station of the LPS (S6). Stations S4, S5, and S6 contain two pots, *up* and *down*, while stations S1, S2 and S3 each have a single pot mounted in the horizontal plane. In the present work the trigger placed in stations S4, S5 and S6 is discussed while the trigger design for S1,S2 and S3 is at the moment under study These two parts of the spectrometer can be considered indepenedent and complementary in acceptance.
The spectrometer location in the tunnel and the layout of the HERA magnets is shown in Fig. 4.

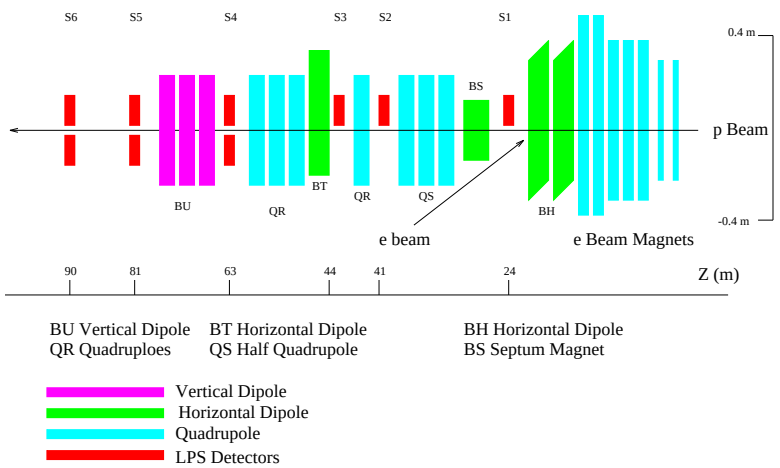

Figure 4: The LPS Spectrometer of ZEUS

We have generated 10000 events from $x_L = 0.95$ to $x_L = 1$ at each step of $\Delta x_L = 0.01$ and with
$\frac{d\sigma}{dp_T} \sim const. \cdot e^{-4.0 p_T^2}$.

In order to determine the best trigger configuration we have selected events with a triple coincidence detected in the silicon detectors adjacent to the future trigger planes position. By analyzing the events reconstructed at different values of x_L in the three stations, we determined two optimal trigger configurations: *S4down S5up S6up* and *S4up S5up S6up*. For mechanical reasons, S4down could not be operated at nominal position and we have therefore chosen the latter configuration. The x, y distribution for $x_L = 1$ protons for this choice can be seen in Fig. 5. Here one can see how the detector region where the x_L tracks are reconstructed in the LPS planes is very limited in space. The trigger detector can be therefore quite small.

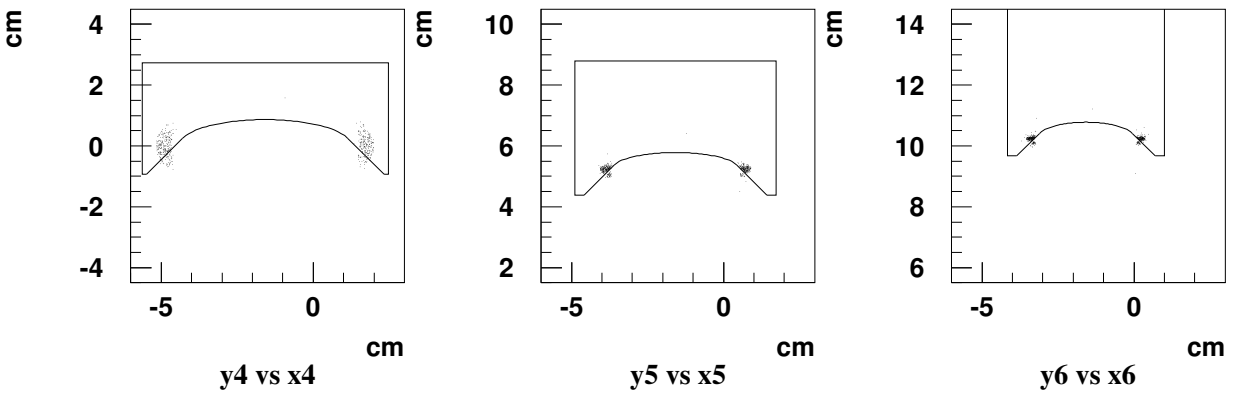

Figure 5: Hit distribution for $x_L = 1$. Detectors and hits are drawn in the HERA reference frame, where the beam is at $x = -1.579, y = 0$ *cm* at S4 and is then bent vertically up by the BU dipole magnets placed between S4 and S5.

The hit pattern is broader when $x_L < 1$ events are taken into account. Although the trigger has to be designed to maximize the acceptance at $x_L = 1$, we do not want to lose an important fraction of the acceptance at lower values of x_L. The shape of the detector is derived keeping in mind these two requirements.
In order to determine the size, we have to follow several hardware constraints, the most important being that we are limited to a maximum number of 80 readout channels per plane, which comes from both the physical space for the cabling (which is extremely small, $2 \times 70 mm^2$ space for the cable slot in the pot), and the readout cost. This means that the determination of the size of the sensitive area of the detector directly defines the strip pitch.
In order to determine the pitch we introduce the concept of "linear correlations" between hits in different stations of the LPS. As we will see, the fact that hits in different stations are linearly correlated allows a clean selection of tracks of defined x_L at the First Level Trigger.

Given a track starting at a fixed point (x_0, y_0) at $z = 0$ with some momentum $\vec{p}$, one can predict how this particle will travel through the HERA beam optics and where in x and y it will intersect an LPS pot. This can be expressed for the x and y coordinates separately. For example in x we have:

$$\begin{pmatrix} x \\ p_x \end{pmatrix} = \begin{pmatrix} T_{11}(x_L) & T_{12}(x_L) \\ T_{21}(x_L) & T_{22}(x_L) \end{pmatrix} \begin{pmatrix} x \\ p_x \end{pmatrix}_{z=0} \tag{1}$$

where each element of the matrix T is a function of $x_L = p_z/E_p \approx p/E_p$, where E_p is the incident proton momentum. Eq. 1 is indeed the *beam transport equation* and T the *transport matrix*. Note that eq. 1 is a linear equation, which holds because HERA magnets are designed to produce fields inside the beampipe that closely approximate ideal quadrupole and dipole fields. Also note that in this approximation horizontal x and vertical y equations are not coupled, except for their common dependence on x_L.

By eliminating (p_x, p_y), one can construct a linear equation that relates the intersection of a track in two different pots $a(x_a, y_a)$ and $b(x_b, y_b)$:

$$\begin{array}{rcrcl} A_x(x_L, x_0)x_a & + & B_x(x_L, x_0)x_b & = & C_x(x_L, x_0) \\ A_y(x_L, y_0)y_a & + & B_y(x_L, y_0)y_b & = & C_y(x_L, y_0) \end{array} \tag{2}$$

where the elements A, B, and C are a function of both x_L and the starting point of the track (x_0, y_0) at the origin $z = 0$. Again, except for their common dependence on x_L, the x and y solutions are independent.

If drawn in (x_a, x_b) or (y_a, y_b) planes, eq. 2 form a line, and if a common vertex is assumed, each value of x_L produces a unique line in these coordinates.

Since the linear correlations are in the $x - y$ plane, we chose horizontal and vertical strip orientations for the trigger planes.

As an example we show in Fig. 6 linear correlations fitted from a Montecarlo sample of 1000 events generated with $x_L = 1$ within the nominal interaction region.

If we look at the two-dimensional distributions of the residuals of the vertical and horizontal coordinates with respect to the predicted lines (from eq. 2), after digitizing the hits with different pitches, we find elliptic distributions (multiple scattering through the pot windows and the detector planes is simulated in the program, see Fig. 7).

These elliptic distributions define the phase space in the trigger logic that one would like to select. This selection is done, in the trigger readout electronics, by using coincidence matrices which select the linear correlations of eq. 2, as will be described in detail in section 6.1.

By fixing the aspect ratio (ratio of major to minor axis) of the ellipse we can finally study the trigger efficiency as a function of a given axis of the ellipse (e.g. R_{minor}), where the efficiency ϵ is defined as the ratio of the number of events collected inside the ellipse over the total number of events. The efficiency can be studied for various pitches and the results are shown in Fig. 8.

Obviously smaller pitches will allow higher resolution of the road definition in the correlations and therefore higher efficiencies for fixed R_{minor}. However, since the number of readout channel is fixed, the smaller the pitch, the smaller the detector and therefore the trigger acceptance ϵ. A plot of the trigger acceptance for various x_L and pitches is in Fig. 9.

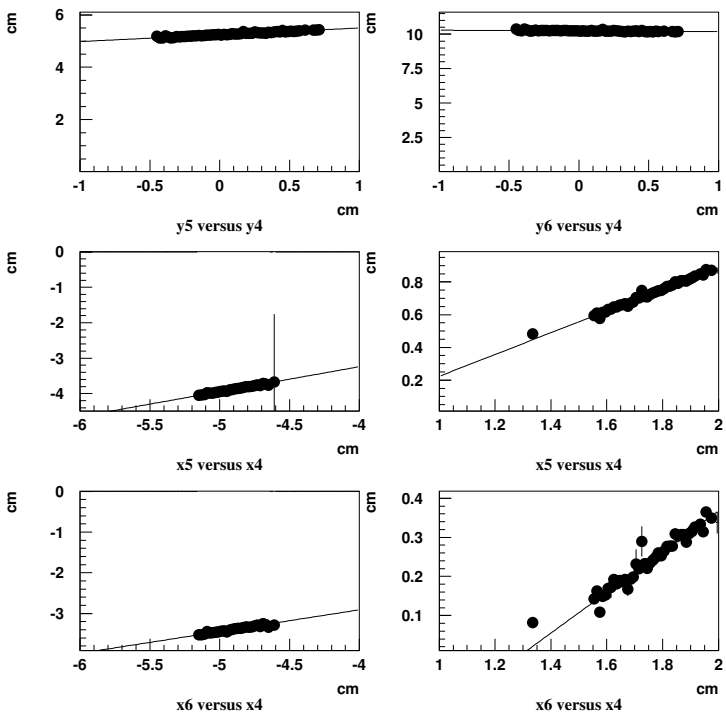

Figure 6: Linear fits to horizontal and vertical correlations

By comparing Fig. 8 and Fig. 9 we determined a detector pitch of $750\mu m$ as our best choice.

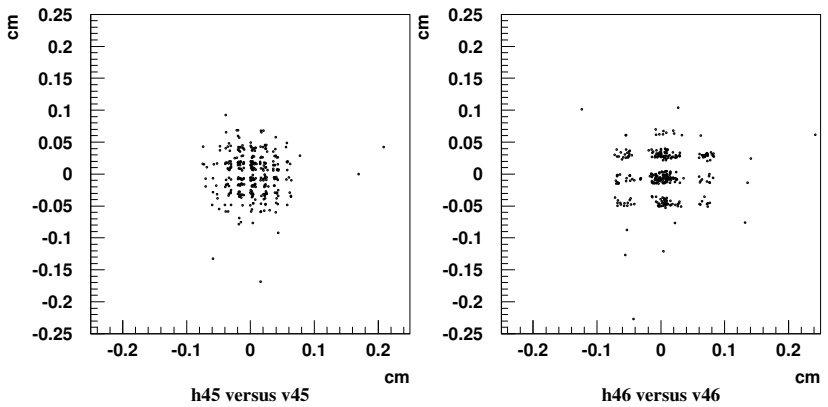

Figure 7: Distributions of horizontal and vertical residuals of linear correlations. H45 represents the residual distribution of the correlation x4-x5, while V45 is the residual distribution of the correlation y4-y5. The empty bands observable in figure are due to the strip digitization ($750\mu m$ pitch in this example).

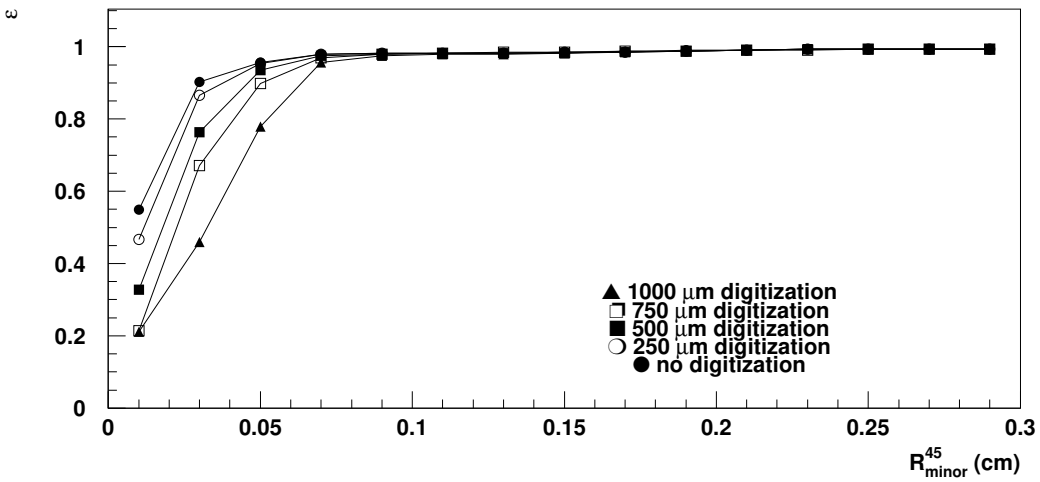

Figure 8: Trigger efficiency as a function of R_{minor} of the ellipse.

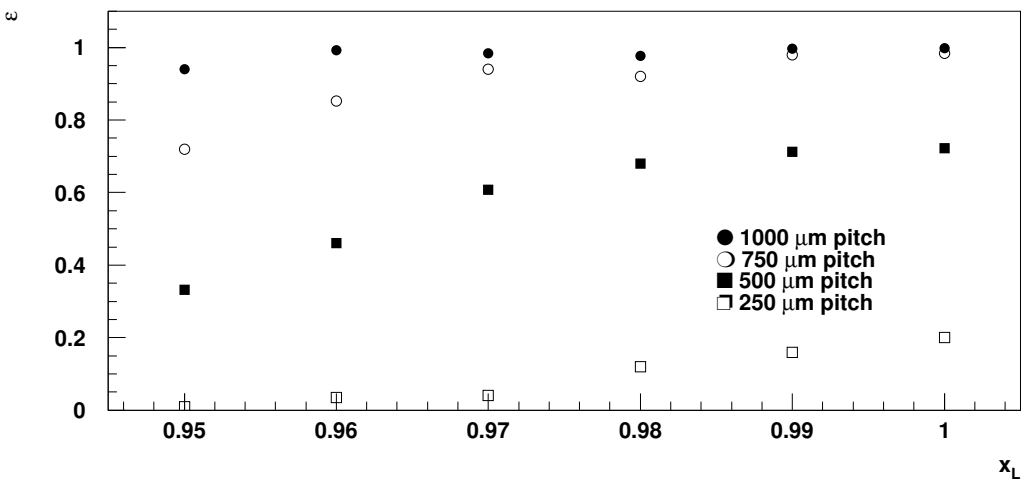

Figure 9: Trigger acceptance for different pitches at various x_L

3.2 Layout of Trigger Detectors

We have designed the detector layout (ITALCAD system) giving relevance to two main requirements:

- Low single strip capacitance in order to keep the amplifier noise at a minimum. The aluminum strip width was designed in order to keep the capacitance to values of 2.4pF/cm maximum.
- AC coupled strips to prevent a large leakage current flow into the amplifier. The leakage current infact will increase from a few nA to several μA after doses of $\sim$ 1 MRad [18]. The coupling capacitor can be built by growing a thin layer ($\sim 0.2\mu$m) of SiO_2 between the strip metallization and the p diffusion. This capacitance can be large because it is in series with the junction capacitance.

In AC coupled detectors, microstrips are biased through a bias ring which runs along the edge of the detector. Each microstrip is connected to the bias ring via a large resistor ($\sim$ 1MΩ). We have investigated different tecniques which are used by the manufacturers to implement these bias resistors:

- polysilicon resistors;
- p-diffusion resistors with variable doping;
- "punch-through" resistors.

Polysilicon resistors are known to be very radiation resistent, but they require several masks for the deposition, and the process is therefore quite expensive. With p-diffusion resistors, which are built by varying the doping concentration from the readout strip to the fanout strips which connect to the bias ring, one cannot achieve high resistance values without using long strip loops, which makes the realization of the detector complicated and requires large areas of silicon dedicated to the bias resistors. We therefore chose the so called "punch-through" type biasing scheme (see Fig. 10) which makes use of the punch through effect which occurs in npn type

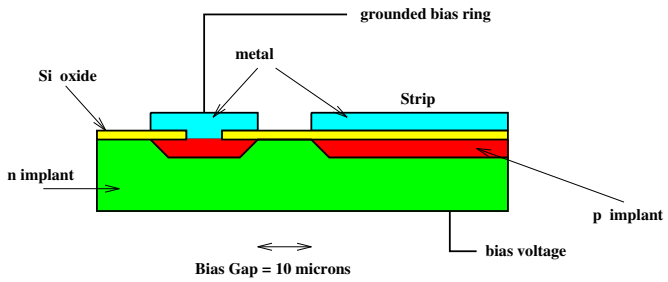

Figure 10: The LPSFLT Bias Scheme

junctions [19]. In this scheme the strip implants are left floating and the bias ring is placed very close to the strip ends ($\pm 10\mu m$). The strips are then biased when punch through effect occurs between the bias ring and the strips. AC coupled detectors fabricated with this technique are cheaper because they require a limited number

of masks with respect to polysilicon resistor biased detectors, and they have been recently shown to be quite radiation resistent [20].
As discussed in Section 3.1, the strip orientation chosen for the trigger planes is one plane of vertical strips and one plane of horizontal strips in each trigger plane. Since we have to assemble the two planes with orthogonal strip orientation on the same multilayer support we considered the option of using double sided detectors. This option was rejected mainly because:

1. two overlapped single sided planes offer two order of magnitude better syncrotron background rejection;

2. single sided detectors are cheaper and easier to assemble.

The chosen design foresaw therefore two detectors glued on the same support but on opposite sides of it. In other words rather than using a single sided multilayer support with a double sided detector, we used the option of two single sided detectors glued on a double sided support. For a detailed description of the detector support see Section 5.1.
The layout of one of the trigger detectors is shown in Fig. 11.
The detectors mounted on a single support are symmetric with respect to the vertical axis passing through the beam. So we have for one trigger plane four detectors: $a_{left}^{horizontal}$, $a_{left}^{vertical}$,$a_{right}^{horizontal}$,$a_{right}^{vertical}$, where, in our convention, left means towards the HERA center. This is illustrated in Fig. 12.

3.3 Test of Trigger Detectors

The trigger detectors have been manufactured by Eurysis (Intertecnique) and delivered in January 1994. Each detector was inspected, measured and tested with a probe station in the clean room of the INFN laboratories in Torino. The parameters checked for each detectors were:

- Geometrical measurements
- Leakage Current
- C-V characteristic curve
- interstrip capacitance
- punch-through voltage

Geometrical measurements of the actual sizes of the detectors show residuals of the order of 20 μm when compared to the design specifications. Pitch and distances of the sensitive area of the detector from the bias ring are precise within 2-3 μm. A microphotograph of one detector is shown in Fig. 13.
The picture shows a detail along the 45^o edge of the detector with the ends of three strips, the two bias rings, the fanout shape, and several guard rings. The two inner rings are the bias ring, which are bonded to ground. The other rings are left floating and they guarantee the uniformity of the electric field up to the detector edges. Each bonding pad has dimensions of $200 \times 100 \mu m^2$.

The leakage current has been measured in test structures which had DC contacts on each strip. In these detectors the breakdown voltage is $\sim$ 100 V. The leakage current is constant and below 3 nA in the depletion region. The bias voltage to operate these detectors has been determined by measuring the capacitance of each strip as a function of the junction voltage. As one can see in Fig. 14, where we plot $1/C^2$ as function of V_{bias}, the bias voltage is $\sim 60\ V$ and the detector is fully depleted at $\sim 80\ V$.
The bias ring leakage current has been measured on all detectors and is typically less than $5nA$. The punch-through has been measured to be equal or less than $2mV$ at depletion voltage.
The coupling capacitance of these detectors has been measured to be $400 \pm 20pF$ per channel. The capacitance measured between a single strip and the backplane is $4 \pm 1pF/cm$, whereas the interstrip capacitance is $2.5 \pm 0.2pF/cm$.

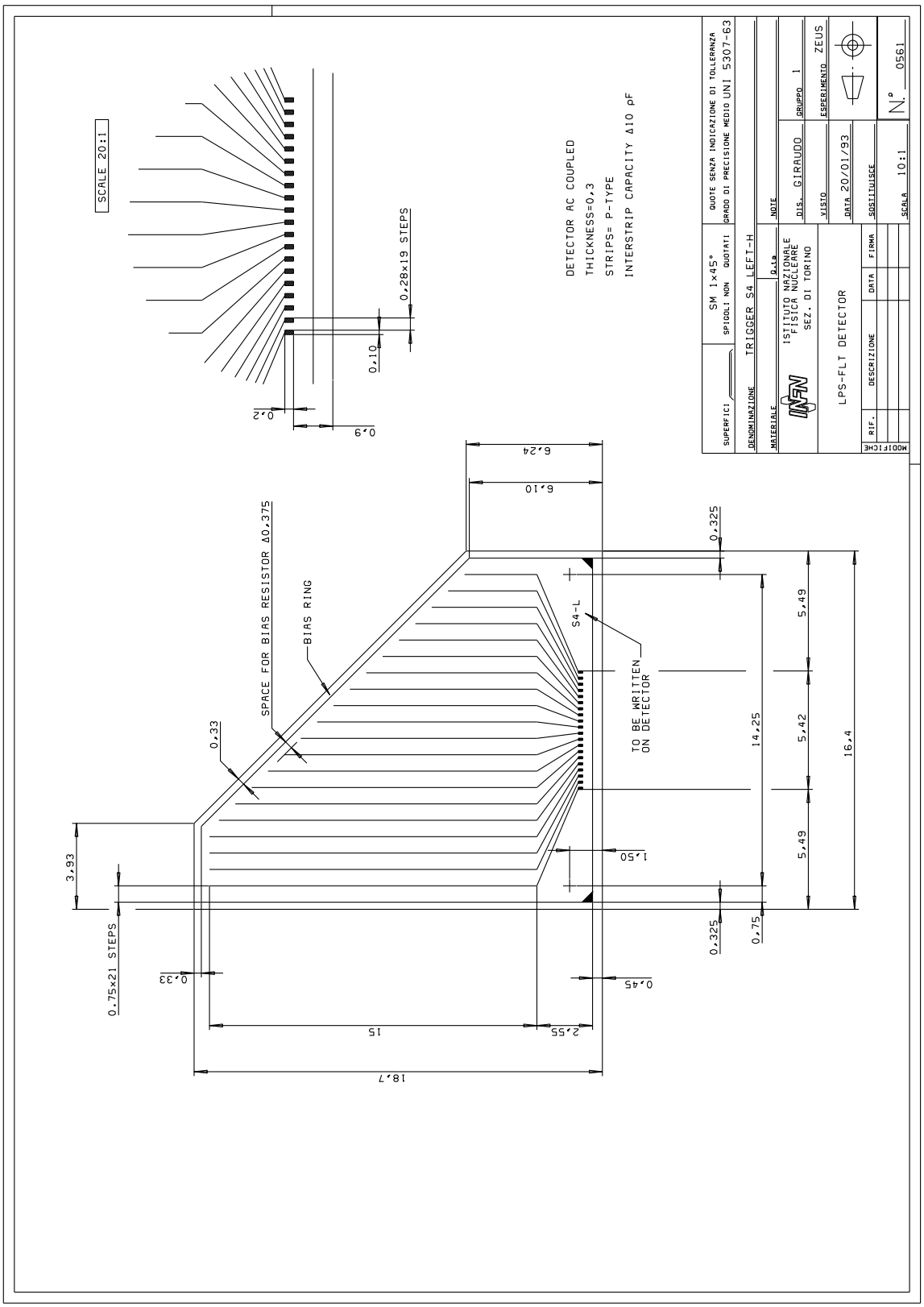

Figure 11: LPSFLT detector

Figure 12: Final detector positions for one LPS trigger plane. Left and right detector couples are designed overlapped.

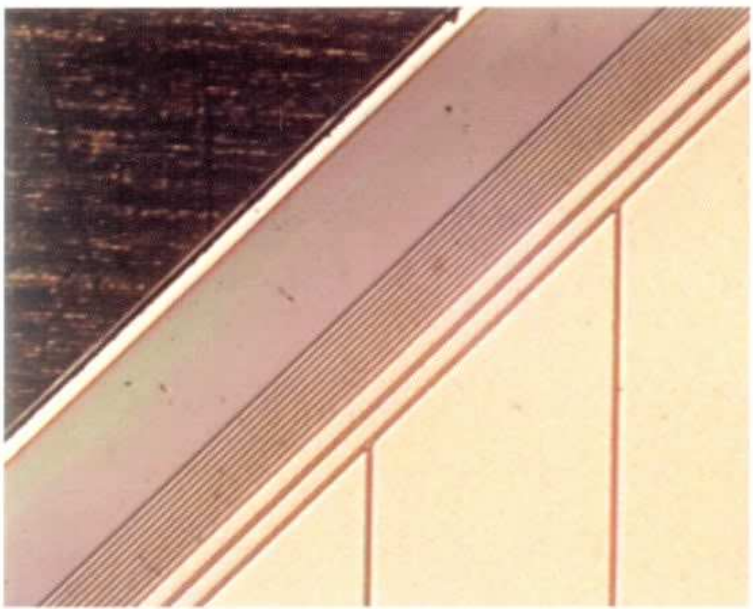

Figure 13: S6HL Trigger Detector

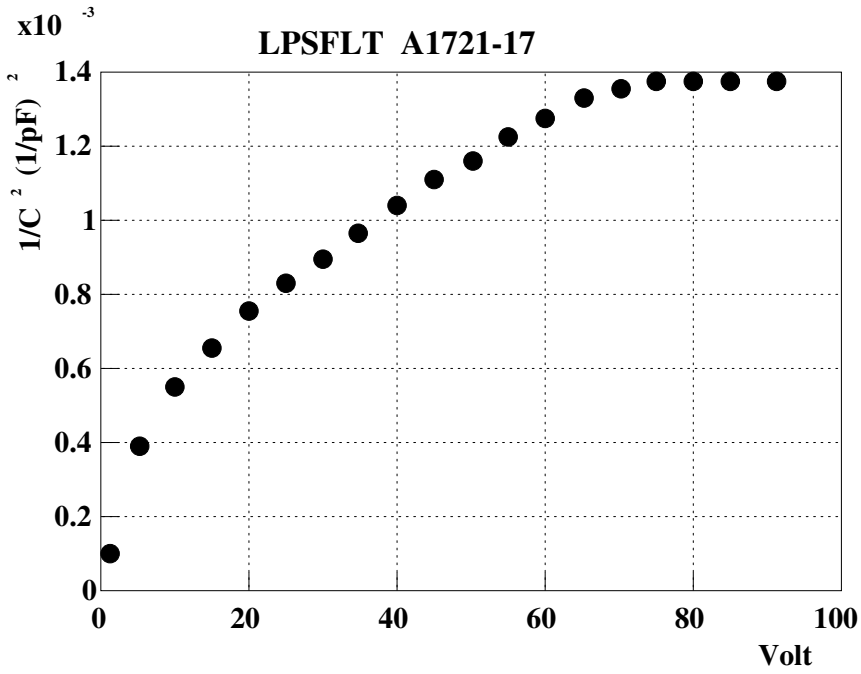

Figure 14: LPSFLT C-V curve

4 Front End Electronics

Two different front-end (FE) schemes were studied, the requirements being:

- radiation hardness of the VLSI front end system;
- fast shaping time (the HERA clock running at 10 MHz);
- capability of driving the signal out of the roman pots to the readout electronics.

4.1 Scheme *a*

The performance of the prototype built with this schema is thoroughly described in [21]. In this scheme we used a 64 VLSI amplifier-comparator chip designed to meet the HERA specifications for the LPS [22] and built in BiCMOS technology. The emitter follower at the output stage of the discriminator had limited driving capabilities. In order to drive out the signal along 10 meters of twisted pair cable to the shelter crate in the HERA tunnel, a dedicated 8 channel jFET low power driver has been designed [23] and produced by ORBIT inc. (see Fig. 15).

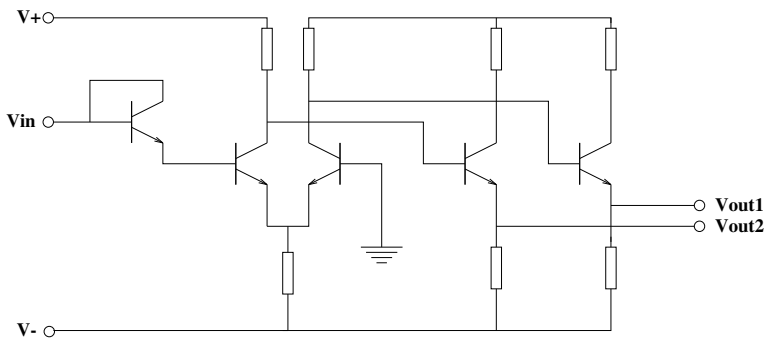

Figure 15: Circuit Diagram of the jFET driver

These two chips were bonded to an AC coupled μstrip silicon detector and tested for:

- Noise of the amplifier,
- Gain of the amplifier,
- Time propagation delay and walk of the full system,
- Dead time.

All of these measurements have been done before and after irradiating the electronics and the detector with 815 kRad from a Co^{60} source (FE electronics is more sensitive to photon radiation damage than to charged particles). The measured noise was $\sim$ 2000 electrons, and remained unchanged after irradiation. We observed a slight change of the amplifier gain. The offset moved from 70mV to 103mV after irradiation. Also time walk was found stable and meeting the required specifications,

that is $\leq$ 10 ns at 12 fC input pulse. The measured dead time however was also measured to be limited to 170 ns because of pulse lengthening by the driver. An improvement of this value would have been still possible by reoptimizing the driver design.

4.2 Scheme b

For this scheme we used as preamplifier-comparator the $TEKZ$ chip, designed at UCSC for the LPS [24]. This chip is modelled on the amplifier circuit used in *scheme a*, but it is fabricated in BIPOLAR technology by TEKTRONIX. The gain is slightly higher ($\sim$ 150 mV/fC) and it has an average intrinsic noise of $\sim$ 650 electrons. In this scheme, the unipolar signal of the TEKZ comparator output is connected to a driver board designed for this pourpose [25] and installed 1.5 m away from the pot (see Fig. 16). The signal is then transformed through a double MC10116 driver, to a double differential ECL signal which is then sent through 100 meters to the LPS/FMUON hut, where the readout trigger electronics is. Both the distance from the TEKZ to the driver board and from the driver board to the readout electronics were chosen to be as close as possible to final operating conditions.

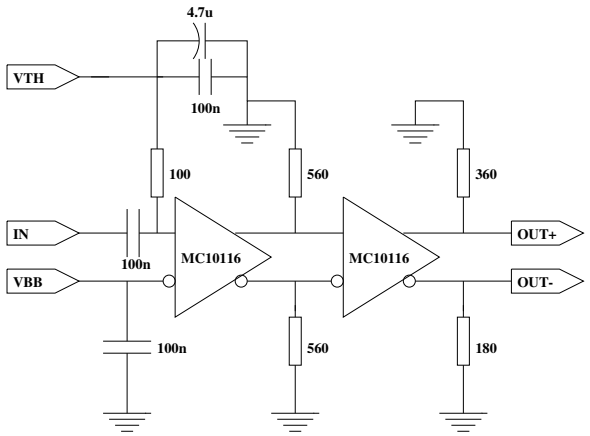

Figure 16: Circuit Diagram of the LPSFLT 1 channel Driver Circuit

Since good results were obtained in the lab, a prototype of this scheme was mounted and installed in the HERA tunnel, the TEKZ being mounted on a chip carrier, and left operational during 1992 data taking in order to check reliability, noise and pick up in the tunnel environment under normal machine operation. A receiver board was built and installed in the LPS electronics hut in order to analyse the signal. Under these conditions we used input calibration signals to measure the noise of the amplifier, and found $\sim$ 1400 electrons which was a factor two higher than the specifications, mainly due to the chip carrier filter connections, but was still very good for our purposes. Cross talk was checked to be negligible up to input charges of 12 fC (we recall that 1 MIP in silicon corresponds to $\sim$ 4 fC).
Given the satisfactory results of the test we chose *scheme b* which has the following advantages:

- only one chip/detector mounted on the front end board, which means fewer bonds, lower operating temperature, fewer control cables to the pots, and greater reliability,
- better performance of the amplifier-comparator chip,
- use of the same amplifier as used in the LPS standard planes,
- use of the same power supply and same control software as for the standard LPS planes.

5 Assembly and Test

5.1 Design and Realization of Multilayer Cu-Invar Support

The multilayer support for the trigger detectors and the front-end electronics has been partly designed with PCAD at Torino and partly at CERN [26]. This support is a 6 layer double surface mounted device. The opposite faces of the support are both designed to support detectors, amplifiers, SMD filters, and output fan out. The technology used allows strip lines with 100 μm pitch. Given the limited size of the trigger detectors, in order to keep the preamplifier far from the beam, and to avoid inhomogeneous materials in front of the other LPS planes, we decided not to connect the TEKZ directly to the detector. The detector is bonded to strip lines (typical length of the order of $2 \div 4$ cm) which are then bonded to the amplifier (see Fig. 17). For this purpose we require a maximum strip capacity of 1 pf/cm. These values have been checked to be correct on the fabricated multilayer.

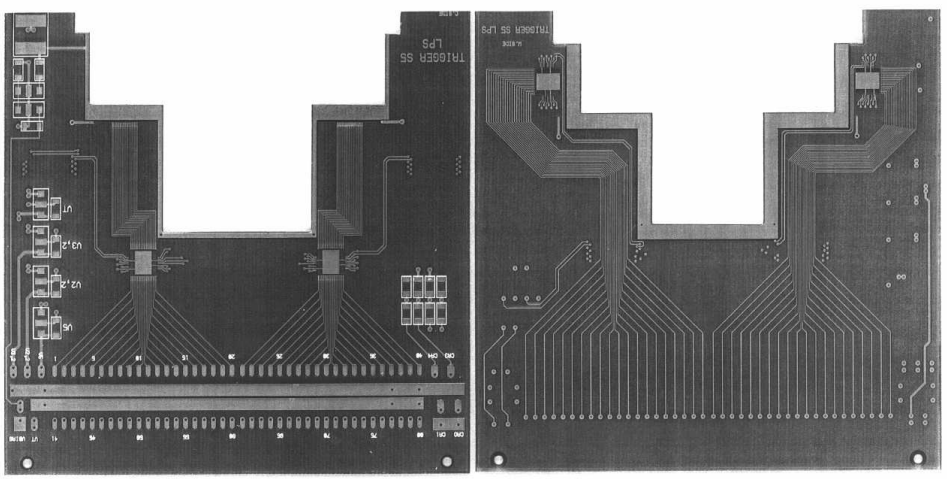

Figure 17: The two sides of a LPS FLT front end multilayer support. NB: the two supports are slightly different versions of the S5 support, and this is why the contour geometry is different

On each side of the multilayer support, as one can see from Fig. 17, there is place for two TEKZ chips. On one side (Fig. 17a), there are also all the SMD components (these are all the LCR power filters for the TEKZ and the detector power lines) and the 80 readout pads.
Two calibrations lines (`CAL1` and `CAL0`) are used, out of four available on the TEKZ. These are sufficient since we use only 20 out of 64 available TEKZ channels. `CAL0` is bonded to channels 0,1,18,19 and `CAL1` is bonded to channels 2→ 17.
Each support was carefully checked before mounting by controlling all connections and insulations.

5.2 Assembly and Bonding

Detectors, FE electronics, HV filters and connections were assembled on the multilayer support at the Torino INFN laboratory. In order to glue the detectors with good position accuracy, special support boxes were built which allowed also the

mounting of the detectors and electronics on both sides of the multilayer support and then served as final transportation boxes.
After all the SMD components had been soldered on the multilayer board, the detectors were glued with conductive epoxy with an accuracy of $\sim 100\mu m$ using the wire bonder microscope. TEKZ's were glued with non conductive epoxy. Both sides of the board were finally bonded, with a total of 284 bonds per board.
A picture of a fully mounted trigger plane (S4) is shown in Fig. 18. One can see the two detectors with vertical strips on the two sides (left and right). The horizontal strip detectors are not visible in the picture (they are glued on the other side of the the same support in the same geometrical position as the vertical detectors).

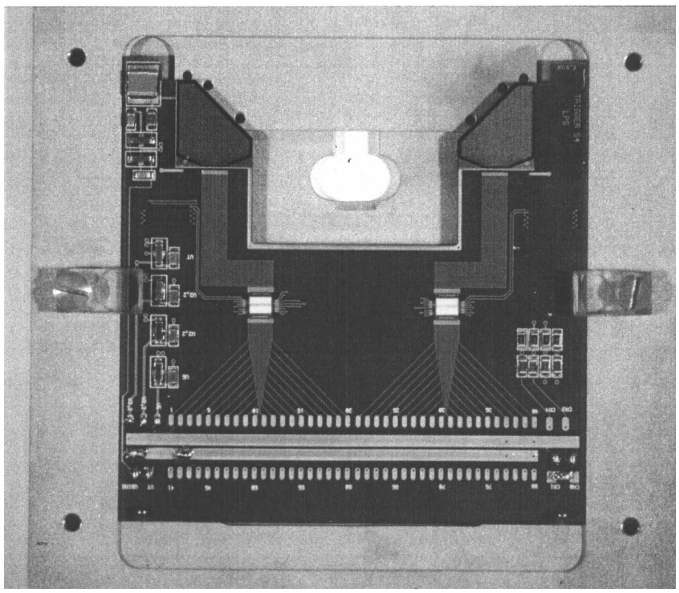

Figure 18: LPSFLT (Plane S4) after assembly

5.3 Lab Test

After assembly, each plane was tested with the calibration lines and with a radioactive source, in order to check all channels and all bonds. Few channels, out of the three trigger boards, were found dead, due to faulty channels in the amplifier/comparator chip. The TEKZ channel in this cases had to be unbonded and the neighbouring channel was rebonded to the strip.
TEKZ noise and gain were measured again in the final configuration, that is with the amplifier bonded to the detector and the detector bias powered on the final multilayer printed board. The gain (see Fig. 19) is measured by injecting different input charges to the amplifier through the calibration line and by measuring the threshold value, called $(V_{3.2} - V_t)$, at which the comparator output rate is 50% of the input rate. This leads to a measured gain of 152 mV/fC with a comparator offset of 134 mV. The noise is measured by injecting a fixed charge in the amplifier and by varying the threshold at steps from the 100% efficient point to 0 output rate (see Fig. 20). The noise can be estimated by measuring the FWHM of this erf

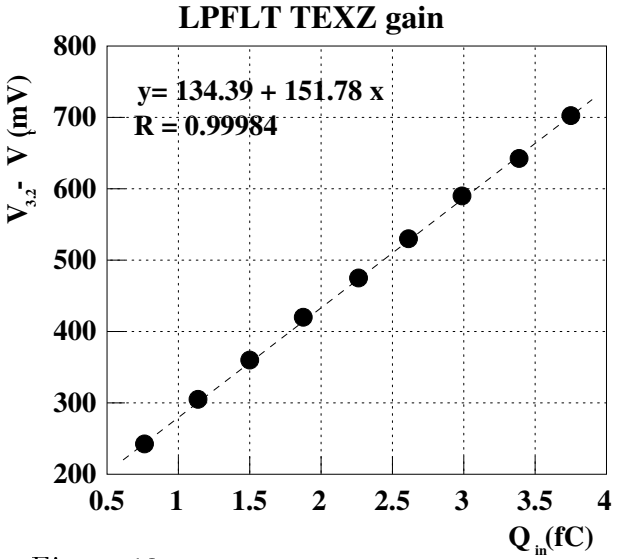

Figure 19: LPSFLT TEKZ gain measurement

distribution (by taking the width between the 12% and 88% points) and using the measured gain of the amplifier (Fig. 19) to convert this value in *equivalent noise charge* (enc). We find $\sigma_{noise} = 1045$ electrons, which correspond to a signal over noise ratio of $S/N = 25$.

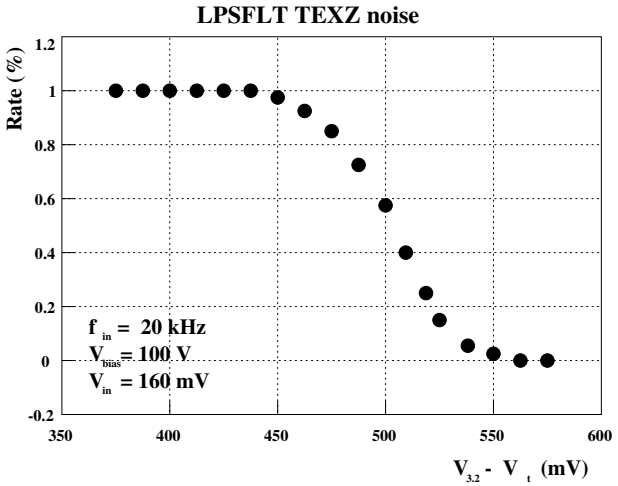

Figure 20: LPSFLT noise measurement

This value is nicely consistent with the strip capacitance measured in the lab (see Section 3.3) as one can see from the relationship [24]

$$\sigma_n = 690 + 40C,$$

since the detector strips are on average 1 cm long and we measured (see section 3.3) a typical strip capacity of 4 pF to the backplane in parallel with 2.5×2 pF interstrip capacitance.
Finally we made a geometrical survey of the position of the strips with respect the two assembly locating pin holes which are visible at bottom of Fig. 17, and which

are used to accurately mount the trigger plane in the LPS mechanical supporting hand. The survey was done using the x-y moving platform of the probe station. The precision achieved on the location of the strips was better than $10\mu m$. The final alignment will be determined using reconstructed LPS tracks.

6 Readout Electronics and Trigger Logic

6.1 General Layout of the LPS First Level Trigger

As has been described in Section 3.2, the trigger is organized with 2 left and 2 right detectors per station (stations *S4up*, *S5up*, and *S6up*). The two pairs (left and right) have two orientations, horizontal and vertical. Each detector has 20 strips and is read out independently. Left and right triggers are completely independent. In our convention $left$ means toward the HERA center.
The LPS has 13 bits reserved at the GFLT. We use 6 bits, defined as follows:

- bit 6: No Momentum Cut Right (triple coincidence)
- bit 5: No Momentum Cut Left (triple coincidence)
- bit 4: Momentum Cut Right (double coincidence)
- bit 3: Momentum Cut Left (double coincidence)
- bit 2: Momentum Cut Right (triple coincidence)
- bit 1: Momentum Cut Left (triple coincidence)

Bit 6 is defined as (see Fig. 21 for trigger plane names definition) :

$$(S4HR\ .AND.\ S4VR)\ .AND.\ (S5HR\ .AND.\ S5VR)\ .AND.\ (S6HR\ .AND.\ S6VR)$$

while bit 5 is:

$$(S4HL\ .AND.\ S4VL)\ .AND.\ (S5HL\ .AND.\ S5VL)\ .AND.\ (S6HL\ .AND.\ S6VL)$$

where S4HR is a hit in ANY of the 20 horizontal strips of the right detector in S4, and so on for the other detectors. This is the trigger which we called "No Momentum cut" since we do not use matrices to impose a restriction on track momentum. The sketch of this trigger is shown in Fig. 21.
Bits $4 \rightarrow 1$ make use of the matrix selection. 16x16 matrices are used to define a road on the linear correlation between two stations, described in Section 3.1. The detailed description of the matrix board is given in Section 6.4.
The difference between bits 3,4 and bits 1,2 is the number of pots used to trigger. In bits 3,4 a double coincidence

$$S4\ .AND.\ S5\ .OR.\ S4\ .AND.\ S6$$

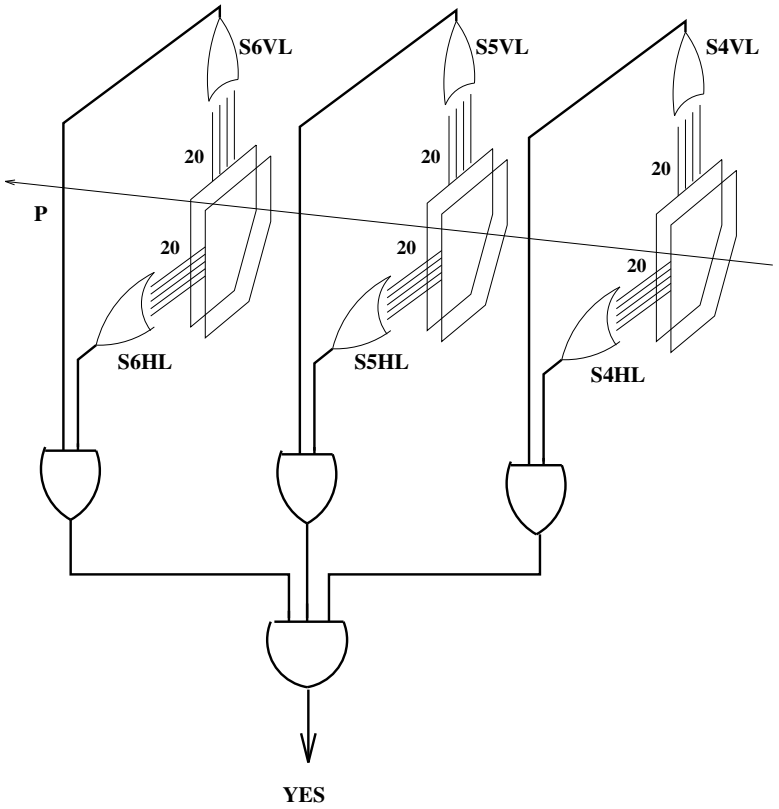

Figure 21: Sketch of the "No Momentum Cut" Trigger

is used whereas the full triple coincidence is used for bits 1,2. The logic of the (16x16) matrices is shown in Fig. 22. The triple coincidence is selected in the matrix called (AND,OR). This matrix works as a diagonal matrix for bits 5 and 6 and as a global OR for bits 3 and 4.
During 1995 data taking only bits 5 and 6 were used. The matrix boards were installed and put in operation close to the end of the data taking. The matrices were however operated like the *No Momentum Cut* trigger, that is with all matrices bits set to 1, because further trigger rate limitations were not required by data taking conditions.
The global structure of the trigger electronics and its interface with the GFLT is sketched in Fig. 23. The signals from the LPSFLT detectors (sketched as small trapezoids in the figure) go through a microtwisted pair cable to the LPS_TRS board (see Section 6.2). From here the signals are transmitted through a 100 m twisted pair cable to the LPS_PIPE board placed in the LPS hut. The details of this board are described in Section 6.3. The main task of this board is to split the signal, after a global latch, to the trigger matrices (LPS_MAX card, see Section 6.4), and to the readout pipeline and primary buffer (the length of the primary buffer being 18). The trigger signal from the LPS_MAX board is sent to the GFLT through the LPS_GFI board (see Section 6.5). This card essentially forms the trigger signal in the correct bit format before sending it to GFLT. A similar board with a totally different function is branched to LPS_MAX to form an alarm signal in case of high rates. The

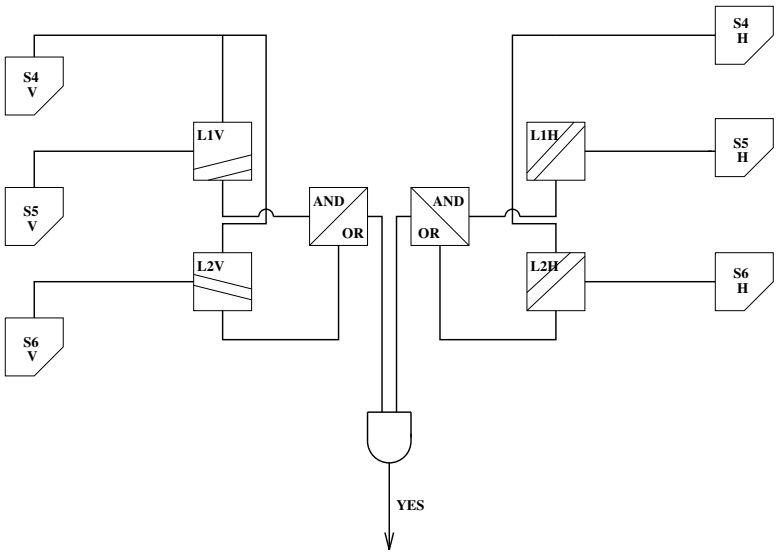

Figure 22: Sketch of the "Momentum Cut" Trigger

specific alarm logic for this board (LPS_ALARM) is described in Section 6.6.
The LPSFLT trigger electronics is fully contained in a VME crate, see Fig. 24. There are 13 LPS_PIPE boards (one per detector+one used as crate monitor), 4 LPS_MAX boards for the trigger matrices, 1 LPS_GFI module for the GFLT interface and one LPS_GFI module programmed to operate the trigger alarm (LPS_ALARM).

6.2 The LPS_TRS Card

The basic cell structure for one channel in this board has been already shown and briefly described in Fig. 16. The signals coming from the front-end electronics are fed through a 1 m microtwisted pair cable to this board. The board receives the single ended signal out of the front end amplifier (a shaped signal of $\sim 150mV$), and transforms it to a double differential ECL signal. The signal is then sent to the LPS hut, through 100 meters of twisted pair cables, to the input of the LPS_PIPE board. Each board has 20 channels, and it is connected to a given trigger detector. These are 4 LPS_TRS boards for each station, assembled in a small custom crate placed in the vicinity of the pot (see Fig. 25).

6.3 The LPS_Pipe Card

6.3.1 Functional Description

In this section, the functionality of the card will be explained. Fig. 26 shows a block diagram of the LPS_PIPE module.
The description follows the data path, starting where the data enters from the frontends.

Syncronizing Fifo

The hit pattern (20 bit) from the tunnel is received by differential positive offset ECL (PECL) receivers and enters a short fifo. This fifo allows data from different

distances along the beam to be resynchronized to a common clock thus simplifying further data treatment.
The closer the detector is to the interaction point (and the LPS-hut) the more delay is needed to phase match with the detector farthest away from the interaction point. In order for the fifo to work correctly, the depth must be programmed. This consists of 2 values: coarse delay and fine delay. The coarse delay is the delay in number of clocks, and fine delay in units of 4 ns per step. There are 3 coarse delay steps and 32 fine delay steps.
In order for a delay to be valid, the programming of the register must be followed by an INIT. INIT is the action which clears the pipelines and circular buffers in all frontends.

Barrel Rotater

After the re-phase fifo, the 20-bit hit pattern, splits up into a barrel rotater, and a scaler. The barrel rotater allows to rotate the 20-bit base word to the right by 0 to 4 positions. This feature allows selection of a slice of 16 bits out of the 20 bits. It is used to limit the amount of data which passes to the downstream matrix logic thus simplifying this logic. The barrel rotater is fully software programmable, which allows the *position* of the 16 active bits to be moved relative to the main detector geometry.

Online test pattern injection, DINAMTEST

To allow dynamic tests of the logic, a simplified testpattern injection scheme has been incorporated. The pattern is fixed, only the moment of its application can be programmed. The test pattern is 00001000010000100001. This pattern is applied to the *entry* of the barrel rotater, and it replaces the hit pattern from the sync-fifo, when the frontpanel input signal JAMTEST (on the upper connector) is true. Normally it is the global LPS read-out controller (ROC) and GFLT which is responsible for application of this signal. All LPS_PIPE cards will receive this signal simultaneously. The testpattern does *not* pass through the scaler and Veto circuit. The veto remains connected to the online data through the mask register. Note that it is possible to change the test pattern to some extent, by using the barrel rotater to shift the pattern, and eventually OR it with itself. This mode is a tool for offline testing, because it is not possible to change the barrel rotater with the JAMTST signal.

Scaler, counting of number of hits

Before passing to the scaler, all the 20 hit's are gated by a mask register. This allows disconnection (when corresponding maskbit = 1) of the associated strip. The scaler counts the number of hits in every crossing and accumulates the number of hits in a 20 bit register. An interrupt can be generated when a certain number of hits has been reached, or the register can simply be read by polling at convenient intervals.

Veto

The scaler also supplies a veto signal associated with each crossing. This veto is true if the number of hits per crossing is higher than a programmed limit. It takes effect immediately after programming and need no activation command. Programming a veto limit of > 20 will effectively disable the veto, as there can never be more than 20 hits. Programming veto limit to 0 correspond to veto being equal to the logic OR of all the bits. The veto is subjected to the same mask register as the hit count accumulator.
The veto signal is passed onto the lower frontpanel connector together with the hit

pattern and the error flag. The veto signal is *not* in phase with the associated hits, but delayed by 2 clocks cycles (due to the pipeline time it takes to calculate the veto). This difference in delay is corrected in the LPS_MAX, since in the LPS_MAX the matrix takes more time than the veto-gating so that the two signals line up again.

LPS L1 fatal error flag

An error flag is set true by the control, whenever the resync-fifo is being restarted (after an INIT signal) since during this period the hit patten is corrupted. This error source can no be cleared. It goes away by itself after about 10 clock cycles.
In addition, the error flag is set when the HERA machine clock, as seen by the LPS_PIPE module, is unstable, either too fast or too slow.
This flag is cleared by a hardware system reset or by setting a dedicated bit to zero. The clock error flags can generate interrupts, if enabled.

Offline Static Test data Injection

In static test-data injection mode, hitpatterns are injected, under VMEbus control, into the *entry* of the sync-fifo. This pattern is static, in the sense that it does not change with the HERA clock, but by VMEbus commands. This mode is only intended to test the data path through the cards in the trigger, and obviously only makes sense while in offline mode.

Online Data-Passing mode or Monitor mode

The LPS_PIPE card can operate in two major modes: "Online data-passing mode", which is the most common mode, and in the "monitor mode".

1. In the "Online data-passing mode" data from the front-end passes to the lower back panel connector and (normally) into the LPS_MAX for coincidence calculations. In this mode the lower frontpanel connector is an output signal connector.

2. In "monitor mode", data are can injected into the lower frontpanel connector, and they are passed through the pipeline and the circular buffer in the same way as if they were online data. In this mode, the front-end signals are completely ignored, and the lower frontpanel connector is an input signal connector. This mode allows online monitoring of the functionality of the LPS_MAX. By adjusting the length of the pipeline to account for the delay through the LPS_MAX, it is possible to record with every GFLT L1 accepted event the corresponding LPS_L1 tags. It is *not* possible to see the LPS_L1 tags for events which were rejected by the GFLT. This mode is the default after a hardware system reset.

   Whichever is the mode, only 18 bits can be recorded in the pipeline and its following circular buffer.

Pipeline control

In "Online data-passing mode", the data from the sync-fifo pass the barrel rotater before being applied to the frontpanel lower connector. This leads the data to the LPS_MAX. The data going to the lower front panel connector also go into the pipeline fifo, where it awaits the L1 decision. The length of the pipeline must be adjusted such that the L1 decision for the corresponding crossing arrives at the same time as the data at the output of the fifo. In practice all the LPS_PIPE's will need

the same pipeline length. The length of the pipeline is fully programmable in the range 1 to 64 crossings. The proper value must be found during installation and in principle never changes.
In Monitor mode, the data to the pipeline does not come from the barrel rotater (frontend), but from the lower frontpanel connector. In this mode the lower frontpanel connector is an input signal connector.
Circular buffer control
The L1-accepted events, awaiting L2 decision, are stored in a circular buffer with up to 255 entries (18 bit wide).
The buffer can be controlled from the Read Out Controller or by VMEbus commands for offline analysis.
The normal circular buffer operational mode is so called **ONLINE_MODE**. In this case the LPS_PIPE card is controlled from the ROC.
It can also operate in offline modes, so called **ROC_STREAM_MODE** and **VME_STREAM_MODE** where commands are coming from the ROC as well as the VMEbus (for details see [32]).

6.3.2 Implementation details

The core of the module is implemented in two ALTERA FLEX8820-R208 programmable logic devices (PLD). They are packaged into 208 pin quad-flat-packs. In addition there are two fifo's, 18bit * 256 deep, holding the pipeline and the circular buffer.

- **Control PLD:** In this PLD are the state-machines which provide the fifo functionality. In addition it holds the VMEbus interface, hit pattern register after the circular buffer, and numerous auxiliary functions. This PLD can be booted either from a serial EPROM (normal mode) or from a 10 pin scotchflex connector using ALTERA's serial passive boot protocol and the "BitBlaster" or similar device.

- **Frontend PLD:** In this PLD are located sync-fifo, the barrel rotater, the scaler and the veto processor. This PLD, must be booted from the VMEbus every time power is cycled or a reboot command is issued. It is booted in passive parallel asynchronous mode.

Almost all components are surface mounted to gain space.
The two PLD's support IEEE Std. 1149.1 JTAG boundary scan for production testing of chip interconnects. They are chained on the same scan path onto a 10 pin connector. The PLD's are the only components supporting JTAG testing on this module, so in order to profit from this technology the test must include extensive cluster testing capabilities. Notably it must be capable of testing the pipeline and circular buffer path, which is entirely connected to the PLD's, and thus in principle fully cluster testable, as all inputs, used on this card, can be controlled and all (used) outputs can be monitored.
The PCB has 6 layers: Gnd, Vcc and 4 signal layers.
All signals to/from the card, apart from the VMEbus, are differential. The advantage is that it is possible to use long flat unshielded cables for interconnect. Several meters should pose no problems as long as the delay is not an issue.

The machine clock frequency may go up to 12 MHz.

6.4 The LPS_MAX Card

6.4.1 Functional Description

In Fig.27 it is shown a block diagram of the LPS_MAX module, when configured as dual coincidence matrix. The input to the LPS_MAX consists of three 20 bit words plus a veto for each word. Each word comes from a detector, herein called S4, S5, and S6. Each bit in the words corresponds to a detector strip. If a particle has passed through this strip the corresponding bit is set to 1 or, for the use of this mathematical description, to logic TRUE. The signals are defined as follows:

- Input vectors $In(4)$,$In(5)$,$In(6)$ carrying hit patterns from the detectors.
- Veto for each input word: $Veto(4)$, $Veto(5)$, $Veto(6)$
- Matrices are two times 16*16 bits. They connect to the lower 16 bits $In(16..1)$ of the 20 bit long input vectors. The matrices are called $Matrix_{45}(i,j)$ for coincidence between word 4 and 5 and $Matrix_{46}(i,j)$ for coincidence between word 4 and 6.
- The masks for the no-momentum trigger are called $NomoMask_4$, $NomoMask_5$ and $NomoMask_6$ respectively. They are each 20 bit long vectors.
- The masks for the rate counter alarm are called $AlarmMask_4$, $AlarmMask_5$ and $AlarmMask_6$ respectively. They are each 20 bit long vectors.

Multiplication in the following equations are boolean AND, whereas addition correspond to boolean OR. The symbol $\overline{Q}$ means boolean negation of Q.
With these definitions, the bits in $In4$ which coincide with bits in $In5$ is a vector called Z_{45}. This vector is not available external to the LPS_MAX, its an intermediate variable inside the processor. It can be written:

$$Z_{45}(j) = In_4(j) \times \sum_{i=1}^{16} In_5(i) Matrix_{45}(i,j) \tag{3}$$

Likewise for coincidence between $In4$ and $In6$:

$$Z_{46}(j) = In_4(j) \times \sum_{i=1}^{16} In_6(i) Matrix_{46}(i,j) \tag{4}$$

The coincidence between $In5$ and $In6$: Z_{56} is not available.
If one or more coincidences exist between the bits in Z_{45} and Z_{46} this correspond to a hit pattern from one or more particles which has passed all detectors. The veto is set to 1 if the corresponding input vector In has too many bits set to one. This is typically the case for very noisy events, since it does not make sense to reconstruct tracks with too much noise. The veto disables any trigger results for this event. The veto is generated in the LPS_PIPE module and the number of bits necessary to

activate a veto is programmable from the VMEbus[32]. This result is called $L1_{456}$ and the equation is:

$$L1_{456} = \overline{Veto(4)}\,\overline{Veto(5)}\,\overline{Veto(6)} \sum_{k=1}^{16} Z_{45}(k) Z_{46}(k). \tag{5}$$

If one is only interested in tracks from S4 to S5 the equation for the corresponding signal is:

$$L1_{45} = \overline{Veto(4)}\,\overline{Veto(5)} \sum_{k=1}^{16} Z_{45}(k), \tag{6}$$

While for S4 coincidence with S6 is:

$$L1_{46} = \overline{Veto(4)}\,\overline{Veto(6)} \sum_{k=1}^{16} Z_{46}(k). \tag{7}$$

To count the rate of events one counts the rate at the outputs $Alarm(4)$ to $Alarm(6)$. The bits first pass the mask vector. Note that programming a logic 0 into the mask lets the corresponding bit pass through. This is the opposite of what is used for the matrices! The alarm outputs are described by the equations:

$$Alarm(4) = \sum_{i=1}^{20} In_4(i) \overline{AlarmMask_4(i)}, \tag{8}$$

$$Alarm(5) = \sum_{i=1}^{20} In_5(i) \overline{AlarmMask_5(i)}, \tag{9}$$

$$Alarm(6) = \sum_{i=1}^{20} In_6(i) \overline{AlarmMask_6(i)}. \tag{10}$$

Similarly the so-called "no-momentum trigger" is defined for each word as in eq. 11 to eq. 13.

$$L1_{nomo}(4) = \overline{Veto(4)} \sum_{i=1}^{20} In_4(i) \overline{NomoMask_4(i)}, \tag{11}$$

$$L1_{nomo}(5) = \overline{Veto(5)} \sum_{i=1}^{20} In_5(i) \overline{NomoMask_5(i)}, \tag{12}$$

$$L1_{nomo}(6) = \overline{Veto(6)} \sum_{i=1}^{20} In_6(i) \overline{NomoMask_6(i)}. \tag{13}$$

Note that the veto when set disables the trigger. These signals are actually available at the output of the LPS_MAX, but in the initial configuration, they will not be used outside of the module. They currently serve (internally) to generate the complete no-momentum trigger by $AND'ing$ of the individual $L1_{nomo}$ triggers, as:

$$L1_{nomo} = L1_{nomo}(4) L1_{nomo}(5) L1_{nomo}(6). \tag{14}$$

This result is send to the LPS_GFI for combination with the other 3 detector sets.

6.4.2 Implementation details

The core of the module is implemented in one ALTERA FLEX81500 programmable logic device (PLD) packaged into 304 pin quad-flat-pack. In addition another PLD EPM7032 handles the VMEbus interface.
In Fig.28 it is shown a block diagram of the LPS_MAX module, without details of the particular configuration down-loaded into the PLD.
Both PLD's are programmed using ALTERA's MAX+PLUS-II compiler running on the SUN sparc workstation. The PLD's are verified in a VHDL test-bed simulating the VHDL output file generated by the MAX+PLUSII compiler. In the test-bed, a random input pattern and mask pattern is loaded into the device, and a VHDL behavioral model is used to verify the functions. The tool used is LeapFrog.
Also in this board almost all components are surface mounted to gain space, and all signals to/from the card, apart from the VMEbus, are differential.
The machine clock frequency may go up to 18 MHz.

6.5 The LPS_GFI Interface Card

6.5.1 Functional Description

Referring again to Fig. 23 on page 31, the block diagram of the LPS L1 trigger electronics, the LPS_GFI module combines the trigger results from the sub-triggers and submits them to the GFLT together with the BUSY signal from the LPS main detector.
In this section, the functionalty of the card will be explained.

Clock monitor

When the Hera machine clock disappears for several 100 ns, a circuit detects this occurence, and sets a dedicated bit in out-signals register. To clear this, firstly the clock has to be present, secondly one should either write a 0 in the location which gives the relation between the fine+coarse delay and the effective delay, or one can make a VMEbus system reset. The VMEbus system reset does not itself require a reboot as the LPS_GFI. Only cycling of the power will require a reboot.

Bunch crossing counter monitor

The component bunch crossing counter (CBC) is a free running counter, counting 0,1,..219,0,1,2.. Only once per accelerator revolution, it is preloaded with the reference value. BCN0 is the flag used for this function. BCN0 is sort from the GFLT. In other words, when BCN0 is true, the value in the register cnt_At_Bcn0 is loaded into the CBC. The count value is valid in the period after the positive clock edge which samples the flag true. A circuit compares the CBC count at BCN0 with the cnt_At_Bcn0 value, and if they differ, an error flag is set. The flag is cleared in the period after the positive clock edge which samples the flag true. This flag is cleared by a VMEbus system reset.

Monitor ports

To facilitate system debugging and to make online histogramming of the system performance, one can take snapshots of the trigger data passing the LPS_GFI. The output signals are sampled at a moment where they are corresponding to the sampled insignals, so a consistent set of data is supplied.

6.5.2 Implementation details

The core of the module has uses the same components of the LPS_PIPE module (see Section 6.3.2). In addition there is a non volatile PLD making interface with the VMEbus.
The signals to the GFLT are differential ECL referenced to -5.0V, and not -5.2V as is usually used. Measurements has shown that the performance difference between the two types of supplies is insignificant.
The machine clock frequency may go up to at least 15 MHz.

6.6 The LPS_ALARM Card

6.6.1 Functional Description

The rate in the Level 1 trigger detectors is a good measure of the radiation flux in the pot containing the ensemble of detectors including the LPS main detectors. To find the count rate, the ideal would be to count the number of hit strips, but this approach is rather expensive in hardware. Much simpler is it to do a logical OR of all the strips in one detector (20 channels). This gives the exact rate only when there is one or zero hit strips per crossing, but with low dose rate, this is a good approximation
By counting the event rate on this OR signal, one can obtain a good measure of the rate in the detector. The LPS_MAX supplies this logical OR for each of the 3 detectors attached to it. See details on Fig.29 where a block diagram of the alarm system is shown.
To lower the noise level, one may mask individual strips before the OR so that they do not contribute to the logical OR. Typically one would mask out strips which by experience are found to be noisy. This mask register is called the Alarm-mask-register, and is located in the LPS_MAX module [33].
The qualified *OR*-signals from all 12 detectors are collected together in the LPS_ALARM module. This module makes the necessary coincidence gating, measures the event rates and compares to threshold values. If the rate is out of range, an alarm is issued, and normally this will cause the detectors to automatically be removed from the beam region.
LPS_ALARM module is a multipurpose module. The same hardware serves as in the LPS's interface with the GFLT (LPS_GFI), the original application of this hardware. Because the module is programmable from the VMEbus, it is just a matter of loading the appropriate boot file into the module to have it working as an alarm module.
On the rear of the module on the VMEbus P2 connector, the alarm signal is output in differential TTL level. When the module is not correctly booted, this signals goes to Alarm active level. An adapter card attached from the rear to this connector converts the TTL level into a floating relay switched signal. The alarm is active when the switch is open.
Since the implementation details exactly match those of LPS_GFI module, we refer the reader to Section 6.5.2.

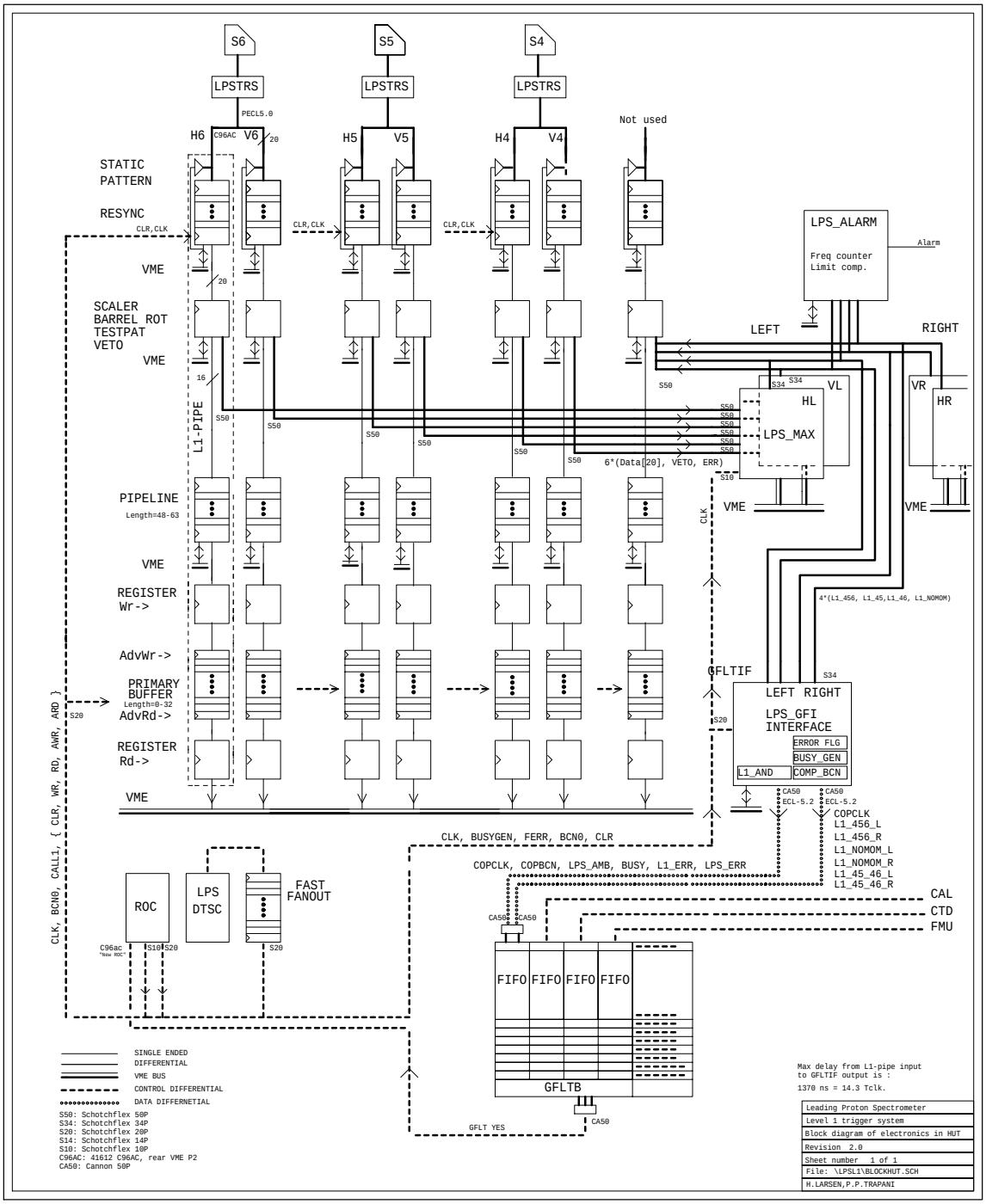

Figure 23: Global structure of the LPSFLT electronics

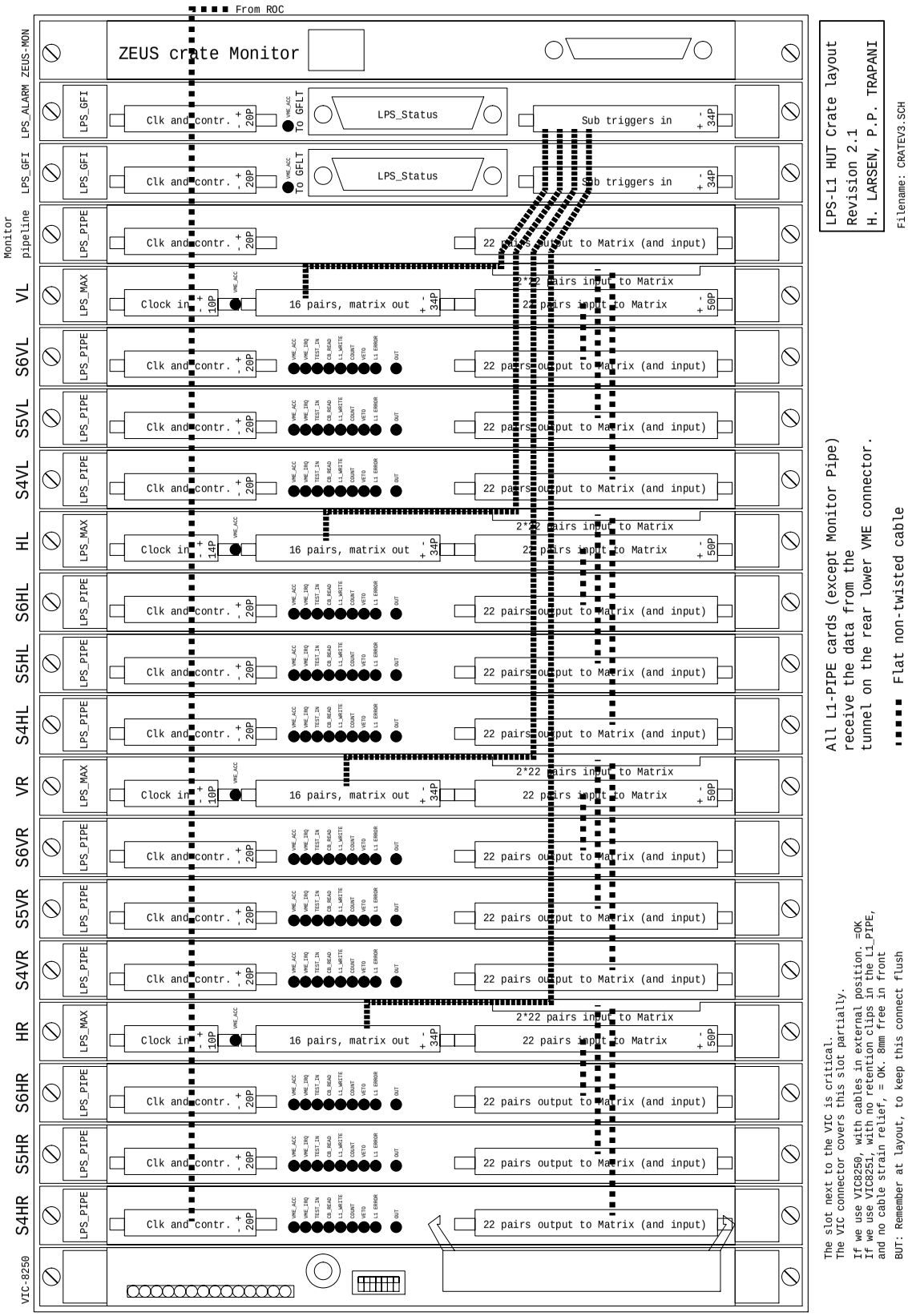

Figure 24: LPSFLT VME crate

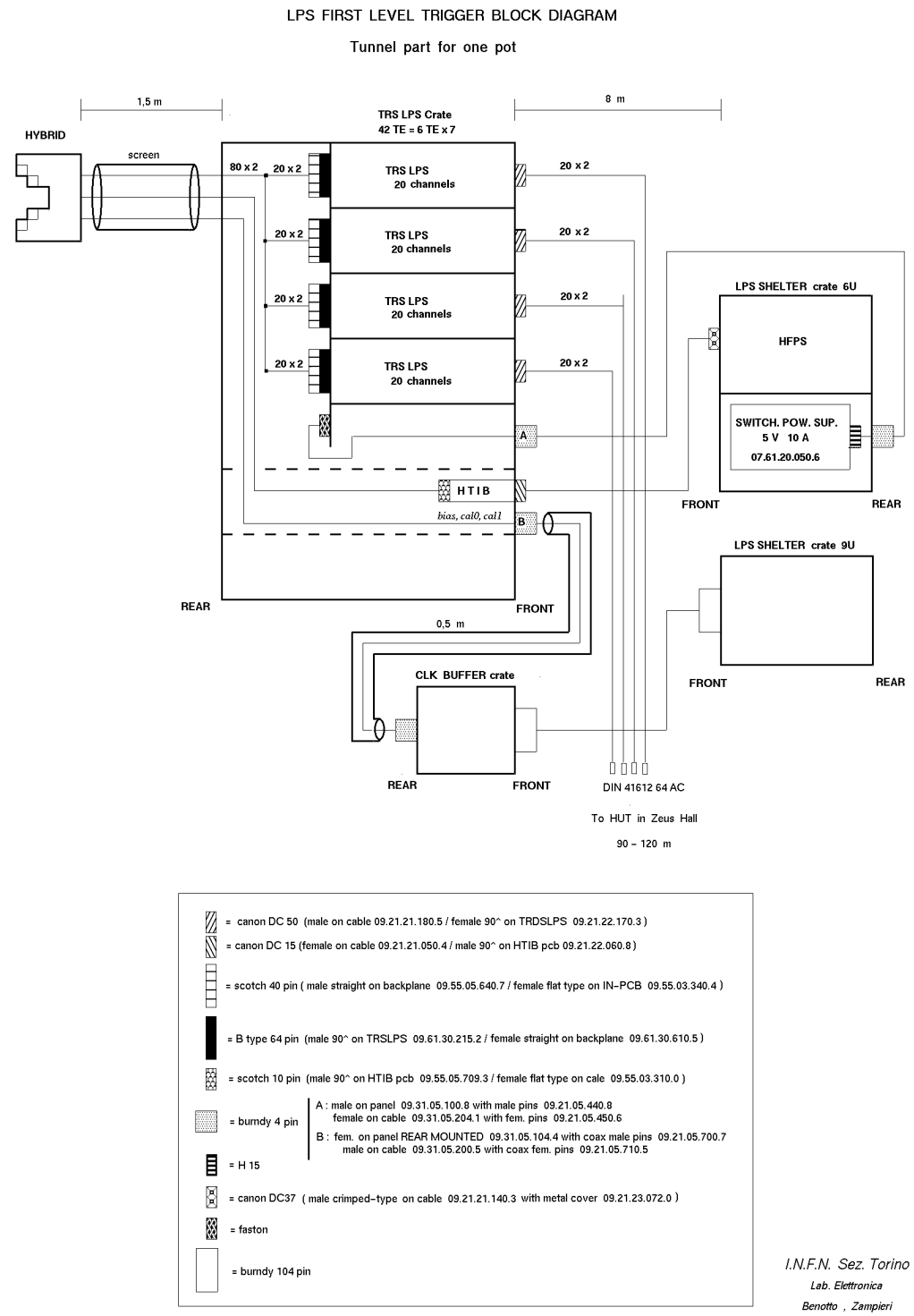

Figure 25: LPS_TRS Board

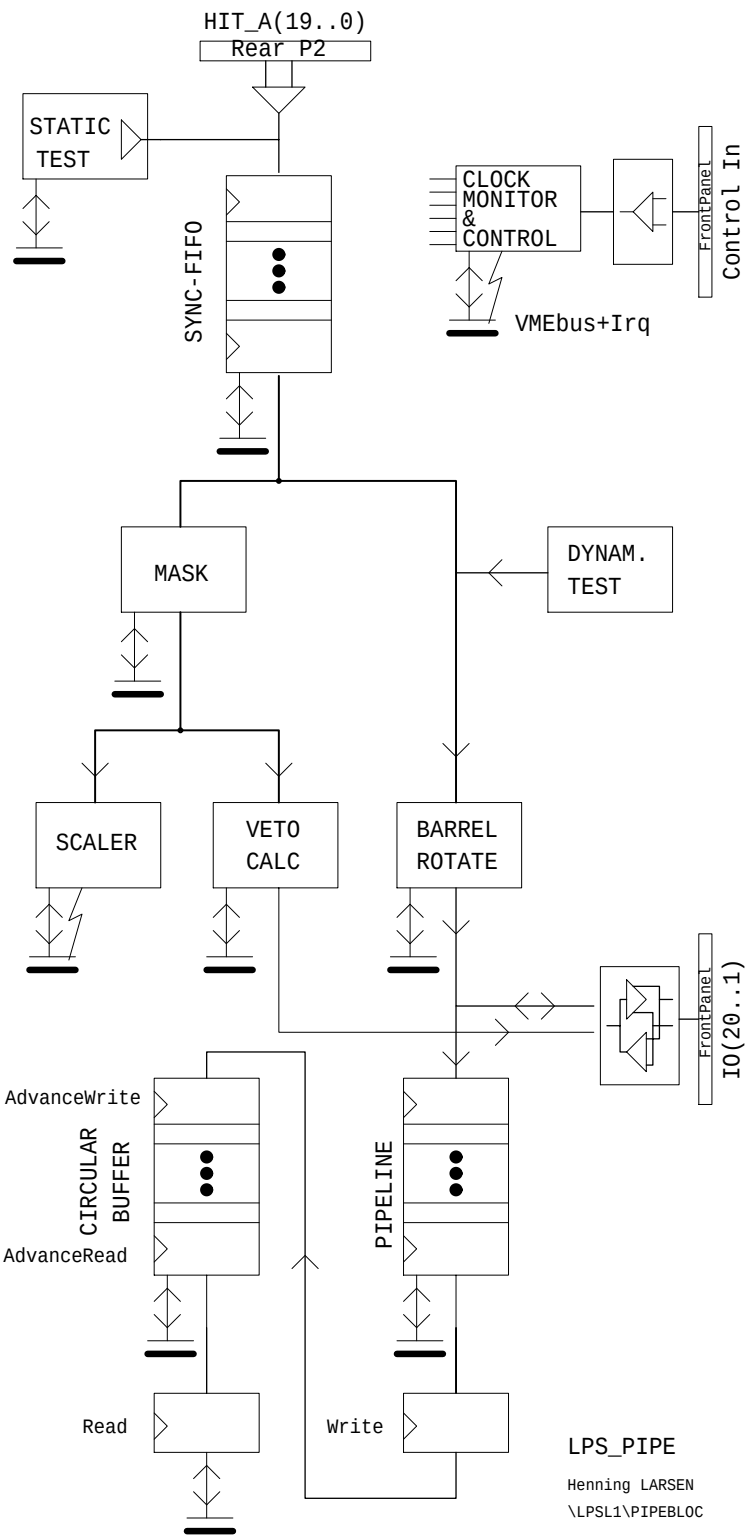

Figure 26: Simplified block diagram of the LPS_PIPE module.

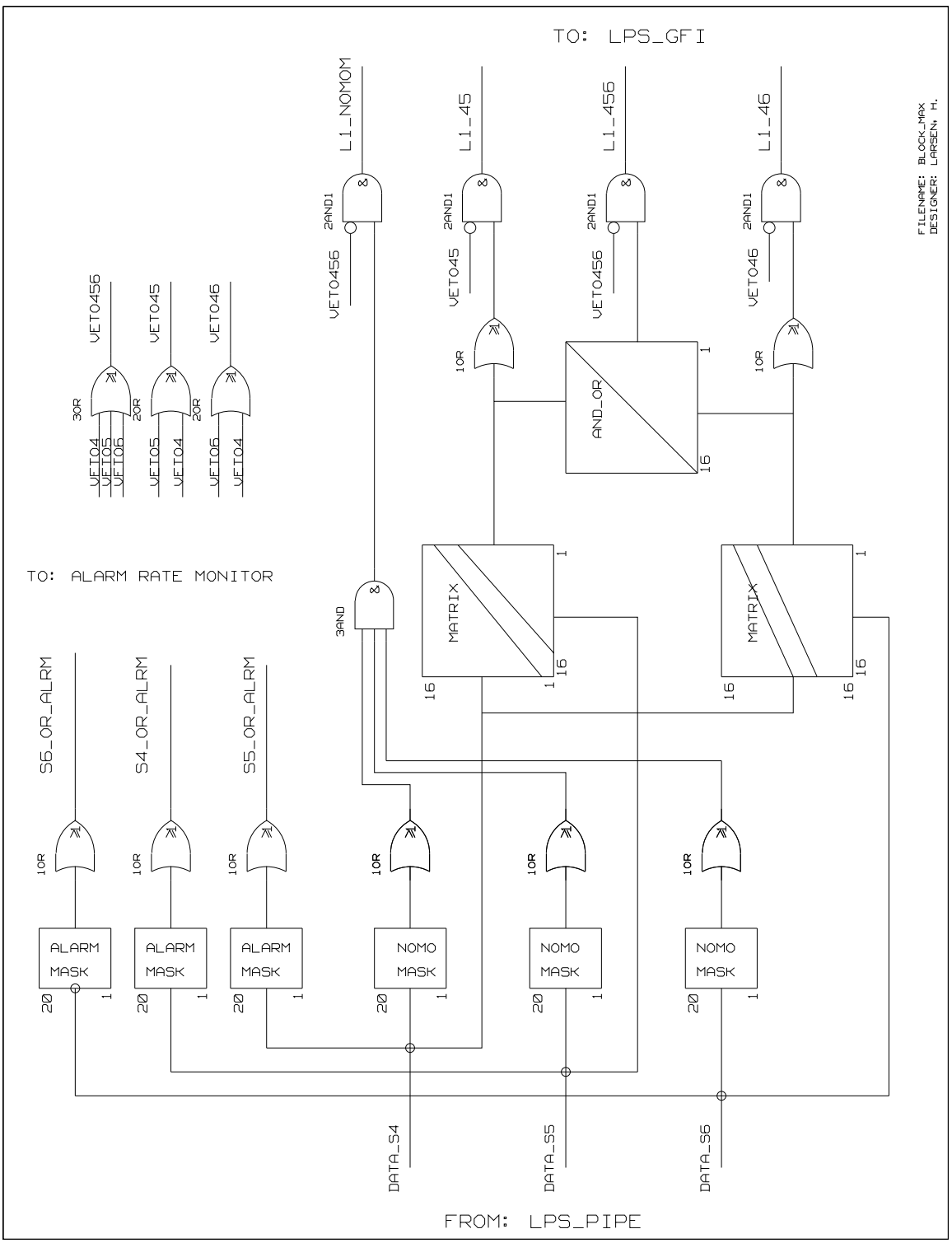

Figure 27: Simplified block diagram of the LPS_MAX module, when configured as dual coincidence matrix

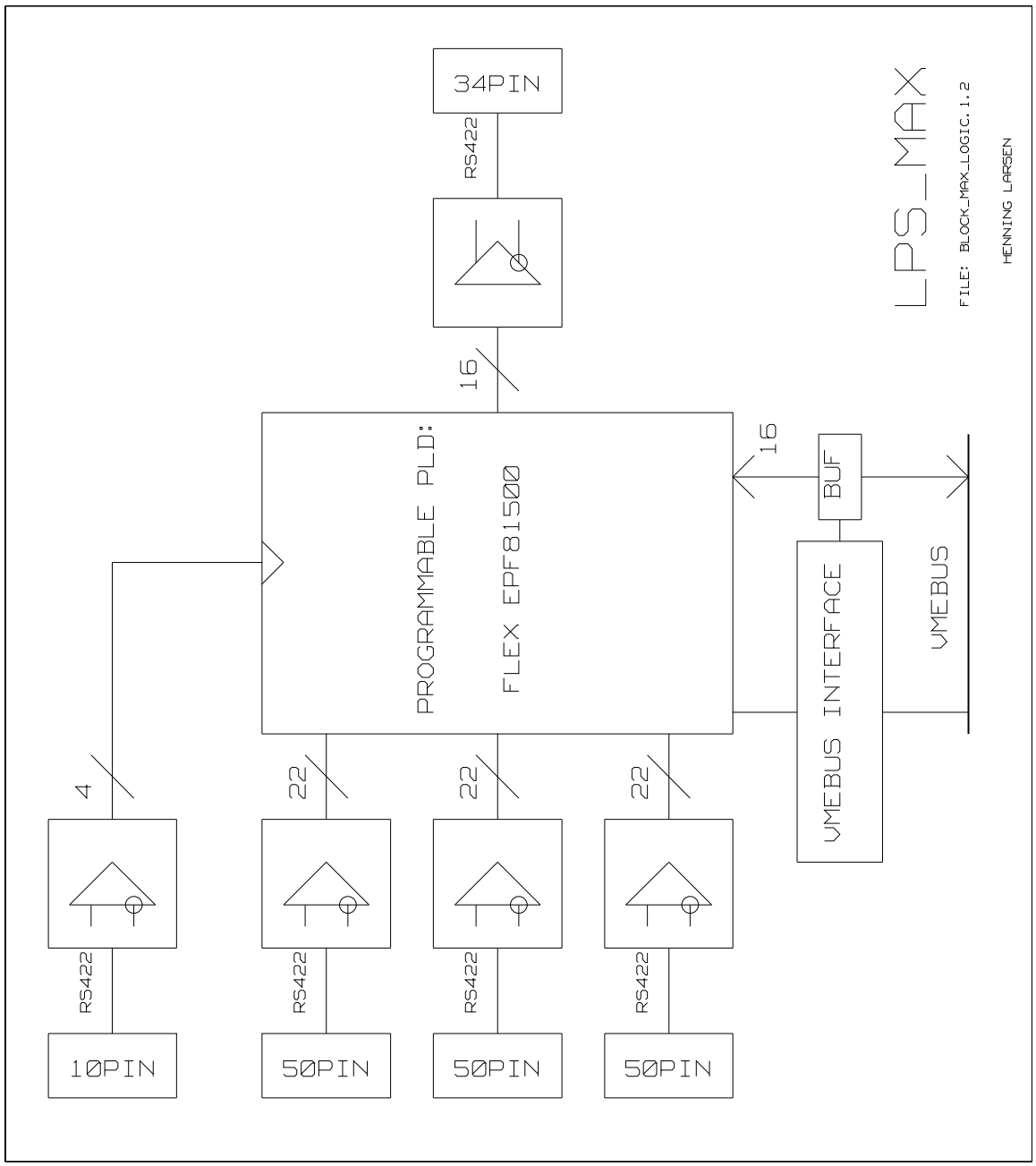

Figure 28: Block diagram of the LPS_MAX module. Without configuration details.

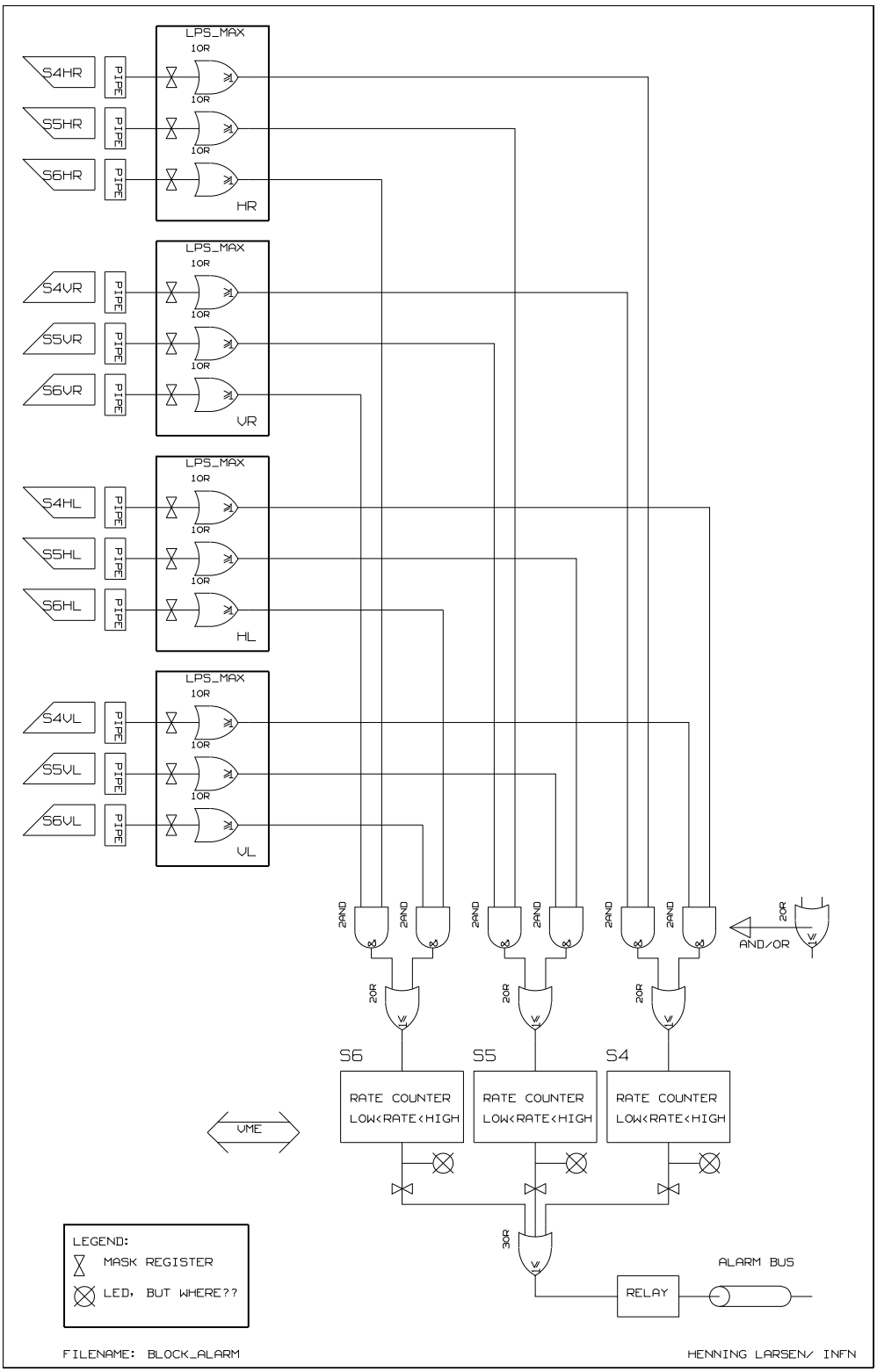

Figure 29: Simplified block diagram of the alarm system.

7 LPS Online Trigger Control

The LPS *equipment* computer, a Motorola 68030 processor (MVME147) running the OS9 operating system is installed in a VMEbus crate and interacts via TCP/IP and Ethernet with the LPS *component* computer, a microVax (LPSVXD) running VMS operating system.
A dedicated task running on the OS9 initializes the LPS FLT cards, since the frontend *pal* must be loaded with the correct "program" before being functional after a power cycle. The loading must be done from the VMEbus, passing through a dedicated register. First one has to reset the frontend PLD putting it in bootmode and then, following a special protocol for flow control, one can do the booting itself. This procedure is automatically performed at the initialization of the system, but the user can also do it, with some restrictions, via the OS9 local task `MON` (see [36]).
The setup parameters which the user can access are saved in a database. For each LPS_PIPE module one needs to set:
delay - Coarse and fine delays needed to syncronize the fifo to the MCK;
veto- Limit to be applied to the veto counter, expressed in terms of detector occupancy;
barrel shifter - A single byte to define the number of shift units to be applied to the barrel shifter;
scaler mask - A word to define which strips should be masked out in the rate counting;
revision - A word to define the module revision number.

For each LPS_MAX module one needs to set:
NOMO mask - A word to define which strips should be masked out when forming the no-momentum trigger signal;
ALARM mask- A word to define which strips should be masked out when forming the alarm signal. This word was simply taken equal to the corresponding scaler mask;
matrix - Two 16×16 matrices to program the coincidence logic; since this logic depends on the working position, the database contains the default setup values, but the possibility of modifing them before the acquisition starts is foreseen;
revision - An integer to fix the module revision number.

For the LPS_GFI module they consist of:
revision - An integer to define the module revision number.

For the LPS_ALARM module in correspondence of each pot there is:
enable - A bit to enable or disable the pot in the alarm logic;
threshold - The threshold (in Hz) to be applied to the counting rate to trigger the alarm system.
revision - An integer to fix the module revision number.

At every run SETUP all the parameter values are checked against the hardware ones, and any inconsistency returns an error to the Run Control.
The system is continuosly measuring the rate on each trigger plane integrated over

a time interval fixed by the user (and stored in the database). These rates are all written in the ENV triggers.
The status of the alarm as well as the rates are monitorable by means of the local program `MON`.
The trigger plane information is a fundamental quantity for the LPS automatic pot insertion procedure [35] and in this sense is also continously monitored via the local OS9 run control task `RC` (see [36]).
The LPS L1 trigger is normally disabled while we are moving the spectrometer into operating position and it is set to enable just before sending the LPS aquistion state bit.

8 Trigger Simulation (ZGANA)

The logic of the LPS First Level Trigger has been completely simulated and implemented in the ZEUS trigger simulation package `ZGANA` [27]. The reader will find in the `ZGANA` manual all the necessary information to run the LPS trigger simulation.
We made a preliminary analysis using different generators in order to calculate the LPSFLT trigger efficiency for various physics channels [29]. In order to do this we added few trigger slots with the LPS trigger to the `SUMMER93` trigger configuration, and generated various Montecarlo samples with the following generators:

- Diffractive DIS (NikZak) [8], [7];
- Photoproduction of Elastic ρ (HERWIG) [30]. The generation interval used with this generator is $40 \leq W \leq 150\ GeV$, $10^{-8} \leq Q^2 \leq 1 \times 10^{-2}\ GeV^2$;
- Diffractive Vector Meson Production (DIPSI) [12], [13], [14]. The kinematic range used for this generator is $10 \leq W \leq 300\ GeV$, $10^{-7} \leq Q^2 \leq 10^2\ GeV^2$. Here DIPSI is therefore used to explore a different kinematical region with respect to HERWIG.

The results are summarized in Table 1. The simulation assumes prescale 1 for all trigger slots which were enabled in `SUMMER93` trigger configuration. The fraction of events gained with the LPS for the NikZak generator with the present trigger is small ($\sim 4\%$), although interesting because extends the kinematical region toward high values of M_x^2. The LPS FLT slot however, already when compared with a low luminosity trigger like `SUMMER93`, can add an important fraction of events in the elastic ρ photoproduction channel, expecially in the low W range, as one can see by comparing the different acceptances of DIPSI and HERWIG (these two generators give the same results when compared in the same kinematic range, for a detailed comparison see [28]). Other important physics channels will be studied in future.
LPS and ZEUS triggers are affected mostly by uncorrelated background. While ZEUS trigger is mostly sensitive to proton beam gas, the LPS is sensitive to beam halo. Therefore it is appropriate to use the most general slot to include the LPS in the ZEUS trigger, that is `LPS.and.CTD`.
We also made an estimation with `MOZART` of the possible background due to beam gas. We assumed a beam gas rate of $0.49 kHz/m$ [31] at nominal HERA luminosities, and we generated a flat beam gas vertex distribution between -90 and +90 meters

	NikZak diffractive 2-jets events	Photoprod. HERWIG	Elastic J/Ψ Ryskin (DIPSI) decaying $\mu^+\mu^-$	Elastic ρ Ryskin (DIPSI) decaying$\pi^+\pi^-$
Total number of events	1000	1000	1000	1000
Acceptance after LPSF_NOM trigger (no momentum cut)	$6.1\% \pm 1.9\%$	$8.9\% \pm 0.8\%$	$6.1\% \pm 0.9\%$	$3.1\% \pm 2.1\%$
Acceptance after LPSF_hit trigger (momentum cut)	$3.1\% \pm 1.4\%$	$8.8\% \pm 0.8\%$	$4.5\% \pm 0.8\%$	$3.0\% \pm 2.1\%$
Acceptance after SUMMER93 trigger	$41.5\% \pm 4.0\%$	$26.2\% \pm 1.3\%$	$50.8\% \pm 2.0\%$	$5.8\% \pm 2.9\%$
Acceptance after SUMMER93.OR. LPSFLT	$43.1\% \pm 4.0\%$	$32.7\% \pm 1.4\%$	$52.1\% \pm 2.0\%$	$8.5\% \pm 3.5\%$

Table 1: Comparison of LPS trigger acceptance for different physics generators

(we used for this purpose the UA5 beamgas generator). The results are shown in Tab. 2. The acceptance for the combination `LPS.and.CTDany` is 0.009%, which corresponds under the above assumptions, to a trigger rate of 7.93 Hz. This rate is significantly reduced by using the combination `LPS.and.CTDgood`, as used during 1995 data taking.
Background due to beam halo has been estimated before installing the trigger by looking at the proton pilot bunches, during 1993 data taking [29]. We found $\sim 5\%$ probability of halo tracks being seen in the LPS in chance coincidence with a physics event in ZEUS, after rescaling the p-pilot bunch to the ep bunch currents.

	Total Entry=54000			
Slot	Prescale	Subtrigger	Entry	Effic.(%)
		GFLT decision (sum of all active slot)	1201	4.44
0	1	FMU⋆CALmx⋆aTRK⋆CVv(1250,464)	608	2.24
14	1	CAL_E⋆BMU⋆aTRK(464)	0	0.00
16	4096	RANDOM	0	0.00
17	1	RCAL_E⋆RMU⋆aTRK⋆CVv(464)	62	0.22
25	0	LPS_hit	5	0.009
33	32768	LUMI_Eg93490)	0	0.00
36	1	LEe⋆REMC_E(4999,464)	0	0.00
38	1	LEe⋆REMCth(4999,1250)	0	0.00
40	1	EMC_E(10068)	24	0.08
41	1	BEMC_E(3404)	20	0.06
42	1	Et(11574)	329	1.20
44	1	CAL_E(14968)	269	0.98
45	1	REMC_E(2032)	87	0.32
50	1	REMCth(3750)	304	1.12
54	1	REMC_E⋆aTRK⋆Fbpv(464,3750)	74	0.26
57	4	BEMC_E⋆aTRK(2032)	63	0.22
58	1	el_psi_test(2032,2500,3750)	114	0.42
65	0	LPS_NOM	44	0.08
66	0	LPS⋆CTDANY	5	0.009
67	0	LPS⋆LUMI_EE(5000)	0	0.00
69	0	LPS⋆FCAL_ISOMU_2⋆FCAL_EBPveto	0	0.00
70	0	LPS⋆CAL_NUM_ISOMU_2	0	0.00
71	0	LPS⋆CAL_NUM_ISOMU⋆RCAL_ISOMU	0	0.00
72	0	LPS⋆FCAL_ISOMU_EBPveto⋆CAL_ISOMU	0	0.00
74	0	LPS⋆REMC_E(464)	0	0.00
75	0	LPS⋆BEMC_E(460)	0	0.00
76	0	LPS⋆FEMC_E⋆FCAL_EBPveto(460)	0	0.00

Table 2: Trigger Efficiency for beamgas events integrated in the region $-90 \rightarrow +90$ m (UA5 model), as simulated with the 1993 trigger configuration. The prescale factors refere to the values used in the hardware configuration, whereas the entries are counts independent of the prescale factor

9 Performance of LPSFLT during 1995 Data Taking

9.1 History of LPSFLT slots during 1995 Data Taking

The LPS First Level Trigger has been activated from run 11635 onward, at the very beginning of 1995 ZEUS data taking. It has been implemented as a standalone trigger (prescale = 0) in slot 18, and as an active slot (prescale = 1) in slot 23 in *AND* with the *CTD good* trigger. This latter slot was not changed during data taking except for the veto signal which was updated in various steps from the initial configuration $C5v$, $VWiv$, $VWov$, $SRTD95v$ to the final $C5v$, $VWiv$, $VWov$, $SRTD95v2$, $TRKveto$, $noTRKvld$. Slot 18 is referred to as `LPS_hit` which corresponds to (bit 5 .or. bit 6) as described in Section 6.1.
During the 1995 data taking, other slots with the LPS have been added:

- Slot 27: **Double tag** `(LPS || FNC) && (CTD || REMC) && (LUMI || LowW tagger || BPC)` [3]. Active from run 13573.
- Slot 31: **BPC and LPS** `BPC || BPC_phys1 && LPS_hit`. Active since run 12429.
- Slot 47: **RCAL_ISOe_special**. This slot contains looser cuts with respect to the DIS slot, but requires a signal in $LPS.or.FNC.or.BPC.or.LUMI$. Active (with the LPS) since run 11635.

The LPSFLT has been completed in september by adding the LPS_MAX board which allows, via the trigger matrices, the definition of trigger bits $1 \rightarrow 4$. However, as said before, due to the low FLT rate, these bits have not been enabled yet.

9.2 The LPS Third Level Trigger

The LPS Third Level Trigger uses the information from ALL LPS planes, (except the LPSFLT planes). The trigger is based on the LPS pattern reconstruction algorithm implemented in the offline reconstruction program, and uses a *pot quality code* and an *event quality code*.
The pot quality code (referred later as PQCSn) is defined for each pot n^o. It is a number in the range $0 \div 3$, and its definition depends on the number of operational planes in a given pot:3 is the maximum quality code while 0 means no hit. The definition of pot quality code is summarized in Table 3, where we introduce the following definitions (we remind the reader that in each pot of the LPS there are 6 planes with 3 different strip orientations):

- **CC** one hit in two planes with different strip orientations;
- **CCC** one hit in three planes with three different strip orientations;
- **MC** one hit in two planes with the same strip orientation and the same strip number (± 4) and one hit on another plane;

- **MCC** one hit in two planes with the same strip orientation and the same strip number and one hit in two planes with different orientation;
- **MM** one hit in two planes with the same strip orientation and the same strip number plus the same for another couple of planes;
- **MMC** As the previous plus one hit on another plane;
- **MMM** Obvious.....

	MMM	MMC	MM	MCC	MC	CCC	CC
Pot Quality Code S1	3	3	2	2	1	1	1
Pot Quality Code S2	N/A	N/A	3	3	2	2	1
Pot Quality Code S3	1	1	1	1	1	1	1
Pot Quality Code S4up	3	2	1	1	1	1	1
Pot Quality Code S4dw	N/A	3	2	2	1	1	1
Pot Quality Code S5up	3	2	1	1	1	1	1
Pot Quality Code S5dw	3	2	1	1	1	1	1
Pot Quality Code S6up	N/A	N/A	3	3	2	2	1
Pot Quality Code S6dw	N/A	3	2	2	1	1	1

Table 3: LPS TLT Pot Quality Code Definition. N/A means that this specific configuration was not available during 1995 data taking

The two sections of the LPS S123 and S456 are treated separately in the trigger logic (they do not mix). The *event quality code* is therefore defined independently for the two spectrometers and is defined as the maximum of the *event quality code* of S123 and the *event quality code* of S456. The user can select in the physics filter an event quality code based on a single pot coincidence (`C1COIN`), a double pot coincidence (`C2COIN`), and a triple pot coincidence (`C3COIN`), as defined in common `LPSEVT`. The definition follows:

- `C1COIN`≡MAX(`(PQCS1,PQCS2,...PQCS6down)`);
- `C2COIN`≡MAX(`[(PQCS1+PQCS2+PQCS3)-MAX(PQCS1,PQCS2,PQCS3)-`
  `-MIN(PQCS1,PQCS2,PQCS3)],`
  `[(PQCS4up+...PQCS6dw)-MAX(PQCS4up,...,PQCS6dw)-`
  `-MIN(PQCS4up,...,PQCS6dw)]`);
- `C3COIN`≡MAX(MIN`(PQCS1,PQCS2,PQCS3)`,MIN`(MAX(PQCS4up,PQCS4dw),`
  `MAX(PQCS5up,PQCS5dw),MAX(PQCC6up,PQCS6dw))`.

We recommended to the physics groups the requirement of a good hit in at least two stations, which maximizes the trigger acceptance whilst minimizing the noise (we remind the reader that a hit in two stations is the minimum requirement by the LPS reconstruction program to reconstruct the track momentum). The LPSTLT code recommended is therefore

C2COIN$\geq$2.

Note that this is a safe selection which does however lead to different rates of background in the various pots, which are then eliminated during reconstruction.
The LPSFLT has been implemented by the physics groups in the following filters:

- **DIS08**: FLT bits (BEMC_E, REMC_E, RCAL_Isoe*LPS, RcalIsoe, LPS) + E-pz >30, Ee> 4, box cut at 12 cm, LPS reconstruction+ (after 22nd July: lower box cut)
- **DIS20**: BPC and LPS
- **HPP11**: LPS very high E_t [prescale 1]
- **HPP12**: LPS dijet [prescale 1]
- **HFL15**: FNC/LPS and $c\bar{c}$ [prescale 1]
- **SPP03**: Double-tagged (LPS) [prescale 1]
- **SPP16**: LPS 2 and 4 track [prescale 1]
- **SAP01**: LPS filter [prescale 16]

9.3 Trigger rates from LPSFLT slots and trigger purity

The average trigger rates at the FLT for the slots discussed in Section 9.1 are shown in Table 4 (values averaged over 300 runs, from run 13000 $\rightarrow$ *end*).

Slot N^o	Slot name	Rate (Hz)
18	LPS_hit	1100
23	LPS && CTDgood	2.8
27	Double Tag	1.2
31	BPC && LPS	0.24
47	RCAL_ISOe_special	1.9

Table 4: Average trigger rates for FLT slots with LPS

Note that the LPSFLT rates were constantly zero when the LPS was not in position. The trigger detectors were always kept ON during the full data taking period, but the trigger was enabled only when the LPS had been *completely* inserted in position for data taking.
The performance of the LPS FLT detectors has been quite stable during the full period of data taking (see Fig. 30).
The hit distribution of events triggered by the LPS in a typical run is shown in Fig. 31, 32, 33, where the contours of the trigger planes are hatched. The higher background rate seen in Fig. 33 is most probably due to scraping on the pot bottom of S4,S5.

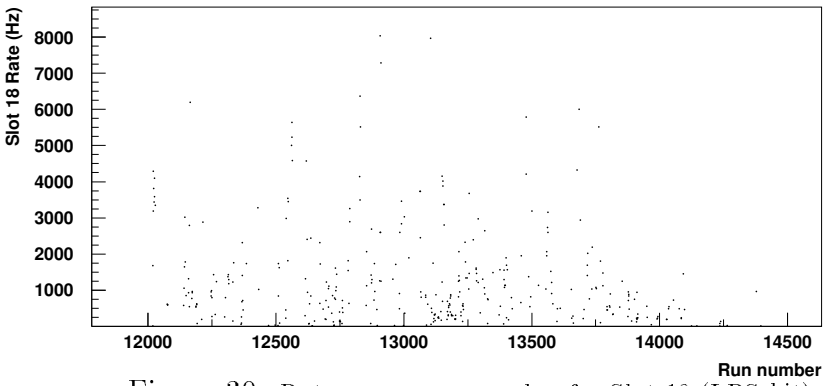

Figure 30: Rate versus run number for Slot 18 (LPS_hit)

The multiplicity distribution in the trigger planes for events selected with LPSFLT (slot 23) are shown in Fig. 34, where it is seen that the mean multiplicity ranges from 1.6 to 1.8, increasing from S4 to S6 due to higher syncrotron radiation background in S5 and higher scraping track multiplicity in S6.
The spatial resolution of the detector can be determined by looking at the distributions of the residuals $x_{LPSFLT} - x_{LPS}$ and $y_{LPSFLT} - y_{LPS}$ where x_{LPSFLT}, y_{LPSFLT} are the hit positions as recorded by the trigger planes, and x_{LPS}, y_{LPS} are hits reconstructed by the LPS planes. These distributions are shown in Fig. 35 and 36 for a sample of events which were triggered by LPSFLT. We find an average resolution of $285\mu m$ which is in good agreement with the expected value of $pitch/\sqrt{2} = 216\ \mu m$ ($\sim 25\mu m$ spread due to average beam tilt of a track in a pot plus $\sim 30\mu m$ resolution of the LPS detector are neglected in the residual calculation).
The offset in the residual distributions which can be seen in some planes, indicates a misalignment of at most one strip. The final alignment of the detector as well as the determination of the trigger efficiency will be done with LPS reconstructed tracks when the LPS 1995 alignment will be available.
The purity of the LPSFLT triggered sample has been monitored constantly during data taking by comparing the SLT passthrough events which had a good track reconstructed by the LPSTLT and were triggered by LPSFLT with the number of SLT passthrough events which had been triggered by the LPSFLT. This ratio has been found quite constant in time and high in value, typically $70 \div 80\%$.

Finally we would like to stress the fact that the LPS trigger has been extremely valuable during 1995 data taking to detect the impact of operations of HERAB wire target on the ZEUS background. A summary of the tests performed in collaboration with HERAB has been described in [37].

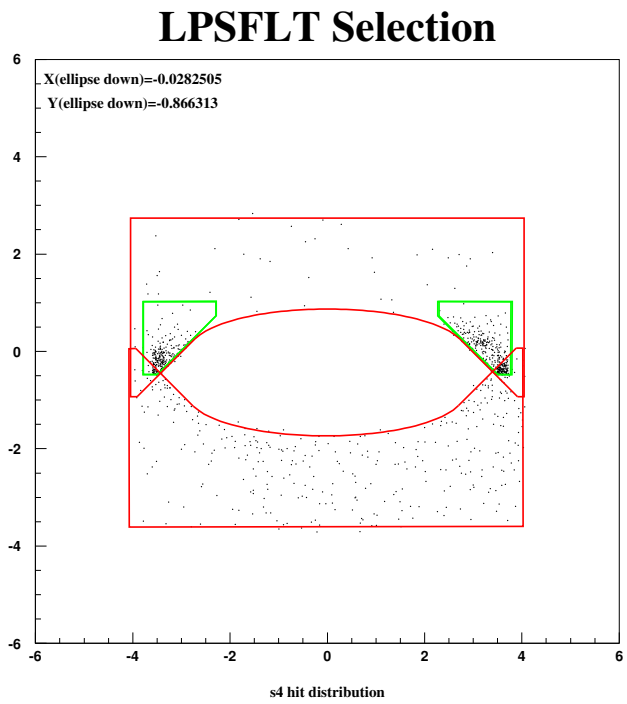

Figure 31: LPS Reconstructed hits in S4 for LPSFLT tagged events

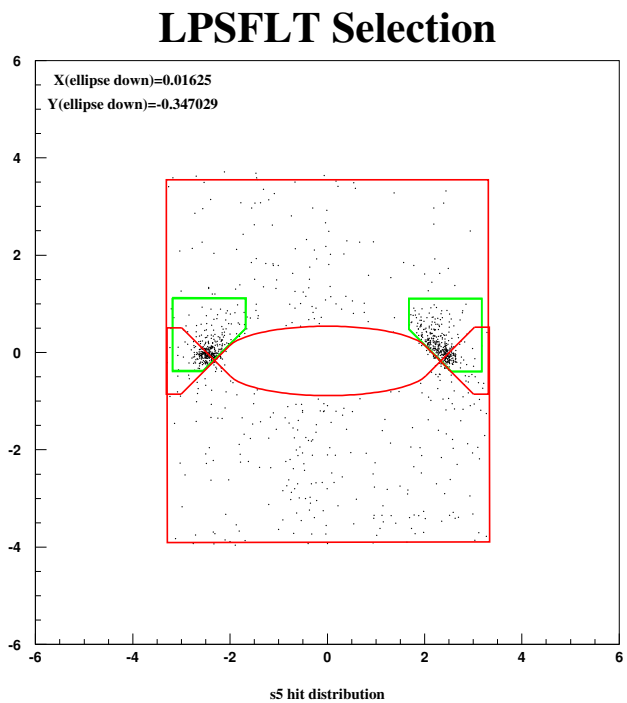

Figure 32: LPS Reconstructed hits in S5 for LPSFLT tagged events

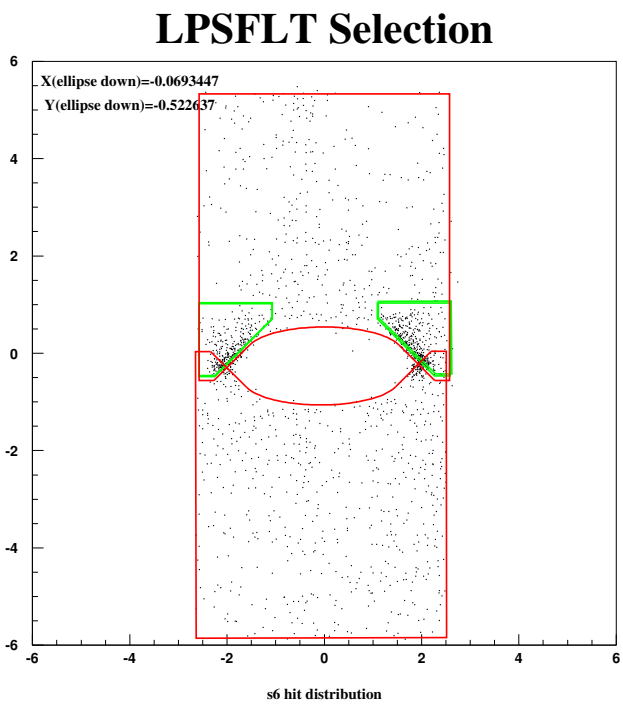

Figure 33: LPS Reconstructed hits in S6 for LPSFLT tagged events

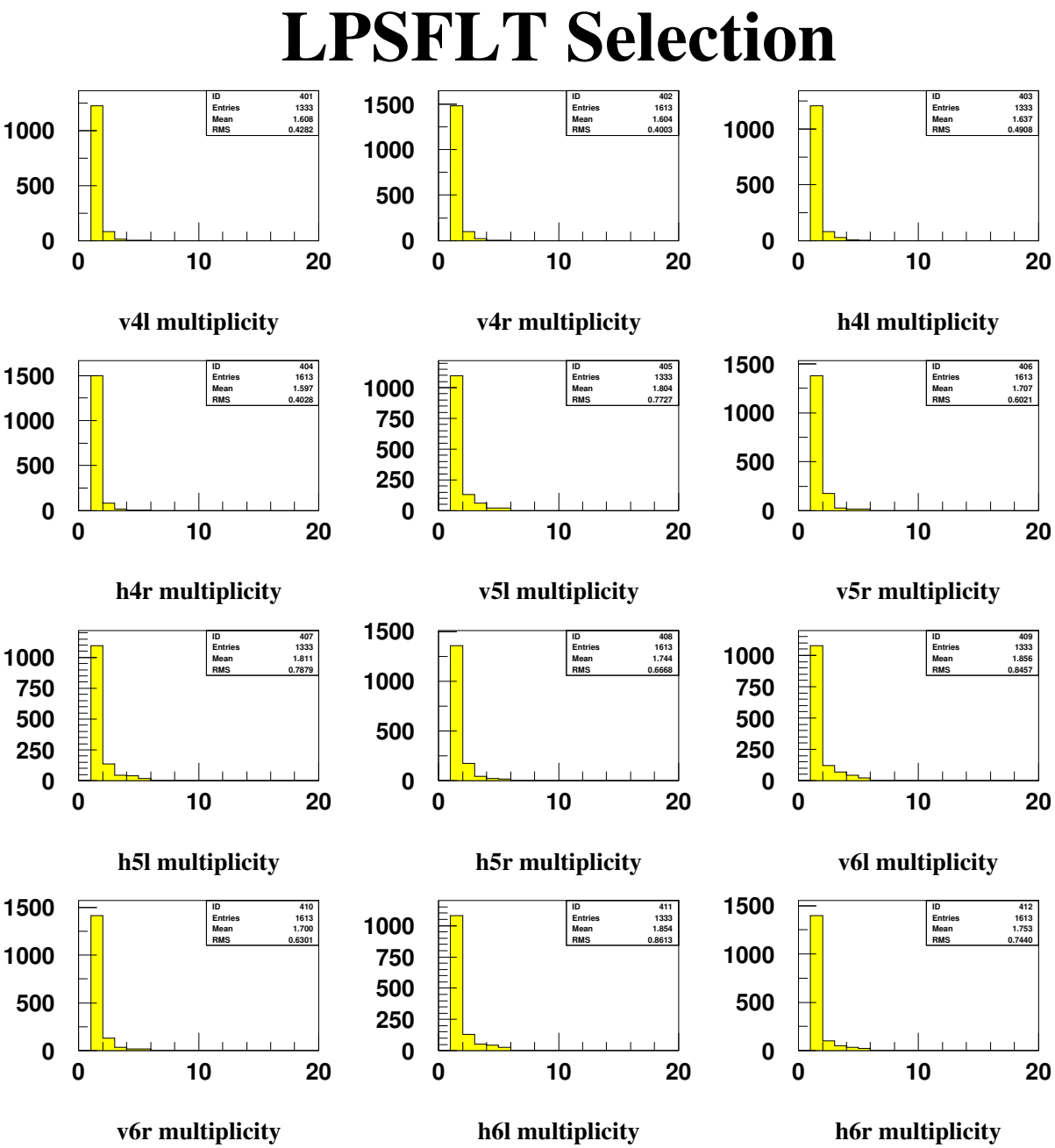

Figure 34: LPSFLT tagged multiplicity in trigger planes

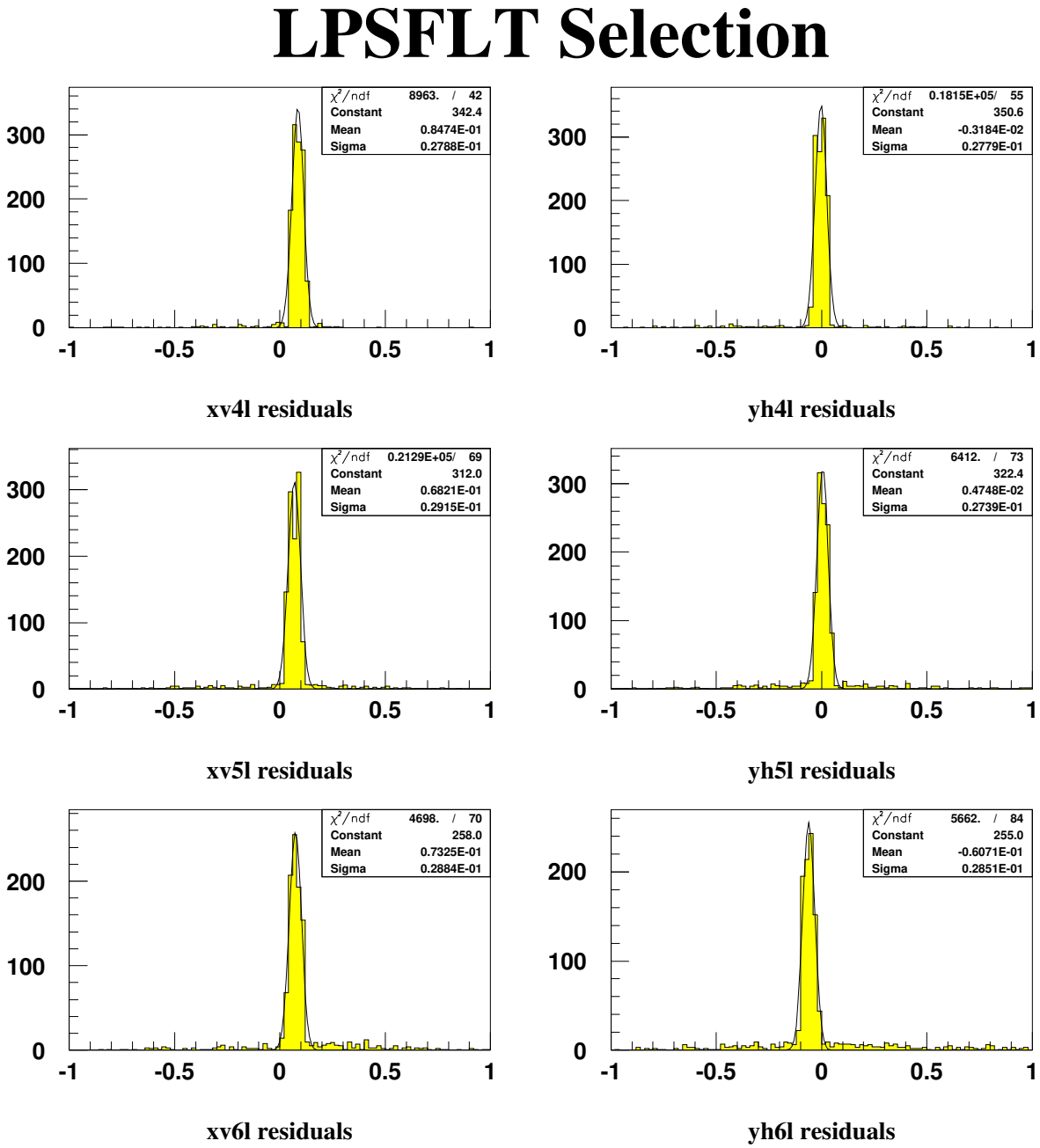

Figure 35: LPSFT-LPS hit residual distributions (scale is in cm)

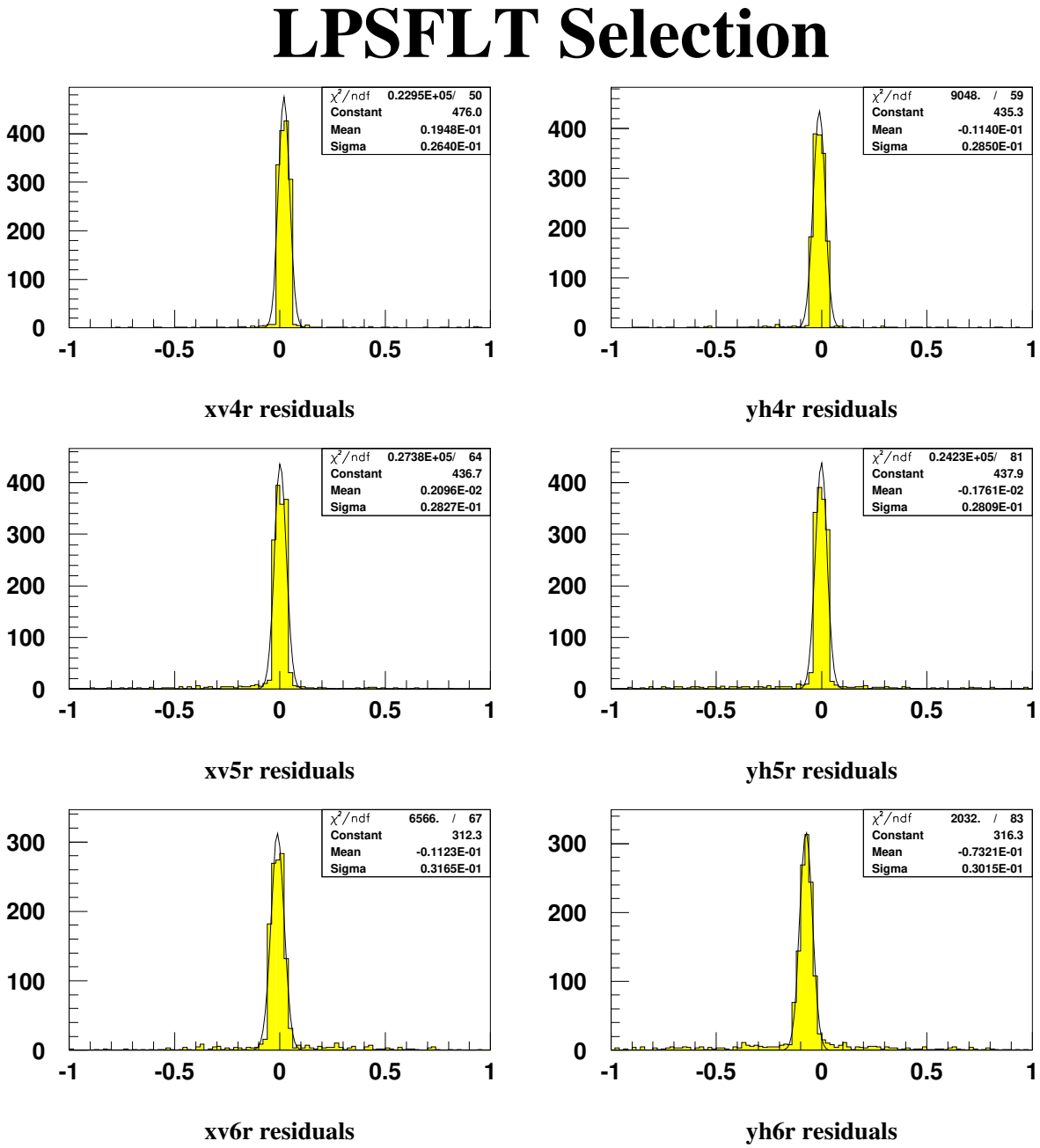

Figure 36: LPSFT-LPS hit residual distributions (scale is in cm)

10 Aknowledgments

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