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Online readout and control unit for high-speed/high resolution readout of silicon tracking detectors

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Abstract

We are describing a high speed VME readout and control module developed and presently working at the H1 experiment at DESY in Hamburg. It has the capability to read out 4×2048 analogue data channels at sampling rates up to 10 MHz with a dynamic input range of 1 V. The nominal resolution of the A/D converters can be adjusted between 8 and 12 bit. At the latter resolution we obtain signal-to-noise ratio better than 61.4 dB at a conversion rate of 5 MSps. At this data rate all 8192 detector channels can be read out to the internal raw data memory and VME interface within about 410 μs and 510 μs, respectively. The pedestal subtracted signals can be analyzed on-line. At a raw data hit occupation of 10%, the VME readout time is 50 μs per module. Each module provides four complementary CMOS signals to control the front-end electronics and four independent sets of power supplies for analogue and digital voltages (10 V, 100 mA) to drive the front-end electronics and for the bias voltage (100 V, 1.2 mA) to assure the full functionality of the detectors and the readout.

1. Introduction

In 1995 the H1 detector has been upgraded by the installation of silicon detectors near the beam pipe. The silicon detectors, the Central Silicon Tracker (CST) and the Backward Silicon Tracker (BST), are systems of silicon-microstrip detectors [1] which are read out by the APC chip, which is an ASIC that has been especially developed for the readout of the H1 silicon detectors [2]. It reads out 128 stripes and stores the analogue signals in a pipeline made of 32 capacitors. After a trigger decision the capacitor which stores the event is read out serially. Several APCs can be interconnected in a way that one after the other is read out. The pipeline capacitors are read in at the HERA bunch crossing frequency of 10.4 MHz. The serial readout is performed at about 2 MHz well matched to read out 10×128 stripes during the latency of the first level trigger of 800 μs [3].

The scope of this paper is the VME module "OnSiRoC" (*On*line *Si*licon *R*ead*o*ut *C*ontroller), which controls and reads out the detector modules. The conceptual development of this module was guided by the idea, to have one module which assures the complete functionality of the silicon strip detector and its front-end electronics namely:

- readout and digitization,
- pedestal subtraction and hit detection,
- complete controlling and monitoring,
- delivery of all supply voltages to the Si-detectors and their electronics.

The highly complex front-end chips of the most recent generations need an increasing number of control signals which cannot be provided externally. This demands a hierarchial system of chips, which demultiplexes the number of control lines. On the other hand, such a system requires a feature to generate the sequence of control signals for this chip. This feature, the "sequencer", has been integrated into this module. A further advantage of a single unit for the entire functionality of the detector is the possibility to avoid ground loops by having a well designed grounding scheme. The presented module has been designed for the H1-Si-detector system, it can, however, be configurated very flexible to operate any similar type of detector.

In other experiments so far modules have been used for the readout of silicon-strip detectors readout [4], which focused on the readout, however, did not attempt to integrate the complete functionality to operate the detector. Furthermore given the readout architecture of the H1 detector [5], a VME compatible module was mandatory.

In the following section the module architecture is described and the functions of the interface are summarized. A detailed description of analogue signal processing follows in Section 3. Different readout modes are docu-

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mented in Section 4. A summary of experimental results of the module characteristics is given in Section 5.

2. Module architecture

The VME module OnSiRoC consists of the following items: *readout and digitization* circuitry, *sequencer* logic, the *power supplies*, *registers* and *interfaces*. The sequencer logic controls the front-end electronics during the two phases of operation, namely the front-end running phase and the front-end-to-back-end readout phase. The module is able to read out sequentially, to process, digitize and store the data of up to 4 analogue inputs, each of $2^{11} = 2048$ detector channels. Registers permit the controlling and monitoring of all operation modes as well as the power supplies for the front-end analogue and digital electronic and the detector bias. A short description of these items is given in the following paragraphs.

2.1. Readout and digitization

According to Fig. 1 the input analogue signal is pre-amplified, and pedestal subtracted before it is digitized by a 12-bit FADC. The results of the digitization are stored with an additional overflow bit in a raw data memory. Simultaneously to the storage of the data, the hit and cluster detection is performed by a digital comparator circuit. A hit is defined as a signal of a single detector channel, that is bigger than a programmable threshold. A cluster is a set of neighbouring hits. It is accepted if its width is bigger than a programmable minimum cluster width. The values of the thresholds and the minimum cluster widths are programmable via the VME bus. A cluster is finally parametrized by the address of the first detector channel and the cluster width, i.e. the number of neighbouring channels fulfilling the hit condition.

Each hit increments the pointer counter (as indicated by the pointer block in Fig. 1). If the cluster width condition is fulfilled, a pulse is generated to store the width and the corresponding raw data memory address into the pointer memory. Both memories, the pointer memory and the raw data memory, have the same depth of 2048 words. The pedestal memory contains 32 times the memory space, thus the pedestal values for all 32 cells of switched capacitors of the front-end analogue pipeline can be stored [2]. Furthermore a 5-bit counter serves to store the corresponding pipeline-cell address. Two channel counters, CH1 and CH2, are needed to compensate the timing delay between the analogue input of the FADC and the digital

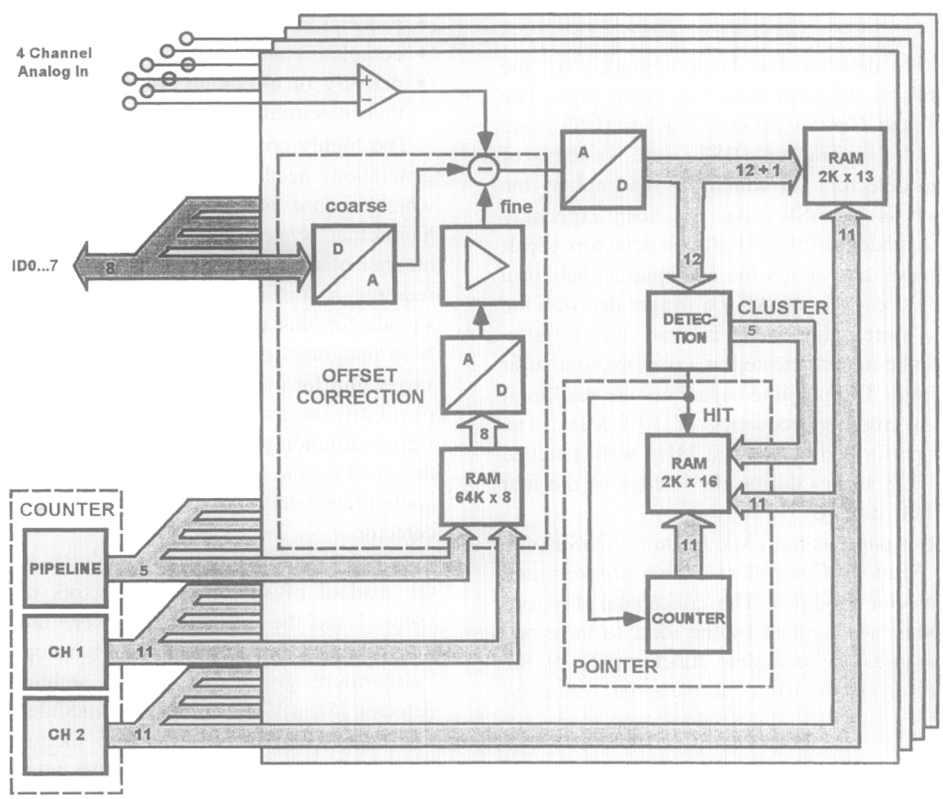

Fig. 1. Block diagram of the analogue and digital input and address paths. Each module contains 4 parallel input channels.

input of the raw data memory. CH2 runs several clock cycles later than CH1.

All memories and counters are read- and writable via VME bus. There are several options to read out event information via VME. In the raw data mode the entire memory is read out, which is the maximum of event information however on the expense of read-out time.

The most condensed information is available from the pointer memory (hit address and cluster width). Reading out this memory only ("hit mode") is the fastest access to the event data.

In the "hit-and-cluster mode" which is a compromise between the two other modes, the hit address is read out from the pointer memory together with the corresponding raw data information from the hit channels forming the cluster (plus some additional information from adjacent channels).

There are analogue switches provided in the analogue branch to use the pedestal memory for testing the complete functionality of the module in a stand-alone mode. To this end the pedestal memory can be loaded with test patterns, e.g. simulated analogue input signals.

2.2. Sequencer

The sequencer generates signals to control the front-end chip (which is in case of the H1 experiment the APC) and the internal readout of the board itself. As shown in Fig. 2 the sequencer has been realized as a classical microprogram memory. The memory space are 128 K words of 32 bits each. The lower 16 bits (SQD0...15) contain the data, the higher 16 bits (SQD16...31) are representing the address of the next step to be performed. The 16 data bits are provided for control tasks: 8 bits for the board internal control, 3 bits for free external use and 5 bits for front-end specific use. The sequencer is clocked at twice the readout frequency. The duration of the high and low periods corresponds to the clock frequency, for special applications the high period of SQD1 and SQD2 can be reduced by 50% by setting the bit SQD4.

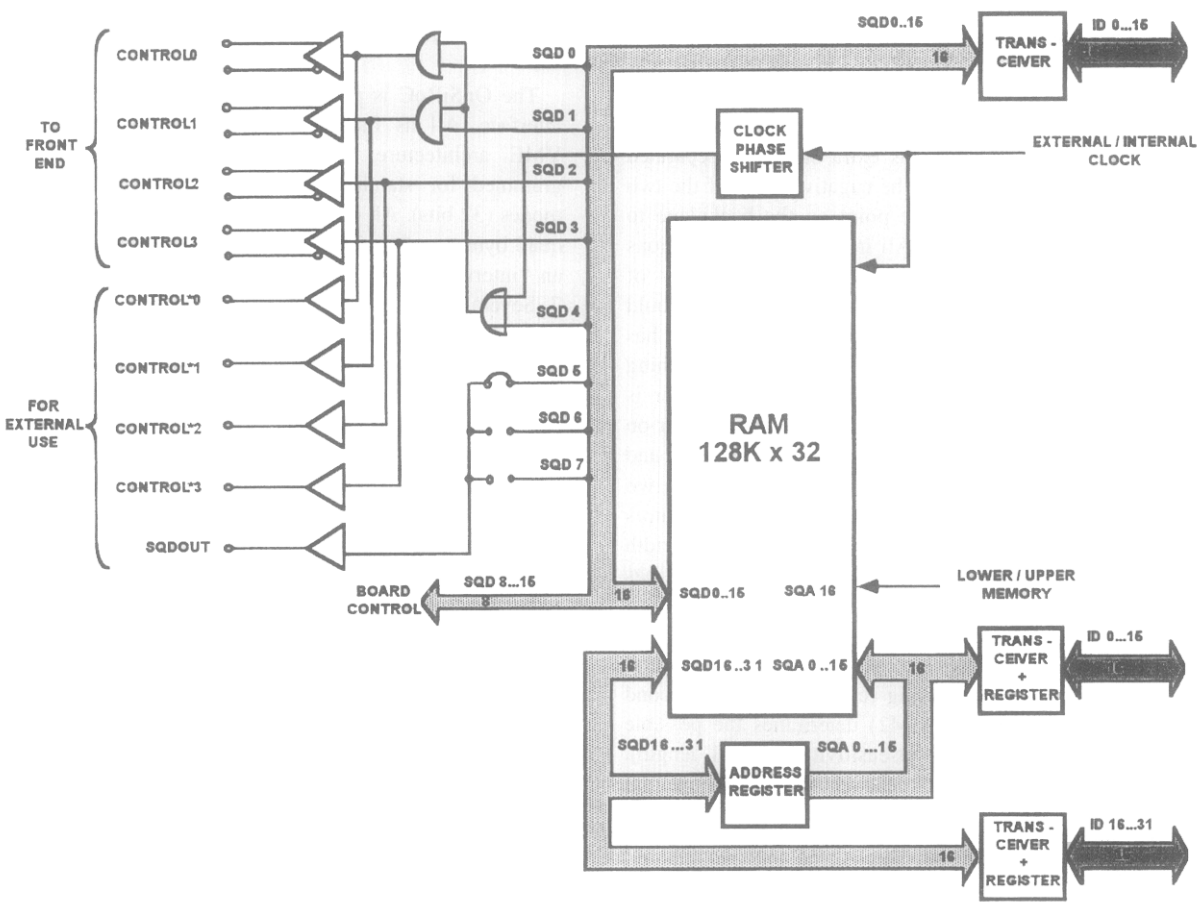

Fig. 2. Block diagram of the sequencer. ID 0...31 represent the internal module-data bus. The sequencer bit SQD 14 represents the lower/upper memory address bit SQA 16.

Two standard operation mode sequences, usually the so called scan and readout sequence, located at different memory areas, are possible. Their start addresses are stored in the registers of the lower and upper transceivers on the right hand side of Fig. 2. The address register of the feedback branch (SQD16...31-to-SQA0...15) holds a third start address for test purposes. The startup circuitry of one of the operation modes is designed to interrupt the progress of the other sequence and to take the system control. The maximum length of a sequence can be 128 k of fully programmable steps with possible endless loops. A typical program is much shorter, e.g. 3000 words for a sequence. To generate a sequencer code in a comfortable way a high-level programming language compiler has been developed [6].

2.3. Power supplies

The OnSiRoC module contains four groups of three switching power supplies V_a, V_d and V_b. The analogue and digital voltages V_a and V_d have insulated outputs in order to permit floating sources. The bias voltages V_b are equipped with a current measurement circuitry with a range from 0 to 1.2 mA. Whereas the analogue and digital 10 V-sources V_a and V_d are adjustable on board, the 100 V-sources V_b are adjustable via VME bus. In order to minimize the switching process impact to the analogue circuitry, all switching power supplies use a separate power supply in the VME-crate. The current loop of this extra supply is separated from that of the regular one. The negative poles of the two supplies are connected at one point on the backplane to realize a common reference. All input supply connections are protected by melt-fuses on the card. This way of protection is not viable for the outputs, because it would cause power losses. Thus a special protection circuit has been developed which uses the continuous switching behaviour as a criterion for overload. If the regulator is switching continuously with the exception of the power-on phase, the protection circuit detects an overload and switches the regulator off. This circuit is realized with two in series connected retriggerable monostable multivibrators (Fig. 3). The first one (MM1) holds an output pulse width between one and two regulator oscillator-periods and has to be restarted by each negative edge on the regulator output. Consequently during overload, there should be only one continuous pulse present on the multivibrator output due to the steadily retriggering (cf. Fig. 3c). The second monostable multivibrator (MM2) determines the possible overload duration (startup insensitivity interval length). This circuit is triggered by the edge of the MM1 output signal. The MM2 output controls directly the ON/OFF-regulator input. To hold the power supply operating, this monoflop has to be continuously retriggered within its fly-time. Therefore the regulator ON/OFF-control signal (c.f. Fig. 3a) is actually a MM2 output pulse, e.g. its unstable status. If this circuit is not retriggered within the fly-time (overload conditions), it returns to its stable state and switches the regulator and thus the power supply off.

2.4. Registers

Beside the transceivers and registers, which enable the access to memories and counters via the internal data bus, the OnSiRoC comprises three additional 16-bit registers, namely the control registers 1 and 2 and the status register. The bit-significances are summarized in Table 1. The control register 1 controls the external trigger signals and the VME-bus interrupts. The control register 2 is used to switch the power supplies on and off and to disable the analogue inputs for test purposes. Furthermore, it is used to disable the external third-level-trigger keep and rejection signals, which are used to continue or abort the readout phase, respectively. The status register reflects the state of several hardware signals. Thus it can be used to decide whether the front-end readout is finished and whether an event is ready in the front-end memories. It also indicates the state of the power supplies.

2.5. Interfaces

The OnSiRoC is provided with a complete VME slave interface. All its functions are controlled by a standard VME architecture. Address modifier codes are programmed for standard (24 bits) and extended address modes (32 bits). All data transfers are either double byte or quad byte transfers. The VME interface is able to generate an "interrupt on" at one of the interrupt request levels 1 to 7. Several user-definable pins of the J2/P2-bus connectors are connected to the signals of the external trigger system, to the additional + 5 V-source for the switching power supplies (see above) and to a − 5 V-source for internal board use.

The control signals generated by the sequencer are complementary CMOS-compatible and available at a 20-pin cable connector (3M mini delta ribbon) at the front panel. A voltage devider provides the matching of the output levels in accordance with the front-end requirements. A 50-pin front panel connector (3M mini delta ribbon) contains the analogue input and the power pins. The analogue signals are transferred differentially with admissible variations of ±0.5 V and an allowed common mode of ±2.5 V. The input termination is 120 Ω.

The VME module OnSiRoC (Fig. 4) consists of a 12-layer printed circuit mother board and a 14-layer printed circuit daughter board. The mother board is 6 units (26 cm) high and 22 cm deep, the top-side is mainly assembled with surface mounted components. The daughter board is 16.5 cm high and 11.5 cm deep and is fully top- and bottom-side assembled with surface mounted components.

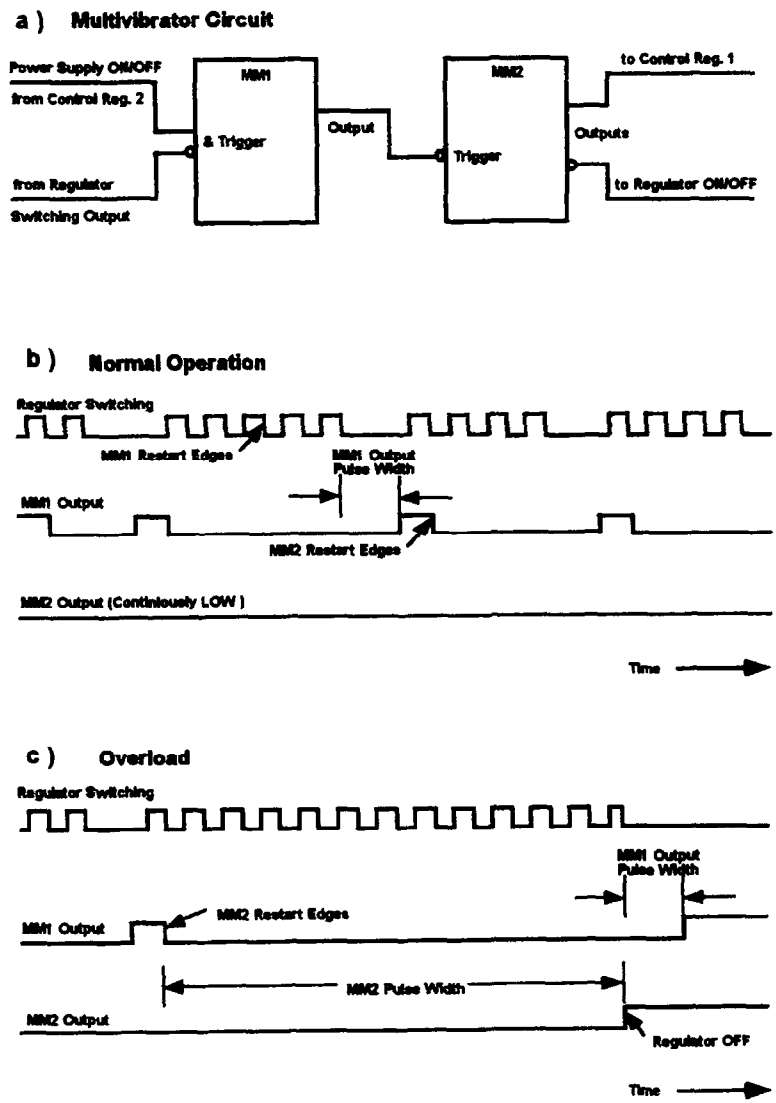

Fig. 3. (a) Overload protection circuit with two multivibrators, (b) operation at normal operation mode, and (c) at overload mode.

3. Analogue signal processing

The signal amplitudes of the analogue inputs are transformed by an instrumentation preamplifier (Analog Devices AD830) with a closed loop gain of $(R_{i1}+R_{i2})/R_{i2}$ according to Fig. 5 to a full dynamic range of -2 V to 0 V. If the active switch is closed (i.e. INPUT Enable = TRUE as shown in Fig. 5) the preamplifier delivers the input signal for the post-connected inverting analogue-adder stage (Comlinear CLC409) for an offset correction. The values of the coarse and fine pedestals (R_{coarse}, R_{fine}) are defined by the digital input of the 8-bit DACs (Analog Devices AD7228 and Sony CXD1177) within their full-scale ranges (FSR), 2.5 V and 2 V, respectively. The actual pedestal values at the analogue adder output are further depending on the values of the corresponding resistors R_c and R_f. The reference voltage current feed is supplied by V_{ref} and depends on R_{ref}. It shifts the dynamic range from -1 V to $+1$ V, which corresponds to the analogue input range of the 12-bit FADC (Analog Devices AD872). Thus the output voltage V_{out} of the analogue adder is given by

$$V_{\text{out}} = \frac{R_0}{R_i}\frac{R_{i1}+R_{i2}}{R_{i2}}V_{\text{in}} - \left(\frac{R_0}{R_c}V_{\text{coarse}} + \frac{R_0}{R_f}V_{\text{fine}}\right) - \frac{R_0}{R_{\text{ref}}}V_{\text{ref}}.$$

$R_{i1}=R_{i2}=\frac{1}{2}R_{\text{ref}}=560\ \Omega$ and $R_i=R_0=430\ \Omega$ are limiting the dynamic ranges. The coarse and fine pedestals may be expressed as:

$$\left.\begin{matrix}V_{\text{coarse}}\\ V_{\text{fine}}\end{matrix}\right\} = \sum_{i=0}^{7} k_i \cdot 2^i \cdot \left\{\begin{matrix}\Delta V_{\text{coarse}}\\ \Delta V_{\text{fine}}\end{matrix}\right. \text{ with } k \in \{0;1\}.$$

Table 1
Definition of the bits of the control registers 1 and 2 and the status register

Bit	Control register 1	Control register 2	Status register
0	Pedestal enable	Power supply V_{a1} on	Sequencer in operation
1	Internal clock	Power supply V_{a2} on	Scan phase on
2	Internal run enable	Power supply V_{a3} on	2nd level trigger prompt on
3	External run disable	Power supply V_{a4} on	2nd level trigger delayed on
4	External fast clear disable	Power supply V_{d1} on	Front end ready on
5	Front end ready enable	Power supply V_{d2} on	Interrupt on
6	External 1st level trigger disable	Power supply V_{d3} on	2nd level trigger keep on
7	Automatic 1st level trigger sequence	Power supply V_{d4} on	3rd level trigger keep on
8	Control signals enable	Power supply V_{b1} on	3rd level trigger reject on
9	Encoded interrupt level 1	Power supply V_{b2} on	Power supplies V_{a1} and V_{d1} on
10	Encoded interrupt level 2	Power supply V_{b3} on	Power supplies V_{a2} and V_{d2} on
11	Interrupt vector 0	Power supply V_{b4} on	Power supplies V_{a3} and V_{d3} on
12	Interrupt vector 1	Disable inward analogue signal	Power supplies V_{a4} and V_{d4} on
13	Interrupt vector 2	Disable inward analogue signal	Not used
14	Interrupt vector 3	Disable 3rd level trigger reject	Not used
15	Interrupt vector 4	Disable 3rd level trigger keep	Not used

For the given 8-bit resolution the voltage increments are given by

$$\left.\begin{matrix}\Delta V_{\text{coarse}}\\ \Delta V_{\text{fine}}\end{matrix}\right\} = \left\{\begin{matrix}\text{FSR}_{\text{coarse}}\\ \text{FSR}_{\text{fine}}\end{matrix}\right\} \cdot \frac{1}{2^8-1} = \left\{\begin{matrix}10\text{ mV}\\ 8\text{ mV}\end{matrix}\right.$$

It can be further reduced by increasing R_c and R_f at the cost of a decreasing pedestal range.

The proper dimensioning of the resistors R_c and R_f depends on the pedestal variations of the input channels. In Fig. 6 examples for the worst case (a) and a typical case (b) of pedestal variations are shown. We first consider a signal with high pedestals (a). The diagrams (i) and (ii) show, that an error-free signal analysis is only possible, if the channel independent coarse pedestal values are less (i) or equal (ii) to the minimum pedestal amplitude. In case (ii) the lowest maximum values of fine pedestals, drawn as dotted lines with its peak values at $0.7V_{max}$, are required. Lower coarse pedestals result always in higher fine levels (cf. case (i): $0.8V_{max}$). An increase of coarse values above the measured minimum pedestal amplitude leads to errors at these positions (cf. errors 1 and 2 in diagram (a, iii)). To avoid this situation the following procedure to get reasonable values for R_c and R_f should be followed:

Measurements of events without pedestal correction have to be performed over a longer time period in order to determine the time averaged maximum and minimum input values $\overline{V_{\text{in, max}}}$ and $\overline{V_{\text{in, min}}}$.

- Increase R_{i2} until $|V_{\text{out}}| = |\overline{V_{\text{in, max}}}| \cdot (R_{i1} + R_{i2})/R_{i2} =$ 2 V is valid.
- Change R_c until $|V_{\text{coarse}}| = |\overline{V_{\text{in, min}}}| \cdot R_c/R_0$ becomes 2.5 V−10 mV.
- Change R_f until $|V_{\text{fine}}| = (\overline{V_{\text{in, max}}} - \overline{V_{\text{in, min}}}) \cdot R_f/R_0$ becomes less than 2 V−8 mV.

The overall-resolution is limited by R_f. In Fig. 6b the maximum pedestal variations are less than $\overline{V_{\text{in, max}}}/16$. The chosen ratio of $R_f/R_0 \approx 15.8$ results in a voltage increment of 0.5 mV at the FADC input. In this case the nominal resolution of 12 bit is obtained. However a ratio of $R_f/R_0 = 1$ yields a resolution of only 8 bit.

4. Operation modes and timing

Two different sequences control (i) the *scan phase* of the running front-end electronics until an event is detected and (ii) the subsequent *readout phase* triggered by an event detection. This readout phase consists of two parts. The first one is a synchronous readout from the front-end to the raw data memory, after which the scan phase is restarted. During the second part of the readout phase the stored data will be sent asynchronously (VME handshake procedure) from the raw data memory to an external unit via VME bus. A somewhat more complex situation is shown in Fig. 7, where a second event occurs already during the second part of the readout phase. The 2nd-level trigger occurs and sets the two internal trigger bits, *2nd-Level Trigger Prompt*, *2nd-Level Trigger Delayed*, and sets the *Front-End Ready* (cf. status register, Table 1) off. The delayed trigger bit avoids the readout of a second event before the first event has been read out completely. It is on, if the readout phase is in progress. After finishing the data transfer from the front-end to the raw data memory the sequencer sets the stop bit *SQD15* (cf. Section 2), which activates *Front-End Ready* and stops the sequencer. Then the external readout processor is initiated and starts the asynchronous raw data transfer from the raw data memory via VME bus. At the end of this readout phase a VME-command resets the *2nd-Level Trigger Delayed* bit. The sequencer starts again the readout phase and the transfer of the data of a second event is invoked.

A *Fast Clear* is generated by the central trigger logic

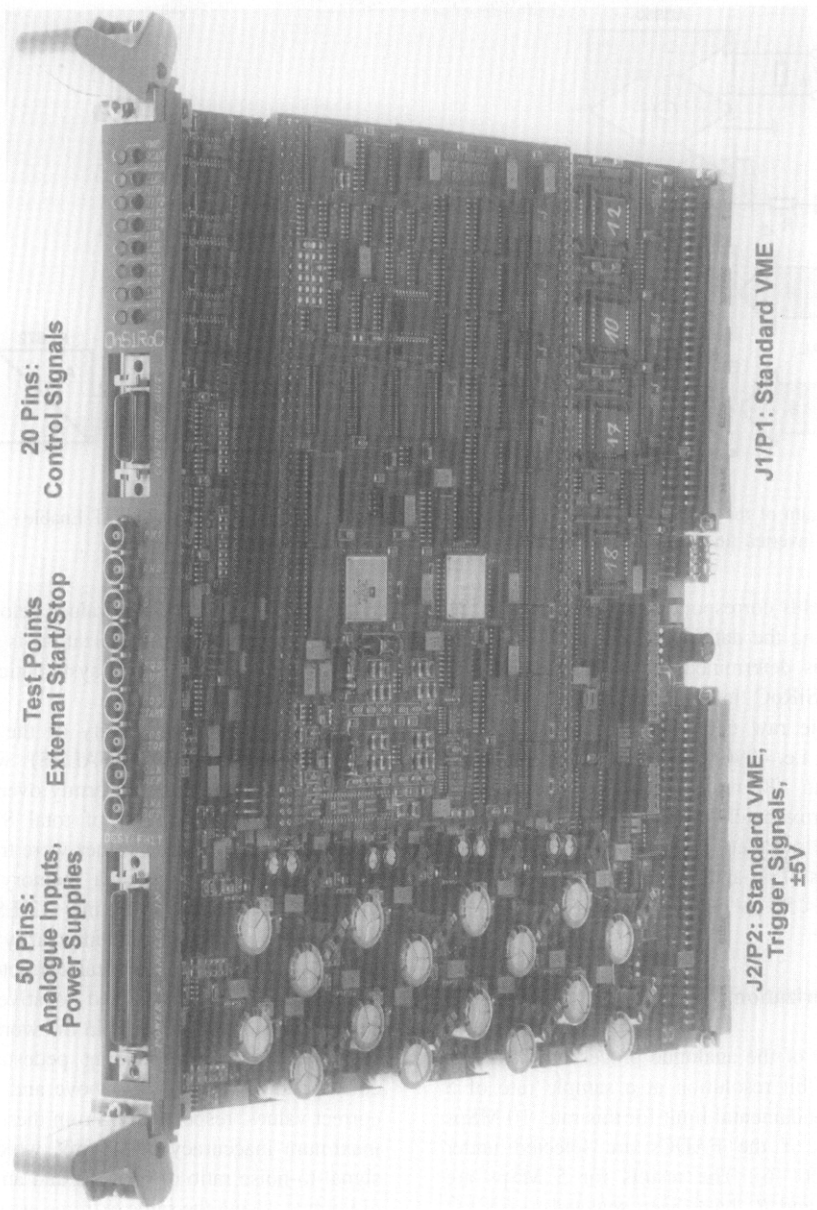

Fig. 4. Photography of the OnSiRoC VME module.

once all other branches of the experiment have set their *Front-End Ready* and acknowledged the 3rd-level-trigger. Because the readout time is event-dependent and branch-specific, the *Fast Clear* may arrive before, during or after the readout phase. The *Fast Clear* invokes the sequencer to start the scan phase, which requires a few cycles setup time before really reading out the strip signals. Usually as a readout phase is inactive, the scan phase is active. This situation is shown by the hatched areas at the right- and left-hand side in Fig. 7. The timing diagrams of the keep- and reject-bit of the 3rd-level trigger (cf. Table 1) are not shown. Whereas the keep signal activates only the corresponding status register bit, the reject signal interrupts the running sequence.

The actual event number is readable via VME from an on-board 32-bit event counter. The time intervals Δt_{ro1} and Δt_{ro2} in Fig. 7 mark the readout times of the internal (front-end- to raw data memory RDM) and external (raw data memory RDM to VME) data transfers, respectively. As it will be shown in the following section the OnSiRoC works without any bit errors at data rates up to 5×10^6 samples per second (5 MSps). At this data rate 4×2048 detector signals can be processed and stored in the raw data memory within $\Delta t_{ro1}\approx410$ μs. A further increase of

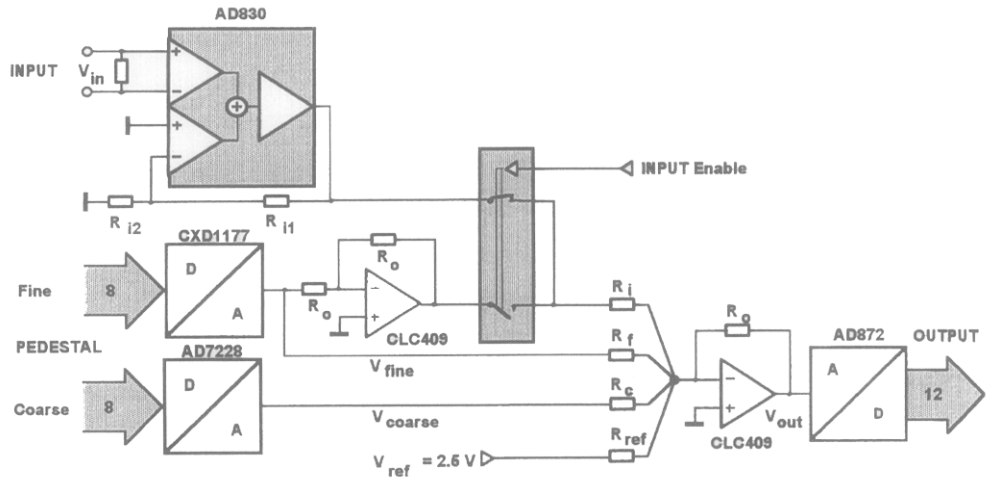

Fig. 5. Schematic diagram of the analogue branch. The shown switching position corresponds to INPUT Enable = TRUE. In the opposite switching position the inverted fine pedestals can be used as test signals.

the sampling rate yields correspondingly lower values and vice versa. Concerning the data transfer via VME bus the readout time Δt_{ro2} is determined by the handshake procedure and the OnSiRoC internal signal processing. A readout of the whole raw data memory needs 2×2048 32-bit data transfers, i.e. 4096 VME commands, each of a cycle time of about 120 ns. This causes a maximum readout time of approximately 500 μs. In a typical event less than 10% of the raw data memory space is related to hits, so that a successful hit and cluster detection decreases the readout time to <50 μs per OnSiRoC.

5. Module characterization

The linearity error of the analogue processing has been determined for a 12-bit resolution at a sample rate of 5 MSps. There is no fundamental limit for this rate. 10 MSps are also guaranteed, if the FADCs are selected under special timing aspects [6]. The results for 5 MSps are shown in Fig. 8. R_f and R_c have been selected to 6.8 kΩ and 1.12 kΩ, respectively. The measurements of the analog input circuitry (INPUT Enable = TRUE) have been made without any pedestal correction ($V_{coarse}=0$, $V_{fine}=0$). In Fig. 8a the FADC OUTPUT signal is shown in steps of the least significant bits LSB_{12} for 18 input voltages between 0.05 V and 0.95 V. At the right hand side of the figure the deviations from the linear relationship is shown. A quantization error of ±0.5 LSB_{12}, which is the typical nonlinearity for the bipolar operation mode has been found. In contrast to differential nonlinearity, the integral nonlinearity INL amounts to -3 $LSB_{12} \le LSB_{12} \le 2$ LSB_{12} (1 $LSB_{12}=0.5$ mV). A comparison with the manufacturer's specification of ±2.5 LSB_{12} indicates, that the accuracy of the analogue input circuitry is dominated by the quality of the FADC. Replacing the FADC by the more recent type AD872A, values below ±1.75 LSB_{12} can be obtained. Further minimization is attainable by arithmetical correction of this systematic error in the subsequent data analysis.

The maximum nonlinearity of the pedestal correction circuit (INPUT Enable = FALSE) was determined by storing a randomly and uniformly over the whole dynamic range distributed data set of total 8×256 bytes in the pedestal memory. These values were transformed via DAC and FADC to the raw data memory (cf. Fig. 8b). The integral nonlinearities result in -12 $LSB_{12} \le INL_{12} \le +10$ LSB_{12}. The differential nonlinearity amounts to ±2.5 LSB_{12}. At a nominal pedestal corrected 12-bit resolution ($R_f=6.8$ kΩ) the positive and negative limiting values are summed to about ±0.7 mV. In the worst case the analogue value and the corresponding pedestal are lying 1 mV corresponding to 2 LSB_{12} above and 0.7 mV below their correct values, respectively. From these results we obtain a maximum inaccuracy of 1.7 mV, which corresponds to a signal-to-noise ratio of 61.4 dB and an effective resolution of 9.9 bits. Using the same extreme estimation for $R_f/R_0=1$ (nominal 8-bit resolution) leads to values of 49.1 dB and 7.9 bit.

The measurements of the voltage sources were made using a test adapter with variable terminating resistors. The test points are located on the 50-pin connector at the front panel. The analogue and digital sources can be loaded with a maximum of 1.9 W. Their voltages can be fixed between 5 V and 10 V. In this region the ripple voltages have been measured to be less than 30 mV. Their insulated outputs are well protected against overload. The voltages of the bias supplies are adjustable via VME between 0 V and 100 V and their maximum load is 120 mW. During a measurement period of several ms the ripple voltage remains well below 160 mV. Usually such high voltages are unregulated at the front-end side and an additional ripple voltage

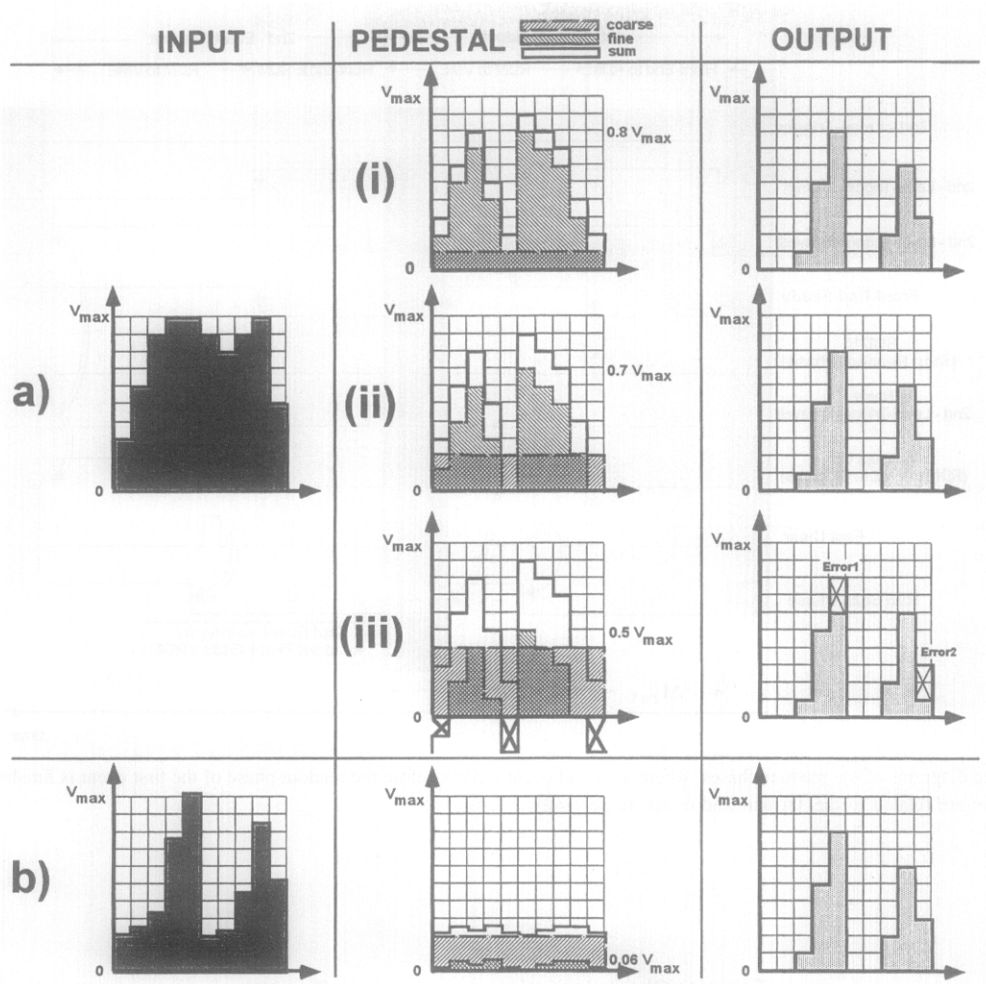

Fig. 6. Input, pedestal and output signal amplitudes for the cases of high (a) and low (b) pedestal variations. The abscissa on all plots represents the channel number, corresponding to the number of the sequentially sampled analogue value of a strip. The position of the channel independent coarse pedestal determines the system resolution as well as the error rate. Its value is constant for each of the analogue channels and drawn as broken lines. The solid lines describe the sum of the fine and coarse pedestals.

measurement has been made with shielded multicoaxial cables, terminated with 100 nF in parallel to 100 kΩ. At 100 V the ripple voltage drops to peak-to-peak value of <15 mV, corresponding to an accuracy $<1.5\times10^{-5}$.

6. Conclusion

The described OnSiRoC module can read out 4×2048 analogue data at sampling rates up to 10 MHz with a dynamic input range of 1 V. The resolution of the ADC branch depends on the resistance ratio R_f/R_0. The following values were found at a conversion rate of 5 MSps:

At a nominal best case pedestal corrected 12-bit resolution ($R_f/R_0=16$) a maximum inaccuracy of 1.7 mV was found, which corresponds to a signal-to-noise ratio of 61.4 dB and an effective resolution of 9.9 bits. On the other hand, at a nominal worst case 8-bit resolution ($R_f/R_0=1$) 49.1 dB and 7.9 bits were found, respectively. The OnSiRoC can read out up to 8192 analogue detector signals from front-end to raw data memory within less than 410 μs and from raw data memory via VME to external signal processor within less than 510 μs. In the case of effective hit and cluster detection the VME readout time can be reduced to less than 50 μs per OnSiRoC.

The OnSiRoC has been used in complete read out systems both in laboratory and in the H1 experiment. The described properties were confirmed. The signal-to-noise ratio in these setups, however, were largely dominated by the characteristics of the front-end systems [6]. In case of strong common mode fluctuations or frequent changes of pedestal values of the input signal to the OnSiRoC, the hit-finding electronics may have reduced efficiency. This can be cured by frequent downloading of pedestal values

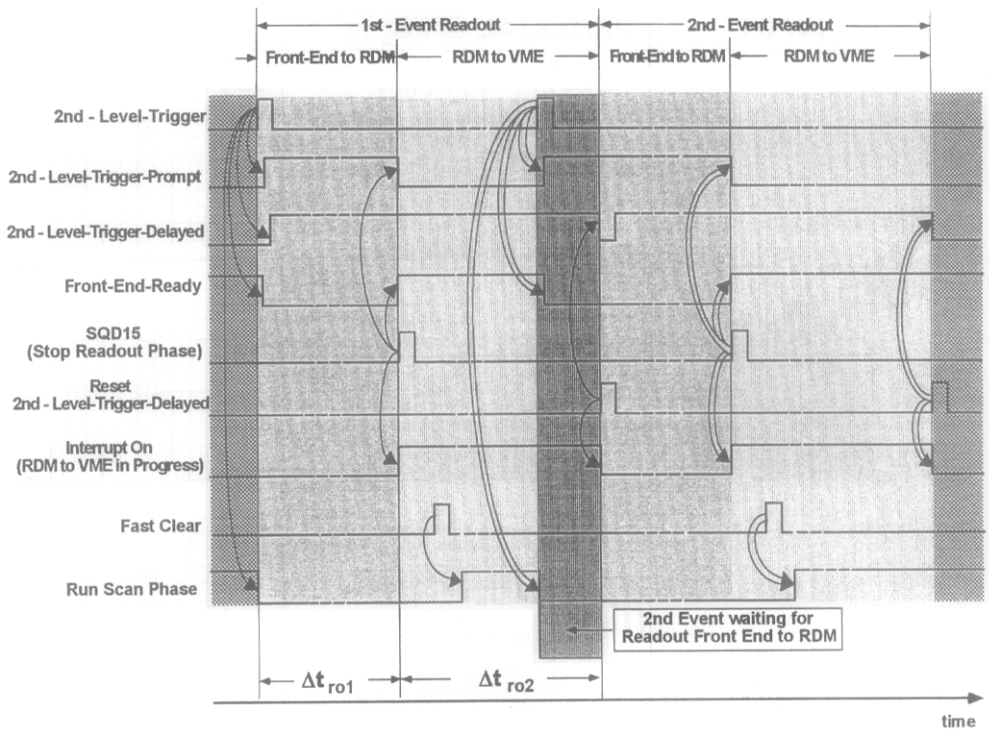

Fig. 7. Timing diagrams of the readout phases, where a second event arrives before the readout phase of the first event is finished. Single and double arrows are related to the 1st and 2nd event, respectively.

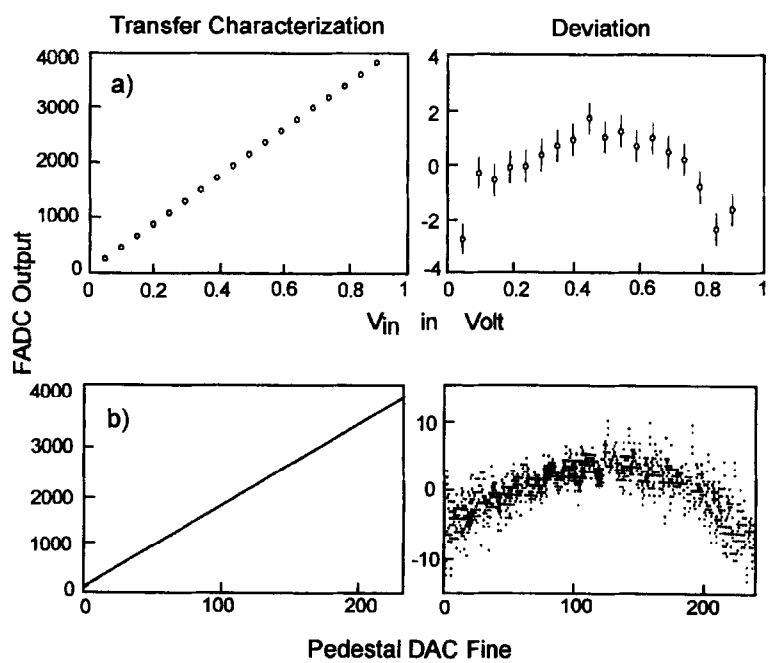

Fig. 8. Accuracy of the analogue processing for both the boarderline cases of a nominal resolution of 12 bit (a) and 8 bit (b).

or by reading out the raw data memory for later processing. In both case the read out speed becomes considerably reduced. To overcome this drawback, a future development of the OnSiRoC architecture has to include processing power on board or on a separate module. The later way is foreseen for the read out of the H1-silicon detectors.

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