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DESIGN AND PERFORMANCE OF A 10 MHz CMOS ANALOG PIPELINE

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The development of an analog pipeline which will be used for the readout of the ZEUS high-resolution calorimeter is described. The pipeline will be built in CMOS-technology and will use the switched capacitor technique. Performance tests of a test chip which incorporates the main features of the pipeline are presented. The following results on the main parameters have been achieved: dynamic range about 8000 : 1, chargeup time better than 4 ns, timing accuracy better than 1 ns. First results on radiation sensitivity show that the chip operates properly up to 5 krad. On the basis of these results an improved design of a prototype chip has been started.

1. Introduction

ZEUS [1] is one of the experiments which are being constructed for the new electron–proton storage ring HERA at DESY. In HERA 30 GeV electrons will collide with 820 GeV protons with a time between crossings of 96 ns, i.e. a crossing rate of 10.4 MHz. The high crossing rate requires a pipeline to store the analog data from the calorimeter until the first-level trigger has made the decision if a particular bunch crossing contains an event of interest. The length of the pipeline has been defined to be 5 μs, the time in which the first-level trigger, which is also built as a pipeline, reaches its decision.

The high-resolution ZEUS calorimeter [2] has a dynamic range from about 100 MeV up to about 400 GeV. This large range is covered by a high- and a low-gain channel, each with a dynamic range of about 4000 : 1. In addition to its large dynamic range the pipeline should be linear and provide a timing accuracy in the 1 ns range. Commercially available ADCs, followed up by a digital pipeline, do not provide such a performance at reasonable prices. The ZEUS collaboration has followed two lines of technologies for analog pipelines:
- charged coupled devices (CCD), and
- switched-capacitor circuits (SC).

We report here on the design and performance tests of a SC circuit design.

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Our development was guided by the analog memory unit AMU of the SLD collaboration [3]. It was carried out at the Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme IMS at Duisburg. We have profited from earlier studies which have been done jointly by IMS and the Max-Planck-Institut München [4].

2. Description of the analog pipeline

The ZEUS calorimeter uses depleted uranium plates as absorbers and plastic scintillator as detectors. The light from the scintillators is collected by wavelength shifters and transformed into electrical pulses by photomultipliers. The signal is shaped by a network of a single differentiation followed by three integrations with time constants of about 35 ns, so that the total charge and the arrival time of the signal can be precisely measured by sampling every 96 ns by the analog pipeline.

Fig. 1 shows the SC circuit layout, which has been realized in CMOS technology (2.5 μm feature size, silicon gate, n-well process, supply voltages ±6 V). In the following we explain the operation principles. During the write phase the switches S_2 and S_5 are open, and one electrode (bottom plate) of all storage capacitors C_s^n is connected to the input line via S_1. By switching S_3^n with the writing frequency, the other electrodes (top plate) of the storage capacitors are consecutively connected to ground through the closed switch S_4. The

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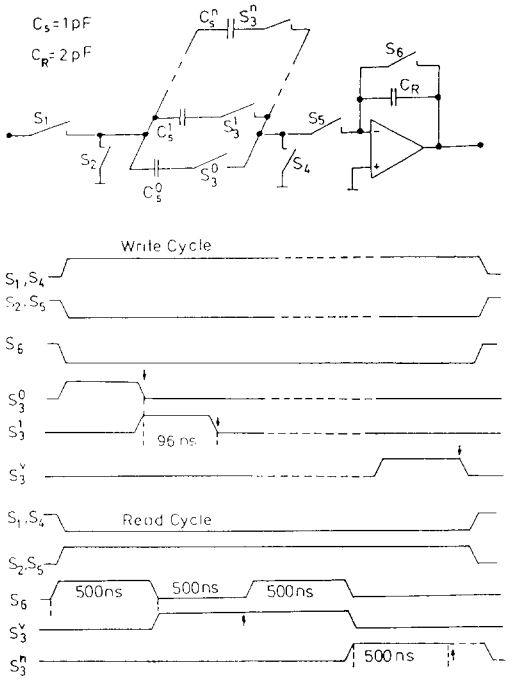

Fig. 1. Schematic of the analog pipeline. The pulse sequence is explained in the text.

charge stored on the capacitor C_s^n will be proportional to the input voltage when the switch S_3^n opens. During the read phase S_1 and S_4 are opened and S_2 and S_5 are closed. To read the capacitor C_s^n, first the output amplifier is reset by closing and opening S_6. Upon closing of S_3^n the charge of the capacitor C_s^n will flow onto the feedback capacitor C_R and will be kept there for readout by an ADC. Because of the high open-loop gain of the operational amplifier the gain of the pipeline is equal to the ratio of the two capacitor values, C_s^n/C_R.

Besides the requirements on dynamic range and linearity mentioned above and listed in table 1, we aim for a design such that each pipeline can be described by two constants only: an offset values and a gain constant. This necessitates equal values for the different storage capacitors within 0.4% and equal values of the pedestals within 1 mV. In order to achieve these stringent requirements, the individual cells (C_s^n, S_3^n) have to be laid out identically. In the following the design features of the pipeline are described.

- Since the gain is given by the ratio of two capacitors it is necessary to minimize the effect of unavoidable stray capacitances. In the design these capacitors are either short-circuited by a switch during writing or switched between ground and the virtual ground of the operational amplifier. Furthermore, the two capacitors – the storage and the feedback capacitor – should be laid out in the same geometric way, and, lastly, a very uniform oxide thickness over the area of the chip has to be provided. The capacitors have been laid out as metal over an active n^+-area with an oxide thickness of about 60 nm.
- The switches S_3^n, which are operated at 10.4 MHz under the control of a shift register, have been laid out as transmission gates. When properly designed this configuration reduces the clock feedthrough of the gate signal. In addition, by a proper choice of sizes of the PMOS- and NMOS-transistors, the voltage dependence of the on-resistance is minimized. The reset switch S_6 is also a transmission gate to reduce the offset from the clock feedthrough of the reset signal.
- The switches S_1, S_2, S_4 and S_5 are wide NMOS-transistors. In this way the charging time constant given by the on-resistance of S_1, S_3^n and S_4 is about 4 ns. This time constant is short enough, compared to the 96 ns between crossings, to guarantee a stored charge independent of earlier stored charges and short enough compared to the rise time of the shaped signals.
- The design of the operational amplifier is based on a circuit described in ref. [5]. Changes have been made to increase the open loop gain and to improve the settling time. The simulations show that an open-loop gain of around 100 dB can be reached providing good linearity. Model calculations for the signal to-noise ratio (S/N) predict a value of 87 dB.

Not all of these design features have been successfully implemented in the test chip.

A more detailed description of the design considerations, the design itself and of the simulations is given in ref. [6].

Table 1
Specifications for the switched-capacitor pipeline

Input	0 to −4 V unipolar
Signal-to-noise ratio	better than 12 bit
Matching of capacitors	better than 8 bit
Linearity	better than 0.25%
Charging time constant	< 4 ns
Time jitter	< 0.5 ns
Write frequency	> 10 MHz
Settling time of output amplifier (0.1%)	< 300 ns
Read frequency	> 1 MHz

3. Measurements on test chips

The development was started with a test chip which contains the essential parts of the pipeline. It is a pipeline of eight storage capacitors designed in a way which can be extended easily to full length without major modifications. The test chip uses a larger set of

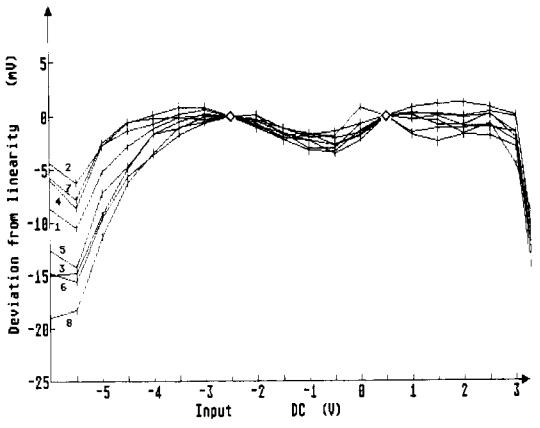

Fig. 2. Linearity of the pipeline. Deviation of the output voltage from a straight line through the values of −2.5 and 0.5 V for different cells.

control signals to allow flexible operation for easier understanding. The pipeline of the test chip is organized in two rows of four capacitors, an upper and a lower row. The storage capacitor has a value of 1 pF and the feedback capacitor one of 2 pF, resulting in a gain of 0.5.

The output of the operational amplifier was buffered for the measurements by an external high-impedance buffer amplifier. All test measurements have been done at 10.4 MHz shift frequency. The shift register alone has been run up to 25 MHz.

The linearity and dynamic range measurements have been done with a 12-bit ADC and a 16-bit DAC. The measured noise was 0.5 mV. Part of this noise is introduced by the test setup itself. The deviations of the output voltages from a straight line through the values for −2.5 V and 0.5 V input voltage are given in fig. 2. For a range from −4 to 2.5 V it shows deviations of less than 2 mV. The difference for positive and negative polarity is expected since the wide write- and read-switches are NMOS-transistors, which are switched off by large positive input voltages. The measured noise and the range of linearity give a dynamic range of 8000 : 1.

Fig. 3 shows the gain for the eight different storage cells for chips from two wafers. In fig. 3a there is a systematic difference of about 1% between capacitors 1–4 (upper row) and 5–8 (lower row). Inspection under a microscope showed that the difference is due to a misalignment of masks still within the allowed tolerances. Within the two groups the gains differ by about 0.25%, which is within the required 8 bits. Fig. 3b shows a much better uniformity for chips from another wafer. Within one wafer the gain of the same storage cell varies from chip to chip by about 0.5%. We have changed the design of the capacitors, so that their values do not change given alignment errors within tolerances.

Fig. 4 shows the output voltage for the eight storage cells for dc input voltages of 0 and −1 V input. The pedestals differ by up to 350 mV, due to differences in the layout of the signal paths in the region of the transmission gates for different storage cells. This deficiency could be cured by a simple redesign.

The settling time of the operational amplifier to 0.1% of the signal has been measured through a fast high-impedance buffer. It is about 300 ns.

The effective charging time constant during the write phase was measured by delaying a square wave pulse of 1 ns rise time with respect to the clock signal for the shift register. An RC-constant of about 3 ns is found, as shown in fig. 5.

The time of opening of the different transmission gates S_3^n relative to the shift clock signal was measured.

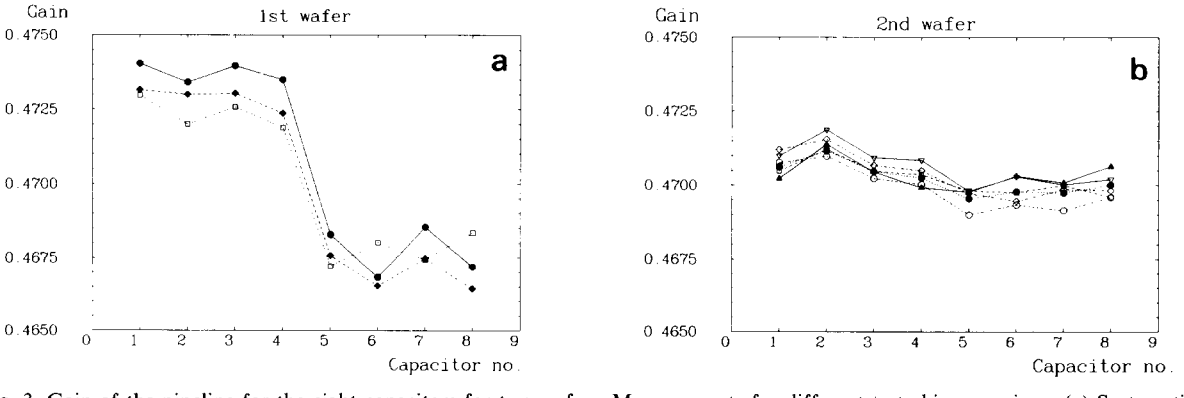

Fig. 3. Gain of the pipeline for the eight capacitors for two wafers. Measurements for different test chips are given. (a) Systematic shift of gains due to misalignments of masks still within tolerances. (b) Gains for a wafer with better alignment.

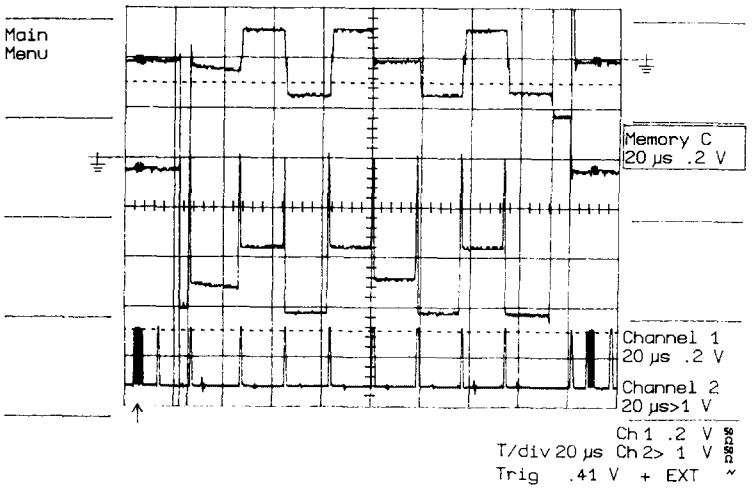

Fig. 4. Oscilloscope traces showing pedestal variations. Upper trace: 0 V input voltage (0.5 V/div); middle trace: −1 V input voltage (0.5 V/div); bottom trace: clock sequence.

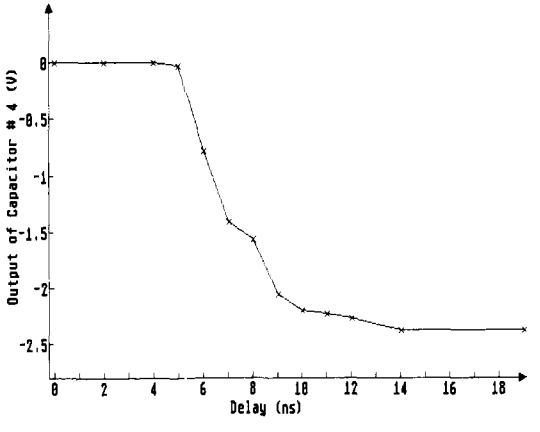

Fig. 5. Charging time constant.

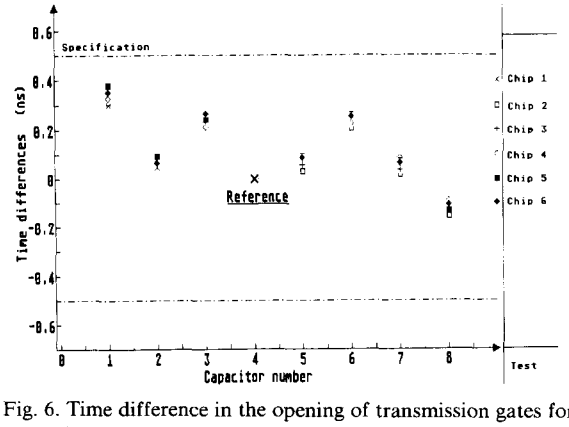

Fig. 6. Time difference in the opening of transmission gates for the eight capacitors. Cell 4 has been taken as reference. Measurements for different test chips are given.

The difference for the different storage cells is less than 0.5 ns, as shown in fig. 6.

4. Radiation sensitivity measurements

In ZEUS the analog pipeline will be mounted directly on the detector for best noise performance. A radiation field of ionizing radiation and neutrons with about 1 krad per year and about 5×10^{11} n/cm^2 per year, respectively, is expected. Irradiations have been done using gamma rays, neutrons and a mixed radiation field close to a target being hit by 800 GeV protons. The irradiations were done with the test chips under operation conditions. Preliminary results show no degradation in performance up to 5 krad. A chip irradiated by gamma rays with a dose of 10 krad shows a deteriorated performance. The irradiation done with neutrons are still being analyzed. Close to the proton beam the test chips received a dose of about 15 krad ionizing radiation and 30 krad neutrons, corresponding to about 10^{13} n/cm^2. This dose damaged the test chips severely. The investigations are being continued with the aim to understand the cause for the degraded performance, to achieve a more radiation-tolerant design without a change of the technology.

5. Conclusions

The measurements on the test chip for an analog pipeline have proven that the proposed design is able to meet the requirements to read out the ZEUS calorimeter. The experience with the test chip has resulted in an

improved design of the prototype chip. The prototype chip will have four independent pipelines, controlled by one set of signals. The pipeline will be 58 cells long. The first wafers of the prototype have been processed. First tests have shown that the chip is functioning; in particular, the large cell-to-cell difference in the pedestals has been reduced to a few mV.

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