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The ZEUS calorimeter first level trigger

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Abstract

The design of the ZEUS Calorimeter First Level Trigger (CFLT) is presented. The CFLT utilizes a pipelined architecture to provide trigger data for a Global First Level Trigger decision 5 μs after each beam crossing, occurring every 96 ns. The charges from 13 K phototubes are summed into 1792 trigger tower pulseheights which are digitized by flash ADCs. The digital values are linearized, stored and used for sums and pattern tests. Summary data is forwarded to the Global First Level Trigger for each crossing 2 μs after the crossing occurred. The CFLT determines the total energy, the total transverse energy, the missing energy, and the energy and number of isolated electrons and muons. It also provides information on the electromagnetic and hadronic energy deposited in various regions of the calorimeter. The CFLT has kept the experimental trigger rate below ≈ 200 Hz at the highest luminosity experienced at HERA. Performance studies suggest that the CFLT will keep the trigger rate below 1 kHz against a rate of proton–beam gas interactions on the order of the 100 kHz expected at design luminosity.

1. Introduction

The HERA accelerator at the DESY laboratory in Hamburg, Germany collides 26.7 GeV electrons with 820 GeV protons. Interesting physics data occurs in the ZEUS detector and is written to tape at the rate of a few Hz. However, background from proton-beam–gas interactions has a much higher rate, on the order of 100 kHz. The time between beam crossings at HERA is 96 ns. This is too short a time for the ZEUS detector to read out the 200 kBytes of data for each event and provide a trigger decision. The data are therefore kept in a pipeline and the first level trigger decision is postponed until 5 μs after the crossing. In order to avoid deadtime, the trigger electronics itself is pipelined: every process in the trigger must be repeated every 96 ns [1]. The total first level trigger output rate from all components is limited to less than 1 kHz by the front end electronics readout and the second level trigger input capacity [2]. Therefore, the ZEUS calorimeter first level trigger (CFLT) rate from beam–gas interactions must be reduced to a fraction of a kHz.

The ZEUS CFLT detects charged and neutral current processes. In these events the current jet(s) and lepton emerge on opposite sides of the beam axis, balancing each other in transverse momentum. The debris of the proton is emitted forward in a narrow cone (10 mrad). Neutral current events are characterized by an electron and jet(s) with balanced transverse momentum p_T. Charged current events contain jets and missing p_T. In addition, exotic processes are distinguished by the presence of lepton(s) and jet(s) with missing p_T.

The CFLT identifies charged and neutral current, photoproduction, and exotic physics events while rejecting beam gas background using three different approaches. They are: (i) detection of isolated electrons and muons using pattern analysis logic, (ii) identification of patterns of energy deposits obtained from local energy sums, and (iii) recognition of characteristic deposits of total transverse and missing transverse energy.

The ZEUS calorimeter consists of depleted uranium plates interleaved with plastic scintillator. The scintillator plates form towers which are read out on two sides with wavelength shifter bars, light guides and photomultipliers. The calculations required for the calorimeter trigger include summing all of the pulseheights recorded in the photomultipliers every 96 ns. In addition, calculation of the transverse energy and missing p_T requires algebraically summing pulseheights multiplied by geometric factors. The detection of an electron requires evidence of electromagnetic energy. This is done by comparing energy

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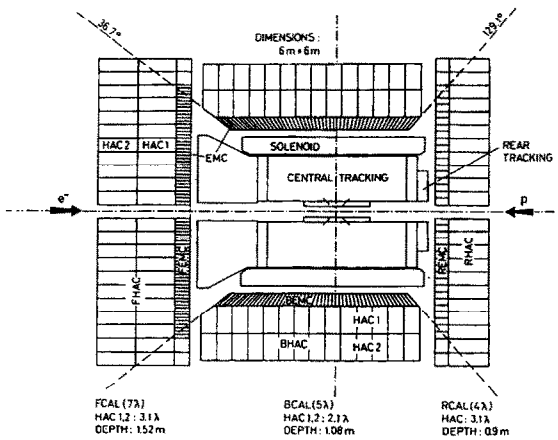

Fig. 1. Side view of the ZEUS calorimeter.

deposited in the first interaction length of the calorimeter with that deposited in subsequent interactions lengths on a tower by tower basis.

2. Overview of the calorimeter and first level trigger

2.1. Calorimeter geometry

The Forward Calorimeter (FCAL), Barrel Calorimeter (BCAL), and Rear Calorimeter (RCAL) sections of the ZEUS calorimeter are built in modules, running vertically in the case of FCAL and RCAL and longitudinally in the case of BCAL. Each module is segmented into towers, as depicted in Figs. 1 and 2. The layers of scintillator and depleted uranium making up calorimeter towers are divided into four different types of cells, depending on their position within the tower. Cells are either electromagnetic (EMC) or hadronic (HAC) and are classed as EMC, HAC0, HAC1, and HAC2.

The first interaction length in FCAL, BCAL, and RCAL consists of EMC cells, except for those near the edges of FCAL and RCAL, where the cells are shadowed from the interaction point by the BCAL. The EMC cells have a front area of 5 cm by 20 cm in the FCAL, 5 cm by 23 cm in the BCAL, and 10 cm by 20 cm in the RCAL. The

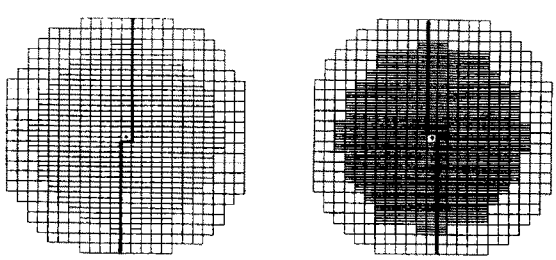

Fig. 2. View of FCAL (left) and RCAL (right) as seen from the interaction point.

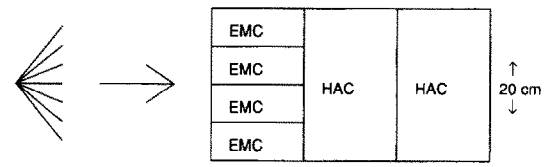

Fig. 3. View of a typical calorimeter trigger tower.

BCAL EMC cells are the only projective cells in the calorimeter.

Certain FCAL and RCAL cells in the first interaction length are designated as HAC0 cells, and have 20 cm by 20 cm front faces. Particles from the interaction point passing through these cells first pass through BCAL EMCs. In the RCAL, 24 HAC0 cells are used as EMCs because the BCAL does not fully shadow them.

The subsequent 3 interaction lengths in FCAL and RCAL and 2 interaction lengths in BCAL are HAC1 cells. The last 1.5 to 3 interaction lengths (depending on radius from the beampipe) of FCAL and last 2 interaction lengths of BCAL are HAC2 cells. HAC1 and HAC2 cells in the FCAL and RCAL have 20 cm by 20 cm front faces, while the BCAL HAC cells have front faces of 27 cm by 23 cm for HAC1, and 35 cm by 23 cm for HAC2 [1]. Fig. 3 shows a typical trigger tower (similar to FCAL at small θ or BCAL at $\theta \approx 90°$), with 4 EMC cells in front, followed by a HAC1 and a HAC2.

2.2. Trigger towers

The problem of defining trigger towers is complicated by the fact that the calorimeter is largely nonprojective. The regions of greatest difficulty are at $\theta = 37°$ and $\theta = 129°$. In these regions trigger towers must be made which include towers in both FCAL and BCAL and both BCAL and RCAL, respectively. Trigger towers consist of a block of 4 (FCAL and BCAL) or 2 (RCAL) EMC cells, and those HAC1 and HAC2 cells that lie most projectively behind the EMC cells. Fig. 4 shows a side view of the calorimeter with the trigger tower arrangement shaded in, and Fig. 5 shows views of the FCAL and RCAL with the BCAL projection from the interaction point outlined on it. The total of 896 trigger towers are organized into sixteen 7×8 regions. These regions are themselves divided into 4 edge subregions and 1 contained subregion as shown in Fig. 6.

2.3. Zeus trigger system

The overall architecture for the ZEUS detector trigger and data acquisition system is shown in Fig. 7. A three-level trigger system reduces the trigger rate to a few Hz. The

[1] All dimensions given above are approximate.

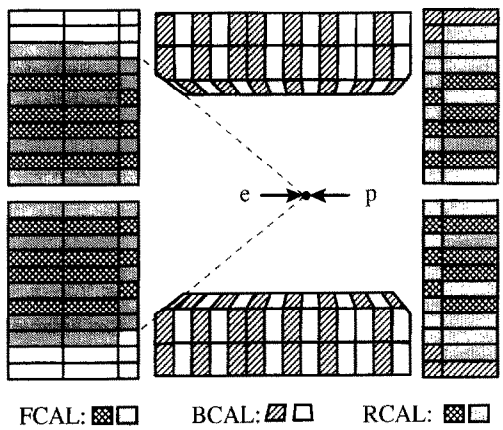

Fig. 4. Side view of trigger tower arrangement.

First-Level Trigger has the task to reduce an input rate as high as 100 kHz to less than 1 kHz by eliminating most of the beam–gas background. Dedicated logic, in combination with many programmable parameters, is used throughout this level. Results of the local processors are combined in the Global First Level Trigger (GFLT). At the Second-Level commercially available microprocessors – mainly INMOS Transputers – analyze the digitized data of the components. Combining the results of the local processors in the Global Second Level Trigger (GSLT) results in a further reduction of the trigger rate below 100 Hz. After a positive decision the data of all subdetectors is gathered and sent to a Third-Level processor farm of Silicon Graphics workstations.

For every bunch crossing all data are stored in a pipeline, clocked at 96 ns, for $\sim 5\mu s$ while the first level trigger calculations are being performed and the first level trigger signal is propagating back to the component. For some components, such as the calorimeter, this pipeline is a switched capacitor array, which is an analog device that stores charge. For other components, such as the tracking detectors, the information is already digital and stored in a digital pipeline. The trigger processing for all components is pipelined and basically free of deadtime, accepting data from a new crossing every 96 ns. The first level trigger operates on a subset of the full data. Each component completes its internal trigger calculations and passes information for a particular crossing to the GFLT between 1.0 and 2.5 μs after the crossing occurred. The GFLT calculations take 20 crossings (1.9 μs) additional time after receiving information from the individual components. The GFLT is issued exactly 46 crossings, or 4.4 μs after the crossing that produced it. If a GFLT is not issued for a crossing, the component data are discarded.

There is additional processing of calorimeter trigger data by the Fast Clear [4] between arrivals of global first level triggers. The Fast Clear aborts events before processing by the second level trigger. The design goal of the first level trigger when combined with the Fast Clear, is to produce an output below 1 kHz. When the Fast Clear is operating, the GFLT rate can run at 2–3 kHz with the Fast Clear aborting sufficient GFLTs to bring the rate below 1 kHz.

The issuing of a first level trigger causes component data to be transferred to buffers for processing by the second level trigger. The second level trigger processor functions as an asynchronous pipeline, i.e. a series of parallel processors. The second level trigger decisions are made in the order of events received. The second level trigger has access to a large fraction of the full data for the event. The data passing the second level trigger is then

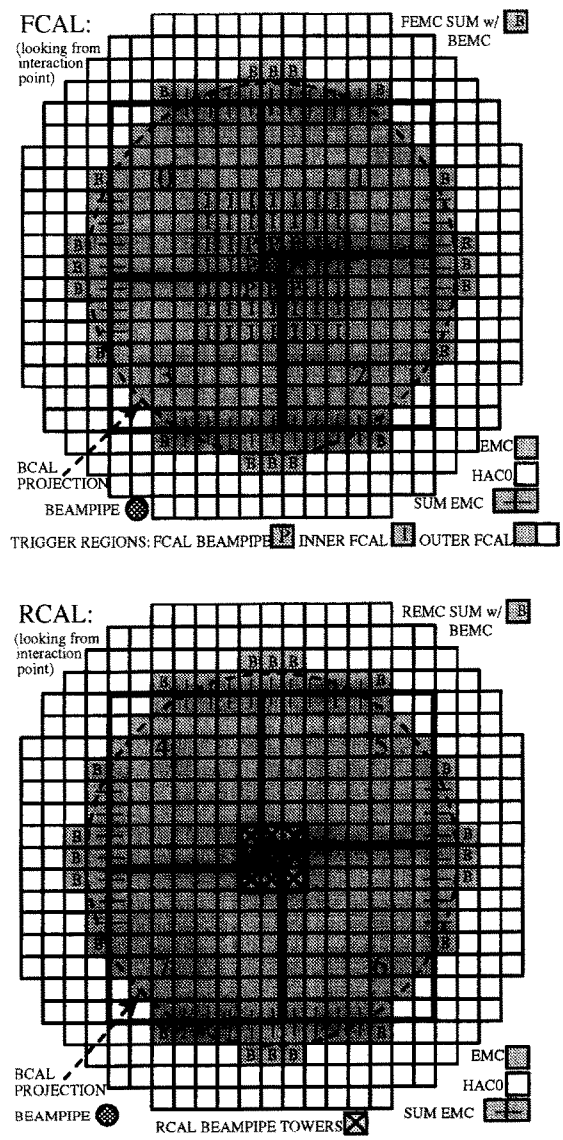

Fig. 5. View from the interaction point of the FCAL and RCAL trigger regions and trigger towers.

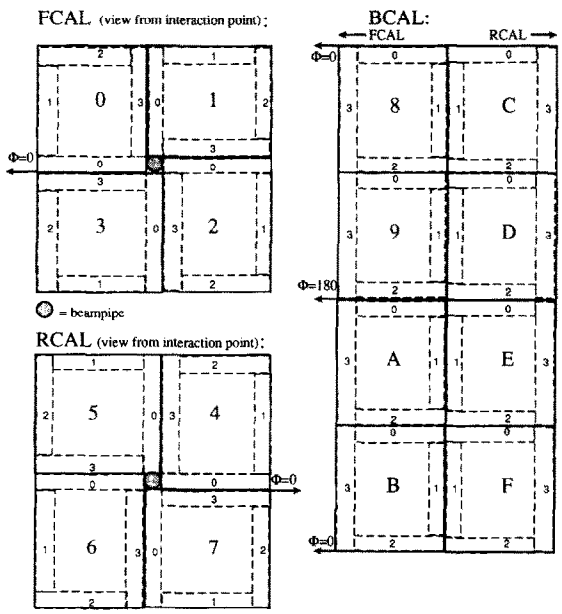

Fig. 6. Trigger regions of the calorimeter (O–F) with edge regions shown.

sent to the level 3 computer farm, where trigger decisions are based on the full analysis. The third level trigger runs a version of the full offline analysis code and passes an output rate of about 3–5 Hz.

2.4. Organization of calorimeter first level trigger

The Calorimeter First Level Trigger has to make each step of its calculations, including digitization of the PMT pulse, at a rate of 96 ns in order to keep up with the incoming data. However, in order to reduce the amount of electronics, cables, and crate backplane required, the data is at several points multiplexed in time, so that many elements of the system run at rates up to 83 MHz. The Calorimeter First Level Trigger passes trigger information to the Global First Level Trigger within 2 μs.

The organization of the CFLT is shown in Fig. 8. The first element of the CFLT is the the Trigger Sum Card (TSC), which is mounted on the detector next to the Front End Cards (FEC) [3]. The FECs are the first step in the calorimeter data acquisition chain. Each FEC accepts pulses from up to 12 photomultiplier tubes (PMT) and passes 5% of sums of up to 4 PMTs to the TSC. The TSC receives 8 inputs, 4 left and 4 right phototube sum signals. These are integrated and summed for each left and right pair, and the baseline restored quickly after the integration. The TSC, having shaped the signal, sends it as a differential signal down 60 m of shielded twisted pair cable to the electronics house, where it enters the Trigger Encoder Card (TEC) for digitization.

After digitization the TEC linearizes, pedestal corrects, and zero suppresses the energy. It also tests whether the energy is consistent with a minimum ionizing particle or a quiet tower. The corrected energy is used to calculate E, E_T, E_x, and E_y. These values are fed into adder trees, which combine like values for towers of the same type (EMC or HAC). The partial sums from each TEC are sent to the Adder Card which completes the summation of E, E_T, E_x, and E_y for a single 7×8 region. The linearized energy for each channel is also placed in a FIFO. The data at the head of the FIFO is sent to the Fast Clear [4] via the Adder Card upon receipt of a trigger. EMC and HAC data from the same tower are also used to address a memory lookup table which determines which of 6 thresholds the trigger tower energy has passed. The same table determines if there is an electron candidate in that tower. Threshold level, electron candidate, minimum ionizing particle, and quiet tower information are all forwarded to the Adder Card.

The Adder Card sends control signals and clocks out to the TECs on the backplane. It collects FIFO data from the TECs and sends them to the Fast Clear upon receipt of a trigger, and continues the summing of E, E_T, E_x, and E_y. It determines, from the tower energy thresholds, the energies in programmable subregions of the 7×8 crate region. The Adder Card histograms the number of towers in the region which reached each threshold, and finds the number of isolated muons and electrons in the region. This information is sent from the Adder Cards in the 16 trigger crates to the CFLT processor (CFLTP) [5].

The CFLTP calculates the total E_T, missing E_T, electromagnetic and hadronic energy, compares region boundaries to calculate the number of isolated electrons and muons, and computes regional EMC, HAC and total energies, particularly around the beam–pipe region where the beam–gas background is greatest. The summary of this information is transmitted to the Global First Level Trigger (GFLT) for each 96 ns crossing.

3. Trigger sum cards

Each calorimeter cell is read out by one left and one right PMT. Generally, up to 12 left or 12 right PMT signals are sent to a module-mounted Front End Card (FEC) [3]. Usually, there are 2 HAC sum outputs (HAC1 + HAC2) and 2 EMC sum outputs (EMC1 + EMC2 + EMC3 + EMC4). In the RCAL, the FECs produce 8 sum outputs, consisting of 4 individual HAC1s and 4 EMC sum outputs (EMC1 + EMC2). The outputs of pairs of right and left FECs are sent to Trigger Sum Cards (TSC), also mounted on the module. Depending upon the setting of jumpers on the TSC, these FEC outputs may be combined to make either 4 sums (2 HAC and 2 EMC) of 2 channels each, or, in places where there are HAC0 instead of EMC cells, to make 2 HAC sums of 4 channels each. These

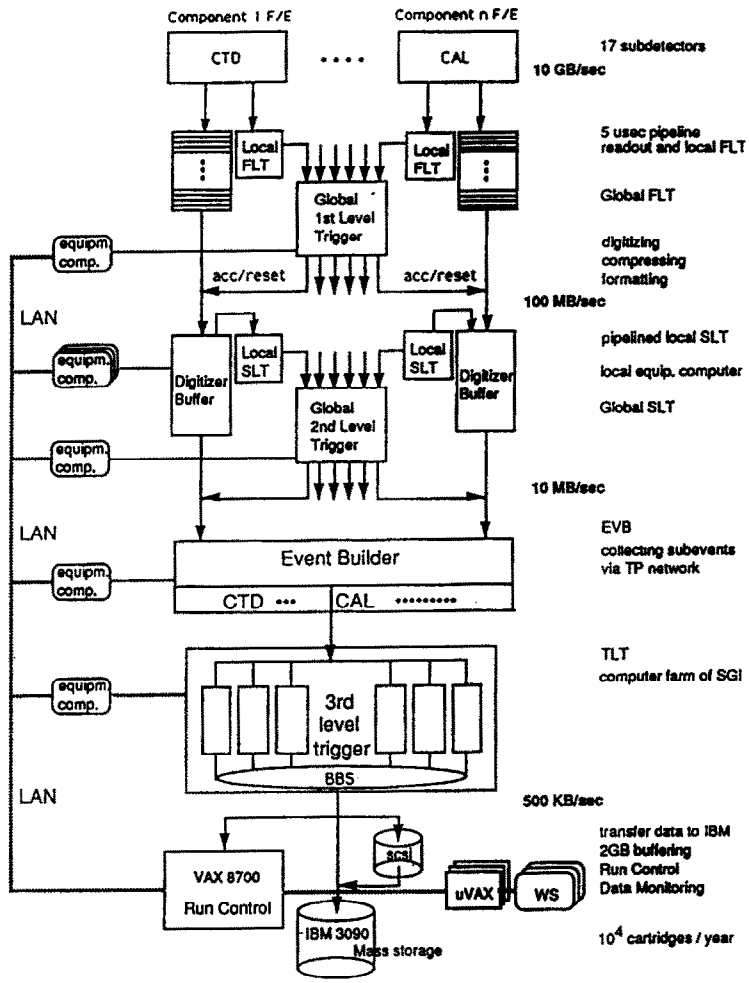

Fig. 7. The ZEUS trigger and data acquisition system.

sums are then sent to the TECs located in the electronics house.

3.1. TSC input and output

The TSC sits in the calorimeter backbeam area adjacent to the FECs. It has 8 current inputs (4 left and 4 right) and generates 4 outputs. The cables from the FEC to the TSC are the same length throughout the FCAL, BCAL and RCAL. The only major exception is additional cable length

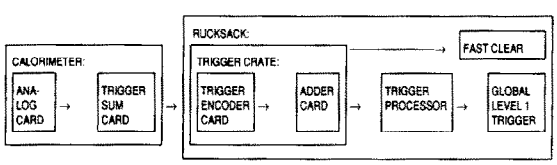

Fig. 8. Organization of the Calorimeter First Level Trigger.

added to compensate for faster tubes used in the FCAL EMC towers. The result is that the groups of FCAL, BCAL and RCAL TSCs receive their signals within 2 ns of each other.

Each TSC output consists of two amplifiers each driving one half of a shielded twisted pair cable in differential mode. The TSC sums left and right FEC sums for each trigger tower to produce 2 sums (EMC and HAC) for each of 2 towers containing EMC and HAC sections. The TSC produces up to 4 separate HAC sums for towers without EMC sections. In order to facilitate special combinations of HAC cells in those FCAL and RCAL regions which are shadowed by BCAL EMC towers, the TSC has internal jumpers that can be used to combine up to all 8 of its inputs to generate a single output. In practice, up to 6 inputs are combined. In these cases, 1 or more of the 4 output channels are unused. In most locations, 2 input channels are summed in 1 output channel. However, in regions of complex geometry, the TSC is used to directly

combine the left and right sides of 2 HAC (4 inputs) sections in a single output sum.

3.2. TSC gain

Phototube gains are set so that 1 GeV of energy in a single FCAL section produces a charge of 3.65 pC on each of the two phototubes attached to it, and 1 GeV of energy in a single BCAL section produces a charge of 5.30 pC on each of the two phototubes attached to it. This means that the when the left and right phototubes attached to a section are summed, the total charge produced per GeV of deposited energy is 7.3 pC in the FCAL and 10.6 pC in the BCAL.

Each FEC separately sums the hadronic and electromagnetic phototube signals for each of the trigger tower sections connected to it. The FEC outputs 1/20 of the total hadronic and electromagnetic phototube current for either the left or right side of the trigger tower section. The charge delivered to the TSC for a minimum ionizing particle (Q_{mip}) is 1/20 of the section total (left and right PMTs), in pC/GeV given above, times the energy deposited by a minimum ionizing particle (E_{mip}). The HAC energy is the sum of both HAC1 and HAC2 sections. The maximum charge delivered to the TSC (Q_{max}) is 1/20 of the section total, in pC/GeV given above, times the maximum energy that can be deposited in a section (E_{max}), where E_{max} is 400 GeV for the FCAL and 100 GeV for the BCAL and RCAL. In addition, there are a few BCAL trigger towers which have FCAL sections summed with BCAL sections. For the BCAL sections in these trigger towers, the gain is set so that E_{max} is 400 GeV.

The TSC can drive at most a signal of 2 V on its output cable to the Trigger Encoder Card (TEC). This sets the gain of the TSC at 2000 mV/Q_{max}. The digitization scales of the low gain and high gain channel FADCs in the TEC are computed based on the requirement that the high gain scale for all calorimeter sections be 0 to 12.5 GeV. This gives a high-to-low gain ratio of 32 in the FCAL and 8 in the BCAL and RCAL.

3.3. TSC design

The TSC has 4 identical input channels, each with 2 current inputs (left and right halves), and 4 output channels each driving one shielded twisted pair cable. The current source is transmitted from the FEC to the TSC on 50 Ω coaxial cable. Each input line is connected through a 34 Ω series resistor to an emitter, biased by 1 mA (the current drawn by the front end FEC). This series resistor, in combination with the impedance of the emitter, provides a suitable termination for the cable.

The total charge entering the input is integrated and converted to an output voltage. The capacitor in the feedback path of the operational amplifier differs between TSCs in the RCAL/BCAL and FCAL due to the different gains required in the two calorimeter sections. The resulting voltage is split and applied to both inputs of a second

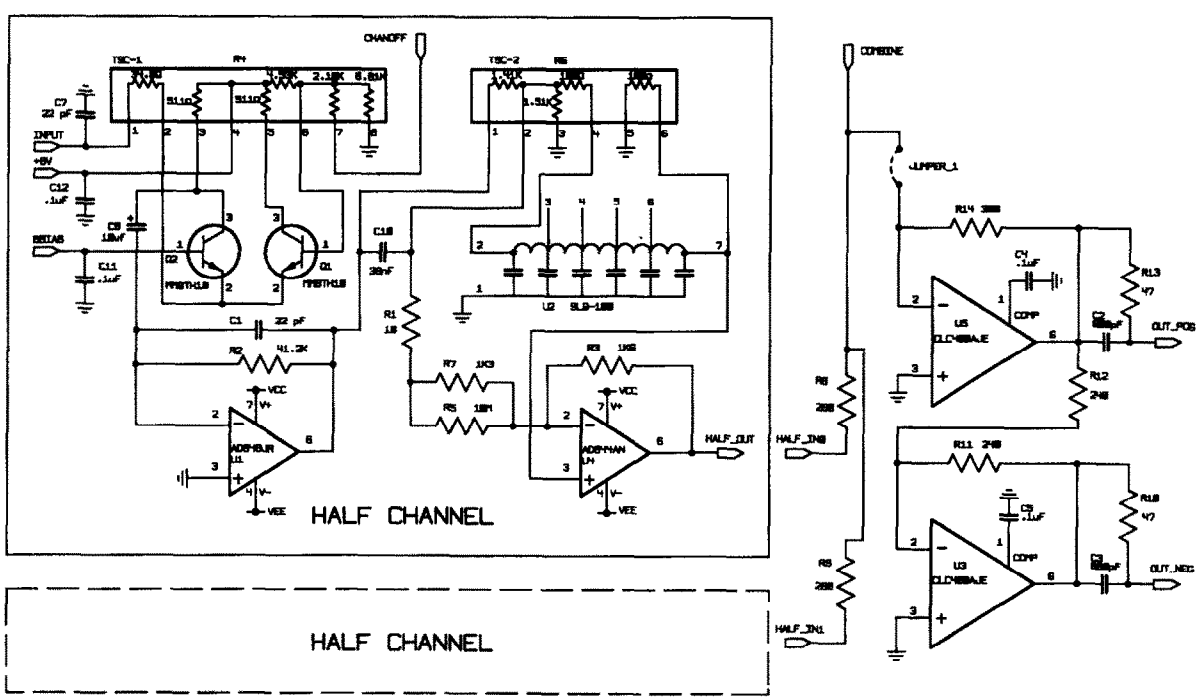

Fig. 9. Circuit diagram of one channel of the Trigger Sum Card.

Table 1
Trigger tower threshold values (3 bits). These are programmable and can be changed

	Threshold number							
	0	1	2	3	4	5	6	7
Threshold (bit representation)	000	001	010	011	100	101	110	111
Tower energy greater than (GeV)	–	1.25	2.5	5.0	10.0	20.0	40.0	overflow

Op Amp. The signal on the plus input is passed through a 100 ns delay line. Thus, the output of the amplifier produces a voltage proportional to the total charge collected, and then, 100 ns later, restores the output to zero.

The outputs of the amplifiers for the left and right inputs of each channel are passed through resistors, and a jumper, to the summing node of a high speed Op Amp (CLC400) with 50 mA drive capability. This CLC400, in conjunction with a second CLC400, is used to drive 60 m of shielded twisted pair between the calorimeter and the electronics house. The line to line impedance of the twisted pair is approximately 95 Ω. The gain of the Op Amps is adjusted to produce a full scale output of 2 V. Series terminating resistors of 47.5 Ω are placed between the outputs of the Op Amps and the cable. Peaking capacitors are placed across these resistors to partially compensate for the frequency response of the cable (similar to RG174). The series resistors act as part of a potential divider network, halving the voltage on the cable to a maximum of plus or minus 1 V. A schematic of the TSC circuit is shown in Fig. 9.

3.4. TSC control

The TSC has a serial interface connected to a command cable. This cable carries commands that direct the TSC to disable either the left or right input sum. This feature is used to compensate for the failure of a left or right signal. If, for example, the right sum of a particular trigger tower section was very noisy, it would be shut off, while the TEC gain memory lookup table would be changed to multiply the gain of the trigger tower section by 2, compensating for the loss of pulseheight from the right sum. Under normal conditions, all sums are turned on. Turning power off and on causes all channels to turn on.

The TSC also applies a threshold to each pair of left and right inputs. The threshold voltage is provided on a cable input to each TSC. The threshold is set by a digital-to-analog converter (DAC) situated on each calorimeter module. This DAC is controlled by the same command cable that controls the TSC input on/off circuitry. If either the left signal or right signal, but not both, exceeds the threshold, a logic signal is generated for the time that the disagreement is present. The signals from the 4 output channels on an individual TSC card are ORed together. These signals are called the TSC Veto because they are designed to veto false electron signals resulting from noise on an individual EMC PMT. If this noise is the correct amount, it will pass the electron threshold on the TEC. Since the tower HAC section and the surrounding tower HAC and EM sections are likely to be quiet, the noise will pass as an isolated electron.

4. Trigger encoder cards

Each TEC has 8 input channels, and each input channel can be connected to 2 TSC outputs. 14 TECs in each trigger crate, located in the electronics house, cover an entire 7×8 trigger region. There are 16 crates covering the entire calorimeter, one for each of the 16 trigger regions. Each crate covers 56 trigger towers and contains 14 TECs and 2 trigger adder cards, giving a total of 896 trigger towers, 224 TECs, and 32 adder cards.

4.1. TEC overview

The function of the Trigger Encoder Card is to receive and digitize the analog trigger sum signals. The card produces a linearized energy value for each of these signals. For each of four towers, the TECs digitize and linearize the EMC and HAC energy and store them in a 64-element FIFO buffer so that they can be sent to the Fast Clear [4] upon receipt of a Global First Level Trigger (GFLT). The TEC multiplies these linearized energies by geometric factors to calculate, on a tower by tower basis, electromagnetic and hadronic E_{total}, E_{T}, E_x, and E_y [2] using programmable geometric lookup tables. The TEC sums these EMC and HAC energies separately over 4 towers for transmission to the Adder Card, located in the same crate.

In parallel with the energy sums, the TEC also performs tests for quiet towers (Q bit – a value of energy consistent with noise and less than "minimum ionizing"), towers with the ratio of EMC to HAC energy consistent with an electromagnetic shower (E bit) and towers with the amount of EMC and HAC energy consistent with muonic (M bit) energy deposits. The TEC also tests the sum of HAC and EMC energy against against 6 different thresholds and for overflow (energy beyond the input

[2] $E_{\text{T}} = E \sin\theta$, $E_x = E \sin\theta \cos\phi$, $E_y = E \sin\theta \sin\phi$.

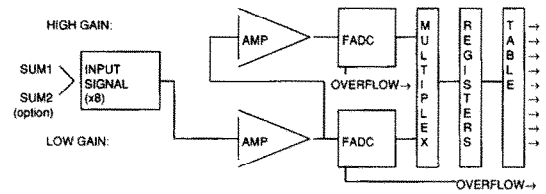

Fig. 10. Organization of the TEC front end.

dynamic range). The trigger tower energy thresholds used in this analysis are shown in Table 1. They are programmable and can be changed, with the requirement that each threshold be a factor of 2 greater than the one below it. The TEC forwards the results of these tests to the Adder Card.

The 8 analog channels in each TEC produce an EMC energy sum and a HAC energy sum for each of four trigger towers. Each channel can sum two inputs, for a total of 16 possible signal inputs per TEC. This feature is provided to complete the summation of the EMC and HAC energies in those regions of the calorimeter where two TSC outputs are required to produce partial energy sums for a single trigger tower.

Although each TEC makes EMC and HAC sums of the 4 towers for the digitized values of E_{total}, E_{T}, E_x, and E_y, should a trigger be accepted, the individual tower EMC and HAC energy digitizations stored in a FIFO buffer are sent to the Fast Clear [4] for additional processing and transmission to the data acquisition system.

4.2. TEC front end

The organization of the front end of the Trigger Encoder Card is shown in Fig. 10. The signal is received, summed, and passed on to 2 amplifiers with high and low gain. These 2 amplifiers each drive a Flash Analog to Digital Convertor (FADC) which digitizes the signal. These digital results are then used as input to a memory lookup table that produces linearized energies.

Up to 16 signals from a TSC are received by a single Trigger Encoder Card (TEC). However, only 8 of these may be independently digitized; 4 are EMC and 4 are HAC. The basic organization is that the EMC and HAC sums from 4 trigger towers are digitized by each TEC. In those cases where two HAC sums were grouped with an EMC sum, the card digitizes the HAC sums in pairs from up to 8 tower sections. Each of the channels on the TEC receives its input from 2 connectors. Each input is received by a single operational amplifier configured as a differential receiver. The outputs of these differential receivers are summed, in pairs, by a third amplifier (CLC502) with high and low clamping thresholds. The clamping is applied to protect the FADCs that follow in the circuit. This input configuration provides for the combination of 2 separate HAC trigger tower sums before amplification. This is used where sums are combined from different modules of the calorimeter. Such sums cannot be made out on the calorimeter modules. They can only be made on signals that overlap closely in time.

The output of the summing amplifier is applied to the low gain FADC. It is also applied to a second amplifier (CLC501) which produces the input for the high gain FADC. Both these amplifiers have clamping on their outputs, 2 ns propagation times, and settling times of 12 ns. The Comlinear CLC502, with gains between 1 and 8, is used for the low gain channels, and the Comlinear CLC501, with gains between 7 and 50, is used for the high gain channels. The gains of these amplifiers are set so that full scale corresponds to a 2 V output into 50 Ω.

The TEC sets full scale for all high gain EMC and HAC channels to EMAX = 12.5 GeV, and sets two low gain scales, one for FCAL and the other for BCAL and RCAL. The FCAL TECs have a low gain channel with full scale at EMAX = 400 GeV, and the BCAL and RCAL TECs have a low gain channel with full scale at EMAX = 100 GeV. Since the least significant bit for each of these scales is EMAX/256, the high gain scales are 0.05 GeV/bit, and the low gain scale is 1.6 GeV/bit for the FCAL and 0.4 GeV/bit for the BCAL and RCAL. The offsets for all the high gain channel Comlinear amplifiers are set together on 1 TEC by a single DAC, and those of the low gain channels are set by a second DAC. This allows independent adjustment of the FADC pedestals for the high and low gain channels.

After amplification, each signal is digitized by an 8-bit FADC, Motorola 10319. The least significant bit is equivalent to 7.8 mV. Therefore, the high gain FADC is digitizing signals that are 7.8/32 mV on the cable. Noise in the system is less than 4 counts on any individual high gain channel.

The outputs of the high and low gain FADCs are OR-tied together. The overflow bit of the high gain FADC is used to disable the high gain FADC outputs and enable those of the low gain FADC. The value of both the high gain and low gain FADC overflow bits are written into a register along with the output of the active converter. This register is clocked with a 96 ns clock, whose phase is fixed with respect to the FADC clock. The overall phase of the FADC/register pair can be adjusted, independently for each channel, to set the FADC sampling aperture to the peak of the incoming waveform.

A second register, following the FADC/register pair, synchronizes the incoming data with the 96 ns clock driving the entire trigger system in lockstep. The register holds 10 bits of data, the 8 bits of FADC data (either high or low) and the high and low channel overflow bits.

4.3. TEC memory lookups

The contents of the 10-bit synchronized register (8 bits of either high or low gain FADC data plus two bits of high

and low gain FADC overflow) form the address presented to a TTL BiCMOS memory (Linearization Memory) organized into 2 pages. An 11th bit of address, changing state every 48 ns, switches the memory between the two pages.

The first page of the Linearization Memory converts the raw FADC pulseheight and range information into a calibrated energy on two different 8-bit scales, depending on whether the high or low gain FADC data was used. This is determined by the high gain FADC overflow bit (0 if high gain was used, 1 if low gain was used). When the high gain FADC data is converted, it is placed on a scale of 12.5 GeV/256 = 49 MeV/bit, and when the low gain is converted, it is placed on a scale of 400 GeV/256 = 1.6 GeV/bit for the FCAL and 100 GeV/256 = 0.39 GeV/bit for the BCAL and RCAL. The value of true energy corresponding to each FADC value is recorded as an 8-bit word at the address of the FADC value. This energy is fully corrected for gain, pedestal and nonlinearities. Energies below a low threshold, presently at about 500 MeV, are set to zero. The values in the linearization memory are determined by comparison with the calibrated calorimeter analog physics and charge injection data as processed through the data acquisition system.

The 8 bits of energy, along with the high gain FADC overflow bit are placed in a 9-bit register for the geometric factor memories that feed the E, E_T, E_x, and E_y values to the adder trees. The contents of this 9-bit register are also placed in a 64×9 FIFO and stored for use by the Fast Clear. Data at the head of this FIFO is timed in to correspond with a Trigger Accept propagating back down through the trigger system from the GFLT.

The second page of the Linearization Memory contains 8-bit words that include one bit ("M") indicating the section (either HAC or EMC) has an energy that is consistent with that deposited by a minimum ionizing particle. A second bit indicates that the section has an energy less than that which is consistent with a minimum ionizing particle, and therefore is tagged as quiet ("Q"). The remaining six bits place the energy on a compressed (nonlinear) scale between minimum ionizing and the maximum possible energy that could be deposited. The value of the six bits ranges between 0 and 62. The value of 63 is reserved for when the low gain FADC overflow is set. The layout of the TEC front end linearization and tests for one trigger tower (1/4 of a TEC) is shown in Fig. 11.

The 8 bits of energy from the linearization memory is presented to two additional TTL BiCMOS memories (Geometric Factor), organized into two pages apiece. In addition to the linearized energy, the corresponding overflow bits from both the high and low gain FADCs are included to make up a 10 bit address. An 11th bit, clocked at 48 ns, switches between the two pages. The first and second pages of the first memory contain E and E_T values, respectively, while the first and second pages of the second memory contain E_x and E_y values, respectively.

The values in these memories are stored as 8 bits. For

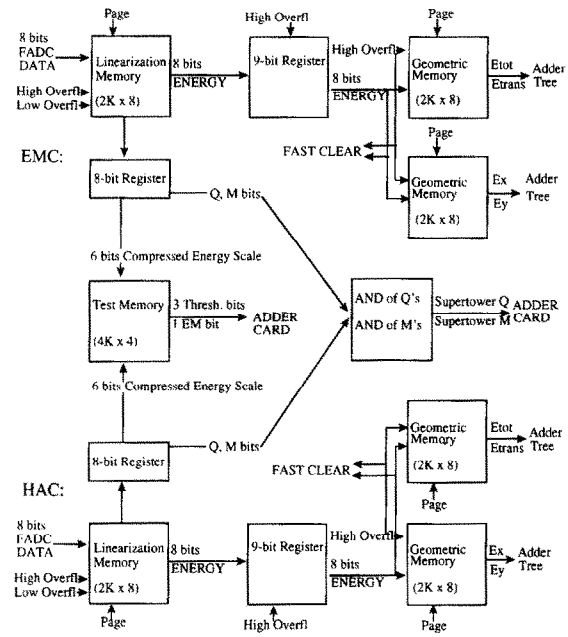

Fig. 11. Layout of TEC front end linearization and tests.

the total energy sum, the scale is set for all channels at 400 GeV/256 = 1.6 GeV/bit. Since the maximum value of E_T is 75 GeV, the E_T ($E \sin\theta$) values for all channels are placed on a scale of 75 GeV/256 = 0.29 GeV/bit. Since the E_x ($E \sin\theta \cos\phi$) and E_y ($E \sin\theta \sin\phi$) values are signed numbers ranging between −75 GeV and +75 GeV, they are expressed in 2's- complement notation on a scale of 75 GeV/128 = 0.58 GeV/bit. The output pages of these memories are used as inputs to two parallel adder trees, clocked at 48 ns. The first page of the first memory provides the E for the first adder tree, and 48 ns later, the second page provides the $E \sin\theta$. The first page of the second memory provides the $E \sin\theta \cos\phi$ to the second adder tree, and 48 ns later, the second page provides the $E \sin\theta \sin\phi$.

4.4. TEC sums

There are 4 parallel, 4 operand, TTL adder trees employed on the TEC. One pair of adder trees sums up E, E_T, E_x, and E_y from the 4 HAC sections serviced by one TEC card, and another pair sums up the 4 EMC sections. In either pair (HAC or EMC) the first adder tree uses the 2 pages of the 4 TTL memories that contain the E and E_T values. At the beginning of the 96 ns cycle, the 4 E values are presented to the adder tree, and after 48 ns, the 4 E_T values are presented. The second adder tree of the pair uses the 2 pages of the 4 TTL memories that contain the E_x and E_y values for either the HAC or EMC section. At the beginning of the 96 ns cycle, the 4 E_x values are presented to the adder tree, and after 48 ns, the 4 E_y

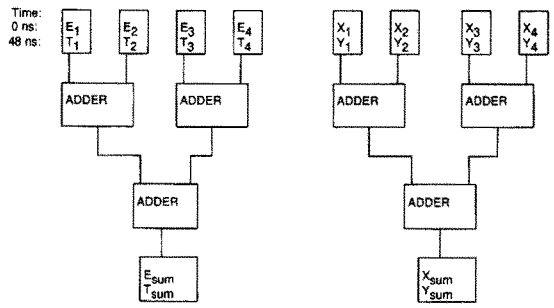

Fig. 12. Trigger encoder card adder tree.

values are presented. These values are combined separately for EMC and HAC sections to make the E, E_T, E_x, and E_y sums. The energy scales defined at the output of the Geometric Memories are retained in each adder tree. The Geometric Memories are shown in Fig. 11. A diagram of one of the two pairs of adder trees on a TEC is shown in Fig. 12.

New results from the 2 HAC sum networks and the 2 EMC sum networks are multiplexed onto one set of 9 lines, translated to ECL and transmitted over 9 bus lines on the backplane at a 12 ns rate. Each of the 7 TECs in a half Trigger Crate broadcasts data on one of 7 sets of bus lines. The set used by a TEC is selected under software control.

4.5. TEC test encoding circuitry

The test encoding circuitry uses the Q, M and 6 compressed energy scale bits from the EMC and HAC sections of a single trigger tower. These are produced by the second page of the linearization memory as detailed above, and shown in Fig. 11. These 8 bits are placed in one register for each section. The tests made on a specific trigger tower are "quiet", minimum ionizing, electromagnetic energy, overflow of the low gain channel, and 6 different energy thresholds. There are 4 test circuits on each TEC. Each circuit makes all of the tests on one trigger tower. The bits for the 4 trigger tower EMC and HAC sections are brought together simultaneously to each of the 4 test circuits, one per tower. The energy threshold and electromagnetic tests for each tower are made by a memory with 12 bits of address composed of the 6 compressed energy scale bits from the EMC section register and the 6 compressed energy scale bits from the HAC section register.

Each test memory address location has a 4 bit word consisting of 3 bits of energy threshold test (T1, T2, T3) and one bit of electromagnetic test ("E" bit). The 3 bits of energy threshold test contain the result of testing the sum of the EMC and HAC energies against 6 energy thresholds. The E bit is set by a comparison of the EMC and HAC section energy. As in the case of the energy threshold test bits, the EM bit can be set by any arbitrary function of the 6 EMC and 6 HAC compressed energy scale bits that form the table address. The Q and M bits from the EMC and HAC section registers are combined in separate Q and M ANDs, resulting in trigger tower Q and M bits.

The results of the tests are contained in 6 bits: the "quiet" test bit (Q), the minimum ionizing test bit (M),

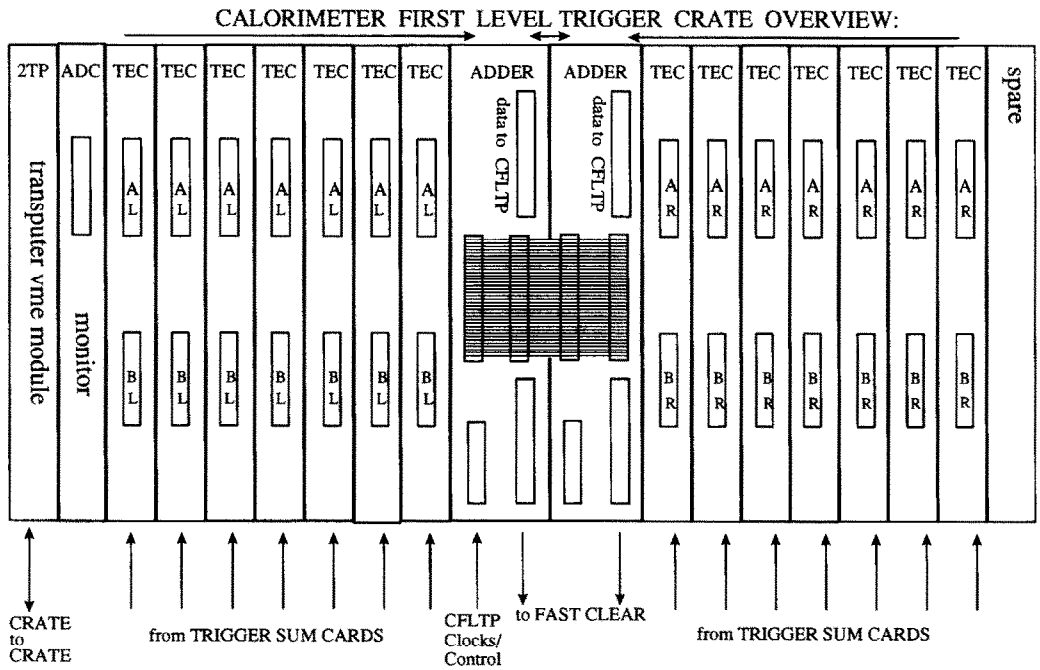

Fig. 13. Schematic outline of a CFLT crate including Trigger Adder Cards, TECs, crate processor card and monitor card. Connections to Fast Clear, CFLTP, and Trigger Sum Cards are also shown.

the electromagnetic test bit (E), and the 3 energy threshold test bits (T1, T2, T3). This data is multiplexed, on a tower by tower basis, to 6 lines, translated to ECL, and further multiplexed to 3 bus lines on the modified J2 and J3 split backplanes at a 12 ns rate.

5. Trigger adder cards

The Adder Card has 2 principal functions. The first is to continue the process of summing up the energies begun on the TEC. The second is to perform pattern tests on the bits that accompany the energy sums. These pattern tests include counting the number of trigger towers passing each of the energy thresholds, summing up the energy from the threshold test bits in subregions of the region covered by the adder card, and finding isolated muons and electrons.

As shown in Fig. 13, there are 2 9U high double-width Adder Cards, which are identical in all respects and reside in the middle of the VME crate in positions 10 and 12. One Adder Card is inserted to the right and the other to the left of the split in the J2 and J3 backplanes. They perform several functions, the first of which is to continue the process of obtaining the total E, E_T, E_x, and E_y. The Adder Card also handles clock distribution, recognition of isolated minimum ionization events, recognition of isolated electromagnetic events, comparison of cell energy against preset thresholds, and some simple histogramming (counting) of the individual cell utilization. Most of the logic is ECL to provide the performance required to process data arriving at nearly 1 Gbyte/s. A short printed circuit card connects the Adder Cards together in the front of the crate. This card transfers data and clocks across the split backplane.

As a result of their central location, the Adder Cards are used to distribute clocks to the Trigger Encoder cards arrayed on either side. The 96 ns and 12 ns clocks are differential ECL signals, fed from the CFLTP on a cable containing only clocks. There is separate, equal-length cabling, from the CFLTP to each of the Adder Cards. The Adder Card generates gated 96, 48, 24, and 12 ns clocks from the CFLTP 12 ns clock. These clocks may be stopped and single stepped under VME control. All actions in the crate occur at the time of the rising edge of the 12 ns clock.

7 TECs on each half of a trigger crate output their data to the nearest of two adder cards located in the center of the crate. The Adder Cards operate as a master and slave, exchanging data to perform their tasks. They continue adding the digitized E_{total}, E_T, E_x, and E_y for those EMC and HAC channels serviced by the crate, perform local sums using threshold information for the subregions shown in Fig. 14, count up numbers of towers passing the various thresholds, and perform pattern tests on the Q, M, and E bits.

The pattern logic searches for contained isolated electrons and muons in the interior 5×6 tower section of each 7×8 trigger region and for edge isolated electrons and muons on each of the four remaining sides of the trigger region. The two Adder Cards then send sums of E_{total}, E_T, E_x, E_y to the CFLTP, along with summaries of the number of edge isolated and contained electrons and muons found in the region. The CFLTP further processes this information, and sends its results on to the global first level trigger processor (GFLTP) [2].

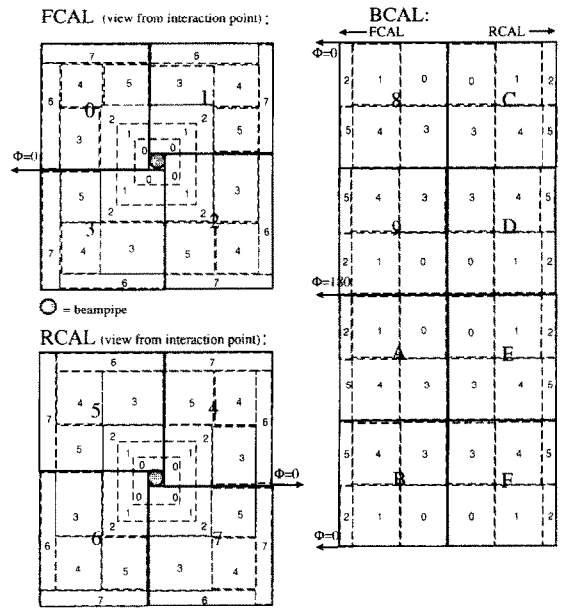

Fig. 14. Subregions of the calorimeter trigger regions (0–7 in F/RCAL, 8–F in BCAL).

5.1. Adder card adder tree

The adder tree is continued from the TECs onto the Adder Cards. The 9 bit results from each of the Trigger encoder cards is received on a set of lines on the J3 backplane. Each Adder Card handles the data from the seven Trigger Encoder cards plugged into its half backplane. Four adders combine the data in groups of two and produce 4 sums each with 8 bits of dynamic range. The summation continues down the adder tree and the dynamic range stays at 8 bits, with subsequent carry's being ORed into a single overflow bit.

Up to this point both Adder Cards have been performing the same operations in parallel. The adder cards are identical in that each have the circuitry just described as well as one more stage of addition. Each card feeds its results to this final stage. It also feeds the same result to the front panel printed circuit board. The front panel printed circuit board connecting the two adder cards is bidirectional. One of the Adder Cards is designated as the "Master" and the other as the "Slave". This nomencla-

ture is in no way related to Master and Slave as applied to the VME bus. The data from the "Slave" adder tree is sent to the input of the final addition stage on the "Master". Thus the last Adder on the "Master" combines the data of the two Adder Cards and stores the sum and its carry ORed with the overflow bit. This crate level total is fed out of the front of the Adder Card on a cable to the Trigger Processor crate.

5.2. Adder card subregion sums

The purpose of the Adder Card subregion sum logic is to compute the energy in subregions of the region of the calorimeter covered by one Trigger Crate. Subregions are defined because the region of trigger towers covered by one Trigger Crate may not correspond to a region of interest for examination of a specific piece of physics. Such regions of interest include the RCAL trigger towers immediately around the beampipe. The assignment of trigger towers to crates described below covers the RCAL with 4 crates, one per quadrant. The subregion sums are used by the CFLTP to calculate the energy in rings of RCAL trigger towers around the beampipe by summing the appropriate subregion energies from each of the 4 RCAL Trigger Crates.

The Adder Card calculates the energy in 8 subregions of the 56-trigger tower region by computing the energy from the threshold test information. These subregions are programmable and may be completely remapped under software control. One set of subregions is shown in Fig. 14.

The two Adder Cards together are able to sum the energy in up to 8 different subregions of the 56 trigger towers. These sums are performed on the data coming into each Adder Card independent of the data being received by its partner. The two Adder Cards send partial subregion sums to each other, with only one performing the final summation to complete the subregion sum. They also compute a total energy from the individual subregion sums. This mode of operation is the result of the need for parallel computation, to handle the high data rates, on cards inserted on either side of the split backplane. The only difference between the two cards is the designation of one of them as the Master and the other as the Slave. The principal distinction between the two is which data each sends to the other.

5.3. Adder card threshold histogramming

The Adder Card sums up the number of trigger towers in the 56-trigger tower region exceeding each threshold and not the one above it. It also sums up trigger towers passing no threshold and those that overflow. One purpose of the Threshold Sums is to search for jet candidates. If a region has a uniform deposition of energy then no trigger towers will pass the higher thresholds; this indicates a lack of jets. If the energy deposition is peaked around a few trigger towers, then it is likely that there is a jet and there will be trigger towers passing the higher thresholds. Another purpose of the Threshold Sums is to set the thresholds based on electromagnetic energy deposits alone and to use this as an unisolated electron trigger in the RCAL. A third purpose is to search for regions in the calorimeter with no towers over a low threshold so these can be declared "quiet".

5.4. Adder card pattern logic

The purpose of the Adder Card pattern logic is to identify isolated muons and electrons. The task is complicated by the edges of regions covered by different Trigger Crates, where isolation requires information from 2 or more crates. This difficulty is surmounted by counting the number of isolated electrons and muons separately for those in the contained part of the region and those on each of the four edges. The corner trigger towers are assigned, under program control, to one of the two adjoining edges.

The identification of isolated electrons is important because it permits triggering without a Q^2 cut. The isolation requirement is necessary to prevent a high background rate from hadrons faking electrons by passing at an angle from the EMC section of one tower through the HAC section of an adjacent tower. This is happens because of the nonprojective calorimeter tower geometry. The isolation requirement does not veto many legitimate neutral current events. The pattern logic first tries to establish an electromagnetic signal in a central region of either 1, 2, 3, or 4 towers, and then checks that the surrounding (up to 12) trigger towers are quiet.

The logic to identify the isolated muons is the same as that used for the isolated electrons except, where one uses the E bits, the other uses the M bits. The identification of muons has always been important to triggering, because it is a signal of heavy quark, neutral heavy lepton, or gauge boson production. While the ZEUS detector has a first level muon trigger, its rate tends to be quite high and combination with the CFLT is used to reduce this rate. In addition, the muon systems are not always able to exactly identify the crossing that triggered the event, whereas all calorimeter triggers are tied to a single crossing. The existence of a good calorimeter muon trigger also is useful for calibration purposes, since it indicates a minimum ionizing particle with a trajectory traversing a single trigger tower.

The pattern logic of the Adder Card pair uses the upper 3 bits (Q, E, and M) of the data coming from each of the 14 Trigger Encoder Cards in the trigger crate. The Isolated Minimum Ionization test is performed on the Master Adder Card and the Isolated Electromagnetic test is performed on the Slave. The front panel printed circuit connector, bridging the two cards, carries the appropriate information between the left and right halves of the crate. The pattern

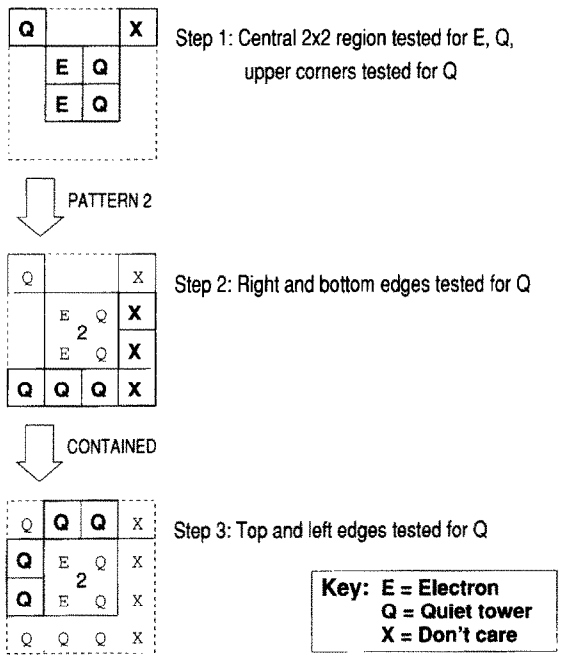

Fig. 15. Three-step algorithm used to identify isolated electrons by the Trigger Adder Card pattern logic.

logic on each Adder Card searches for a single or group of up to 4 trigger towers with electromagnetic or minimum ionizing test bits set that are completely surrounded by "quiet" trigger towers. These are counted as contained isolated electrons or contained isolated muons. The identification of isolated electrons is performed by a three-step algorithm that is illustrated in Fig. 15.

The pattern logic also searches for groups of trigger towers that satisfy these conditions, but have one or more electromagnetic or minimum ionizing trigger towers next to the 56-trigger tower region boundary. In these cases, isolation on one of the sides cannot be proved without checking the adjacent 56-trigger tower region. These are counted as edge isolated electrons or edge isolated muons. The total number of edge isolated muons and electrons are counted for each of the four edges. Examples of edge and contained isolated muon patterns are shown in Fig. 16. The pattern logic also flags which of the four individual edges are "quiet", i.e. have Q, M, or E bits on in every trigger tower. This information is used by the Trigger Processor in verification of edge isolated electrons and muons.

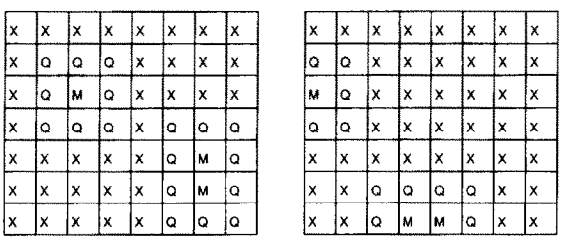

Fig. 16. Examples of two patterns accepted as contained isolated muons (left figure) and two patterns accepted as edge isolated muons (right figure). trigger towers are labelled as quiet (Q), minimum ionizing (M), or do not care (X). The same patterns satisfy the isolated electron test if the same trigger towers passing the minimum ionizing test, would pass the electromagnetic test instead.

The conditions defining an isolated muon or electron trigger tower are slightly different depending on whether the candidate electron or muon trigger tower occurs in the edge or the contained subregion of the 56-trigger tower region. In order to check for an isolated trigger tower it is necessary to perform a 16-trigger tower search in the neighborhood containing the trigger tower of interest. 7 overlapping 16-trigger tower neighborhoods, across the top of the 56-trigger tower region, are tested and then moved down by 1 trigger tower row and tested again every 12 ns. The testing of an isolated muon or electron in a region is completed in 2 pipelined steps. While the first step is being performed on a particular 16-trigger tower neighborhood,

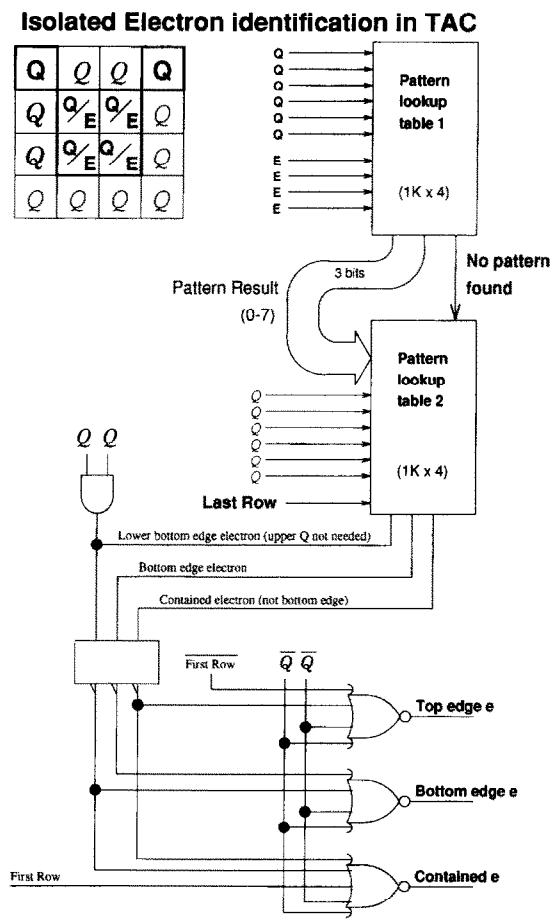

Fig. 17. Trigger Adder Card hardware used in the pattern logic to identify isolated electrons.

the second step is being performed on the 16-tower neighborhood centered one row above in the 56 tower area. The logic used to identify isolated electrons is shown in Fig. 17. A total of eight 12 ns steps is required to fully analyze a 56 trigger tower region for edge and contained isolated events.

6. Calorimeter first level trigger processor

The Calorimeter First Level Trigger Processor (CFLTP) does the final trigger calculations with data from the Adder Cards and ships these results to the Global First Level Trigger (GFLT) for the final trigger decision. The Adder Cards send the number of contained isolated electrons, edge isolated electrons, contained isolated muons and edge isolated muons. The edge counts are also broken down into totals for each of the 4 edges of the 56-trigger tower region. The Adder Cards also send the number of trigger towers that exceeded each (or no) threshold, but not the next higher threshold, number that overflowed their low gain channel, and whether these overflows are corrected for by setting the energy of their tower to zero for the energy sums. The Adder Cards send the energy in 8 specific subregions of the 56-trigger tower region as calculated from the trigger towers passing the thresholds. The total energy in the 56-trigger tower region calculated from these thresholds is also sent. The Adder Cards also send the EMC and HAC 56-trigger tower sums of total energy and transverse energy, E_x and E_y.

The CFLTP produces information on the global and regional status of the calorimeter trigger. It indicates for each of the 16 regions whether there was an electronic overflow and whether this overflow was corrected for by adding in zero energy. The CFLTP counts the total number of isolated muons and isolated electrons. These sums are made by first adding all of the contained isolated muons and electrons. The edge muons and electrons are matched up with the appropriate edge of the neighboring 56-trigger tower region. If the adjoining edge is quiet or has an isolated edge electron or muon in it, a single isolated electron or muon is included in the sum. If the adjoining edge is neither quiet nor contains an isolated muon or electron, the isolated muon or electron is not counted.

6.1. Trigger processor algorithms

The Trigger Processor completes the summation of total, HAC, and EMC energy and transverse energy, E_x and E_y. These sums are made with 8-bit accuracy. The total missing energy $(E_x^2 + E_y^2)$ and the total missing electromagnetic energy are also directly calculated. The total, transverse and x and y components of total, EMC and HAC energy are compared against settable thresholds and the results are forwarded to the GFLT. The same is done for the total and EMC missing energy. These thresholds are scattered through the dynamic range to correspond to the amounts of energy required for triggering when correlated with and without other components. The Trigger Processor also calculates the sum of the energy contained in the beam-pipe region of the FCAL and the RCAL.

The number of isolated electrons and muons found in the detector is the sum of the contained isolated electrons and muons and the verified edge isolated electrons and muons. The totals of contained isolated muons and electrons within 56-trigger tower regions are reported by the Adder Cards. Edge isolated electrons and muons in a specific 56-trigger tower region are verified by checking the edge region of the adjacent 56-trigger tower region for another edge isolated electron or muon, or all "quiet". In the case where another isolated electron or muon is found, the two neighboring edge isolated electrons or muons are combined and counted as a single contained isolated electron or muon. In the case where the edge region adjoining an edge isolated electron or muon is "quiet", the edge isolated electron or muon is counted as a single contained isolated muon or electron. In the case where the adjacent edge region is neither "quiet" nor contains an isolated electron or muon, the edge isolated electron or muon is rejected.

6.2. Trigger processor input card

Each Input Card receives data from the Adder Cards in two crates, 128 bits every 24 ns. It buffers the data down to a 48 ns rate and passes it through to the backplane drivers which send it to the algorithm cards. It also allows data to be written into FIFOs and a Main Memory which can hold up to 4096 crossings. Data can be written to the Main Memory either for every crossing or only for crossings which generate triggers. This data is used for monitoring trigger performance. These memories can be read out by VME without interrupting the dataflow from the input to the backplane. The VME accessible memories also allow testing of dataflow; data can be written to the memory and then driven to the backplane to test the algorithm cards.

There are 8 input cards in the trigger processor crate to handle data from all 16 regional crates. These drive a 20 layer backplane at 48 ns, which provides a 2048 bit wide bus to the algorithm cards [5].

6.3 Trigger processor algorithm cards

Each of the algorithm cards is different, receiving a different subset of data off the backplane and performing appropriate calculations. They make extensive use of programmable lookup tables to perform global calculations from the data from the 16 regional crates. For example, they calculate total energy, total transverse energy, and missing energy. One card uses the subregional energy information for the subregions around the beampipe to

calculate beam–gas event likelihood. Edge isolated electrons and muons are compared with the corresponding edge in the neighboring region to see if they truly are isolated, and the total number of isolated electrons and muons is calculated. Other calculations are also performed, and due to the use of programmable lookup tables the possibilities are somewhat flexible. The algorithm cards drive these results up the backplane to the output cards, which pass 32 words of summary information to the GFLT every 96 ns.

6.4 Trigger processor control

The nucleus of runtime control for the CFLT system is the Communications Card, which receives and distributes clock and control signals from the GFLT. From the GFLT 96 ns clock it creates a 12 ns clock for use by the Adder Card system and a 48 ns clock for use by the input card/algorithm card system. The control signals, the 96 ns clock, and the 12 ns clock for the Adder Card are sent to the Adder Support Module (ASM) for fanning out to the 16 regional crates. The ASM also allows, under control signals from the Communications card, single stepping of the 12 ns and 96 ns clocks used for data processing in the regional crates; it also sends an ungated 96 ns clock which is used for VME transfers in the regional crates.

The Communications Card distributes the control signals from the GFLT to the calorimeter DAQ system and receives back busy and error messages which it passes to the GFLT. It also checks for errors in synchronization with the Adder Cards and sends these to the GFLT. For standalone testing, it can generate the GFLT clock and control signals. Lastly, it allows for adjustment of delay on the various clocks it sends out: on the Adder 96 ns clock so that the flash digitizers hit the correct window on the data, on the Input card 48 ns clock so that the Input Card latches the Adder Data correctly, and on the backplane clock so that the algorithm cards receive the data correctly from the input card.

7. Global first level trigger

The calculations of the CFLTP take 2 μs to complete. The results from the Trigger Processor are shipped to the Global First Level Trigger (GFLT) that combines different detector elements for a final trigger decision in 5 μs. A typical example is to require an $E_T > 12$ GeV in the calorimeter accompanied by a Central Tracking Detector multiplicity of tracks pointing at the interaction point. The GFLT is also pipelined, accepting data and sending a decision every 96 ns. Due to propagation delays in receiving the data and sending the trigger, the GFLT calculation time is also about 2 μs. After the issuing of the GFLT, the event is analyzed by the Second Level Trigger. This system can handle a rate of up to 1 kHz.

8. CFLT performance

Over 550 nb^{-1} of data have been collected with the CFLT in the 1993 run. The total CFLT trigger rate has been about 100 Hz with thresholds as low as 500 MeV. The CFLT was used for every ZEUS first level trigger employed in physics analysis and was responsible for the majority of the reduction of rate written to tape (a few Hz). There was zero trigger rate from noise for trigger tower energy above 500 MeV.

8.1. Calibration

The calibration of the CFLT is accomplished with the charge injection system. This system is used for calibration of the calorimeter. The charge injector is fed into the signal path on the Calorimeter FECs before the trigger sums are split off. Each CFLT tower is the sum of different numbers of calorimeter cells. Therefore, when the charge injectors are fired, the CFLT towers have different expected pulseheights. These pulseheights are individually compared against their expected values. Towers that disagree with their expected values by more than 10% are flagged as defective and are repaired. The returned values are also stored in files. The calibration is known to the precision of the charge injectors (better than 1%).

8.2. CFLT trigger quantities

An important group of triggers have been high resolution (200 MeV) energy sums of towers above a 500 MeV threshold, excluding towers adjacent to the beampipe. The sums of total energy, total electromagnetic energy, total E_T, missing E_T, RCAL electromagnetic energy and BCAL electromagnetic energy were used as principal triggers by themselves and in coincidence with other component triggers. The total FCAL energy, and the electromagnetic energy and E_T in each of the 16 calorimeter regions have been used in coincidence with other component triggers or in calibration triggers. In addition, the RCAL hadronic energy, total electromagnetic E_T, total E_x, total E_y and missing electromagnetic E_T have been operating for diagnostic purposes.

The second group of triggers are composed of low resolution energy sums of all towers (including those adjacent to the beampipe) above 625 MeV (1250 MeV in the FCAL) in specific subregions of the calorimeter. The sum of EMC trigger towers in the RCAL beampipe is used as the primary trigger for Deep Inelastic Scattering physics, with a threshold as low as 3.8 GeV and an output rate of a few tens of Hz. The sum of RCAL EMC towers away from the beampipe is also used. The FCAL sums of towers near and away from the beampipe have been used in muon-coincidence triggers and for rejection of inelastic events in various low-Q^2 event triggers. The energy deposited near the beampipe is separately monitored for each

of the 8 calorimeter regions that surround it. In addition, the BCAL total energy, RCAL tower energy over the kinematic limit, and whether each of the 16 calorimeter regions were "quiet" (i.e. containing no tower with more than 500 MeV) were also operating for diagnostic purposes.

The isolated lepton logic has run in parallel with the energy sum trigger logic for monitoring purposes. Since the HERA luminosity was less than 10% of the design value during the 1993 run, it was not needed in the main trigger. The isolated lepton trigger was then studied with real event data taken in the 1993 run to optimize thresholds in the pattern logic and produce the results below so that it could be activated for the 1994 HERA run period.

8.3. CFLT rates and efficiency

The total 1993 FLT rate was 75 Hz for a HERA luminosity of 0.7×10^{30}, which corresponds approximately to 1/20 of the design luminosity. The efficiency of each subtrigger relative to the rest was studied using CFLT data. The overall efficiency of the CFLT for neutral current events was 98% and for charged current events 85%. The rear calorimeter EMC (REMC) subtrigger was the most efficient trigger for collecting neutral current events.

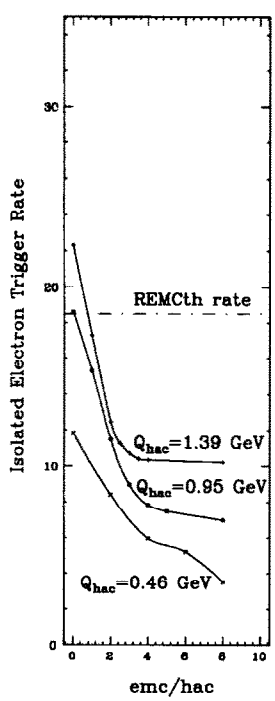

Fig. 18. The isolated electron trigger beam gas background in arbitrary units as a function Q_{hac} and EMC/HAC parameters. The dot-dashed line indicates the rate of the REMC threshold subtrigger at 3.75 GeV.

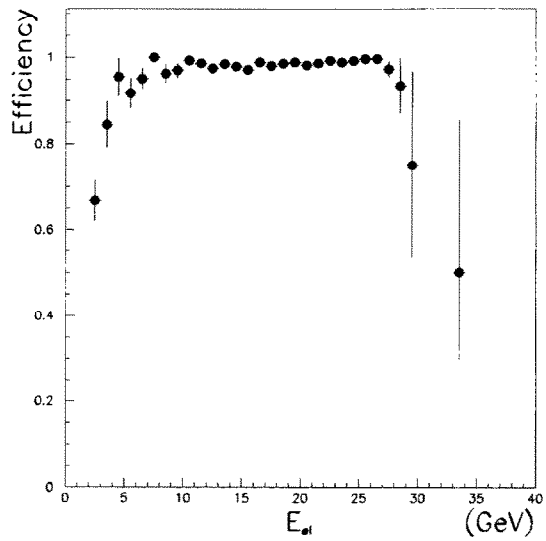

Fig. 19. Efficiency versus electron energy. The efficiency rises between E_{el} 2.5 and 5 GeV due to events where the electron energy is shared between trigger towers ($Q_{emc} = 2.52$ GeV). Events with $E_{el} \geq 30$ GeV are not electrons since they are outside the kinematic limit.

More than 92% of the ZEUS neutral current sample were tagged by this subtrigger and about 49% of it was collected exclusively by the REMC subtrigger. The purity of the REMC subtrigger was low and about 95% of the events from this trigger were rejected by the second level trigger [1] as originating from beam gas interactions. In 1994 the HERA luminosity is expected to increase by a factor of 5 and the REMC subtrigger rate has been estimated to be prohibitively high at the FLT level. Therefore this trigger will be replaced by an isolated electron trigger which has the same efficiency and a factor of at least 2 higher purity.

As discussed above, the CFLT executes the isolated electron algorithm by searching in the calorimeter for patterns of 1–4 towers with the E bits set surrounded by towers with the Q bits set. When such a pattern is found it results in a positive CFLT decision. A tower is defined as quiet if the EMC and the HAC energies deposited in that tower are smaller than the two programmable thresholds Q_{emc} and Q_{hac} respectively. Electron bits (E) are set based on a user programmable function $E = F(EMC, HAC)$. In order to study and optimize this algorithm we collected data from several ep data runs with the isolated electron trigger active. The optimum values for Q_{emc}, Q_{hac}, and F(EMC, HAC) were selected in order to obtain maximum beam gas rejection and high physics acceptance. We have chosen $Q_{emc} = 2.52$ GeV so that the trigger has 100% efficiency (including energy sharing between towers) at electron energy of 5 GeV, and $Q_{hac} = 0.95$ GeV. The electron bits were set if any of the following conditions

were satisfied: $E = \{(\mathrm{EMC} \geq Q_{\mathrm{emc}})$ AND $(\mathrm{HAC} \leq Q_{\mathrm{hac}})\}$ OR $\{(\mathrm{EMC} \geq Q_{\mathrm{emc}})$ AND $(\mathrm{EMC/HAC} \geq 3)\}$.

This isolated electron configuration results to a factor of 2 reduction in Beam Gas background relative to the REMC subtrigger and has the same efficiency as the REMC subtrigger for neutral current events. In Fig. 18 we present the beam gas reduction achieved using the isolated electron relative to the simple REMC subtrigger trigger at 3.75 GeV as a function of the Q_{hac}, EMC/HAC cuts. The overall efficiency of the isolated electron relative to the standard ZEUS electron finder was 98%. In Fig. 19 we present this efficiency as a function of the electron energy E_{el}.

9. Conclusions

The ZEUS Calorimeter First Level Trigger system calculates global and regional energy sums and searches for isolated muons and electrons. It completes these tasks in a pipelined fashion in 2 μs, accepting new data and shipping out results once every 96 ns. It uses digital logic with memory lookup tables to provide programmable flexibility for changing calibration, thresholds and even the types of tests made. The results of its calculations are shipped to the Global First Level Trigger (GFLT). The CFLT reduces the present background rate of 10 kHz of tower energy > 500 MeV to about 100 Hz. At full HERA luminosity, the GFLT must reduce the initial beam–gas rate from about 100 kHz to 1 kHz. The GFLT is also pipelined, reaching a decision in 2 μs after receipt of the component data. The First Level Trigger system reads in a new event every 96 ns and returns a trigger to the detector components for that event 5 μs after it occurred.

The ZEUS Calorimeter First Level Trigger system has operated reliably and according to design in 3 data-taking runs at HERA, and has accumulated 600 nb^{-1} integrated luminosity of physics data, at a 100 Hz output rate. It analyzes the data from 13K PMTs, collecting signals from a mostly nonprojective calorimeter at a 10 MHz input rate. It consists of a 1792 channel system contained in 16 9U modified VME crates with 14 TECs and 2 double-width Adder Cards, followed by a Trigger Processor in a custom-backplane crate that analyzes 5 GBytes/s. The modified VME crate cards and backplanes run at 83 MHz with 14 Gbits/sec of data transfer. The system makes extensive use of memory lookup tables so that thresholds, EM/HAC ratios, geometric factors, dead/noisy channel switchoff, calibration and subregion definitions are programmable. This flexibility has proven very useful and has enabled frequent changes in configurations to accomodate changing physics requirements. The isolated electron pattern recognition trigger has proven to be a powerful tool for beam–gas rejection. The analysis of data taken so far indicates sufficient performance to handle luminosity up to the HERA design value.

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