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Development of the H1 backward silicon strip detector

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Abstract

The development and first results are described of a silicon strip detector telescope for the HERA experiment H1 designed to measure the polar angle of deep inelastic scattered electrons at small Bjorken x and low momentum transfers Q^2.

1. Introduction

The *Backward Silicon Tracker* (BST) of the H1 experiment is designed to reconstruct the tracks of electrons scattered backwards, i.e. along the electron beam direction close to the beam line in deep inelastic electron–proton interactions at HERA. The choice of silicon strip detection is governed by the occurrence of a fraction of deep inelastic events at low and large Bjorken x which leave only the electron for detection as the hadronic flow is occurring either extremely forward or backward, respectively. In these events, contrary to the usual situation, the electron track alone determines the vertex position. Moreover, at small momentum transfers Q^2 the contribution of the polar angle uncertainty to the cross section error becomes important.

The H1 backward silicon tracker [1] will consist of eight planes of silicon detector discs with 16 wedge shaped four inch wafers per disc. It has a polar angle acceptance of about 162° to 176° covering an approximate Q^2 range between 2 and 100 GeV^2 for nominal vertex position. The BST has a strip detector part with circular strips of 48 μm pitch and a pad detector part with pads of about 1 cm^2 size. The strip detector measures the polar angle of backward scattered particles. The pad detector triggers on the backward deep inelastic electrons down to 1 GeV electron energy. Presently four detector planes are equipped with silicon detectors and the BST is being run in. This paper describes the strip detector development and first results prior to the upgrade of the readout electronics in summer 1996. The development of the pad detector is described in a separate publication [2].

2. The backward silicon strip tracker

2.1. Components

The strip sensor has AC coupled, polysilicon biased strips with a second metalization layer to route the signals towards the outer edge of the wafer. The strips are at constant radius measured from the beam axis. The innermost of 1280 p^+ strips is at 59 mm radius, the outermost at 120 mm, every second being read out. On the outer edge a single layer, fine pitch printed circuit board is glued to the wafer backside. This *hybrid* board carries five readout chips. The analog signals are transmitted via a flexible, integrated strip line to the strip *repeater* boards which provide power and signal transmission for all 64 detectors. The repeater is connected to the electronic trailer by 30 m long cables. A sketch of the BST is given in Fig. 1 which illustrates the detector planes and the associated repeater electronics.

During pilot runs of the system in 1995 and early 1996 the signal digitizing, buffering and readout was done by the *Online Silicon Readout Controller* [3] (OnSiRoC) module.

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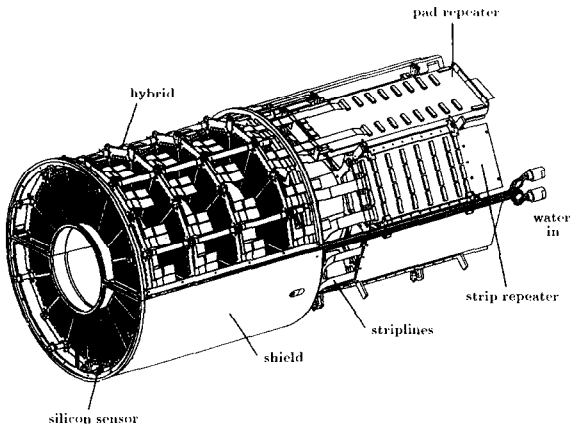

Fig. 1. Schematic view of the four-plane BST detector and associated repeater electronics.

2.2. Mechanics and cooling

The detector in its 1996 configuration has four planes positioned at z values of -725, -794, -868, -950 mm. The support structure is made of carbon fiber reinforced plastics (CFRP) to which the detector modules are fixed with their hybrid. The modules are staggered in beam direction and overlap in ϕ in order to avoid any gap of the acceptance due to the three millimeter guard ring of the wafers. This poses a severe constraint on the planarity of the hybrid and CFRP surfaces. The z positions are defined by precisely machined CFRP/aluminium rods between the detector discs. Final alignment will be done using ep-data. The detector is shielded with a G10 foil carrying a double-sided 35 μm Cu layer.

Position markers on the sensors as well as on the hybrids allow for aligning detector modules on the CFRP support frame such that the strips of the 16 modules of one disc form a circle with respect to the beam axis. This was done using a microscope and a turnable PC-steered x, y-table. The radial position of the modules is determined by position pins on the CFRP frame to a precision of 30 μm.

The BST is operated near the beam pipe at a surrounding temperature of about 40°C. A 1 : 1 model of the detector and heat production was built and the heat dissipation from the hybrids towards the inner end of the sensors was measured [4]. Due to a power dissipation of about 80 mW per readout chip the hybrid temperature exceeds the surrounding temperature by about 15 K. At the inner wafer radius the temperature increases by 5 K. In 1995 the BST was run with a water cooling pipe system which reduced the temperature at the sensors by about 7 K. In a test setup a decrease of the signal-to-noise ratio (S/N) of about 5% was measured for a temperature increase of 10 K. The system stayed operational up to 75°C.

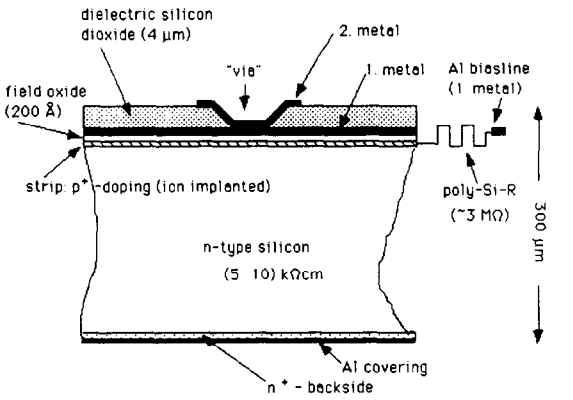

Fig. 2. Cross section of the 4″, double-metal, single-sided silicon strip detector for the H1 BST.

3. Wafers

3.1. Production

The radial microstrip detector for the BST is the first double-metal tracking design from Micron Semiconductor used in an experiment. A cross section of the wafer is drawn in Fig. 2. The wafer specification is given in Table 1.

Table 1
Specification of the AC coupled, double-metal, single-sided wafer for the Backward Silicon Strip Tracker of the HERA experiment H1.

Silicon	4 inch silicon, float zone, n type, 1-1-1 orientation resistivity between 5 kΩ·cm and 10 kΩ·cm
Supplier	Wacker Chemicals, Germany
Wafer	double-sided polished, thickness: 300 ± 15 μm ion implanted, junction: boron, ohmic: phosphorus
Oxides	silicon dioxide, dielectric: 4 μm field oxide: 1 μm capacitor oxide: 0.2 μm
Metallising	sputtered, 1st metal: aluminium 2nd metal: aluminium ohmic: aluminium sacrificial: titanium
Tests	automatic prober capacitor method from 2nd metal
Determination	open circuits / short circuits total leakage current full depletion (FD) total leakage current (FD + 35 V) AHS/ RHS (no shorts)
Limits	guard current at FD: 1 μA active area leakage current at FD: 2 μA
Stability	72 hours minimum

The inter metal dielectric is produced by a plasma enhanced silicon dioxide deposition system using a single deposit of 4 μm. Good uniformity is critical so that via hole etching it is controlled both in depth and laterally which if extended causes layer 1, the front aluminium metal deposition, to be etched away.

To identify the near termination point of the via hole etch, a sacrificial metallic layer which is colored and not too reflective has been introduced. This layer is then removed with selective etch prior to the second aluminium metal deposition which requires a minimal aluminium oxide interface for ohmic contact integrity of metal 1 to metal 2.

3.2. Tests prior to delivery

Low-defect double-metal technology requires extra care in achieving high uniformity of all processes, thereby keeping short circuit and open circuit faults to a minimum.

Initially, there was concern about the passivation ability of plasma enhanced silicon dioxide as performed by Micron Semiconductor and its effect on long term leakage current voltage characteristics of individual microstrip channels. The passivation and reliability results were however very satisfactory for long term biasing in air with a relative humidity less than 50%. All detectors were submitted to a minimum bias of full depletion plus 35 V for mostly 168 hours (72 hours minimum) prior to delivery.

3.3. Tests prior to acceptance

Upon arrival at the Zeuthen lab the detectors were biased for at least 72 hours and the guard and active area leakage currents were measured again for different bias voltages. With a few exceptions the currents were found to be well below the specified limits, see Table 1. More specifically 43 out of 64 detectors had a guard current of less than 100 nA and 49 detectors had an active area leakage current of less than 400 nA. The average depletion voltage of the detectors is 21 V, the maximum is 35 V. A few detectors were biased for more than one year showing a saturation of the leakage currents below the specified limits.

Eight detectors were installed in H1 during 1995 and got irradiated by the full dose of the 1995 run which was measured to be about 5 krad. The active area and guard leakage currents were measured before (prior to the hybrid assembly) and after the run (using the assembled module then). With the exception of one detector which ran to a leakage current of 8 μA all currents remained below the specified limits. On average the guard current of the eight detectors increased from about 10 to 50 nA while the active area leakage current increased from 200 to 600 nA. Due to the AC coupled readout this level of current changes does not affect the signal detection.

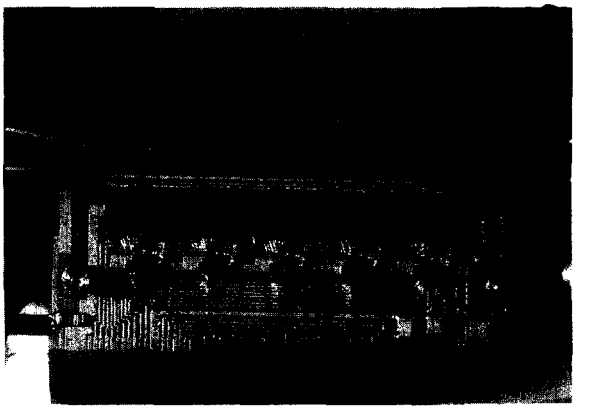

Fig. 3. Photograph of a hybrid (42×13 mm^2) glued on a strip sensor. The hybrid carries five APCs bonded to the silicon pads, five decoders and one line driver. The connection to the repeater electronics is done with a flexible strip line integrated into the hybrid pcb.

4. Modules

Fig. 3 shows the photograph of a module, i.e. of a hybrid with glued and bonded silicon strip sensor. The hybrid is a one-layer fine pitch printed circuit board with integrated flexible stripline of size 42×13 mm^2. It carries the front-end electronics and its main components: five amplifier analog pipeline chips [5] (APC) developed for H1, five decoder chips which generate the necessary 14 steering signals for the APC from only four control lines and an analog cable driver. The silicon sensor is glued to the hybrid on a small area of its backside with Araldite glue and three conducting EPOTEK dots for biasing. The readout lines of the sensor are bonded to the input pads of the APC. Each APC is connected to its own decoder chip by direct bonding. Furthermore, the hybrid carries some passive components to filter the supply voltages.

4.1. APC

The amplifier pipeline chip [5] (APC) is processed in 1 μm-*SACMOS* technique and occupies a die size of 6.3×3.5 mm^2. It supports parallel sampling of 128 channels. According to the HERA bunch crossing rate the sampling frequency is 10.4 MHz. Each channel consists of a low-power, low-noise charge sensitive preamplifier followed by a storage network with a buffer depth of 32 for data recording of 32 consecutive bunch crossings. A shift register controls consecutive switching of the storage capacitors. If sampling is stopped by an external trigger signal the pipeline can be re-read by the input preamplifier and charge will be stored on a latch capacitor of each channel. This re-read technique via the input preamplifier reduces the power consumption and allows online noise suppression by subtraction and addition of several pipeline buffers.

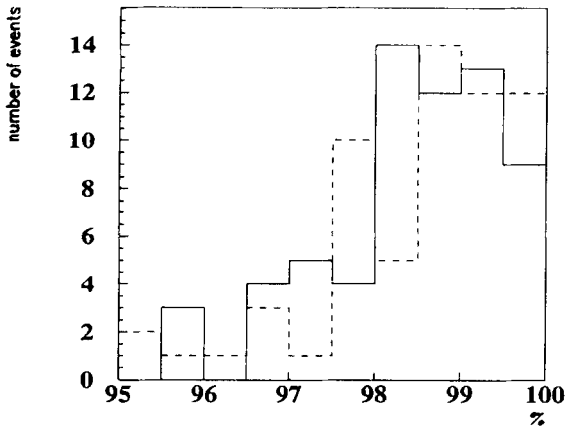

Fig. 4. Detector quality of 64 BST strip detectors prior to (solid line) and after assembly (dashed line). In both cases the mean is 98.5%, see text.

A readout shift register clocked with up to 2.5 MHz controls the sequential readout of the latch capacitors channel by channel through an output amplifier. Tests show a radiation hardness of about 100 krad of the powered chip.

The equivalent noise charge of the APC is 650 e^- + 55 e^-/pF. The total input capacitance is formed by the strip capacitance, the capacitance between the two metal layers and stray capacitances with a measured total value of about 18 pF. This corresponds to an optimum S/N for minimum ionizing particles of about 14.

The APC is steered by a 2.4 × 1.2 mm^2 decoder chip [6] fabricated in the same process as the APC on the same wafer. The decoder chip comprises a 64 bit serial-to-parallel decoder which is operated by the two interleaving sampling clocks and a data and select line only. It provides the APC controls and generates calibration pulses to the APC inputs.

4.2. *Module fabrication tests*

Hybrid pcb's were visually inspected and the flatness was measured. After bonding the APCs, calibration pulse data were taken and the hybrid functionality established.

The 640 bonds from the silicon sensors to the APCs were performed for each APC automatically. The bond machine was equipped to recognize broken coupling capacitors on the sensor. Those strips were not connected. Bonding of one module took less than 3 h including positioning. All assembled detector modules were checked by a pulsed laser diode system. On a computer controlled mover the response of each strip to the laser source was measured which lead to the dead channel map of the detector [7]. Fig. 4 shows the sensor quality as measured prior to delivery by MICRON Semiconductor (solid curve) compared with the result of the laser event analysis of the assembled module (dashed histogram). Some of the classified bad strips were found to deliver laser signals nevertheless while the readout of a few others suffered from the assembly or a malfunctioning APC channel. On average the quality of the installed detectors is 98.5% and did not change by the assembly procedure. During installation, however, two of the 64 modules had to be disconnected because of voltage instabilities. The laser event analysis [7] established a dependence of the pedestal level on the APC buffer position which can be compensated for with the modified readout electronics, see below.

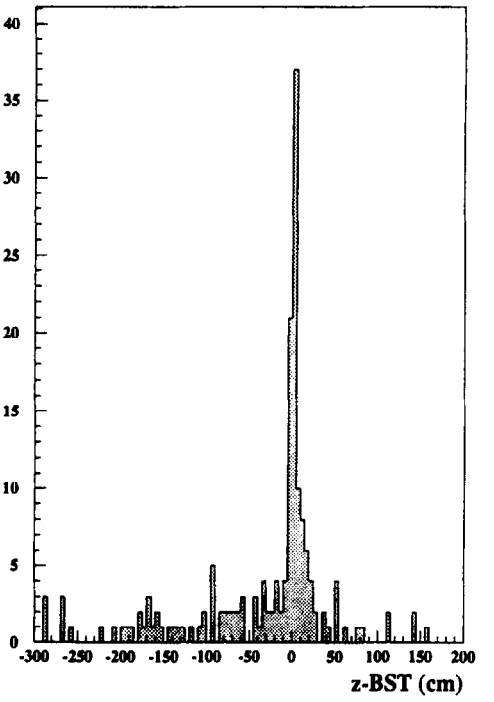

Fig. 5. Distribution of event vertex z positions reconstructed with the BST.

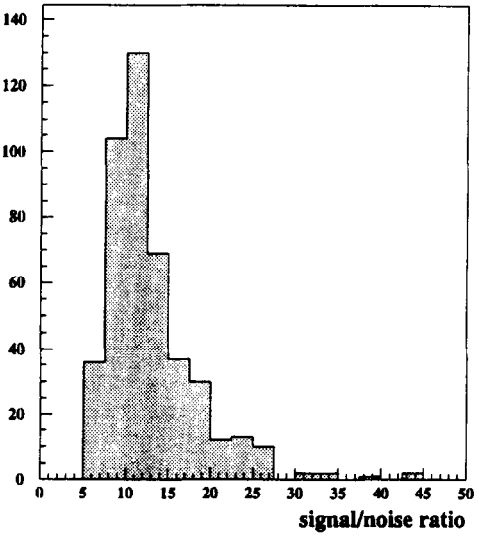

Fig. 6. Signal to noise ratio for all hits contributing to a track for an analysis of 1995 ep-data.

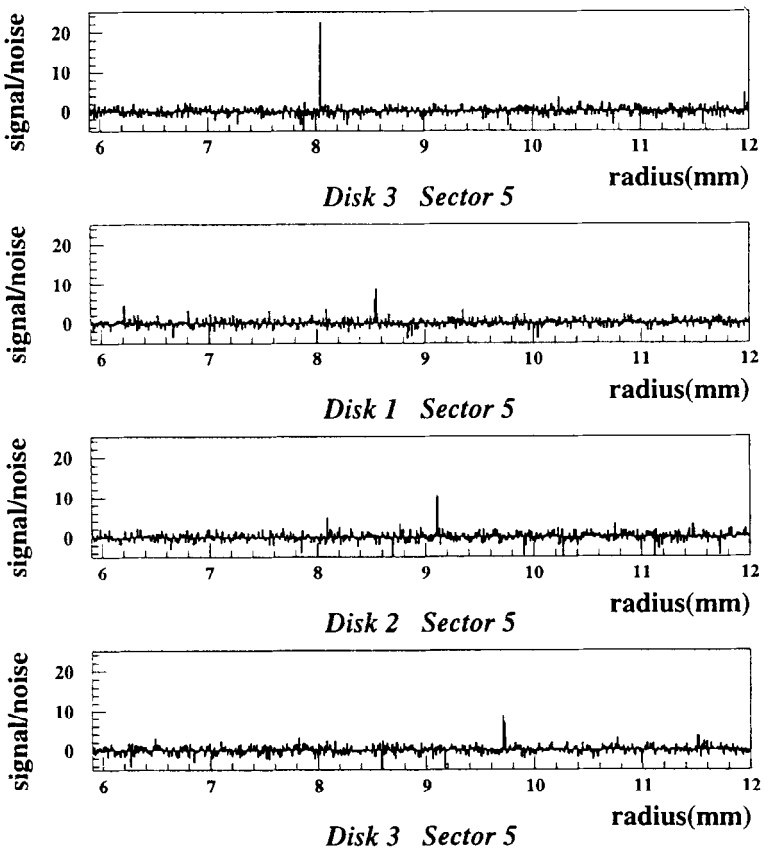

Fig. 7. An event recorded in spring 1996 during HERA machine studies. Plotted is the measured signal normalized to the mean noise level per channel versus radius for four subsequent discs of one ϕ-sector with a crossing track.

5. Readout electronics

5.1. Repeater boards

The strip repeater electronics consists of eight multilayer printed circuit boards placed close to the beam pipe behind the active BST area (see Fig. 1). Each board holds four plugged-in printed circuit subrepeater boards. These contain bias filtering, current sources and power converters for the hybrid supply and a video amplifier for long-line analog signal transmission. The digital control signals for the APC are fanned out in the repeater. Eight detectors of two ϕ-sectors are connected to one motherboard. Each motherboard is connected to the electronic trailer by a 50 and a 20 core cables.

5.2. OnSiRoC

The *Online Silicon Readout Controller* [3] (OnSiRoC) was developed for the H1 backward and central silicon strip detectors. This VME module contains a single-channel sequencer, pedestal memory, buffer and channel counters, a four-channel sampling ADC and raw data memory plus a complete hybrid powering system. APC digital control is generated by a 16 bit programmable, 10 MHz sequencer with loop and branch capabilities. The sequentially read out analog amplitudes are digitized by a 12-bit FADC. We chose an analog sample rate of 2.5 MHz. In one readout sequence amplitudes of 1280 channels of 10 APC's are sequentially digitized. Raw data are written to memory and can be online analyzed by a hit detector with programmable threshold and width. Prior to digitization analog pedestal values (8-bit DAC) can be subtracted.

For each of the four channels three voltages are supplied (analog voltage, digital voltage, bias voltage for the sensor). All voltages can be set separately. The depletion voltage is programmable. The voltage sources are floating and their control is opto-coupled.

In mid 1996 the OnSiRoC system has been complemented by a PowerPC-based system which allows programmable online data reduction, hit detection and multi-event buffering. Commercial PowerPC VMEbus cards have been interfaced to customized 8-channel, 20 MHz, 12-bit ADC mezzanines via the PCI bus standard. This permits up to a quarter of million silicon tracker channels to be read out and processed in a single double-Euro standard VMEbus crate.

6. First results

In 1995 a prototype detector of 8 sensors was run during ep interactions at HERA. Raw data were readout with an OnSiRoC module and analyzed offline. After pedestal and common mode subtraction, a hit was recognized with a minimum amplitude of 150 ADC units in one channel, or a minimum added amplitude of 150 ADC units in two adjacent channels. The average noise in 1995 was 30 ADC units. The average cluster width was 1.7 channels. Note that tracks traverse the BST at crossing angles near to 90°.

The two outer detectors were used to define a straight line and a triplet of hits was used to determine a track when a hit at the intermediate detector was within minimum distance from the expected position. This procedure removed efficiently spurious hits. Noisy strips were excluded from the analysis. Fig. 5 shows the z vertex distribution of the selected BST tracks for those events which had a vertex reconstructed by the central jet chamber. The distribution peaks at the expected position of $z = 5$ cm with a few remaining faked tracks. The tracks pointing to the vertex within ± 30 cm have a signal-to-noise distribution as shown in Fig. 6 with a peak S/N of 11 and a mean of 13.

The common mode in 1995 was up to two times as large as the noise level. This was seen to be connected with the power regulation for the analog voltages at the subrepeater board. For the installation of 1996 the subrepeater board was modified. The common mode observed in 1996 is only about 2/3 of the noise level. Fig. 7 shows an event with a crossing track taken in spring 1996.

7. Summary

The backward silicon strip tracker of the HERA experiment H1 is approaching completion of its first phase. The system of about 40 000 readout channels has been developed over about 3 years and been demonstrated to work under HERA conditions. A pilot run with the first version of the readout electronics allowed to reconstruct the vertex position of ep-interactions and a signal-to-noise ratio of about 11 was achieved. The system will be extended to eight detector planes in the coming year.

Acknowledgements

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