Upgrading the ATLAS Tile Calorimeter Electronics

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The Tile Calorimeter is the central hadronic calorimeter of the ATLAS experiment at LHC. Around 2024, after the upgrade of the LHC the peak luminosity will increase by a factor of 5 compared to the design value, thus requiring an upgrade of the Tile Calorimeter readout electronics. Except the photomultipliers tubes (PMTs), most of the on- and off-detector electronics will be replaced, with the aim of digitizing all PMT pulses at the front-end level and sending them with 10 Gb/s optical links to the back-end electronics. One demonstrator prototype module is planned to be inserted in Tile Calorimeter in 2015 or 2016 that will include hybrid electronic components able to probe the new design.

1 Introduction

The first running of the Large Hadron Collider (LHC) with proton-proton collisions at centre of mass energies up to 8 TeV produced some significant results with the discovery of Higgs Boson and measurements of Standard model processes. For future running the LHC energy and luminosity will be increased in stages, ultimately resulting in the high luminosity HL-LHC. This stage is scheduled around 2024 and plans to increase the peak luminosity to a value of 5-7x10^{34}cm^{-2}s^{-1} with a pileup close to 200 collisions per beam crossing.

The HL-LHC presents some difficult challenges for the detectors because the new operational conditions imply a higher radiation level that can lead to single point failures of electronics or the integrated radiation dose can lead to a permanent component failure. Another challenge is in dealing with the events high rates which requires more efficient trigger algorithms.

The ATLAS Tile Calorimeter [1] (TileCal) is a cylindrical hadronic sampling detector with steel absorbers and scintillating plastic tiles, located in the most central region of the ATLAS experiment [2] at CERN. It consists of a central barrel (divided in half barrels) and two extended barrels along the beam axis. Each barrel is segmented azimuthally into 64 modules reading out up to 48 photomultiplier channels. The Photomultiplier Tubes (PMTs) and the front-end electronics are situated in the outermost part of the modules, in extractable so called super-drawers. TileCal contains a total of 256 super-drawers comprising 9852 PMT readout channels.

The light generated by charged particles crossing scintillating tiles are collected by wavelength shifting fibers and sent to the PMTs. The analog signals produced by PMTs are conditioned and digitized by the

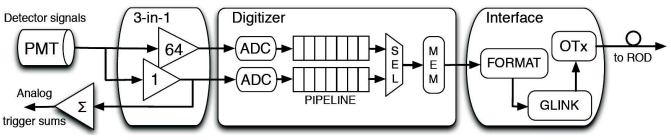

Figure 1: Current Tile Calorimeter readout architecture.

front-end electronics every 25 ns,
while analog tower sums are transmitted to the Level-1 trigger system. When an accept trigger signal is received, data for the selected events are sent to the back-end electronics in the ATLAS counting room where the Read Out Driver (ROD) receives the data at 100 kHz maximum rate. Figure 1 shows the dataflow of the current readout architecture.

To meet the challenges of HL-LHC, a multi-phase upgrade program of the ATLAS experiment has been developed: Phase-0, Phase-I and Phase-II [3]. While TileCal mechanics and optics will stay together with their PMTs, TileCal electronics will undergo major upgrades, because by the time of Phase-II, the current electronics will have reached their end of life and the maximum total integrated radiation dose.

2 Tile Calorimeter electronics for HL-LHC

A full redesign and replacement of the readout electronics of Tile Calorimeter is mandatory to implement redundancy in the signal processing and power distribution, use of radiation-tolerant components and using reliable protocols with error correction for data transmission.

The readout architecture for Phase-II points to a full digital readout where the front-end electronics will transmit digital data from all the channels to the back-end electronics in the counting room for every bunch crossing using high-speed fibre optic links. The data will be pre-processed and transmitted to the first level of trigger with improved precision and granularity. The signal chain for the new readout architecture is shown in Figure 2.

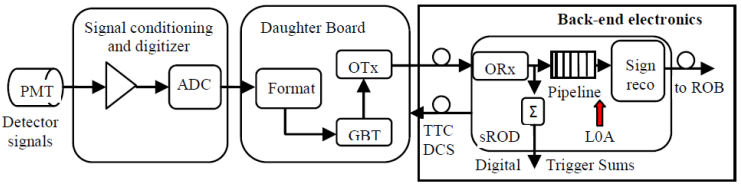

Figure 2: Tile Calorimeter readout architecture for the HL-LHC.

Since redundancy is of utmost importance to achieve maximum reliability, the new front-end electronics will be split into four independent units operating in parallel [4], as is shown in Figure 3. The new design, moving from dependent drawers to independent mini-drawers, reduces the complexity and internal connections, provides a complete redundant readout from cell to back-end electronics and a redundant power supply system.

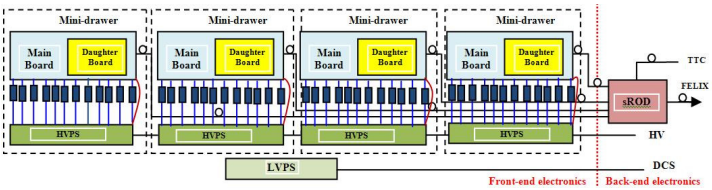

Figure 3: Block diagram of the upgraded super-drawer electronics.

3 Tile Calorimeter Demonstrator Project

To evaluate and qualify the new concept, a prototype called TileCal Demonstrator was developed. In order to gain field experience with the new design, the Demonstrator will replace one super-drawer of the current system for next LHC Run 2 and it must be compatible with present system insofar as it also provides analog trigger signals. Due to this functionality, the prototype is called hybrid Demonstrator. The existing system was redesigned with the respect

to mechanics, electronics, and power distribution.

Mechanics - The current front-end electronics are installed in super-drawers, each composed of two drawers. The modularity implemented by the new concept allows half size drawers called mini-drawers, so that one super-drawer is composed of four mini-drawers. Each mini-drawer is equipped with up to 12 PMTs with corresponding Front-end boards, one Main board, one Daughter board, one High Voltage regulation board and one Adder base board as is shown in Figure 4 (left). The mini-drawers offer a good alignment precision, required in insertion and extraction procedures, due to the improved mechanical links between mini-drawers and a more efficient internal water cooling system. Electrical services organized in two flexible carriers provide easy connection and disconnection of all electrical and optical cables.

The advantages of the Demonstrator super-drawer, shown in Figure 4 (right), consist in an easier access and reduced demand for wide detector opening for TileCal electronics servicing. Also, failing mini-drawers can be more easily replaced than in the present situation, with a minimal radiation exposure of the servicing personnel.

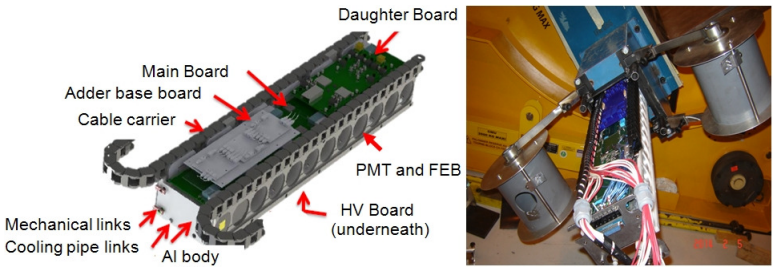

Figure 4: Mini-drawer design (left), Demonstrator and manipulation tooling (right).

Electronics - To improve the reliability and redundancy the new electronics are made as independent as possible and taking in consideration the predicted radiation levels, reliable radiation tolerant components are used.

Front-End Boards (FEB) - three different alternatives are being evaluated: modified 3-in-1 card (redesign of existing FEB), FE-ASIC alternative (including ADCs in an ASIC) and QIE alternative (a charge integrating ASIC). The Demonstrator prototype is equipped with the first version, still based on discrete components but with better linearity, lower noise than current version and acceptable radiation tolerance.

Main Board (MB) - provides the control, monitoring and readout of the FEBs and delivers digitized data to the Daughter Board [5]. MB prototype is divided into halves each hosting six FEBs. Each half has a separated low voltage power supply and is diode-ORed with the other half, ensuring the complete functionality if the power supply for one half stops working.

Daughter Board (DB) - provides high speed communication between the front-end and back-end electronics using redundant high speed links at data rates 10 Gb/s [6]. DB implements slow control functionalities as the distribution of Detector Control System (DCS) commands needed for the control and monitoring of the Main Board and the high voltage power supplies. DB prototype is divided into two separate halves, each equipped with one Kintex 7 field-programmable gate array (FPGA) and one Quad Small Form-factor Pluggable (QSFP) optical module and it can be remotely configured from back-end electronics via safe path using tolerant GBTx and will in turn be able to configure Main Board FPGAs.

Power - Instead of the current daisy-chain power distribution that has proved to be prone to voltage drops, each super-drawer will be outfitted with redundant power supplies.

Low Voltage power distribution - use a three stage power scheme with 200 V from the control room to local power supplies in the TileCal module. Boards receive down-regulated power at +10 V and Point Of Load (POL) regulators locally produce the required voltages. Diode coupling two independent 10 V supplies will provide increased redundancy.

High Voltage power distribution - two solutions are under evaluation to provide HV to the front-end electronics: voltage regulation in ATLAS counting room versus front-end (HV Opto board). For Demonstrator is implemented the second solution, introducing the possibility of switching on/off individual PMTs, based on the current design and for a better linearity the passive dividers have been replaced by active ones.

Back-End Electronics - The upgraded Read Out Driver (sROD) [7] performs the following functions: receiving and processing readout data, interfacing the DCS and the front-end electronics, as well as the reception and distribution of Timing Trigger and Control (TTC) information towards the detector. It was developed a prototype, able to readout a complete hybrid Demonstrator super-drawer. The connectivity between the two Xilinx FPGAs and the optical modules and peripherals is shown in Figure 5. The Virtex 7 FPGA is connected to 4 QSFP providing high speed communication with front-end electronics at a maximum data rate of 160 Gb/s. The Kintex 7 FPGA interfaces the hybrid Demonstrator with current system sending data to the present ROD and receiving TTC information and interfaces with trigger system.

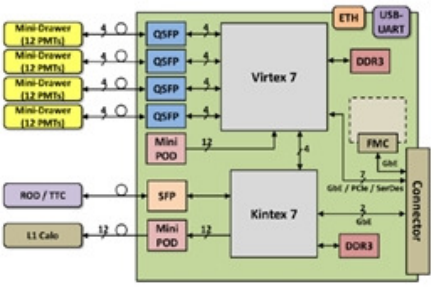

Figure 5: Block diagram of sROD Demonstrator.

4 Summary

The new operational conditions for HL-LHC, with higher radiation levels and data rates, require the implementation of a complete redesign of the Tile Calorimeter readout electronics.

The upgrade plan is to develop a system with full digitization of signals and data transmission at bunch-crossing rate, with a reduced number of possible single points of failure, higher radiation tolerance and higher redundancy on the readout and in power distribution.

To gain an experience and to evaluate the Tile Calorimeter new electronics before the full replacement around 2024, it was developed a hybrid Demonstrator which combines current features, like analog path with the requirements for Phase-II upgrade. It is planned to outfit one full Tile Calorimeter module with the hybrid Demonstrator electronics during first ATLAS opening in LHC Run 2.

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