DEUTSCHES ELEKTRONEN-SYNCHROTRON DESY

DESY 88-118
August 1988

A HIGH ACCURACY PIPELINE TDC

by

H. Klär, M. Schulz, P. Steffen

Deutsches Elektronen-Synchrotron DESY, Hamburg

D. Düllmann

II. Institut f. Experimentalphysik, Universität Hamburg

ISSN 0418-9833

NOTKESTRASSE 85 · 2 HAMBURG 52

DESY 88-118
August 1988

ISSN 0418-9833

A High Accuracy Pipeline TDC

H. Klär, M. Schulz, P. Steffen
DESY, Hamburg, Germany
D. Düllmann
Universität Hamburg, II. Institut für Experimentalphysik
Hamburg, Germany

Abstract

FADCs can be used to store digitized pulses in a memory. The timing of pulses with a risetime of a few units of the FADC-clock can be determined with a small fraction of the FADC-clock time. The memory serves as a pipeline. In case of a $100 MHz$ 8-bit FADC a resolution of $\approx 30 ps$ has been measured.

FADC systems [1] are used frequently for storage and readout of analog pulses of drift chambers. In the H1-experiment at the electron-proton storage ring HERA at DESY the drift chamber readout system [2] uses $100 MHz$ 8-bit FADCs to digitize continuously the input pulses and store the digitized signals in a memory, which is 256 words deep. An external trigger stops this process and starts the subsequent readout into a microprocessor. This allows the numerical analysis of the pulse digitizations stored in the recent 256 time bins. Thus the memory serves as a pipeline of a depth of 256 time bins.

This system can be used also for storage, analysis and monitoring of standard pulses. It is the aim of this note to point out, that the timing can be determined with a resolution much better than the clocktime of the FADC by using standard pulses with a well defined pulse shape.

In order to obtain the timing of a pulse from FADC digitizations to an accuracy better than the clock timing (Δt) it is necessary to use pulses with a rise time $t_{rise} \geq 2\Delta t$. The digitized amplitude measurements allow the reconstruction of the signal and the determination of the timing.

As an input signal one uses a normpulse with a fixed risetime of $N \cdot \Delta t$. The pulse amplitude A_{max} is matched to the range of the FADC. For the subsequent considerations it is assumed that the input pulse has no fluctuations of its shape. Fig. 1a shows as an example a pulse with a risetime of 5 clock bins ($N = 5$).The digitized values of the FADC are shown in fig.1b. From a fit of the digitized amplitudes on the leading edge to a straight line one determines the timing t_f at a given fraction f of the maximum amplitude (as indicated in fig.1b):

$$t_f \quad = \quad t_0 + f\frac{A_{max}}{S},$$

where t_0 and S are the start time and the slope of the fitted pulse, respectively. A constant digitization error σ_d results in a timing error of

$$\sigma(t_f) \quad = \quad \Delta t\frac{\sigma_d}{A_{max}}\sqrt{N}\sqrt{1+\delta}$$

$$\delta \quad = \quad \left(\frac{t_f - \langle t \rangle}{\Delta t}\right)^2 \frac{12}{N^2-1},$$

where $\langle t \rangle$ is the time averaged over the samplings on the leading edge. The term δ is due to the extrapolation of the fitted line. It is minimal if t_f is in the center of the digitizations on the leading edge ($t_f \sim \langle t \rangle$). In average this is the case for $f = 1/2$.

The optimum time resolution is obtained if the rise time of the pulse is two clock bins wide (N=2). In this case the line fit reduces to

$$t_{1/2} = t_1 + \frac{(A_{1/2} - A_1)}{(A_2 - A_1)}\Delta t,$$

where A_1 and A_2 are the two digitizations on the leading edge and t_1 is the time corresponding to A_1. The resulting time resolution is

$$\begin{aligned} \sigma(t_f) &= \Delta t \frac{\sigma_d}{A_{max}} \sqrt{2}\sqrt{1+\delta}, \\ \text{where} \quad \delta &= \left(\frac{t_{1/2} - \frac{t_1+t_2}{2}}{\Delta t}\right)^2 \cdot 4 \end{aligned}$$

varies between 0 and 1. For an 8-bit $100MHz$ FADC one expects a r.m.s. deviation of $\sigma_d = 1/\sqrt{12}$ digit due to the digitization. This results in a timing resolution ranging from $16ps$ to $22ps$ depending on the difference between $t_{1/2}$ and $\frac{t_1+t_2}{2}$. For evenly distributed input pulses one has an average resolution of $18ps$. The timejitter of the $100MHz$ FADCs of $\approx 15ps$ has not been taken into account in these estimates.

The resolution can further deteriorate if fluctuations of the input pulseshape occur, however, the digitized complete pulses allow an easy monitoring. It should be stressed that the only strong requirement for the input pulse is a constant linear rise.

An experimental test of these considerations has been done using the FADC channels of the F1000-System [2] (FADC = SONY CX20116,$100MHz$, 8-bit, maximum amplitude =2 V). The nonlinear response - which is used to increase the dynamic range for the analysis of drift chamber pulses - has been changed to a linear response.

The input pulses of two FADC-channels had a risetime of $\sim 20ns$ and an amplitude of $\sim 1.8V$ ($\sim$ 90% of the FADC range). One of the signals has been delayed by an adjustable delay.

The digitized amplitudes of the signals are stored in a memory at a frequency of $100MHz$. These data are read out by a microprocessor which detects the signals and calculates the time $t_{1/2}$. The time differences of the two signals are shown in fig.2 for two different delays of one of the signals.

The distributions have been evaluated to determine the time resolution of a single channel. As a result we obtained

$$\sigma_t = 28ps.$$

The difference to the theoretical resolution of $18ps$ is attributed to the imperfections of the test setup.

Summary

It has been shown that the described method allows the pipelining of pulses and the determination of the timing to an accuracy of $\approx 30ps$. This resolution is superior to pipelined time measurements which are limited to a resolution of about $2ns$ (e.g. LeCroy model 1879). In addition the repetition rate of $\sim 20MHz$($\sim$ 5 clock bins) is much higher than the one of commercially available high resolution TDC units.

Knowing this method one can simplify the electronics of an experiment by using only FADCs for pulseheight and timing measurements, e.g. for the determination of the phase of the trigger with respect to the FADC-clock when the FADC system is working in the common stop mode. Also the timing analysis of a system with a large number of different channels can be easily investigated with this method. Further application could arise when a sufficiently stable clock with an additional scaler is used. This would allow measurements of time differences even over hours with unchanged accuracy.

References

[1] P.von Walter et al. *IEEE Transactions on Nuclear Science NS-32,626 (85)*

[2] H1 Collaboration: The Central Tracking System of the H1 Experiment, contribution to the XXIV. International Conference on High Energy Physics,Munich 1988.

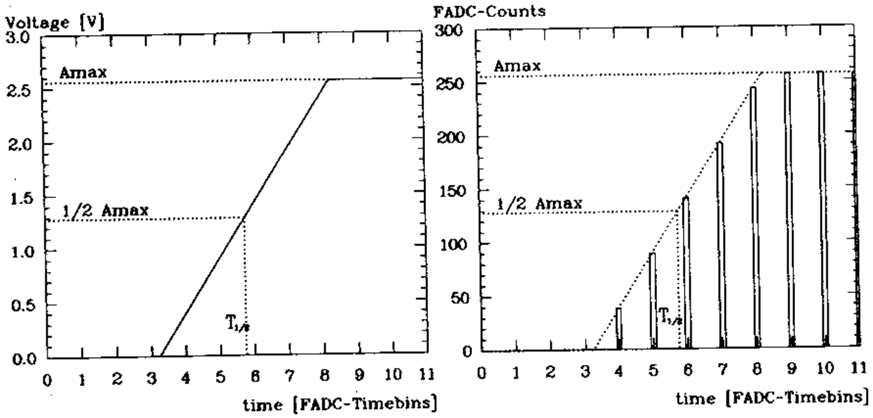

Figure 1: Example of an analog (a) and digitized (b) normpulse for timing analysis.

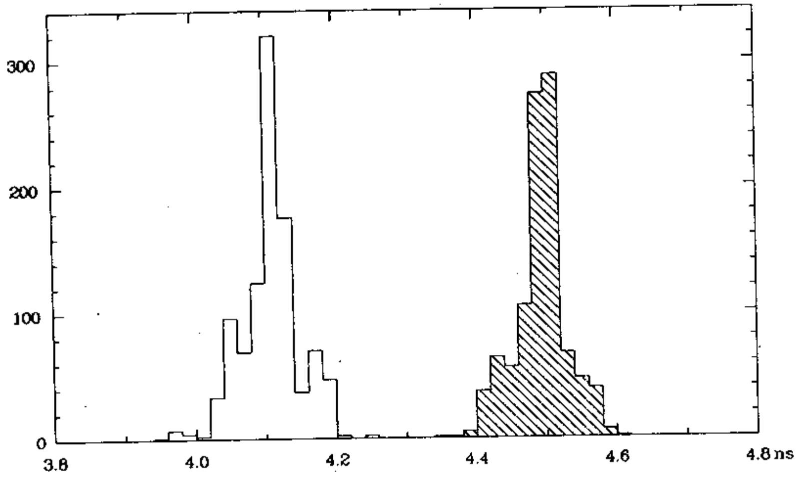

Figure 2: Time difference distributions of two FADC channels. The hatched distribution originates from a signal delayed by $\sim 400ps$.