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The ZEUS Vertex Detector Readout Electronics

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THE ZEUS VERTEX DETECTOR READOUT ELECTRONICS

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CONTENTS

1 - INTRODUCTION

The ZEUS vertex detector (hereafter called VXD) is a multi-wire time expansion chamber designed for the detection of short lived particles that decay in the neighborhood of the HERA beam. For this reason, both a high spatial resolution and a good two-track separation are of the utmost importance. This implies that the signals from the individual wires must be of relatively short duration, and must be timed with great accuracy with respect to the beam crossing time. Montecarlo calculations indicate that in order to obtain the spatial resolution of 35 μm required, a timing accuracy of 4 ns is needed.

The physical structure of the VXD was designed and is being constructed by the ZEUS group (INFN and University) in Bologna [1,2]. It consists of 120 radial cells with 12 sense wires each. In the present design of the VXD, the total drift time in a time expansion cell is of the order of 500 ns; this is equivalent to $\approx$ 5 HERA beam crossings. The delay between the occurrence of an interaction and the time when the Global First Level Trigger (GFLT) is issued is constant, the value of this delay is fixed to be 46 clock intervals, equal to 4.42 μs. The readout electronics must therefore be able to store the information corresponding to this time interval; to read, upon receipt of a GFLT, the data corresponding to the $\approx$ 800 ns of interest (500 ns of drift time plus 300 ns of security margin) and to transmit these data to a buffer within 7 μs. During this time the Pipelined Multi-Hit-TDC (PMHTDC) is in "Transfer Mode" and data acquisition is inhibited. After these operations, the front end of the readout electronics must be ready to start again data acquisition, waiting for a new GFLT.

A second requirement of the readout electronics is that it must be able to store up to 15 GFLT events and upon request of the Global Second Level Trigger (GSLT) yes to format and to transmit the event in question to the Dual Port Memory (DPM). The data is then transferred to the event builder via a 2-T board. The delay between the GFLT and the GSLT of an event is from 4 ms to 7 ms [3].

The time sequence of GFLT's and GSLT's is shown schematically in fig. 1.

Two solutions present themselves to fulfill the above requirements:

i) Flash ADC, that is the solution adopted by the Central Tracking Detector group at Rutherford Appleton Laboratories, and implemented by the electronics group at the University of Bristol;

ii) Multi-Hit TDC.

We have opted for the second choice, for reasons of simplicity and economy.

In what follows we describe the design of a prototype Multi-Hit TDC which is being tested in our laboratories.

It is to be noted that the PMHTDC we are designing is going to be used also in the data acquisition of the Forward Muon drift chambers of the ZEUS experiment. The design and characteristics of these chambers are described in the ZEUS technical proposal [1].

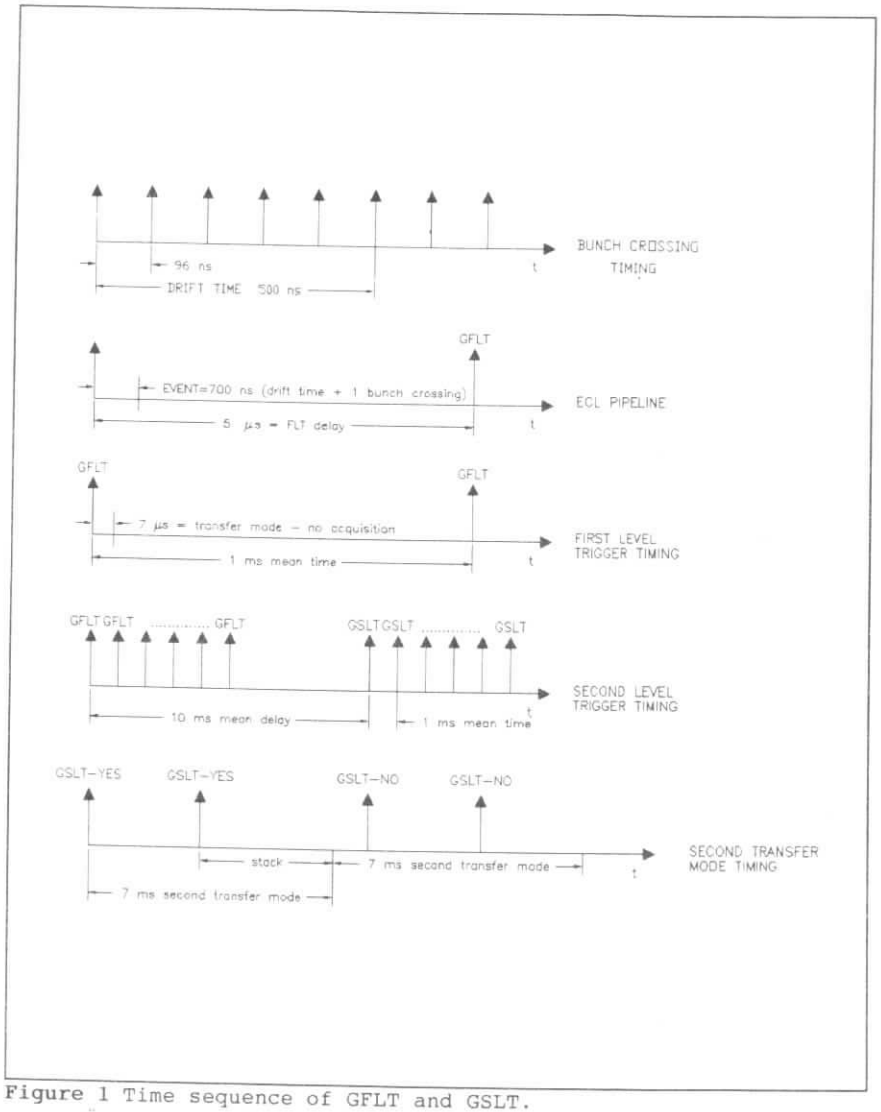

Figure 1 Time sequence of GFLT and GSLT.

2 - OVERVIEW OF THE SYSTEM

The design of PMHTDC that we have built is made possible by the availability of large capacity CMOS memories, Programmable Gate Arrays (PGA) and Digital Signal Processors (DSP) at reasonable prices.

The signals from each wire are amplified by a preamplifier-driver located in the immediate vicinity of the VXD and then transmitted by 40 m of twisted pair cables to low gain amplifier-shapers that eliminate common mode noise and are provided with a zero pole filter designed to decrease the fall time of the pulses. These amplifiers are located in the "Rucksack". Both these components are designed by H. Walenta and E. Badura of the University of Siegen. The signals then enter the PMHTDC system which is composed of three types of 9U cards that are interconnected by a standard VXI bus.

i) **Crate Interconnect cards (CIC).** These cards are located in slot 0 of each PMHTDC crate, they manage the GFLT, the GSLT data and the monitor and control signals. These cards contain a DSP, and drive the private bus that interconnects the PMHTDC cards.

ii) **Pipelined Multi Hit TDC cards (PMHTDC).** The cards receive the signals from 4 VXD cells each. These are constructed in modular sub-units; this structure permits the modification of the system minimizing hardware and software redesign. These changes may depend on the occupancy of the signals, or on the transformation of the PMHTDC into a fast flash ADC. The modules that constitute the PMHTDC are:

a) The Mother Board (MB). It contains a DSP to control the various functions of the PMHTDC. The DSP is also used to compress and format the data and transmit it to a DPM which is read via VME bus. This card provides the addresses for the writing and reading of the pipeline memories and contains a circuit that detects the interruption of the 250 MHz signal that signifies the receipt of a GFLT. On this board are located the interfaces between the private bus and the interrupted bus with the DSP. It also receives via private bus the values of the input discriminator thresholds.

b) The fast Front End card (FE). It acquires the signals from 8 amplifier-shapers through a differential line receiver/discriminator and clocks the digitized signal in two fast ECL pipelines at 125 MHz.

c) The Primary Buffer card (PB). Upon the arrival of a General First Level Trigger (GFLT) it receives the data corresponding to one event from three fast front end cards through an ECL to TTL translator and stores it into a buffer capable of storing 15 events. Upon receipt of a GSLT_yes two PGAs on board of this card elaborate and analyze the data, and send it to the DSP in the MB

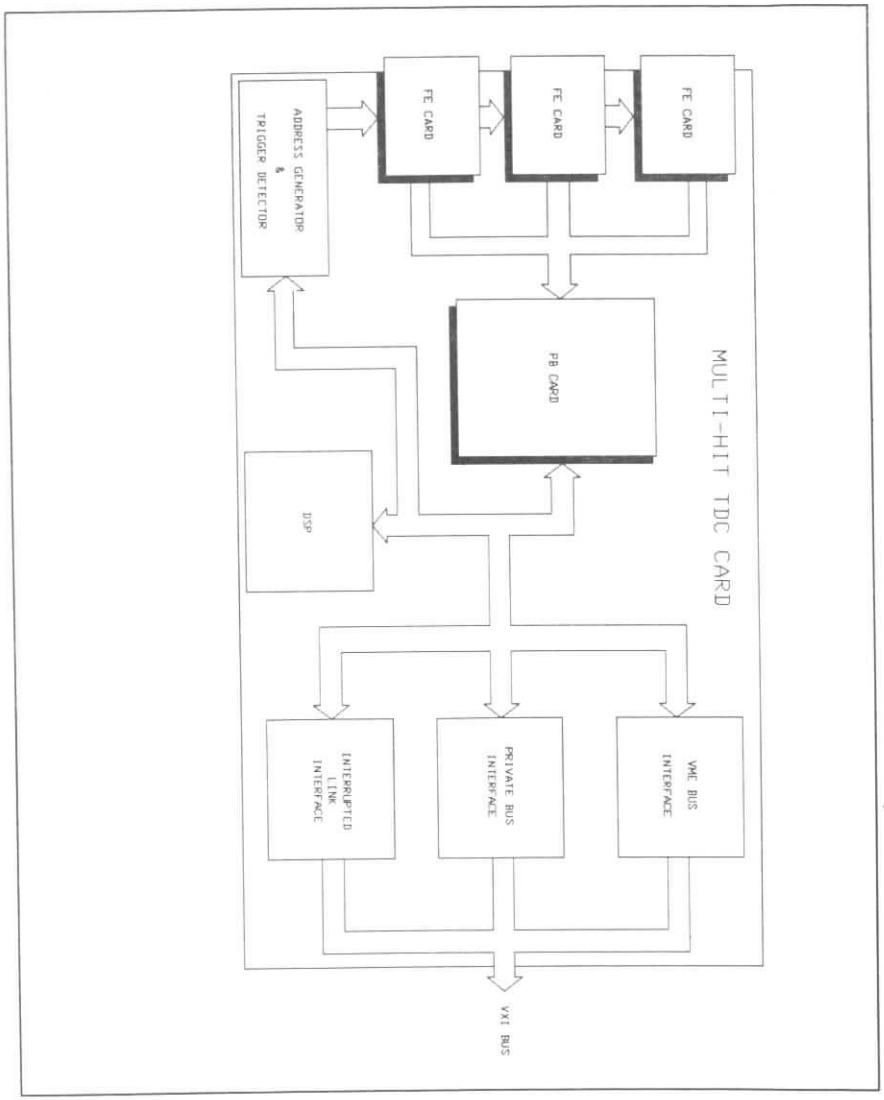

Figure 2 Block diagram of the MHTDC.

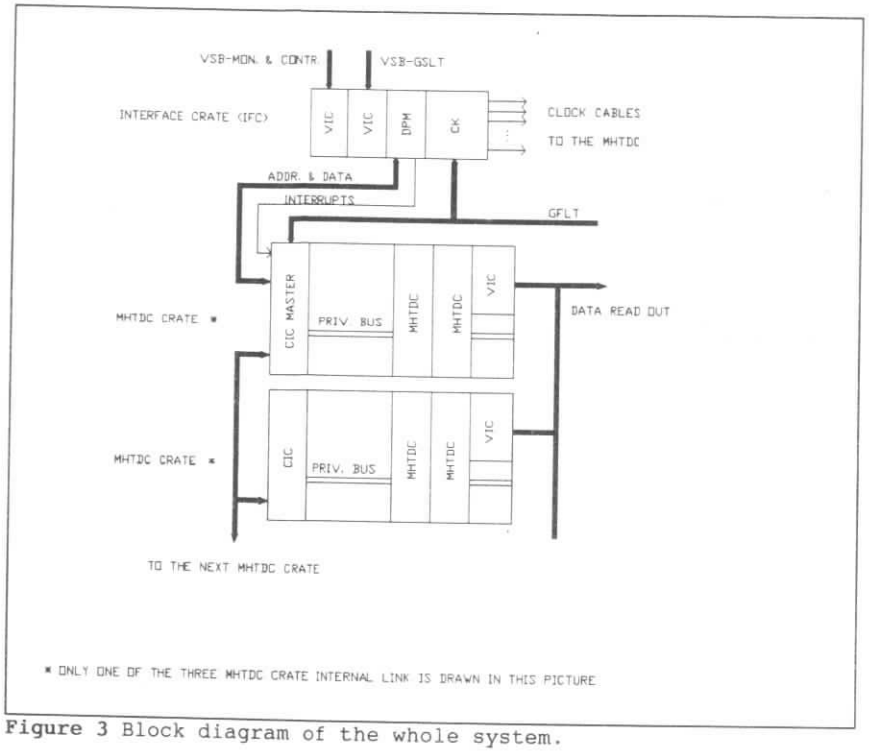

Figure 3 Block diagram of the whole system.

for formatting.

iii) **VME Interconnect Cards.** These cards are used for VME data readout.

In the 6U PMHTDC Interface Crate (IFC) are located:

iv) **Clock generator card (CK).** This card receives the GFLT and the 10.4 MHz beam crossing clock signal generated by the GFLT processor, and sends in parallel to all PMHTDC cards a 250 MHz signal that is interrupted upon receipt of the GFLT.

v) **Two VIC interconnect cards.** These cards receive the Monitor and Control signals and the GSLT signal via two remote VSB connection and transmit this data to the Interface DPM.

vi) **An Interface DPM (IFDPM).** This card serves to store the Monitor and Control signals and the GSLT signal. This memory is read by the master CIC upon receipt of interrupts issued by the IFDPM under request of the two VIC interconnect cards.

A block diagram of the PMHTDC is shown in fig. 2 and the block diagram of the system, as a whole, is shown in fig. 3.

3 - DESCRIPTION OF THE COMPONENTS

In what follows we describe in more detail the construction and operation of the various components of the PMHTDC system.

3.1 - THE CRATE INTERCONNECT CARD

This card performs the following functions:

i) It handles communications via the Private Bus with the PMHTDC boards in the crate.
ii) It ensures communication of the data on the private bus with the adjacent crates.
iii) It provides a RS232 interface accessible via STARX and STARY lines of the VXI backplane with each DSP on the PMHTDC boards.
iv) It provides the 100 Mhz and 10 Mhz differential ECL clock signals as required by the VXI standard.

The above operations are controlled by a RISC processor aided by a DMA for data transfer.
A block diagram of the CIC is shown in fig. 4

The private bus is used for three types of information transfer:
i) The GFLT data stream
ii) The GSLT data stream
iii) The Control and Monitor information and requests.

This information arrives to the chain of CIC's via a Master CIC which is connected to the 6U IFC crate and to the GFLT box. The RISC in the master CIC allocates priorities to the various commands and requests.

The GFLT information arrives directly to the Master CIC via the three FLT cables and are used as follows.
The GFLT_number (GFLT#) and the GFLT_bunch_crossing_number (GFLTbc#) (pairs 1-8 and 9-16 on the GFLT_number cable) are accepted by the master CIC when an Accept_Flag (twisted pair #14 in the GFLT Control cable) is set. The GFLT# and the GFLTbc# are broadcast to all cards in the system. If an Abort_Flag (corresponding to a Fast Clear) is received (on twisted pair #13 of the GFLT control cable) a signal is sent to the DSPs on the PMHTDC boards via the private bus; the DSP on the PMHTDC cards then disregards this event for all successive operations.

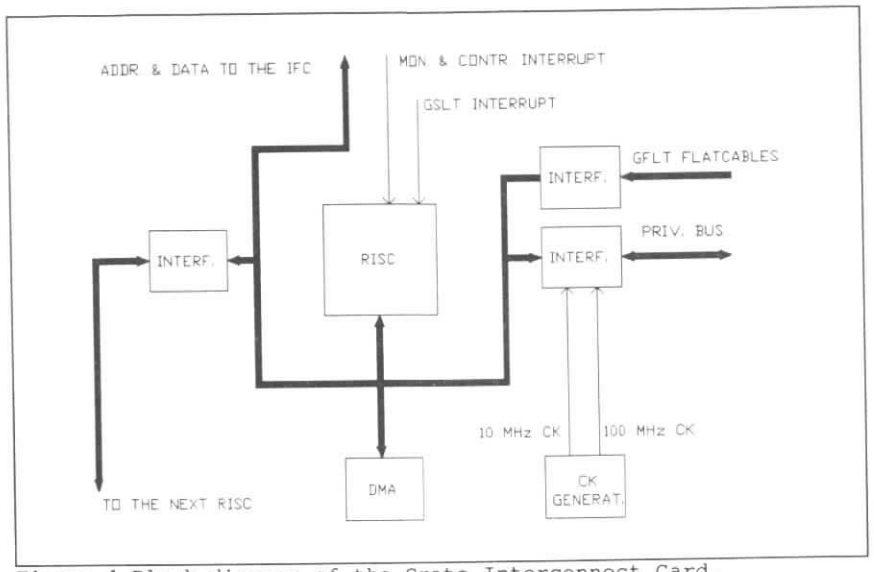

Figure 4 Block diagram of the Crate Interconnect Card.

The master CIC reads the GSLT data and the Monitor and control signals from the interface DPM in the IFC upon receipt of the corresponding interrupts.

3.2 - THE PMHTDC BOARDS

In what follows the different subunits of each PMHTDC board is described.

3.2.1 - THE FAST FRONT END

This board receives: the signals from 8 VXD sense wires, two clock signals, 10 bit memory address, a read enable signal and the analog variable thresholds for the discriminators. The board sends the data to the PB board via a 16 wire internal connection. The detailed block diagram of the FE is shown in fig. 5.

The balanced signals from 8 amplifier-shapers enter the fast front end card through a flat cable connector and then to 2 quad ECL PLESSEY SP9687 discriminators. The thresholds of the discriminators are individually controlled by the DSP on the MB by means of a DAC. The signals are then split into two and frozen by 2 MC100E143 registers R1 and R2 (propagation time 0.8 ns max) and sent to 4 4x1024 bit μPB100474 memories M1, M2, M3, M4

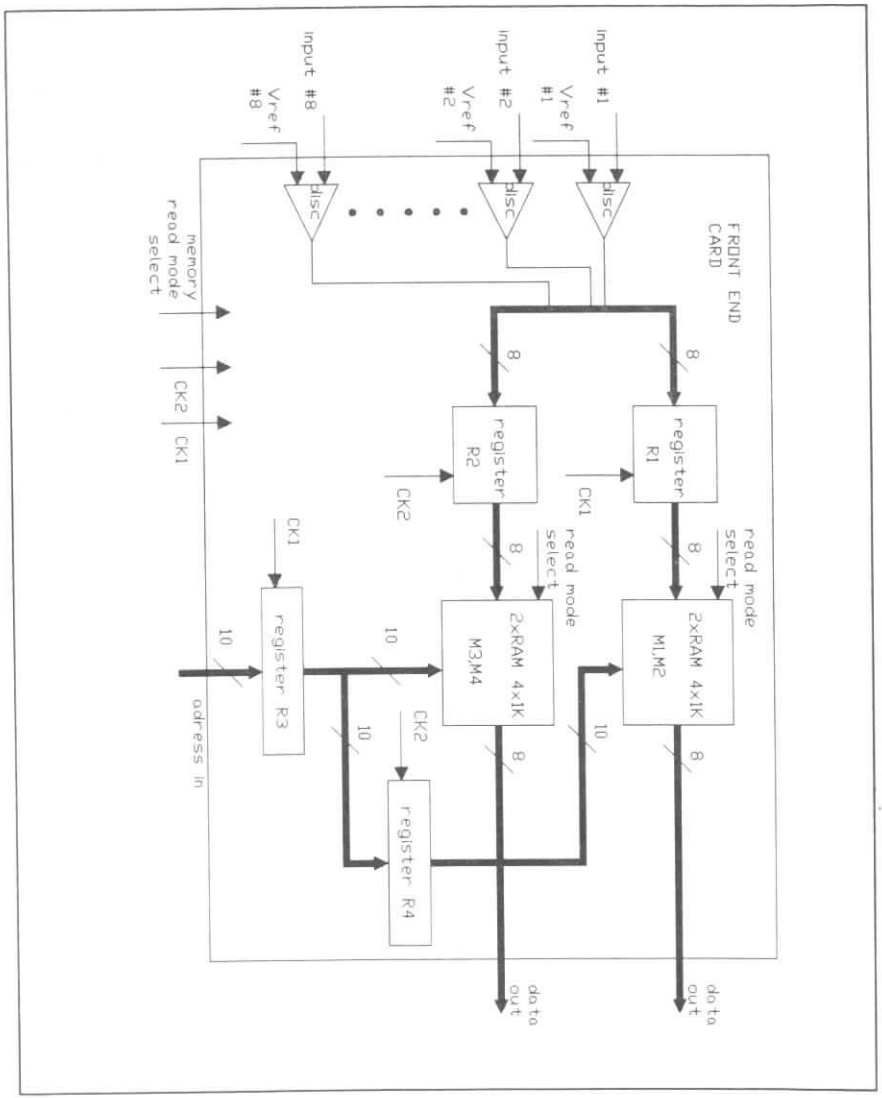

Figure 5 Block Diagram of the Front End card.

(write cycle 6 ns). The addresses of the memories are provided by a 16 bit counter located on the MB and are transmitted to the memories via 4 registers MC100E151 R3, R4 that freeze the addresses; in this way the likelihood of address transition during writing is minimized. When in "Acquisition Mode" the 125 MHz clock signal CK1 is sent to R1 and R3, CK2 is delayed by 4 ns with respect to CK1 and is sent to R2 and R4, in this way an overall accuracy of 4 ns is obtained. Memories M1 and M3 are clocked 4 ns before memories M2 and M4 and therefore the former contain the odd (1,3,..) samples while the latter contain the even samples. The use of two registers to generate the addresses eliminates possible phase errors that may be due to different paths on the MB, and also reduces the number of connections between FE and MB.

The address counter on the MB is set up so that the memories are filled cyclically between a location that is selected by means of a dipswitch and 1023, thus storing a preset quantity of data. Upon receipt of a GFLT the PMHTDC switches to "Transfer Mode", the MB ceases to send the 125 MHz clock signals and sends an internally generated 20 MHz CKR clock signal. The address counter continues advancing, clocked by CKR, through the 128 addresses following the last written address; this corresponds to 1.02 μs of data, this is more than is required to observe 768 ns corresponding to 8 beam crossings with a 4 ns sampling but is the correct amount in the event that 3 ns sampling is required.

The MB also sends a signal to select the memory read mode. The timing sequence of the addresses and the data is shown in fig. 6.

3.2.2 - THE PRIMARY BUFFER

The Primary Buffer card receives 24 data wires from 3 FE cards, a 16 bit bidirectional data bus and 4 control signals from the DSP on the MB. A block diagram of this subunit is shown in fig. 7. This card is constructed with CMOS components in order to reduce the power dissipation and the cost of the system, this also reduces the sensitivity to noise and EI.

The 24 data wires enter in parallel 8 F100125 ECL to TTL translators and then enter the Primary Buffer composed by 6 CY7C132 2Kx8 dual port memories (3 for the odd samples and 3 for the even ones). The addresses to which the data is written during the "Transfer Mode" are provided by a 7 bit counter clocked by the CKR and by the 4 most significant bias bits provided by the DSP on the MB. In order to avoid delays due to the DSP operation time, the 4 most significant address bits are pipelined so that they can be accessed immediately upon arrival of a GFLT.

As soon as the transfer of the data is completed the data is clocked into a PGA (X1) XC3042 that calculates the number of pulses $n_{c,w}$ in wire number w in cell c and the number of pulses in each VXD cell. The maximum number of pulses per wire accepted is 7. This procedure is controlled by a 10 MHz clock located on the MB; the DSP on the MB provides the bias for the addresses that are being read alternating between even and odd memories. This results in 24 data lines with 256 data points each. This operation requires

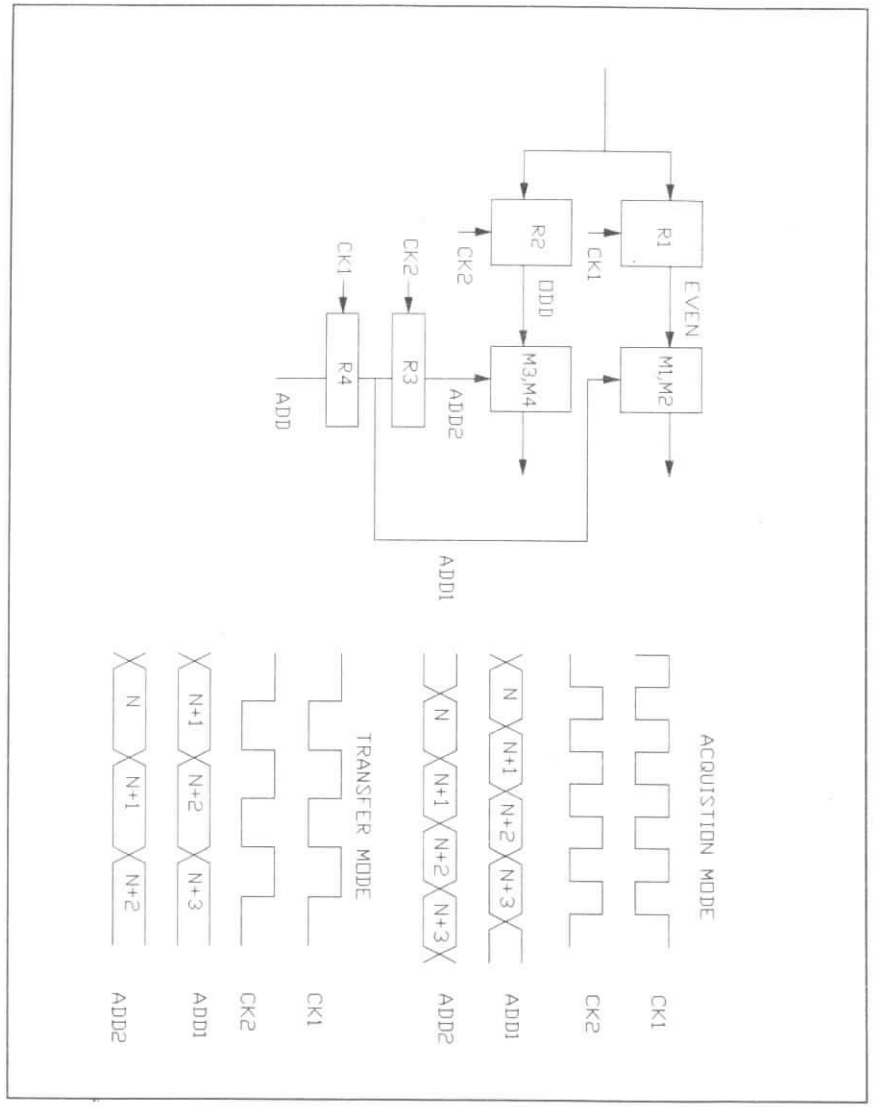

Figure 6 Timing diagram of the addresses and data.

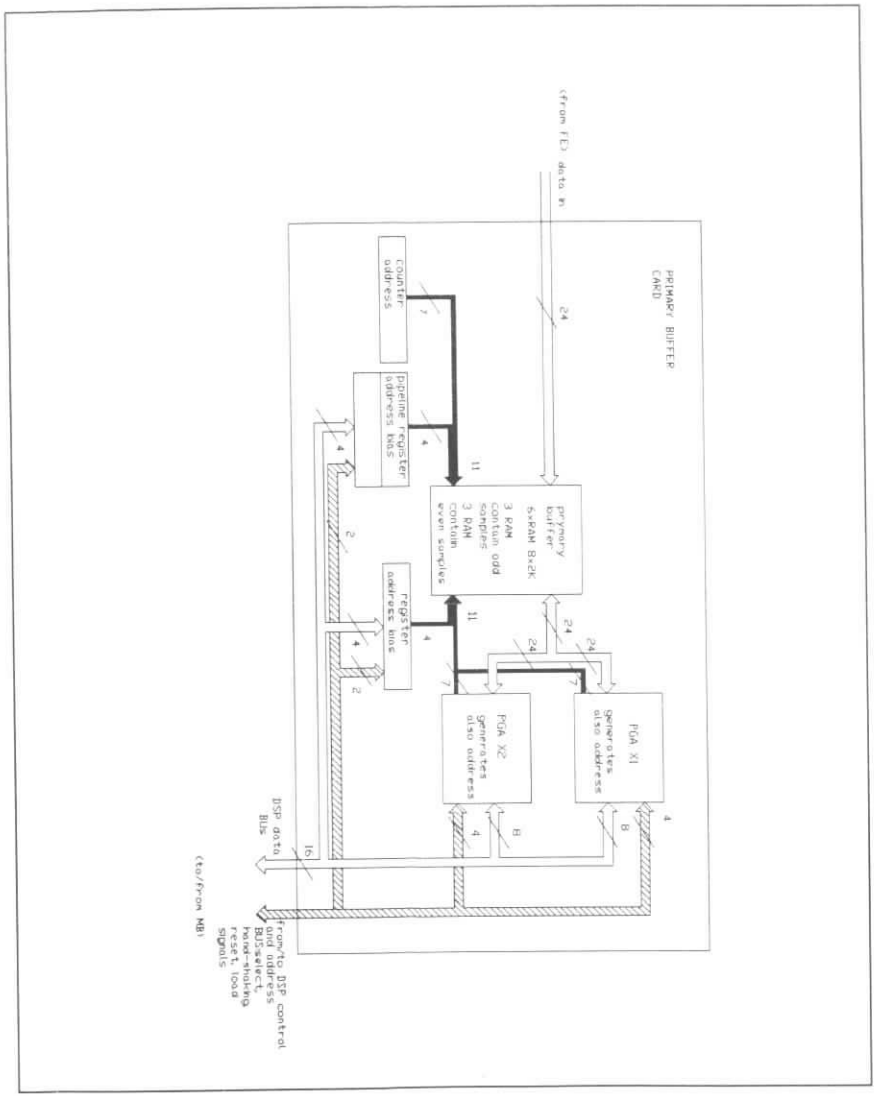

Figure 7 Block diagram of the Primary Buffer card.

25 μs (assuming a 100 ns cycle time for the PGA). This data is then transferred to the DSP via an 8 bit internal bus.

Upon arrival of a GSLT_yes the data is transferred to the second PGA (X2) in a manner similar to the previously described transfer from X1.

This PGA examines the content of each memory one bit at a time under control of the DSP. Only wires that have been found by X1 to have pulses are examined in sequence. The PGA detects the transition of the digitized signals and records their on and off times. This information is available in 8 bit words to the DSP. The two PGA are connected to the same bus and for this reason cannot be operated at the same time. The logic diagrams of X1 and X2 are shown in figs. 8 and 9. All the parameters, and the operation sequences described above can be changed after the system is installed by reprogramming the DSP.

3.2.3 - THE MOTHER BOARD

This card receives the 250 MHz clock signal from CK and is connected to the VXI bus in the crate. It uses the standard VME part of the VXI bus, and subdivides the remaining VXI pins into two parts with separate functions for the DSP interconnections: a private bus and an interrupted link

The card can be conceptually divided in six parts:

i) An ECL GFLT detector that detects the interruption of the clock signal and generates a TRAN signal that initiates the transfer phase.
ii) A clock controller that provides the other sub units with the signals CK1 and CK2 in acquisition phase and CKR when in transfer phase.
iii) An ECL address generator.
iv) The DSP that communicates with the PB board, with the output Dual Port Memory that is connected with the VME transfer bus and with the interfaces of the private bus and of the interrupted link.
v) The interrupted link and private bus interfaces.
vi) The Digital to Analog converters that generate the discriminator thresholds.

A block diagram of the MB is shown in fig. 10.

The GFLT detector (fig. 11) is implemented with a series of CXB1102Q OR gates connected to a CXB1104Q T-Flip-Flop that provides a TRAN level when the clock CK is interrupted. The T-FF is reset by a signal from the Primary Buffer when the transfer phase is terminated.

The clock controller (see fig. 12) receives the external 250 MHz clock and the TRAN signal. When TRAN is high CK1 and CK2 are 250 MHz signals 180° out of phase. When TRAN is low CK1 and CK2 are the same 20 MHz signal; this signal is generated by a local CMOS oscillator and translated to ECL by an F100124.

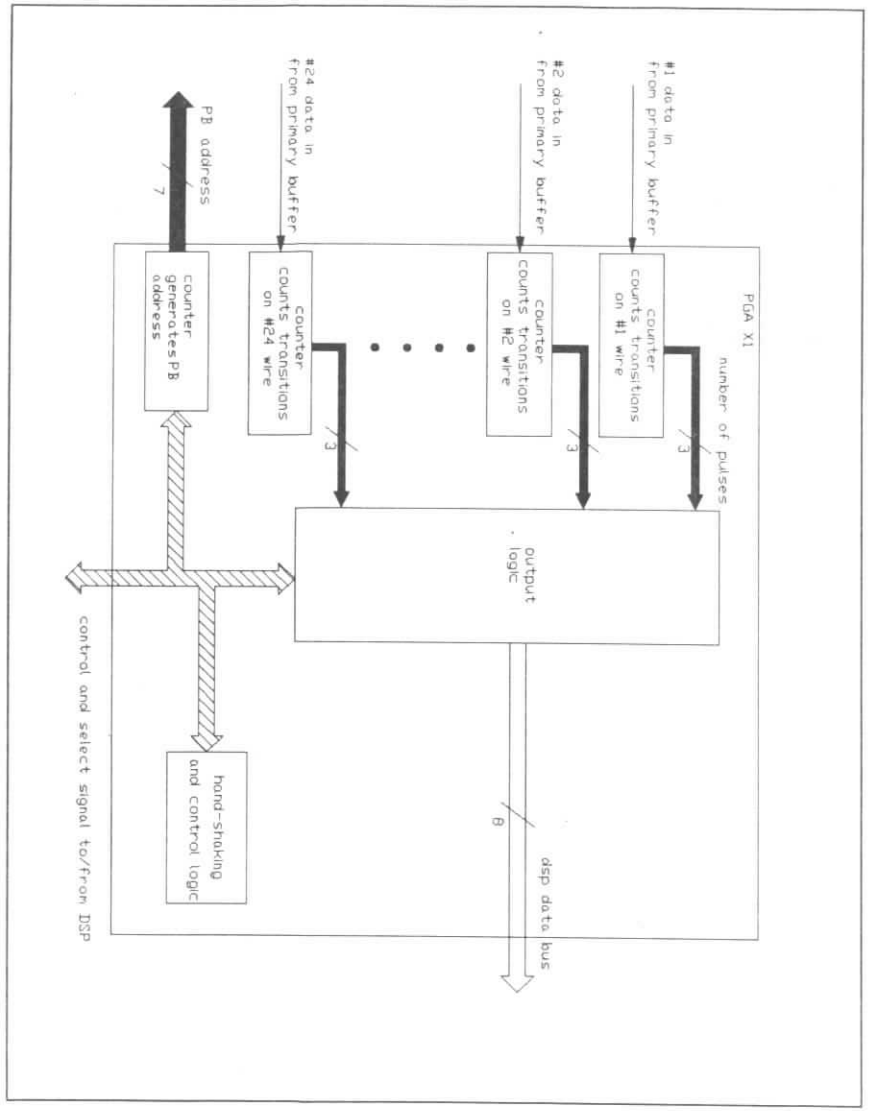

Figure 8 Block diagram of PGA X1.

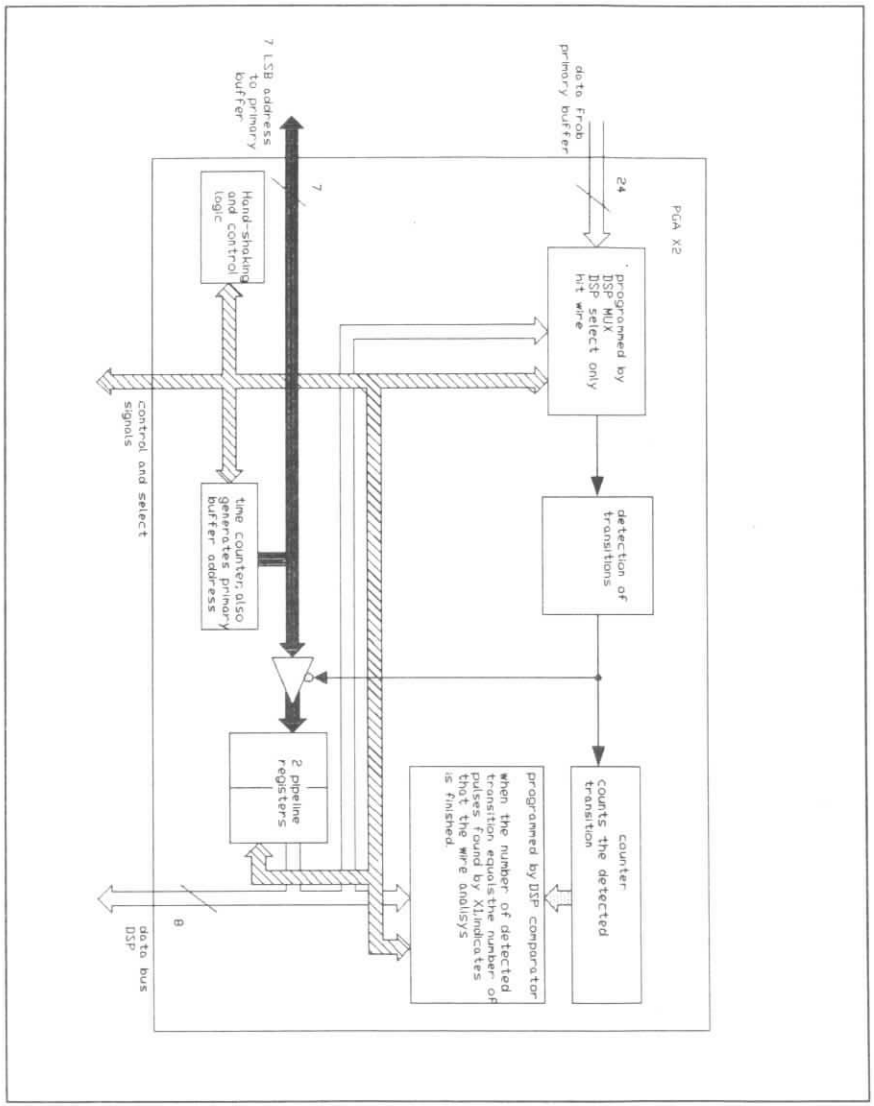

Figure 9 Block diagram of PGA X2.

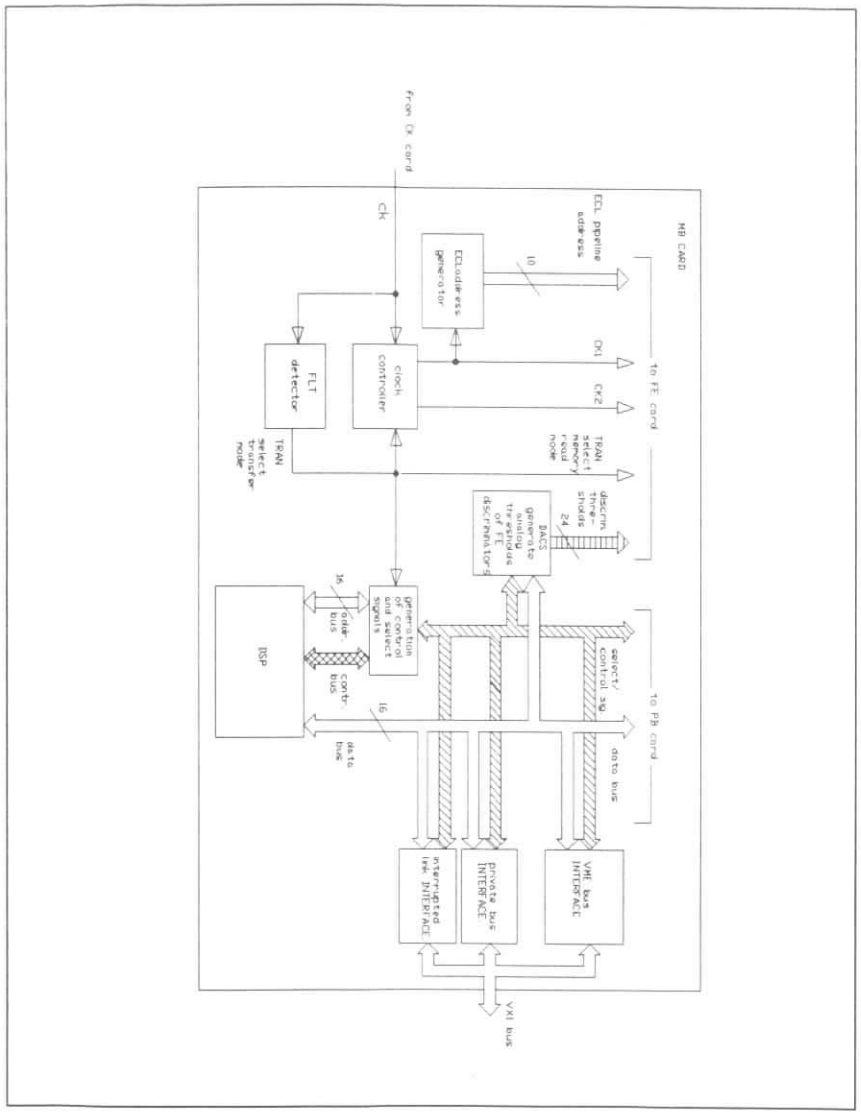

Figure 10 Block diagram of the Mother Board.

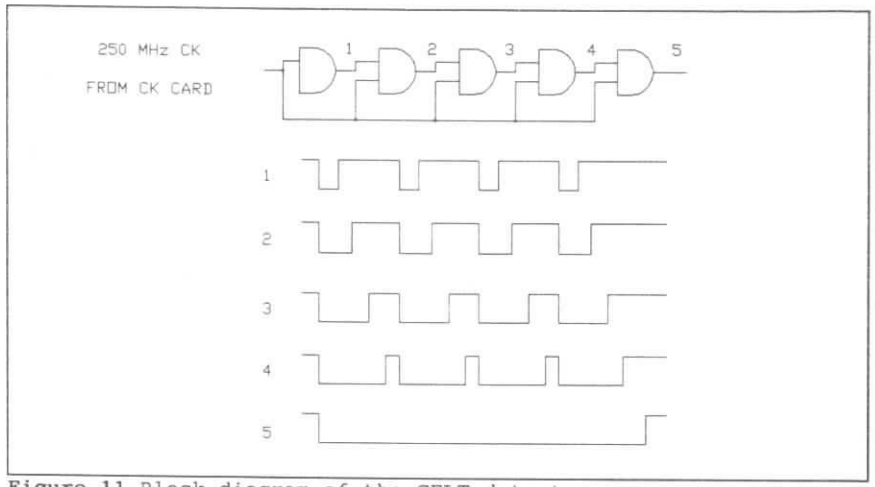

Figure 11 Block diagram of the GFLT detector.

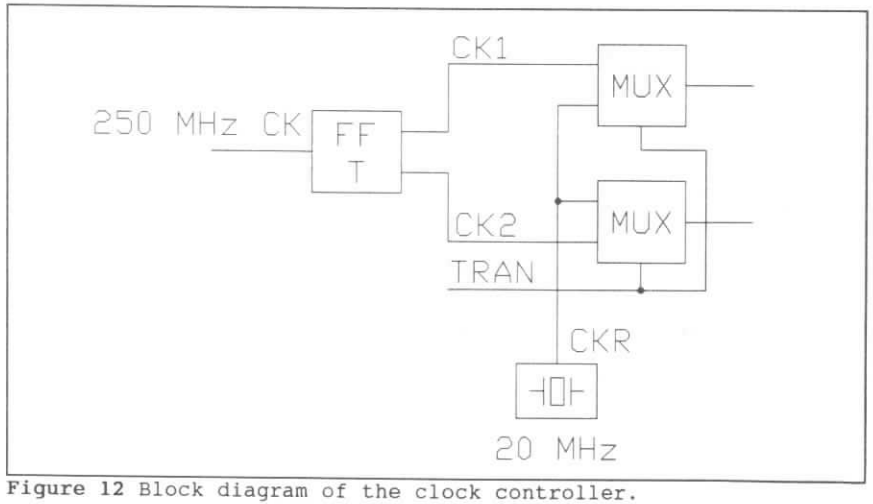

Figure 12 Block diagram of the clock controller.

The address generator is composed of two very fast (1GHz)CXB1136Q eight bit counters; only the 10 least significant bits are used. The counter is reloaded with a value preset with a dip-switch when the relevant bits are zero, so that the addresses vary cyclically between the preset value (at present 399) and 1023. The DSP on the MB card interfaces with all three VXI bus connectors.

The VME interface is formed by a Dual Port Memory (DPM) and a Logic Block (LB) able to process the VME standard protocol signals. The LB handles the 34 possible address modes provided by the VME protocol (only one address mode is used, however all modes are implemented for generality and ease of possible future modifications). Formatted data is transferred on the VME bus as long-words (32 bits), the 2 2Kx16 DPMs are connected to the VME bus and are read in parallel; their VME addresses, both in writing mode and in reading mode, are generated by counters on board

. From the VME side the DPM is divided in two parts: the first part is read as a one cell address Read Only Memory, the scanning of this memory is implemented by means of a local counter chained to all 30 PMHTDC cards; the second part of the memory is a standard Read-Write Memory with standard VME interface which permits direct connection to the DSP on the card.

Each PMHTDC card is provided with a private connection to a serial RS232 interface located in the CIC in slot 0 that permits checking and monitoring the card functions.

The DSP has a variety of functions, these can be divided in three main categories: power up, set up and run. These will be described in what follows.

At power up the DSP functions are:

i) To perform a self check.
ii) To check the communication links between individual DSPs and the main CPU of the system.
iii) To boot and check the PGAs. The two PGAs X1 and X2 are programmed by the DSP using the peripheral mode (i.e. the configuration data is loaded using a byte-wide internal data bus from the DSP). Connection between X1, X2 and DSP is bidirectional; during configuration it is used as input to X1 and X2, during operation both as input and output.
iv) To check the primary buffer memories and Front End cards.
v) To check the communication links between preamplifier, amplifier-shapers and Front End.

During set up the DSP functions are:

i) To measure the time delay differences between the preamplifiers on the VXD and the Front End discriminators by means of a test pulse especially provided.
ii) To set up the discriminator thresholds.
iii) To transmit the set up data to the system controller.

During the run phase the DSP functions are:

i) To establish the priority between function and to send error messages.
ii) To process the GFLT and check the correctness of its synchronization i.e. the coincidence of the GFLT# and the GFLTbc# detected by the GFLT detector on the MB and the broadcasted GFLT data stream received on the private bus.
iii) To maintain and update a stack containing the GFLT# and the GFLTbc# and the address of the data contained in the pipeline.
iv) To receive and process the data from the PGAs X1.
v) To processes the GSLT: upon receipt of a GSLT_no it removes the event from the event stack thereby advancing the address of the next event to be transferred to the PB; upon receipt of a GSLT_yes it formats the data received from the PGA X2; the DSP uses the information received from X1 and X2 to obtain the final format (cell number c, wire number w and the quantity of data gathered on the wire $n_{c,w}$.) and generates a byte sequence formed as follows: cell number c, quantity of data collected in the first cell n_c, number of wire w, number of pulses on the wire n_w, time of leading edge t'_i, time of trailing edge t''_i, (repeated $n_{c,w}$ times), number of next wire,...,number of second cell,....
vi) To generate the information needed by the system DMA controller for the data transfer on the VME bus, to prepare the data on the DPM that interfaces the VME bus, writing serially the two 2Kx16 memories, and to generate the appropriate signal for the transfer of control from one PMHTDC card to the next.

The DMA controller reads formatted data from the PMHTDCs in block transfer mode. The length of the block is calculated by the DSPs on the PMHTDCs boards, and is communicated through the CIC to the DMA controller. To perform this operation the DSPs communicate via interrupted link through the single crate and via private interconnect link (handled by CIC) between different crates.

During a block transfer the DMA controller generates only the starting address, the first PMHTDC board recognizes it and puts its data on the VME bus (the address of DPM are generated on board). As soon as the transfer of its data is completed (this condition is detected by an appropriate logic programmed by the DSP) the first PMHTDC generates a signal which enables the second one to output its data. So the PMHTDCs are connected in daisy-chain fashion. This allows for the maximum speed for the transfer of the data (transfer rate on VME bus is 400 ns per word).

A DPM provides the interfaces betweens DSP's on the interrupted link. The interface between the private bus and the DSP is provided by a DPM and two Erasable Programmable Logic Devices (EPLD) that implement the needed protocol logic.

3.3 - THE VIC CARDS

These cards are 1 slot VME-VSB master/slave commercial interfaces that allow remote interconnection of VME crates to each other and to the remainder of the acquisition system via twisted pair cables (differential signals).

3.4 - THE CLOCK CARD

This card receives the ECL_Level clock (twisted pair #5 in the GFLT clock cable) and the Accept_Flag (twisted pair #14 in the GFLT control cable) and issues a busy_bit (twisted pair #4 on the GFLT control cable; see specifications in [4]). It also receives the Beam Crossing Clock Signal (BCCS) via a coax cable.
The ECL_Level clock is used to synchronize a 250 MHz clock on this board, this signal (CK) is distributed by coax cable to all the PMHTDC MB cards and is the main time reference of the system. When a GFLT is issued with an Accept_Flag the CK signal is interrupted for 7 μs in synchronism with a bunch crossing.

A block diagram of the clock card is shown in fig. 13.

4 - AN OUTLINE OF THE BACKPLANE USE

4.1 - THE PRIVATE BUS

The functions of the private bus can be subdivided in three kinds:
i) Broadcast functions, these are the transmission of the GFLT, the GSLT, and the Fast Clear.
ii) Auxiliary functions such as monitor and control operations.
iii) Error and malfunction signals.
The lines utilized for this bus are:
i) The ECL CK100 and CK10 lines that provide the timing for the signals.
ii) The 8 TTL Trigger Lines, TTLTR0 to TTLTR7 which are used for the transmission of data and addresses between RISC processor on the CIC and the DSP on the MB.
iii) The 6 ECL trigger lines ECLTR0 to ECLTR5. These are used for synchronism and control of the data transmission.
iv) Two LBUS line LBUS1 and LBUS2. These are lines implement a by-directional daisy chain that is used for bus requests by the PMHTDC cards.

The transmission of data on this bus is performed with an packet switching protocol. A data packet is headed by an address and an operation code, followed by the data proper. The timing of each packet is provided by the CK10 line signal, while the beginning and end of data are provided by signals on ECLTR0 and ECLTR1.

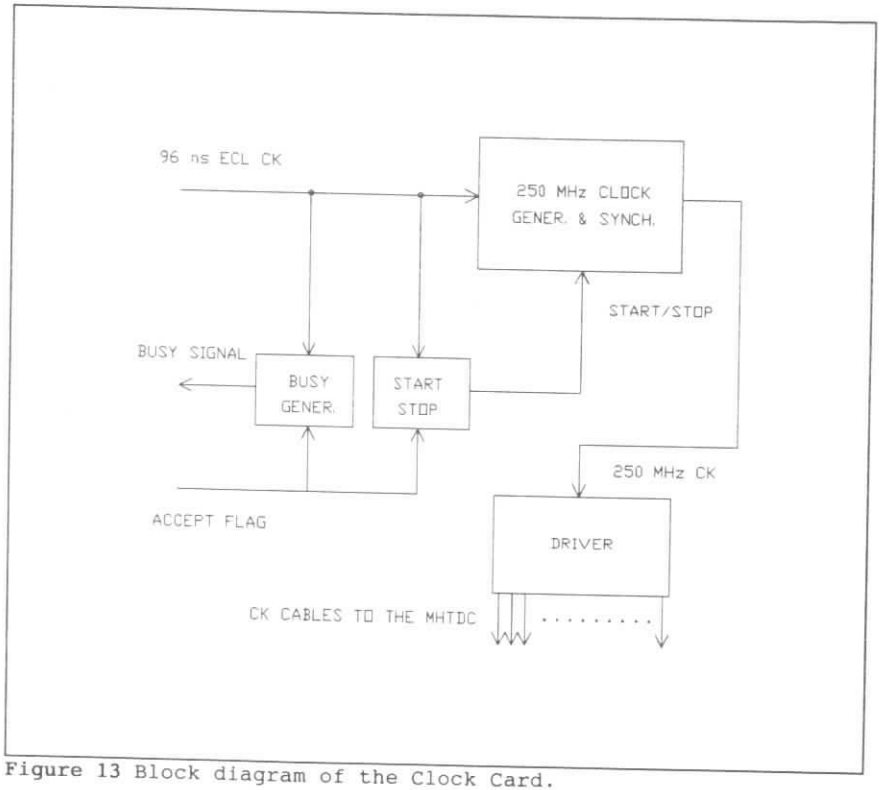

Figure 13 Block diagram of the Clock Card.

4.2 - THE INTERRUPTED LINK

The interrupted link is used for communications between DSPs. A DPM implements the interface between the DSPs in two adjacent PMHTDCs. For this connection between PMHTDCs LBUS pins of the VXI standard are used.

5 - CONCLUSIONS

Preliminary tests of Front End of this system have been performed and it was found that the data was recorded successfully and reliably with 400MHz clock signal, corresponding to a time resolution of 2.5 ns.

Future improvements of this system are being studied, in particular the use of custom ECL chips in the Fast Front End may improve the time resolution and reliability, the use of a more powerful Digital Signal Processor such as TMS320C30 will permit faster formatting and processing of the data.

A future report will describe the structure of the private bus, its communication protocol and a description of the interrupted link.

6 - ACKNOWLEDGEMENTS

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7 - REFERENCES

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