Experiences at HERA with the H1 Data Acquisition System

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ABSTRACT

The recently commissioned HERA collider provides a significant pointer to the problems that have to be surmounted in data acquisition systems at the next generation of hadron machines. With bunch crossings, between 30 GeV electrons and 820 GeV protons, 96 nanoseconds apart, the H1 experiment illustrates the application of sophisticated pipelining solutions in the readout of several hundred thousand electronic channels. A modular, multiprocessor design structure emphasises the architectural concepts necessary to cope with large data throughputs and yet remain flexible enough to exploit ongoing technological advances in both hardware and software. The range of techniques implemented will be surveyed, covering various digitisation solutions at the front-end through to embedded microprocessor arrays in standard busses controlled by graphics-based stations executing object-orientated code. The experiences gained in developing such a system are also discussed.

INTRODUCTION

HERA collides 30 GeV electrons and 820 GeV protons in two rings 7 km in circumference; the main dipole and quadrupole magnets of the proton ring are all superconducting with the 422 dipoles having a field strength of 4.68 Tesla. H1 is one of two large experiments currently operational at this facility, involving over 300 scientists from more than 30 institutes worldwide [1]. The detector, itself, consists of drift and proportional chambers (charged particle "trackers") surrounded by a liquid argon electromagnetic and hadronic calorimeter of lead and iron absorber plates, outlined in Figure 1. This inner region is enclosed by a 6 m diameter, 1.2 Tesla superconducting coil. The coil provides a large field volume for the calorimeter, with a minimal amount of inert material in front, ensuring a strong, homogeneous, solenoidal field for the tracking chambers. Surrounding it are a set of instrumented iron plates which provide the return yoke of the magnet and a muon filter/tracker system together with up to three layers of external muon chambers. Various smaller subdetector elements then complement the backward and forward areas to provide near hermetic coverage of the interaction point. The completed detector, weighing nearly 3,000 tons, was commissioned during cosmic-ray tests in Spring 1991 and has been fully operational in HERA since May 1992 at centre-of-mass energies of 314 GeV.

From the real-time computational point of view, a total of over a quarter of a million analogue channels are read-out and digitised, resulting in some 3 Mbytes of raw digitised information for a "triggered event". As the time between successive electron-proton bunch crossings is just 96 nanoseconds, various levels of hardware triggering, software filtering and digital compression are employed before reducing final data sizes to acceptable storage-media recording rates. For this several hundred processing elements are embedded largely within the IEEE VMEbus standard [2]. Several descriptions of the system during staging exist elsewhere [3, 4].

SYSTEM OVERVIEW

HERA presents an interesting technical challenge for physics extraction in real-time. A maximum 210 proton bunches can each contain 10^{11} protons; simultaneously 210 electron bunches can each contain 3.5×10^{10} electrons. At the design luminosity of 1.5×10^{31} cm^{-2} s^{-1} the physics is dominated by photoproduction at 120 Hz. Even though the bunch crossing period is just 96.064 ns, it would appear at first sight that the problem of trigger selection is trivial. However, to avoid betatron oscillations and "beam blow up", the electrons and protons collide with a zero crossing angle. This necessitates electron bending magnets close to the collision point which results in huge fluxes of synchrotron radiation. Much of this is reduced by means of absorbers and collimators, but again close to the interaction point. Together with proton beam halo and beam-gas, all this results in a background rate of 10 - 100 KHz.

Triggering and readout stages

Figure 2 summarises the overall data acquisition system and the key rates at full HERA design luminosity. Information is digitised and read-out in parallel from many subdetector partitions before
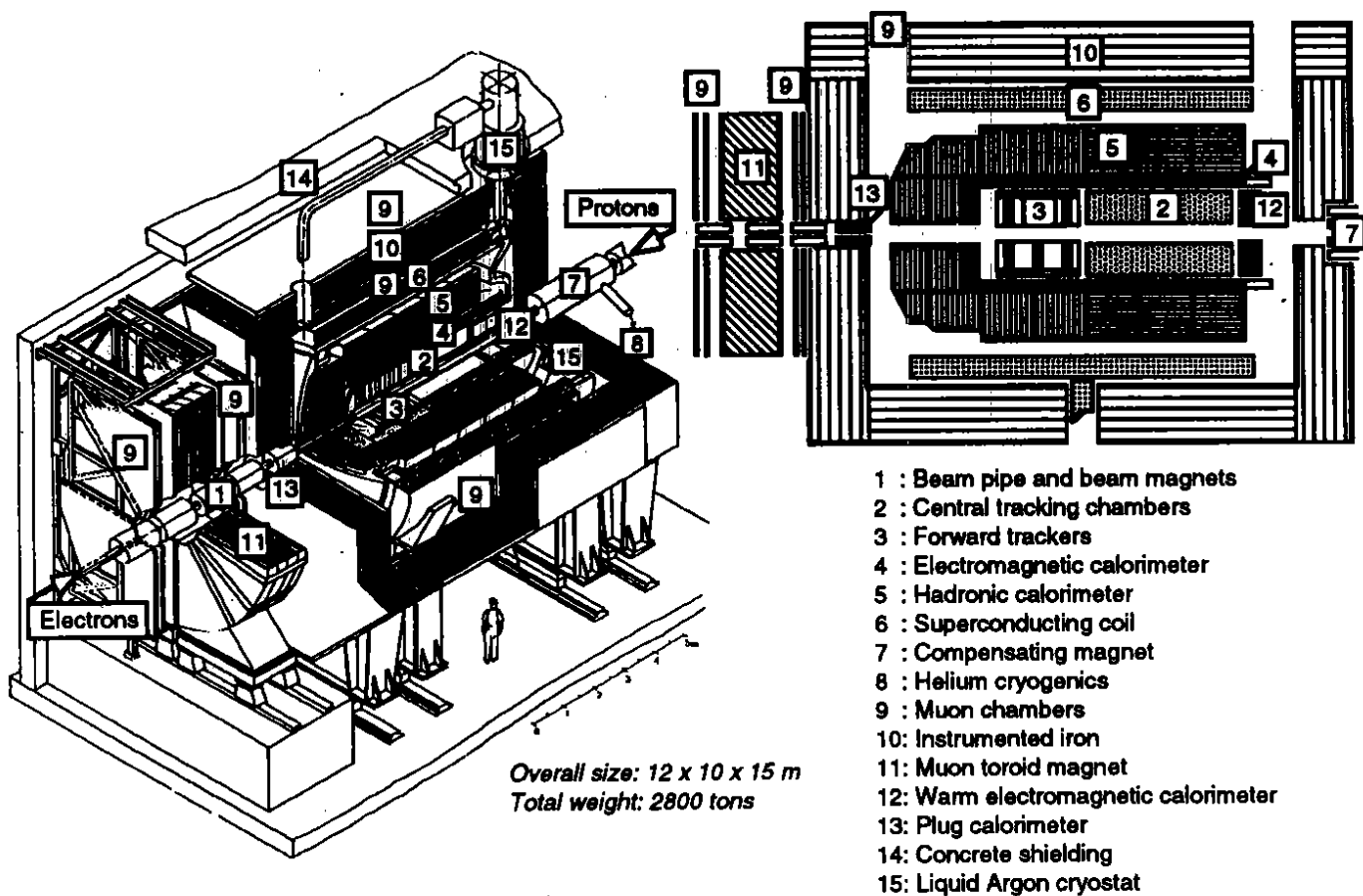
1 : Beam pipe and beam magnets
2 : Central tracking chambers
3 : Forward trackers
4 : Electromagnetic calorimeter
5 : Hadronic calorimeter
6 : Superconducting coil
7 : Compensating magnet
8 : Helium cryogenics
9 : Muon chambers
10: Instrumented iron
11: Muon toroid magnet
12: Warm electromagnetic calorimeter
13: Plug calorimeter
14: Concrete shielding
15: Liquid Argon cryostat

Overall size: 12 x 10 x 15 m
Total weight: 2800 tons

Figure 1 : The HERA detector H1

being finally merged. Four main levels of hardware triggering and software filtering can be enabled on all or part of the various detector partitions. In parallel data compression and formatting reduce the 3 Mbytes of raw data to event sizes of between 50 Kbytes and 100 Kbytes so that final data recording rates are restricted, at present, to a maximum 1.2 Mbytes/s.

A purpose-built pipelined triggering system (22 bunch-crossings long, dead-time free) is used to select initial candidates for data processing from the background [5,6]. This "Level-1" comprises several triggering elements from different parts of the detector, such as FADC energy sums from the calorimeter, fast vertex-position reconstruction from the proportional chambers using XILINX logic cells and veto-wall and time-of-flight subsystems against off-momentum beam particles. A particularly interesting level-1 element is the fast track finder which again capitalises on XILINX cells, this time to find and count charged tracks in the r-Ø projection from a sample of the central drift chamber wires [7].

After a Level-1 accept the front-end pipelines are held. Dead-time then begins. A more refined hardwired Level-2 decision, based on combined information, can then be activated within 20 μs. Solutions based on neural networks and ASICs are presently being prepared in readiness for full HERA luminosity. Front-end electronics readout is not initiated until an early-level triggering decision is made whereupon each component has a maximum digitisation time of 800 μs before the pipelines are re-enabled. This governs a significant fraction of the dead-time of the complete system; with a hadron-hadron collider such a predicament would not be tolerable. A large amount of the data compression also takes place during this phase. However a third level of filtering can be enabled so that should readout commence, the pipelines are immediately reactivated if a Level-3 reject occurs.

Logical structure and data control

In logical structure H1 merges its detector components, in parallel, into individual subdetector VMEbus crates which each contain a readout controller and memory buffer plus a fibre optic link to a
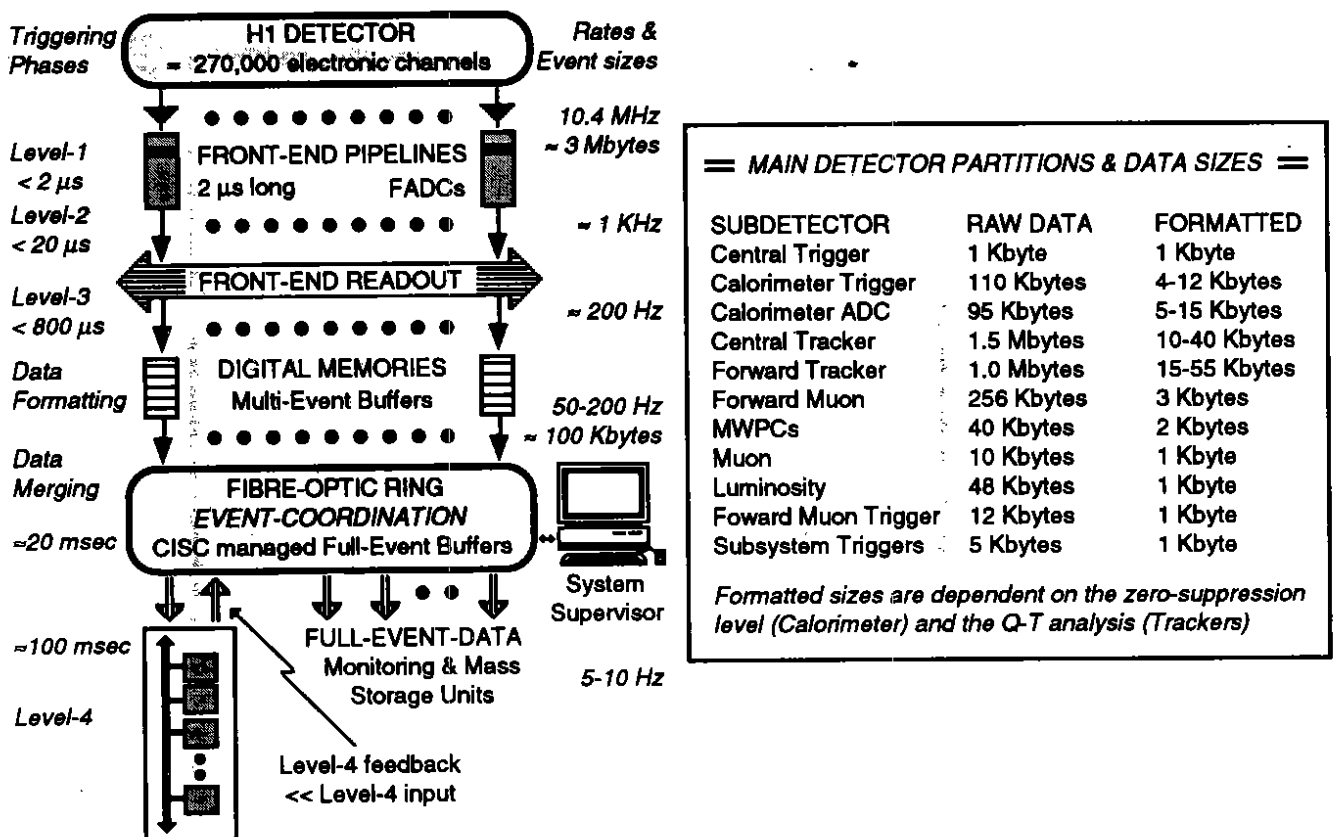
Triggering Phases — H1 DETECTOR ≈ 270,000 electronic channels — Rates & Event sizes

Level-1 < 2 μs — FRONT-END PIPELINES 2 μs long — FADCs — 10.4 MHz ~ 3 Mbytes

Level-2 < 20 μs — ~ 1 KHz

Level-3 < 800 μs — FRONT-END READOUT — ~ 200 Hz

Data Formatting — DIGITAL MEMORIES Multi-Event Buffers — 50-200 Hz ~ 100 Kbytes

Data Merging ≈20 msec — FIBRE-OPTIC RING EVENT-COORDINATION CISC managed Full-Event Buffers — System Supervisor — 5-10 Hz

≈100 msec — FULL-EVENT-DATA Monitoring & Mass Storage Units

Level-4 — Level-4 feedback << Level-4 input

SUBDETECTOR	RAW DATA	FORMATTED
Central Trigger	1 Kbyte	1 Kbyte
Calorimeter Trigger	110 Kbytes	4-12 Kbytes
Calorimeter ADC	95 Kbytes	5-15 Kbytes
Central Tracker	1.5 Mbytes	10-40 Kbytes
Forward Tracker	1.0 Mbytes	15-55 Kbytes
Forward Muon	256 Kbytes	3 Kbytes
MWPCs	40 Kbytes	2 Kbytes
Muon	10 Kbytes	1 Kbyte
Luminosity	48 Kbytes	1 Kbyte
Foward Muon Trigger	12 Kbytes	1 Kbyte
Subsystem Triggers	5 Kbytes	1 Kbyte

≡ MAIN DETECTOR PARTITIONS & DATA SIZES ≡

Formatted sizes are dependent on the zero-suppression level (Calorimeter) and the Q-T analysis (Trackers)

Figure 2 : Overview of the H1 Data Acquisition System

coordinating event management task. A parallel array of RISC processors provides the fourth level of software-coded filtering once all of the full-event information is combined over the fibre-optics [8].

At all stages workstation intervention provides for data monitoring and detector control. To avoid saturation on global VMEbusses, extensive use is made of the local VSB specification [9]. To minimise any further dead-time contributions, memory buffering is provided at the key data processing stages.

Finally a Local Area Network (Ethernet) caters for the relatively slow exchange of general operating conditions, files and even event-records between different subsystems. This also serves the external international community with current status and event information over wide-area networks.

FRONT-END DIGITISATION

The digitisation of the 270,000 front-end signals comprises a vast array of readout electronics.

Calorimetry

The 45000 channels of the liquid argon calorimeter consist of readout pads sandwiched around absorber plates. These are multiplexed onto 65000 inputs into 12-bit ADCs (25% of the channels have double gain) and read out by 69 Digital Signal Processors (56001) [10]. Each DSP performs zero suppression, pedestal subtraction, gain correction and calibration sums [11]. The digitisations are buffered in stages, both before and after the DSPs, to minimise dead-times before being read out over VMEbus. The whole system can be managed by either 68030-CISC or 29000-RISC processors. In parallel, the calorimeter trigger (from analogue channel sums) is read out with 8-bit FADCs and 56001 DSPs via a separate VMEbus branch. In each branch DSP encoding takes place in 800 μs. Single-width VICs are used to interconnect blocks of crates with transfer rates of 8 Mbytes/s [12]. The backward and plug calorimeters together with the instrumented iron are also read-out through the same subsystem.

Charged particle tracking and digital muon readout

A purpose-built solution is used for digitising and compressing the analogue information from the 9,520 sense wires of the inner drift and forward-muon chambers [13]. Each digitising channel consists
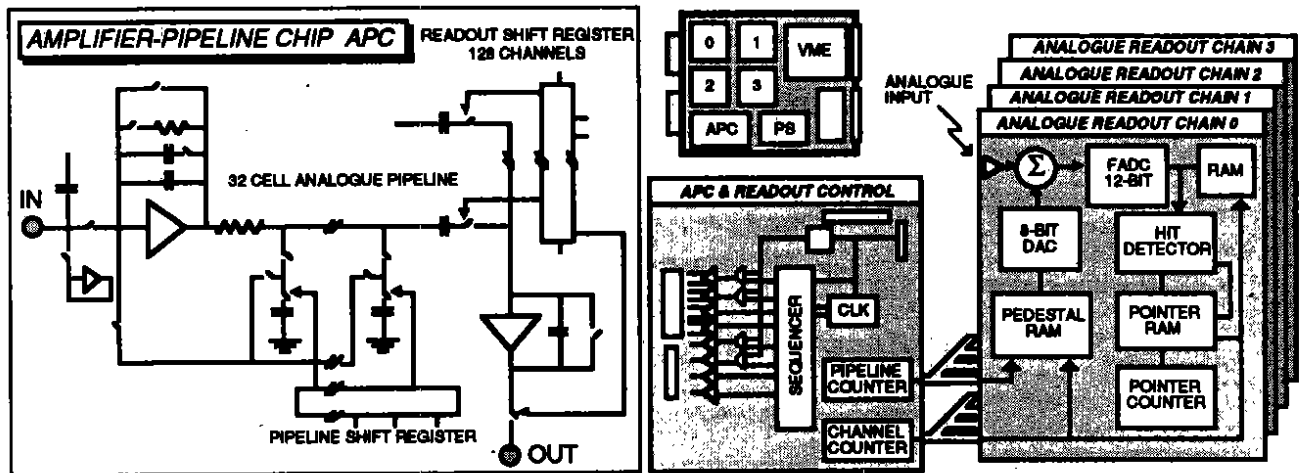
Figure 3 : Silicon tracker readout electronics. Each VMEbus card can read out and control 4 x 2048 channels

of a 100 MHz, 8-bit, nonlinear Flash ADC. A total of 45 triple-height VMEbus-based crates each enable up to 256 channels to be read-out. There are 256, 8-bit words per FADC channel, giving a total of 64 Kbytes of raw data information per crate. A fast scanner module reads out the 256 channels into memory at 80 Mbytes/s within the maximum allowed readout time of 800 μs [14]. The leftmost four slots of each crate can accommodate standard double-height VMEbus cards with VSB. This enables each crate to be equipped with commercial 68030-based processor boards (to be upgraded to 68040-based cards) in order to compress the total of over 2 Mbytes of tracker information into a few tens of kilobytes for each triggered event [15]. The data from the separate crates are merged initially over VIC-bus [12]. The luminosity counters, which confirmed the first collisions from HERA in October 1991, also use the same FADC system [16].

The wires of the muon system contribute a large number of channels sparsely filled with data, so an encoding system is used [17]. It is contained within a total of 6 standard VMEbus crates, with a division of 64 modules (within each module there are 16 chamber planes with a maximum of 512 channels per plane) each equipped with its own readout controller. These controllers work in parallel, independent of each other. Each wire is connected to a comparator whose output is fed into shift register pipelines (depth of 32 stages). On triggering these registers are dumped into memories within the readout controllers at frequencies between 1 and 10 MHz, where the data are zero suppressed and encoded.

The multi-wire proportional chambers (MWPCs) have 3964 pads. All front-end electronics are based on a user-defined backplane split into 4 subbranches where 280 receiver cards are distributed between 16 crates [18]. Each receiver card consists of a discriminator which feeds a pipeline, keeping synchronisation with the HERA clock. Controller cards interface the front-end crates to VMEbus via branch drivers each equipped with a DMA controller and on-board FIFO.

Silicon trackers

A proposal is now under way to implement silicon strip detectors by the end of 1994 [19]. A total of 214,000 electronic channels are to be read out by purpose-built front-end amplifier chips which contain switched capacitor analogue-pipeline buffers (Figure 3). A single chip has 128 low-noise channels with a pitch of 44μm per channel storing 32 consecutive bunch crossings. Pipeline control will be synchronised to the 96 ns bunch crossing period. Each chip is fabricated in a 2μm CMOS process and prototypes have already been tested with a readout speed of 2.5 MHz, allowing a 2000:1 multiplexing within the 800 μs readout time. The total power consumption of a single chip, including the pipeline running at 10 MHz, is 38mW. An external readout unit, with a data reduction processor for hit-finding and zero-suppression, is currently under the early stages of development with a VMEbus interface.

SYSTEM INGREDIENTS

Altogether there exist some 200 electronics crates, the majority VMEbus, spread around the H1 online complex with a multitude of processing tasks executing in parallel. To provide a coherently managed system a certain set of standards was established to ease maintenance and software development overheads.
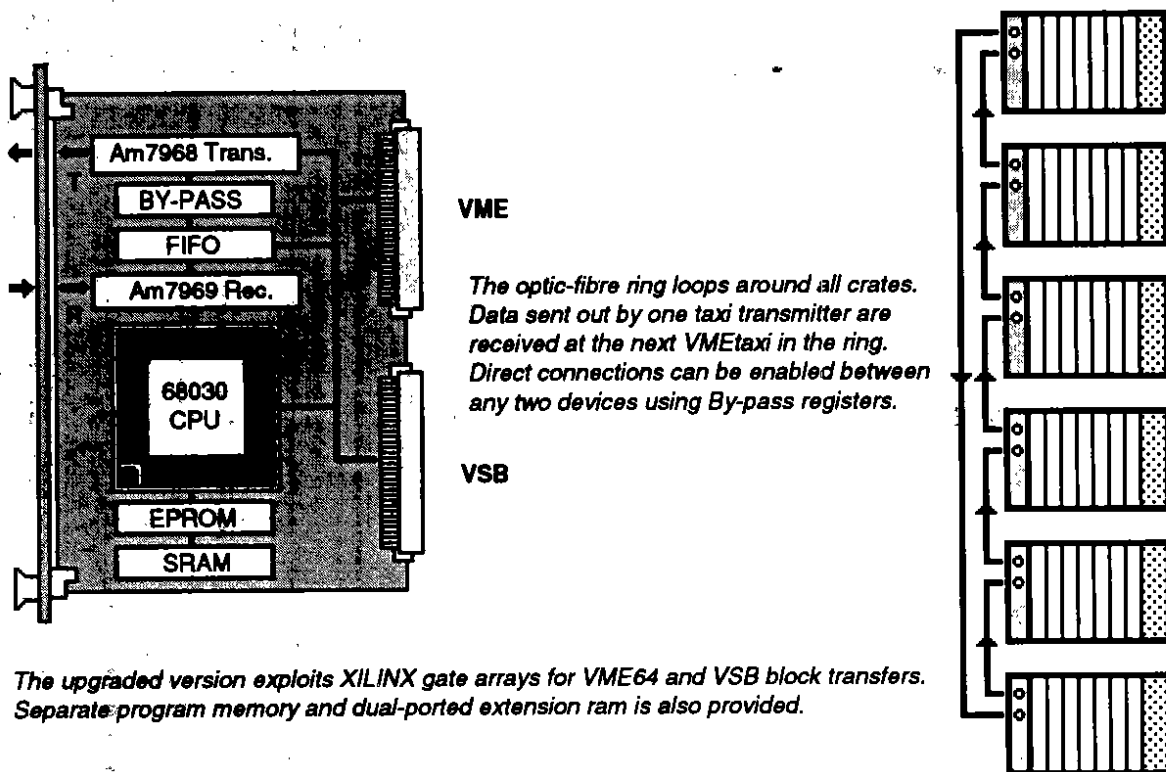
VME

The optic-fibre ring loops around all crates. Data sent out by one taxi transmitter are received at the next VMEtaxi in the ring. Direct connections can be enabled between any two devices using By-pass registers.

VSB

The upgraded version exploits XILINX gate arrays for VME64 and VSB block transfers. Separate program memory and dual-ported extension ram is also provided.

Figure 4 : VMEtaxi fundamentals

Basic hardware components

For general-purpose real-time control within VMEbus, a common 68020/30/40 processor card was selected [20]. On-board memory is *dual-ported* so that it can be accessed externally from the VMEbus (for communication) as well as internally from the processor itself. VSB local bus access can be extended to memory boards in adjacent crates but is *never* used as an inter-crate connection.

For even more calculation-intensive applications RISC processor-based modules are employed. The RAID 8235 is a single-width VMEbus/VSB board based on the 25 MHz MIPS R3000 processor and the R3010 Floating-Point Accelerator with up to 32 Mbytes of onboard DRAM [21]. To enhance memory bandwidths and reduce instruction access times, 128 Kbytes of independent data and instruction cache ensure that each board has an equivalent computing power of around 50% of an IBM 3090 mainframe.

The DPM 8242 is the basic memory module and can be equipped with up to 16 Mbytes of 70 ns static ram, having equal priority in arbitration from the VME and VSB ports [22]. A broadcast mode selection allows any VMEbus master to write to several memories simultaneously. Both the VMEbus and VSB memory base addresses are *software programmable* via VME accessible registers, permitting a managing Event Coordinator task (see later) to switch units between different events.

Due to their graphics-user-interface and open NuBus architecture, Macintosh computers are used extensively for the purpose of software development and operator control. Up to 24 VMEbus crates can be mapped directly onto each Macintosh via MacVEE and Micron, MacVEE Interface Card Resident On NuBus [23]. No sophisticated protocol needs to be initialised, unlike other DMA-based connections.

VMEtaxi

In many of the front-end subsystems the standard VICbus is used to interconnect crates. However for coordinating the fast data acquisition transmission protocol, between the different readout subsystems, VMEtaxi modules are employed [24]. These can connect VMEbus crates up to several kilometres with fibre-optics. Figure 4 illustrates the basic philosophy. All boards are interconnected with multimode optic fibres to form a ring, using AMD 7968/7969 TAXI-chip transmitter/receiver pairs. Because of this, there is theoretically no limit on the number of such devices which can be interconnected within a single ring; in practice one is limited by the software overhead in setting up transfers. Each single-width

CALORIMETER FORWARD & CENTRAL TRACKING MWPCs MUONS

H1 DETECTOR
≈ 270,000 channels
≈ 3 MBytes raw data

LUMI

FRONT-END DIGITISATION

PARALLEL READOUT
FADCs, DSPs, μPs

Mainly VMEbus

200 Hz maximum
10 - 20 Hz typically

≈ 200 crates
≈ 200 μprocessors
≈ 70 DSPs

Qt-analysis in drift chambers

Fwd μ

DATA COMPRESSION

Subdetector Master Crates (12 Branches)

TRIGGER

12 - 50 MBytes/s max.
≈ 1.5 MB/s typically

FIBRE-OPTIC RING

CENTRAL DAQ

SYSTEM SUPERVISOR MACINTOSH

EVENT COORDINATION

L4 PARALLEL FILTER

SYSTEM-MANAGEMENT

FULL-EVENT RECORDS

R3000 RISC NODES

EVENT BUILDING

L4 FILTER RECONSTRUCTION

EVENT DISPLAY MACINTOSH

FULL-EVENT TASKS

RISC PROCESSORS
300 MIPS, 1992

DATA MONITORING

EVENT SERVER FOR NETWORK ACCESS

7 MBytes/s maximum
5 - 10 Hz ≈ .6 MB/s typically

DATA LOGGING
Fibre-optic link H1->DESY

DISCS

IBM

DSTs
25 GB

COMPUTER CENTRE

< 1 MByte/s

CARTRIDGES
Production
Output Tapes
400 GB

SGI

EVENT CLASSIFICATION
DATA REDUCTION

SGI
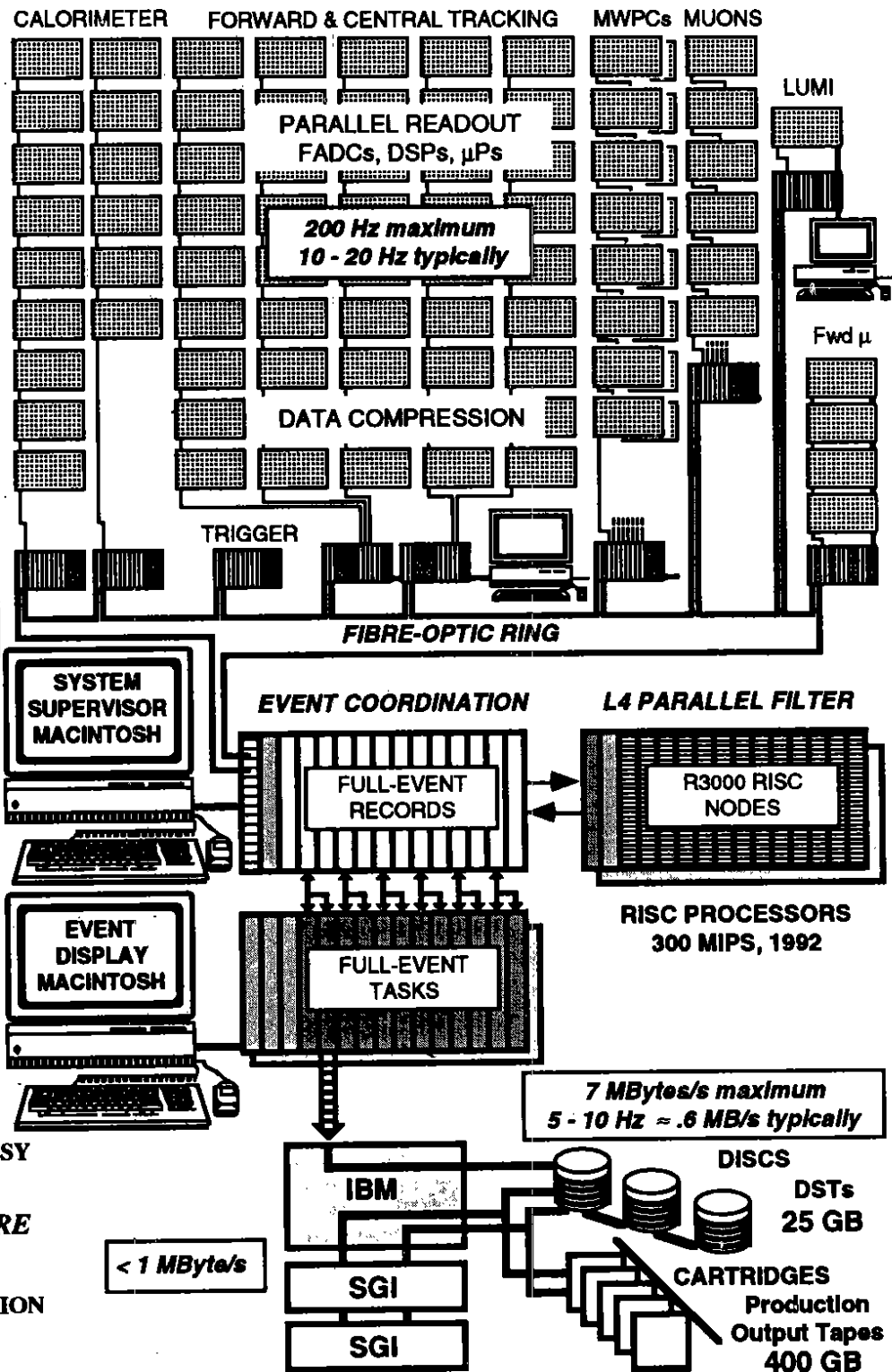
Figure 5 : Physical layout of the key features of the H1 Data Acquisition System. Refer to text for details.

board has a cpu controller and single level VMEbus arbiter. The software protocol, discussed further in the following sections, is purpose-written and optimised for speed and efficiency in a data acquisition environment; no FDDI or similar networking protocol is adopted. In setting up transfers between any two crates, an initial description packet is sent around the ring; those modules not engaged in the subsequent activity can enable by-pass registers so as to establish a direct connection between the two VMEtaxis that are involved, analogous with SCI [25].

Currently a 25 MHz 68020 based board is used with 125 MHz taxi chips; later this year upgraded "Mark-2" modules will be able to exploit 33-50 MHz 68030 processors and 250 MHz taxi chips. With the current 020 boards, the system is capable of sustained 32-bit DMA block transfers of 12.5 Mbytes/s under software control independent of distance; using double-links, on the upgraded 030 cards, up to 50 Mbytes/s will be achievable. The *link* reliability has been tested to a bit error rate of less than 1 in 10^{13}. Program memory is provided for by 128 Kbytes of on-board dual-ported static ram (expandable to 2 Mbytes on the upgraded system), with external memory access through either the VMEbus or VSB ports. On-board EPROM and EEPROM provide for firmware storage and configuration parameters. VME64 and VSB block transfer modes will be provided for on the Mark-2 modules, realised with XILINX gate arrays presently under evaluation with 175 MHz taxi chips.

Software

The architectural structure of the hardware, discussed in the following section, defines how the software is written and developed. Dedicated tasks run on dedicated processors throughout the VMEbus system with operator intervention provided for via graphics-orientated computers such as Macintosh. Different languages and approaches are used depending on the application being developed. Much of the online data acquisition systems code which executes on 68000 series microprocessors, within the VMEbus, is written in either C or Assembler. Final-level filtering algorithms, which execute on the R3000 boards, have large code resources originating offline and written in Fortran [8]. Control programs which run on the Macintosh computers exploit the latest object-orientated and graphics-based packages currently on the market [26]. It can be seen that the Macintosh provides a convenient integral component in both software development and operator-control. In order to encompass the framework of VMEbus, extra tools have been developed to ease the integration into the VMEbus [27]. As a result, no formal operating system is required to run on the VMEbus boards; all basic functions can be controlled from a Macintosh via external directives through dual-ported mailbox memories.

In order to enhance information exchange between control computers a dedicated package has been written based on international networking protocols [28]; this has the added advantage of enabling the complete system to be monitored from external laboratories and institutes.

SYSTEM INTEGRATION

By convention the data acquisition system breaks down into three main categories for the purpose of central coordination and management. First there are the front-end "producers" of data; the end result of extensive electronics digitisation from the subdetectors or "branches". Second, the data are merged and distributed to several full-event "consumers"; subsystems which monitor and record the data onto permanent storage media. Third, the system is initiated and controlled via external processes for overall system supervision and operator intervention.

Figure 5 shows the physical layout of the complete system, managed centrally through several layers of software protocol, purpose-written around the VMEtaxi fibre-optic ring [29]. Common, shared, memory blocks provide for the communication between all system processors and external computer stations. The master of the ring executes the "Event Coordinator" task, controlling the whole sequence of management processes. A separate object module provides a software library to interface the individual subsystem elements, with features ranging from full module testing and control through to basic buffer management and system coordination.

The architecture of the front-end producers

The readout system of each branch is autonomous up to and including a central subdetector VMEbus crate. Each central subdetector crate contains a dedicated supervisory readout controller, a multi-event buffer (MEB), a VMEtaxi and any input drivers necessary to access the data (Figure 6). Consequently the design allows a particular subdetector to be decoupled from the rest of the system, during installation and test phases, and does not exclude the use of other busses for front-end digitisation. Data are placed into the multi-event buffer over VMEbus and then extracted, by the VMEtaxi, through VSB. The Event Coordinator management task runs on the master VMEtaxi of the ring and interacts with each readout controller via shared memory blocks. Before commencing data acquisition, the Event Coordinator is responsible for hardware recognition and initialisation of the various branches. During acquisition, when it is free for event building, it searches the subdetector multi-event buffers for the next event.
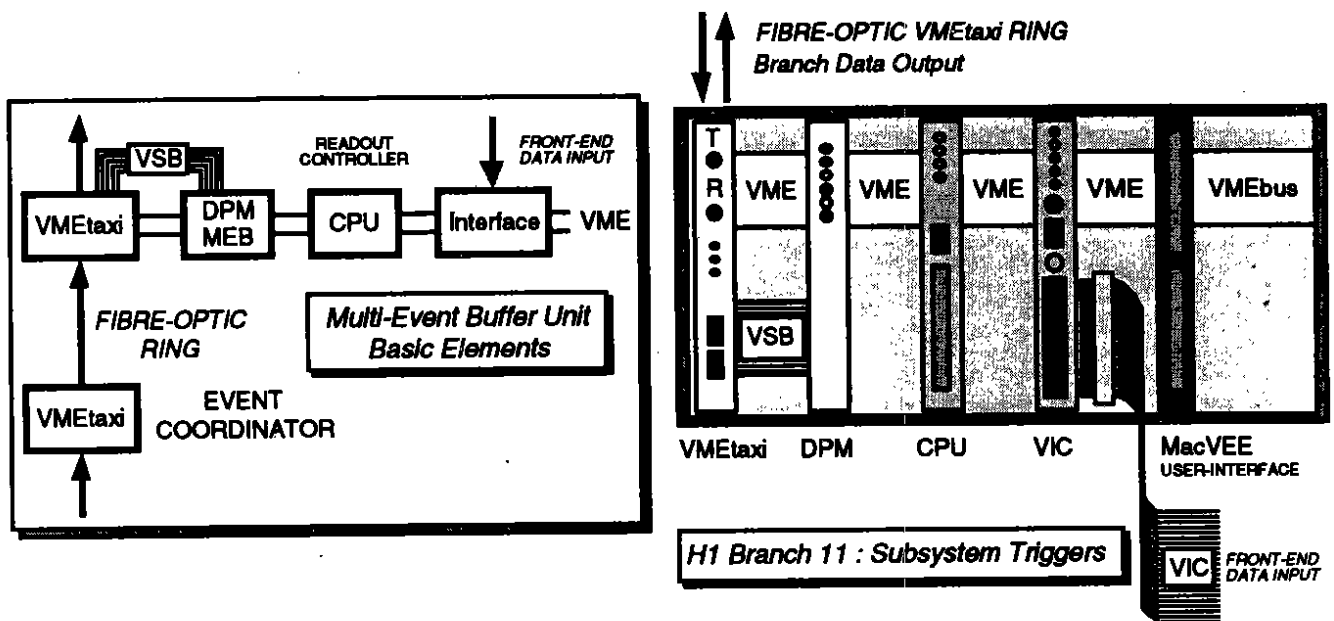
Figure 6 : Multi-event buffer units

When all branches are ready with the same event number, the separate banks are transferred via the optical ring into a full-event buffering system. On completion, each corresponding buffer is released.

A subdetector crate may also contain additional processors for data reduction, an interface to a subdetector monitoring computer and a subsystem trigger controller (STC). All STCs are interfaced to a dedicated central trigger controller which, in turn, coordinates the sequence of all hardware triggering levels together with obtaining information from the HERA machine [30]. Each STC provides signal ports for the component electronics and communicates with the readout through VMEbus read-write cycles and interrupts. A consequence of this is that the Event Coordinator needs no hardwired connection with the central trigger controller itself; all management sequences are handled by software, so providing a portable solution to any large multi-crate VMEbus system.

At the subdetector branch level, the software library [29] provides multi-event-unit routines catering for initialisation, accessing status information, requesting buffers and signalling when event data are ready for merging. Readout error codes are normally indicated as standard parameters, but messages can be sent through the system in standard ASCII format to describe branch-specific anomalies. Figure 6 also shows how the protocol has been transparently mapped from a main branch through to a sub-branch structure by incorporating standard VIC links to merge smaller subsystem components.

The management of full-event consumers

As the Event Coordinator VMEtaxi builds full-event records it simultaneously broadcasts them along its VMEbus to dual-ported memories associated with parallel sets of "full-event units". Event tasks are performed by connecting the unit processors with their respective full-event buffer (FEB) memories via VSB in order to minimise any bandwidth overheads (Figure 7). Since the memory has read/write access from both the event task processors and the Event Coordinator, full-event units need not only be "consumers" of data. An event unit can also become a "producer" of data, "feeding-back" data into the system. Consumers are able to determine which data they wish to receive, ie directly built events from the front-end branches or data fed-back into the system from, for example, a parallel filter farm. All this is handled modularly by the software protocol and its associated library of routines.

Typical full-event tasks are data-logging, event display, data monitoring and histogramming. Final event records are sent to the central IBM facility at DESY, some 3 km distant, at rates of up to 7 Mbytes/s [31]; at present the disc writing rate limits the system to 1.2 Mbytes/s. The data logging task requests every event to be recorded and so there must always be a free buffer associated with it. In case of link failure a backup event task, that drives a storage device directly from VMEbus, can be enabled.
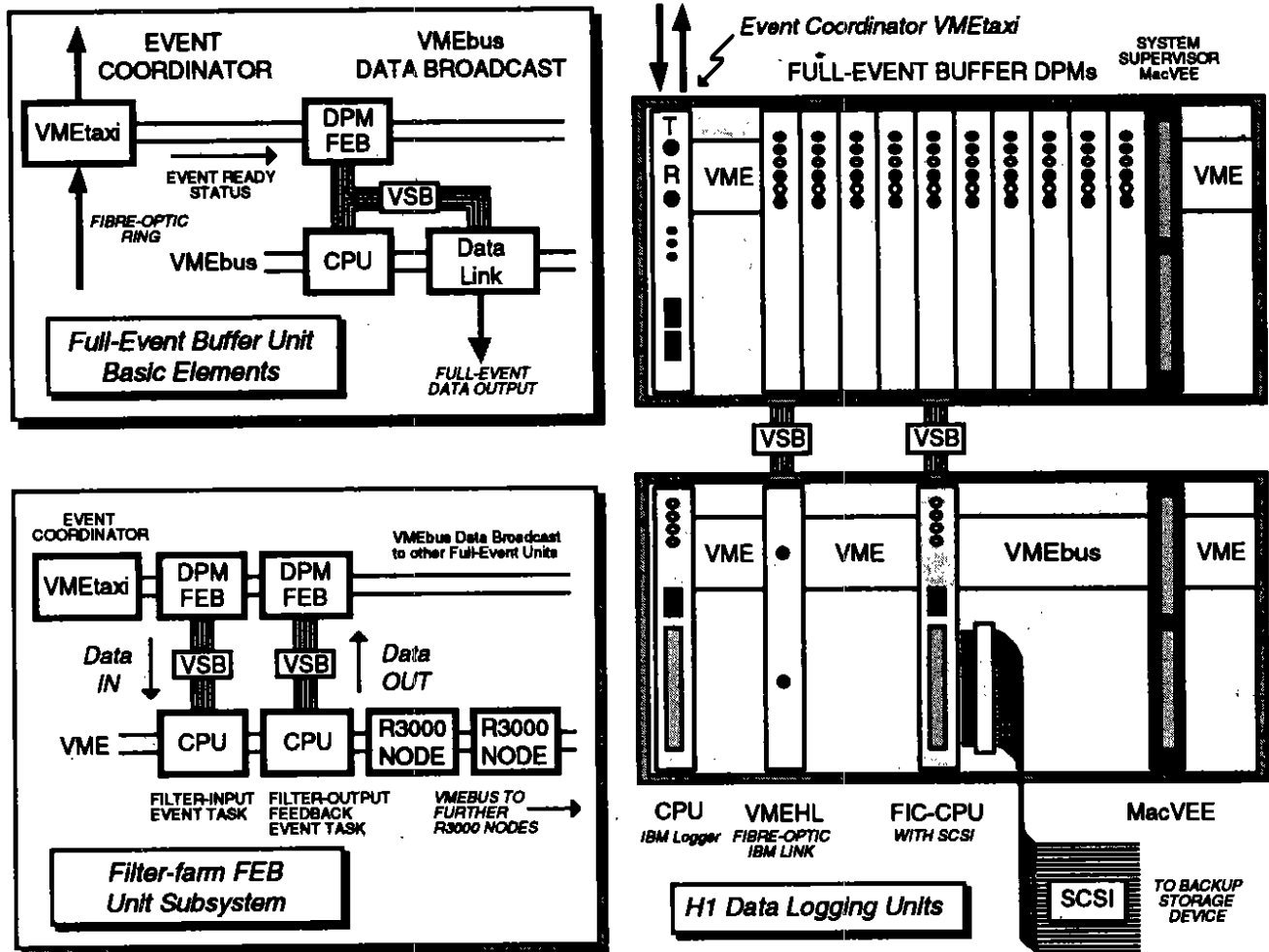
Figure 7 : Full-event buffer units

A more sophisticated form of unit is the fourth level filter "farm" consisting of many R3000 processor "nodes" working in parallel. Each node executes the same algorithm independently on different events. This provides not only a final level of triggering but a further stage of data processing and online reconstruction, as the event display of Figure 8 demonstrates [32]. Event records are passed to the different nodes under control of a filter input controller, which communicates with the Event Coordinator as a normal consumer full-event task. When a node is free it signals this to the filter input task which searches for an event ready in its full-event buffer. The data are then extracted over the VSB and sent to the free node, releasing that particular buffer and enabling a further node to be serviced. When a node has finished processing an event it signals completion to a filter output controller (a "feedback" event task). The latter then decides whether to pass the event back into the central system managed by the Event Coordinator and free the node for further processing. As a full-event unit, the parallel filter can be easily enabled or disabled. Furthermore, the software protocol of the Event Coordinator allows for several banks of filters to be implemented, each with their own input and output controllers. Currently the single Event Coordinator task can accommodate the handling of the filter-output due to the relatively low acceptance rates at Level-4; however, due to the modular architecture, additional processors can be readily introduced to share this task if required.

System supervision and operator-control

The H1 system is capable of running entirely in VMEbus; dedicated processors run dedicated tasks so that the net result is one of a conventional multi-tasking system. This leads to a natural division of tasks and processes. The primary tasks of data acquisition are performed by the subsystem readout controllers, event builders, filter control tasks and event units, all managed by the Event Coordinator. All fast processing and readout is done within VMEbus. An exhaustive software library caters for
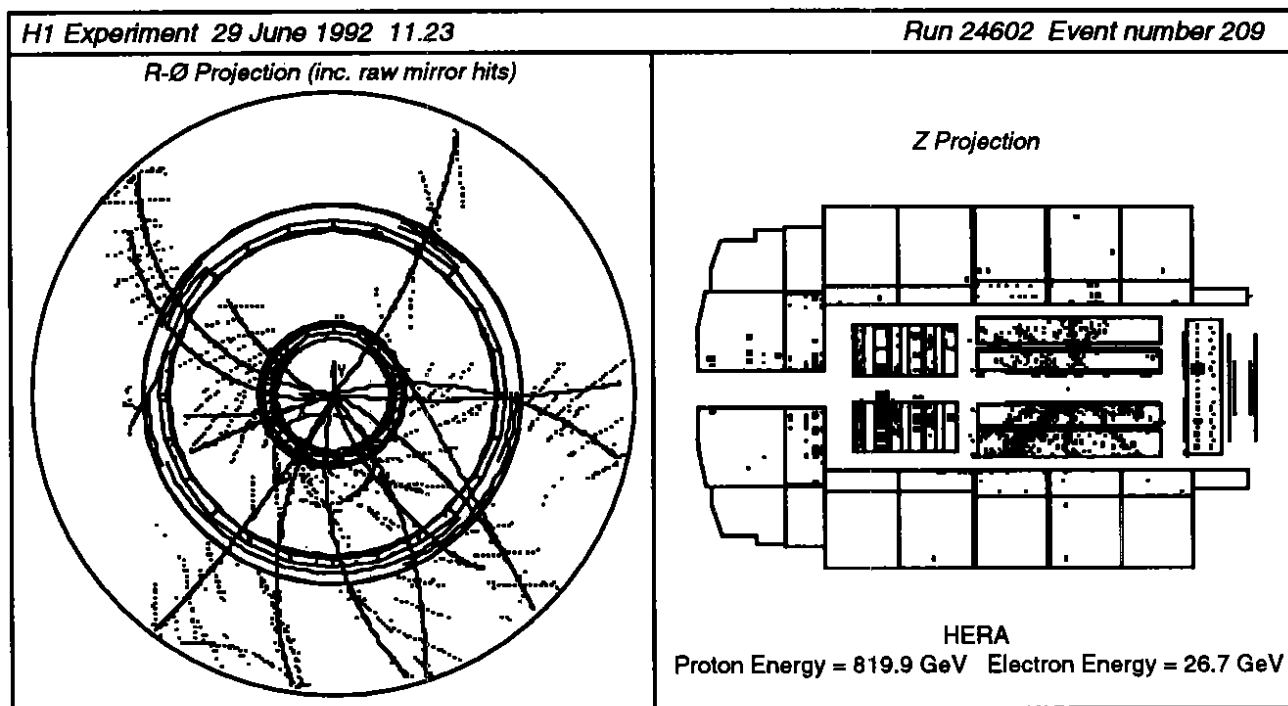
R-Ø Projection (inc. raw mirror hits)

Z Projection

HERA
Proton Energy = 819.9 GeV   Electron Energy = 26.7 GeV

Figure 8 : One of the first e-p deep inelastic events detected at HERA and reconstructed online at H1

external control by providing a full set of routines for system configuration, testing, system-status and monitoring [29]. NuBus-based Macintosh computers take over the responsibility of program development and run-time operator-control. The System Supervisor Mac [33] initialises the readout and checks the status of all elements by initiating VMEbus tasks such as the Event Coordinator. To provide a central focus of monitoring it also communicates with event tasks and subsystems either through VMEbus or over Ethernet. Additionally it serves the network with status information for external monitoring. The graphics-based philosophy of the Mac ensures that the operator is presented with, arguably, one of the most human-interactive interfaces, available today, to a complex real-time system.

OBSERVATIONS AND PERFORMANCE

The H1 data acquisition system was initially commissioned during cosmic-ray tests in Spring 1991 and then used to read out the complete detector during first HERA operation earlier this year. Its advanced preparation, and relatively stable operation, was in no small measure due to the choice of an open, industrial bus-standard and the incorporation of modern commercially-available hardware and software where suitable. Of particular note has been the extensive use of the networking facilities in addition to the main data flow. The ability to control and monitor the system externally, even from the latest generation of portable note-book computers, has been devoured by many users; indeed the first collisions from HERA were seen "live" on Macintosh event displays around Europe before they were preprocessed on the IBM mainframes. Also of note is the youthfulness of the individuals who have mastered the necessary technology in bringing the system to fruition.

From the master VMEtaxi the system can manage up to 32 branches and 16 full-event units, including the parallel filter farm, providing status information and accepting control command sequences from the System Supervisor Macintosh. Presently 60 Kbyte-sized events can be coordinated with 12 branches on H1 at rates greater than 50 Hz; with the Mark-2 VMEtaxi upgrades, 200 Hz will be surpassed. The primary sources of dead-time remain at the front-end, where future injections of greater processing and refined triggers are made more comfortable by working within an international bus standard.

CONCLUSION

The emphasis on modularity within modern large data acquisition systems is highlighted at H1. Systems have to be flexible and upgradable, with a degree of built-in autonomy, in a climate of advancing technology and increased data processing demands online. An open-bus standard, providing it can accommodate the bandwidths required, is a natural choice in the current evolutionary time-slot. However, as the architectural principles mature, it will be interesting to see how far microelectronic

techniques can be exploited and whether the role of future busses will be simply as enhanced networking facilities for the even wider dissemination of information in real-time.

ACKNOWLEDGEMENTS

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