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# An SDH-based Optical Transmission-System for Applications in the High-Energy Physics

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**Abstract :** We report on a concept of an optical transmission system with a baud rate of 2.488 Gbit/s that is based on the SDH-standard and complies with the severe requirements of High-Energy Physics-experiments. The smallest readout time per analog detector channel of 7.6 ns can be realized. A comparison with already realized concepts shows an improvement of the throughput capacity by a factor of at least 10. A novel parallel coding scheme and standardized interfaces guarantee a high flexibility and a simple development towards higher transmission capacities. The area and power requirements of the system are discussed for a suggested form of realization.

## 1 Introduction

The trend towards growing spatial resolutions in High-Energy Physics-experiments (HEP) has led to a number of up to 10 million analog detector channels, which have to be read out [1, 2]. To cope with these large amounts of data the optical data transmission is applied more and more often. In comparison to electrical transmission, an evident reduction of volume and mass of the system components can be achieved. The absorption of radiation can be reduced by almost one order of magnitude. In addition conventional, tight-packaged cable links have proved to be less reliable and less convenient in their handling. The optical transmission itself is characterized by lowest loss, lowest crosstalk and the smallest sensitivity against external influences.

During the last few years several concepts of optical transmission have been realized that use both the digital and analog transfer mode of optical transmission [1, 3, 4, 5, 6, 7]. The analog signal transmission is associated with a higher error rate due to a high sensitivity against level shifts of the optical signal and nonlinearities. These effects are mainly caused by changes of the operating temperature or radiation-induced damages of the transmitting devices. According to lower realizable sampling rates of analog transmission systems, only a smaller number of detector channels can be read out via one optical fiber [1, 6, 7]. Low throughput capacities can lead to an extremely large number of up to 120,000 modules, which are necessary to read out all detector channels of todays HEP-experiments [1, 6]. In correspondance the digital transfer mode is the most suitable form of transmission, in which the noise margin guarantees a high immunity against level shifts and high throughput capacities enable short readout times and large numbers of handled analog channels.

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In this work a concept of an optical transmission system with a baud rate of 2.488 Gbit/s is presented, which is based on the Synchronous Digital Hierarchy (SDH) standard [8]. The input channel number can be adjusted to the demands of a user-specific front-end electronic. In a suggested form of implementation more than 30,000 analog channels can be read out via one optical fiber, associated with the lowest readout time per analog channel in comparison to other transmission concepts. The suitability of the concept for applications between a front-end electronic close to a detector system and the external electronic will be shown. The low attenuation of todays optical fibers of about 0.2 dB/km also enables transmission distances of several kilometers. In the following chapter 2 the basic characteristics of the proposed concept are explained with respect to the SDH-standard and including comparisons with other concepts. In chapter 3 possible forms of realization are discussed including estimations of the area requirement and power dissipation.

## 2 System Concept

### 2.1 Basic Structure

The proposed transmission concept is based on the SDH-standard, which offers a maximum of flexibility concerning the adaption of the system to a user-specific application. The SDH is together with the Synchronous Optical Network (SONET) the first international standard for synchronous transmission systems and networks and has developed to the predominat standard of transmission also beyond the area of telecommunications (BISDN, ATM [9]). The high acceptance of the SDH-standard in industry has led to a large market of single SDH-based components which ensures a high independence of a single vendor. The ability of SDH-based networks to transport asynchronous data, for example of ATM-channels, ensures a high importance of these networks in the future. This demonstrates the high efficiency, flexibility and after all the lower cost, which can be achieved by an introduction of SDH-based optical links in the near future.

The SDH-standard has already been defined in 1989 by the International Telecommunication Union (ITU) [8]. Data, which is provided at the input ports of the transmission system, is arranged in packets, to which control bits are added for control and administration purposes (OAM). These control bits form the so-called Section Overhead (SOH). Its content is used to synchronize the receiver to the transmitter (control function) as well as for monitoring transmission errors by parity generation (administration functions). Both the data and control bits of a packet form a basic frame (Synchronous Transport Module, STM-1). The ratio of the control bits to the entire frame is set to 1/30. The frame building and synchronization process takes place independently of the input data and its format. This results in a good suitability for applications, in which data packets of varying repetition rates have to be transmitted. Higher transmission rates can be realized by time-domain multiplexing steps. By this 16 STM-1 frames can be combined to a single STM-16 frame with a data rate of 2.488 Gbit/s.

The results of industrial research groups show a steady improvement of the performance of optoelectronic devices. Array-based multichannel modules will be also of growing interest in the near future. High throughputs of up to 3.5 Gbit/s per channel [10], high total throughputs and high parallelism of 25 Gbit/s [11] and of 32 parallel channels [12] have been realized, respectively. The threshold currents of laser diode arrays have been reduced down to 2.1 mA [13]. The largest transmission distances exceed 400 meters [14]. Component bit-error rates as low

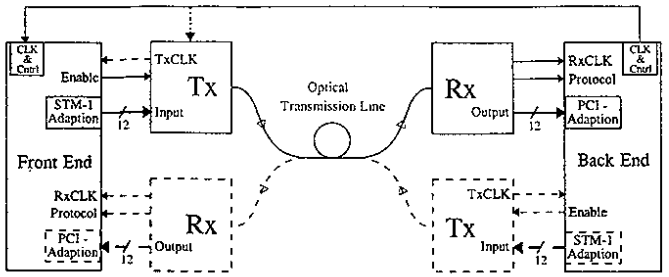



Fig. 1 : Simplified block diagram of the proposed transmission system. An extension in form of an additional Tx-Rx-pair enables a full-duplex transmission (dashed lines).

as $10^{-20}$ [14] have been demonstrated as well as minimum and maximum operating temperatures of −40°C and 100°C [11, 12], respectively.

Fig. 1 shows the core of the proposed transmission system, which is formed by the transmitter Tx and the receiver Rx. The Tx input port and the Rx output port contain 12 parallel and synchronous data inputs and outputs, respectively. Incoming data is organized in packets according to the SDH-standard and is transmitted with a data rate of 2.488 Gbit/s over a serial, optical transmission line. Inside the receiver the serial data is reconverted into the original 12 bit wide, parallel data channels. Afterwards a transmission protocol is generated, which contains for example information about transmission errors. An efficient coding process offers the possibility to use a selectable number of the 12 parallel and synchronous input channels. A multiplexing stage in front of the input port allows an adaption of the application-specific input-data rate and the number of input channels to STM-1 format. Further on it is possible to use only every n-th interface clock-period to write data into the transmitter, which reduces the data rate in integer steps. This corresponds to the STM-1-Adaption in Fig. 1. On the receiver side a conversion of the transmitted data into PCI-format (Peripheral Component Interconnect) is suggested (PCI-Adaption). The PCI-bus, which has evolved into a standard industrial data bus, handles in future expansions data throughputs of up to 528 Mbytes/s (64 bit wide, 66 MHz clock rate) [15]. It enables a high speed, standard data interface between the receiver, which can be realized as a PCI Mezzanine Card (PMC), and a VME-motherboard for a fast storage or digital processing of the transmitted data.

To synchronize the transmission system to a front-end electronic the transmitter provides a defined interface clock of 150.336 MHz (master function), which is generated by a quarz oscillator. The receiver recovers the transmission clock out of the serial data stream and works correspondingly as a slave and synchronously to the transmitter. The clock signal RxCLK can be used for a further clock-synchronous controlling (CLK & Cntrl), e.g. for the front-end electronic. It should be



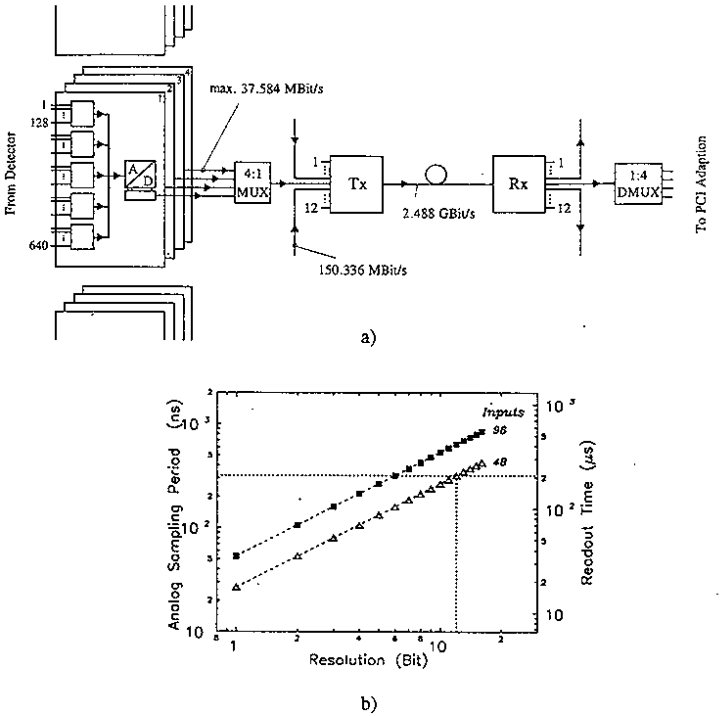



Fig. 2 : Block diagram of a 30,720 detector channel transmitter system (a) and dependency of the readout time and sampling period on A/D-resolution and grade of multiplexing (b).

mentioned that the source clock for the transmitter can also be provided externally.

## 2.2 Applications in HEP-Experiments

In HEP-experiments high demands are made on short-distance transmission systems for a use close to the detector. The most important requirements are small readout time, low power dissipation as well as a high reliability and lifetime (e.g. [16]) which will be discussed in the following. To estimate the achievable readout time we assume modules containing five integrated circuits (ICs), which handle 128 analog detector channels each. This is a typical configuration for todays HEP-experiments (e.g. [3]). As shown in Fig. 2a these 5 front-end chips can be connected in a way that the 640 analog channels of one module are read out sequentially. The analog signals of each module are digitized by an A/D-converter and converted into a serial digital bit stream using a shift register. In this suggested form of implementation twelve multiplexers (4:1 MUX) form the interface to the transmitter Tx. Each of these multiplexers adapts the digital data

| | H1 | CMS / RD23 | L3 | CDF | This Work | Units |
|---|---|---|---|---|---|---|
| **Transfer Mode** | analog | | digital | | | |
| **per Fiber :** | | | | | | |
| Analog Channel Number | 1,280 | 128 | 154 | 2,560 | **30,720** | |
| Data Rate | 0.002 | 0.04 | 0.01 | 1 | **1.804** | Gbit/s |
| Readout Time | 640 | 3.2 | 3,900 | 50 | **232** | $\mu$s |
| A/D resolution | 12 | 8 | 8 | 8 | **12** | bit |
| **per Analog Channel :** | | | | | | |
| Readout Time | 500 | 25 | 25,325 | 19 | **7.6** | ns |
| Power Dissipation | 40 | 500 | 1,500 | 2,480 | **820** | $\mu$W |
| **Analog Channel Number** | 210,000 | 10,000,000 | 74,000 | 260,000 | | |

Table I : Optoelectronic front-end transmitter modules for the optical readout of Silicon Strip-Detectors of the experiments H1 (HERA) [7], CMS/RD23 (LHC) [1], L3 (LEP) [4], and CDF (Tevatron) [3] and this concept.

of four modules to the STM-1 data rate of 150.336 Mbit/s. In this way 30,720 detector channels can be read out via one optical fiber. Fig. 2b describes the dependency of the readout time and sampling at each interface-clock period on the resolution of the A/D-conversion and the grade of multiplexing. The dotted lines mark an example of a 12-bit resolution yielding in a readout time and sampling period of 204 $\mu$s and 302 ns, respectively. Using 8:1 multiplexers at the transmitter inputs, the throughput capacity can be enhanced to 61,440 analog detector channels. The readout time $T_r$ in $\mu$s can be calculated by

$$T_r = M_{Mux}\, N_{A/D}\, n_{FE}\, \frac{128}{150.336}$$

with $M_{Mux}$ as the grade of multiplexing, $N_{A/D}$ as the resolution of the A/D-conversion and $n_{FE}$ as the number of front-end chips per A/D-converter. Assuming an 8-bit resolution [1], the readout of one front-end chip per A/D-converter without multiplexer stage yields in a readout time of 6.8 $\mu$s. Smaller values can also be obtained without a serialization subsequent to the A/D-conversion. A propagation delay of about 28 $\mu$s, which results from a run-time through the transmission system, has to be added to the calculated readout time. The corresponding values of the other concepts of Table I have not been considered.

The reliability of an optical data transfer is characterized by the systems Bit Error Rate (BER). Typical values of about $10^{-14}$ can be achieved for todays systems [16]. The lifetime of the optoelectronic components determines the lifetime of the transmission system. Todays laser diodes show at operating temperatures of 60°C a Mean-Time-To-Failure (MTTF) of 13 years. Another important aspect concerns the operation in a radiation environment. Close to the point of beam interaction in proton storage rings dose rates of 10 Mrad and neutron radiation levels of up to $2\text{x}10^{14}$ n/cm$^2$ during 10 years are expected [1]. Laser diodes operating in the near infrared show the lowest sensitivity against $\gamma$-irradiation [17]. Regarding an exposure to neutron irradiation, the components of the interesting InGaAsP-material system show the highest resistivity against fluxes up to $10^{14}$ n/(cm$^2$) [17, 18]. Therefore a high reliability and lifetime can be expected for applications inside the detector and close to the beam pipe.

Table I summarizes the characteristics of the proposed concept for the implementation shown in Fig. 2a in comparison to already realized transmission systems in HEP-experiments. The readout capacity of 30,720 analog channels per optical fiber is an improvement by a factor of about 10 compared to CDF. The readout capacity can be further enhanced by integer multiples of 30,720, if the data of several transmitter modules is transmitted via the same optical fiber, using the wavelength-division multiplexing technique [19]. The readout time per analog channel, presented in Table I, describes the achievable performance of a transmission concept. It is calculated from the quotient of readout time (232 $\mu$s for the proposed concept) and the number of analog channels, which are read out via one optical fiber (30,720 for this concept). The best value of 7.6 ns for a 12-bit resolution can be achieved with the proposed concept, which is an improvement by a factor of about 2.5 compared to the concept of CDF, using an 8-bit resolution. A considerably lower power dissipation per analog channel can be realized in comparison to the other concepts, which use the digital transfer mode at lower data rates. Regarding the power dissipation the complete transmitter has been taken into account, but it has to be kept in mind that in the concepts of CDF, CMS/RD23 and the proposed concept only a part of the total power is dissipated close to the detector. This value and the achievable data rate of our concept is explained in detail in the following chapter.



# 3 Realization

## 3.1 Functional Blocks

Fig. 3 explains the subdivision of the transmitter and receiver stages into three functional blocks each. Inside the STM-1 Frame Building block of the transmitter the data is converted into 12 parallel STM-1 frames. Subsequent to the Scrambling process (line coding), which also expands the 12 parallel data channels into 16 channels, the parallel data is serialized in a two-stage multiplex-process and transmitted via one optical transmission line to the receiver. At the receiver side (Fig. 3b) the data is demultiplexed and a synchronization to the transmitter reference clock takes place. Afterwards the data of 16 data channels is decoded and converted into the original form of 12 parallel data channels (Descrambling). Finally the control bits of the frames are evaluated, a transmission protocol is generated and the data is given out in its origin form together with the transmission protocol to a back-end electronic (Ouput FIFO).

### *STM-1 Building Block*

As shown in Fig. 4 an adaption of the data to the STM-1-frame format takes place at each of the 12 data inputs. In order to insert the SOH-Bytes of a STM-1 frame to a continous bitstream, a dynamic input FIFO is used, consisting of the two shift registers SR1 and SR2. The data, which is provided at one of the 12 data inputs, is written with a data rate of 150.336 Mbit/s into the SR1. Once the SR1 is filled, its content is written in a parallel way into the SR2. At the same time the 9 SOH-Bytes are written out of the SOH-register (SOH-R) into a third shift register SR3. Now a complete column of a STM-1 frame is stored in the SR2 and SR3. The readout of the last-mentioned shift registers is carried out with the slightly higher STM-1 data rate of 155.52 Mbit/s. By this the SOH-Bytes can be inserted into the continous bitstream at the input port.

The parity generation is realized by the shift registers SR4 and SR5 by a modulo-2 addition previous and subsequent to the coding process, respectively [8]. The first 9 SOH-Bytes (A1, A2 and C1, 3 times each) of a frame, which are used for the synchronization of the transmission system, have to

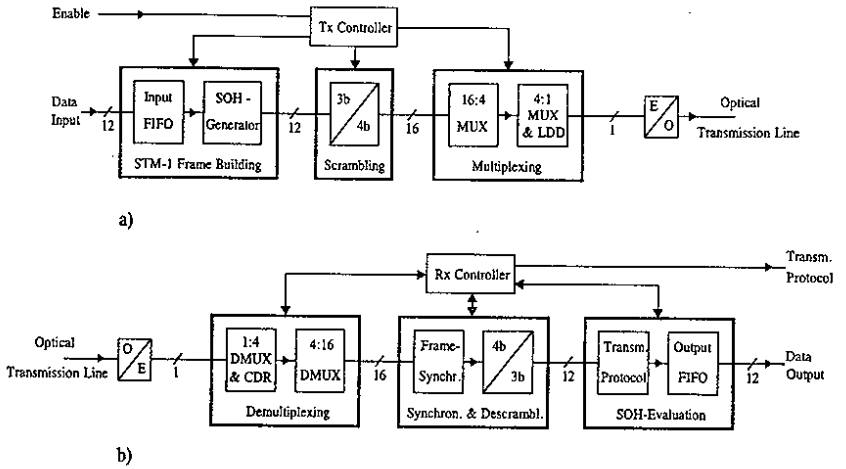



Fig. 3 : Block diagram of the transmitter Tx (a) and the receiver Rx (b).

be transmitted without coding. Therefore they are provided in front of the multiplexing stage via a selector (Sel) by a static memory (ROM).

*Control Unit*

The tasks of the control unit are mainly to control the data handling between the functional blocks inside the transmitter and receiver. If no data is provided at the input port, the synchronization of the transmission system is maintained by a continous generation of frames. In this case, the data section is filled by the control unit with data of no specific contents (Idle Cells). A Phase-Locked Loop (PLL) inside the Tx Controller Block is used to synchronize the transmitter stage to an externally generated 155.52 MHz reference clock, as well as for a synthesis of a 150.336 MHz clock signal of the first shift register stage SR1 and all related clocks of the transmitter and receiver stages.

*Scrambler*

The scrambler is used to generate a binary data stream on the serial transmission line with a maximum of clock information. That means that the number of consecutive data bits with the same logic state has to be as small as possible and independent on the input data format. Longer bit sequences without a transition (NRZ-data pattern) complicate the clock and data recovery at the receiver side and can lead to a loss of synchronization. Unstable sampling rates also cause varying duty cycles and operating temperatures of the driven laser diode. So the efficiency of the scrambler directly influences



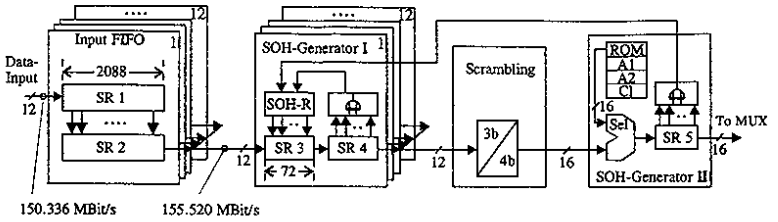



Fig. 4 : Data processing inside the transmitter Tx.

the BER of a transmission system and has to be considered as a key component. A scrambler can principally be placed into the serial or the parallel data stream. A serial implementation is at data rates of a few Gbit/s associated with an obviously higher power dissipation and component cost. For this concept a parallel implementation offers a reduced clock rate of 155.52 MHz for the scrambler components, which enables a reduced power dissipation at the same time [20]. A novel parallel scrambler has been developed, which generates 4-baud words out of 3-bit input-sequences as shown in Table II.

| 3b-input | 4b-output |
|---|---|
| 000 | 0101 |
| 001 | 0110 |
| 010 | 0011 |
| 011 | 1100 |
| 100 | 1001 |
| 101 | 0010 |
| 110 | 1101 |
| 111 | 1010 |

Table II : 3b/4b-coding scheme for data scrambling.

Table II shows all valid 4-baud words, which can be generated by the $2^3$ input combinations. Eight 4-baud words remain as invalid words, because no corresponding 3-bit word exists. If a 4-baud word of Table II is altered during the transmission by noise or jitter into an invalid baud word, this transmission error will be detected at the receiver and written into the transmission protocol. Besides this error detection some of the 4-baud words can be used as idle or synchronization cells. The effective data rate results finally in 1.804 Gbit/s, as shown in Fig. 5.

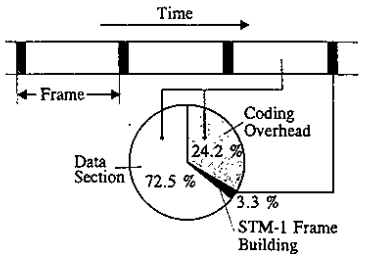
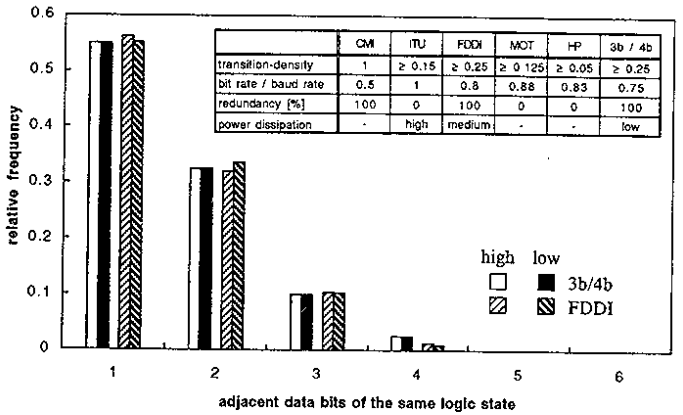



Fig. 5 : Composition of a transmitted frame on the optical, serial transmission line.

The baud rate of 2.488 Gbit/s on the serial, optical transmission line is reduced by the STM-1 Frame Building Process (3.3 %) and the 3b/4b-coding (24.2 %). This coding scheme guarantees that a maximum of only 4 consecutive data bits of the same logic




| | CMI | ITU | FDDI | MOT | HP | 3b / 4b |
|---|---|---|---|---|---|---|
| transition-density | 1 | ≥ 0.15 | ≥ 0.25 | ≥ 0.125 | ≥ 0.05 | ≥ 0.25 |
| bit rate / baud rate | 0.5 | 1 | 0.8 | 0.88 | 0.83 | 0.75 |
| redundancy [%] | 100 | 0 | 100 | 0 | 0 | 100 |
| power dissipation | - | high | medium | - | - | low |

Fig. 6 : Simulation results of the coding efficiency of the parallel 3b/4b coder and an FDDI coder (4b/5b and NRZ/NRZI coding). The corresponding values of the well known CMI (Coded Mark Inversion), ITU and FDDI standards as well as the characteristic values of the commercial available Spanceiver$^{TM}$ (MOT) and HP1000 (HP) are also shown.

state are transmitted over the optical transmission line. Fig. 6 presents the results of logic simulations of the 3b/4b-coding characteristics for all possible $2^{12}$-input combinations (four parallel 3b/4b-coders) in comparison to the FDDI-coding scheme. In contrast to the FDDI coding [21] the same number of logic high and low states is generated for all possible adjacent bit sequences. From Fig. 6 can also be seen that more than 87 percent of the possible input combinations show not more than two consecutive data bits of the same logic state. The reciprocal maximum value results in the so-called minimum transition density of 0.25, which is compared to other standard coding schemes in the table of Fig. 6. Using CMI or Manchester coding, an ideal transition density of 1 can be achieved, though at the cost of a very low effective data rate. Commercially available modules of Motorola and Hewlett Packard [22] include a smaller reduction of the effective data rate, but generate at the same time bit streams of a considerable lower transition density, as it is for the ITU-coding scheme. The parallel implementation of the FDDI-coding scheme offers the same high transition density but is in comparison to the 3b/4b-coding scheme associated with a higher complexity and power dissipation. The disparity, which is the characteristic value for the DC balance of a transmitted bit sequence, was estimated for both coding schemes for a finite quantity of pseudo-random input data. The use of the parallel 3b/4b-coding scheme leads to a disparity of about 200, which is also slightly better than for the FDDI-coding scheme. A low disparity is especially important for the most popular AC-coupled receiver circuits and is not taken into account of the mentioned commercial module of Motorola. The



choice of the 4-baud words of the 3b/4b-coding scheme ensures that in average the same number of logic ones and logic zeros are transmitted, by which a nearly constant average value of the transmitted bit sequence is guaranteed.

*Synchronization*

The synchronization of the receiver is build up in two stages, the bit and frame synchronization. The bit synchronization is established inside the receiver by extracting the clock out of the incoming bit stream and a subsequent clock and data recovery. This is enabled by a commercial component [23], which synchronizes an internal PLL to the extracted clock. The duration of the synchronization process depends on the transition density in the bit stream. In a following frame synchronization the receiver is synchronized to the arriving STM-frames. The frame synchronization is implemented in a parallel way next to the 1:16-demultiplexing stage (cf. Fig. 3). At first the original order of the data channels has to be reproduced. That means that the 16 data channels next to the demultiplexing stage of the receiver must have the same order as before the multiplexing stage of the transmitter. For this purpose the incoming data is searched for the so-called frame-start pattern, the bytes A1 and A2, which are positioned in the first column of the SOH of each frame. If A1 does not arrive in the correct order, the 16 data channels are rotated by a certain number of positions, until the same order as at the transmitter is reproduced. All following data is rotated inside the frame synchronizer (cf. Fig. 3) as often as it had been necessary to reproduce the correct order of the data channels. The transition in the bit stream from the last incoming byte A1 to the first incoming byte A2 defines the beginning of the data section and the position of the SOH in the arriving STM-frame for the receiver electronic.

### 3.2 System Integration

The interface to the transmission system has to be adapted according to the requirements of a front-end electronic. As we described in chapter 2.2 a form of realization is explained here exemplary, including twelve 4:1-multiplexers at the data inputs of the transmission module. Due to the moderate data rate of about 38 Mbit/s at the 48 inputs of these multiplexers, the data transmission between the front-end electronic and the transmitter can be realized optically or electrically. For this concept an optical transmission is prefered in order to use the typical advantages of optical transmission like galvanic separation and low sensibility against external influences. An optical implementation results in a power of 470$\mu$W per analog channel dissipated close to the front-end electronics, which is mainly caused by high threshold currents of commercial laser diodes of about 10 mA.

The transmitter module mainly contains the 48 receiver circuits of the transmission systems from the front end, the transmitter logic (cf. Fig. 3), a 4:1-multiplexer with laser driver circuit (LDD) [23] and a laser diode for the STM-16 data rate. The receiver circuits consist of a PIN diode and a preamplifier each. All components of the transmitter will be placed on a single board. Most of the transmitter logic will be realized in the form of a MCM (Multi Chip Module). In comparison to the use of single, housed components, the needed area can be reduced considerably and the reliability can be improved because of smaller propagation delays between the components. A survey of the area and power requirements of the transmitter components is presented in Table III. In the first part, the essential components of the transmitter logic, which could be integrated in a MCM, are considered. The use of a 0.8-$\mu$m CMOS process for the realization of the Tx-Controller results in an IC with an area of 6.3 x 6.3 mm$^2$,

| | Number | Component | Area in $mm^2$ | Power Dissipation in W |
|---|---|---|---|---|
| Tx | 1 | Tx Logic | 40 | 5.5 |
| | 4 | 4:1 MUX | 16 | 1.2 |
| | 1 | 4:1 MUX + LDD | 160 | 1.9 |
| | 1 | Laser Diode | 400 | 0.1 |
| | 48 | PIN-Diode + Amplifier | 6000 | 1.4 |
| | 1 | Periphery | 400 | 0.5 |
| Front End | 48 | LDD + Laser Diode | 400 | 14.4 |

Table III : Power and area requirement of the transmitter components.

an I/O-number of about 110 and a power dissipation of 5.5 W. By a transfer to a 0.6-$\mu$m CMOS process and a supply voltage of 3.3 V instead of 5 V, a reduction of the power dissipation by a factor of 2 can be achieved. The 4:1 multiplexer is realized in a 0.8-$\mu$m BiCMOS process, because of the higher data rate of 622 Mbit/s. In this form the power dissipation per analog channel results for the entire transmitter in 820$\mu$W (cf. Table I, Table III). The transmitter board will have an area of about 11 x 13 $cm^2$. The area requirement however can be further reduced using receiver circuits in the form of arrays, for example placed on a silicon waferboard with V-grooves for a fiber-to-PIN-diode coupling [24, 25]. By this the area requirements of the transmitter board could be further reduced by a factor of about 2.

At the receiver side of the transmission system it is necessary to evaluate the transmitted data as fast as possible. In correspondance the receiver can be realized on a double PMC-board with a size of 15 x 15 $cm^2$. The PCI-bus represents in its first, already commercially available expansion with a throughput of up to 264 Mbyte/s (64 bit parallel, up to 33 MHz each) a fast output interface of the transmission system [15]. The use of a PCI-bus additionally offers the possibility to adapt the transmitted data by commercial components to ATM-format, which enables the use of the high flexibility of ATM [26].

## 4 Conclusion

We have proposed a concept of an optical transmission system, which is based on the SDH-standard and transmits data with a baud rate of 2.488 Gbit/s. 12 parallel data channels form the interface to the transmission system. A high flexibility of the interfaces offers the possibility to adapt the number and data rate of the 12 data channels to a user-specific front-end and back-end electronic, respectively. The efficiency of the developed 3b/4b-coding scheme allows data of any format to be provided at the data inputs of the transmitter. The achievable characteristics of the transmission system have been discussed with respect to the severe requirements towards readout systems in HEP-experiments. A detailed comparison with already realized transmission systems in HEP-experiments shows an improvement concerning reliability, transmission capacity and development towards higher transmission capacities. The best readout time per analog detector channel of 7.6 ns can be achieved. In an exemplary described form of realization, using twelve 4:1-multiplexers at the input port of the transmitter, the high number of 30,720 analog detector channels can be handled, resulting in the short readout time of about 232 $\mu$s. In a conventional form of



realization the area requirement of the transmitter module results in 11 x 13 $cm^2$, which can be reduced by a factor of 2, when components in array form are used.

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