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The Pipelined Readout for the ZEUS Calorimeter

by

Luis Hervás

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UNIVERSIDAD AUTÓNOMA DE MADRID

Facultad de Ciencias

Departamento de Física Teórica

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Chapter 1

Introduction

A long way has been covered in the understanding of the constituents of matter since the beginning of this century. Probably even longer is the road left behind by the instrumentation methods for the experiments which made that understanding possible.

Which of the two topics favoured the progress of the other is a difficult question to answer. The record shows us that both sciences fed each other as they kept growing.

Recent years have seen the construction of larger and larger High Energy Physics experiments at bigger and bigger accelerating facilities. These experimental efforts and parallel theoretical developments have produced a model, usually called the *standard model*, which explains which are the building blocks making up matter and how forces act upon them.

Even if the model covers successfully most of the empirical data, some 'open questions' remain, many of the predictions the model makes have yet to be tested and the majority of parameters of the theoretical construction need to be measured more accurately.

Answers to some of these open questions can only be given by measurements performed on particle interactions at very high energies. An extraordinary precision in the measurements is also necessary.

One way to get insight into the structure of matter is to collide leptons with quarks and quantify the collision products. This has been done in the last decades by accelerating leptons and striking with them the quarks of nucleons in fixed target experiments.

Such collisions, but at much higher energies, will soon be possible in a machine which is being completed at DESY in Hamburg. At HERA (Hadron Electron Ring Anlage), the name of the storage ring complex, collisions are achieved by accelerating protons and electrons (or positrons) and allowing them to collide. It is the first lepton-quark collider to be built. The open questions which will be illuminated by experimentation at HERA will be discussed in the next chapter.

HERA represents a demanding environment for both accelerator and experimental techniques. Some of these challenges are listed below :

- The use of superconducting magnets in the proton ring or the collisions between a "warm" electron beam and a "cold" proton beam are part of the progress in accelerator technology.
- A big challenge of HERA, for both the acceleration and detection techniques, is the use of a multibunch operation (200 bunches in each ring) such that beams collide every 96 *nanoseconds* in order to reach high luminosity and produce acceptable rates for rare processes.
- As for the experimental techniques, a moving center of mass of the collision due to the large momentum difference between the colliding particles requires an asymmetric experiment setup around the interaction points.
- The submicrosecond bunch crossing time is certainly a further challenge to instrumentation. For the first time an experiment has to measure an enormous amount of data every fraction of a microsecond. Novel concepts have to be developed in order to cope with this measuring rate. The measurement signals have to be stored at the collision frequency. Data reduction based on a quick analysis searching for physics events is necessary and only interesting candidates will be recovered from the storage for further analysis.

This thesis is devoted to describing the experimental readout techniques being developed for use in the high resolution calorimeter detector of the ZEUS experiment at HERA. A description of the ZEUS calorimeter and the functioning principles of this type of detectors are shown in chapter 3. Chapter 4 describes the concept for the readout of the ZEUS calorimeter. The solution to perform the storage of signals in an analog way needs some new and outstanding electronic components. The requirements and how they have been built, is the subject of chapter 5. Chapter 6 covers the testing of these devices. The whole readout implementation for the ZEUS calorimeter is described in detail in chapter 7. This system has been used to measure the behaviour of the calorimeter modules in a beam calibration experiment. In chapter 8 results are presented showing the performance of the modules making up the ZEUS calorimeter obtained at the beam calibration experiment using the concepts and the readout electronics which will be used to readout ZEUS at HERA. Finally some features and solutions for the next steps in the instrumentation road will be anticipated in appendix A.

Ahead of us lies the hope that the instrumentation effort will enhance and sharpen our perception of nature.

Chapter 2

ZEUS at HERA: Machine, Physics and Experiments

The ZEUS collaboration has proposed the construction of one of the two detectors for the HERA storage ring at DESY in Hamburg (FRG). Another collaboration builds and operates the H1 experiment.

2.1 The HERA Collider

HERA is the $e-p$ collider now under construction at DESY, Hamburg. It will provide collisions between $30\,GeV$ electrons (or positrons) and $820\,GeV$ protons and is expected to become operational by mid 1991. The photograph in figure 2.1 shows a bird's eye view of HERA in its location, Bahrenfeld in the city of Hamburg. The layout of HERA together with the beam acceleration and injection systems is shown in figure 2.2. The most important machine parameters are listed in Table 2.1.

The machine is constructed in a tunnel which is between 15 and $20\,m$ deep underground. In the tunnel separate magnet systems guide the electron and the proton beams around the $6.3\,km$ long ring. A cross section of the tunnel is shown in figure 2.3.

The injection system is based on existing facilities DESY and PETRA. A newly constructed LINAC accelerates H^+ ions to $50\,MeV$, these are brought to $7.5\,GeV$ by DESY III, to $40\,GeV$ by PETRA and then injected into HERA. Electrons go from a LINAC (50 - $400\,MeV$) to DESY II ($9\,GeV$) and PETRA ($14\,GeV$), from where they are injected into HERA.

For $30\,GeV$ electrons in the HERA tunnel a bending field of $0.165\,T$ is required. It can be achieved by conventional magnets. In contrast, a bending field of $5.65\,T$ is required to keep $820\,GeV$ protons on their orbit at HERA. At these fields iron cannot be used for magnetic field shaping and the field homogeneity has to be achieved by shaping superconducting coils to obtain a current density following a $cos\phi$ distribution. The use of superconducting magnets reduces the power consumption of HERA.

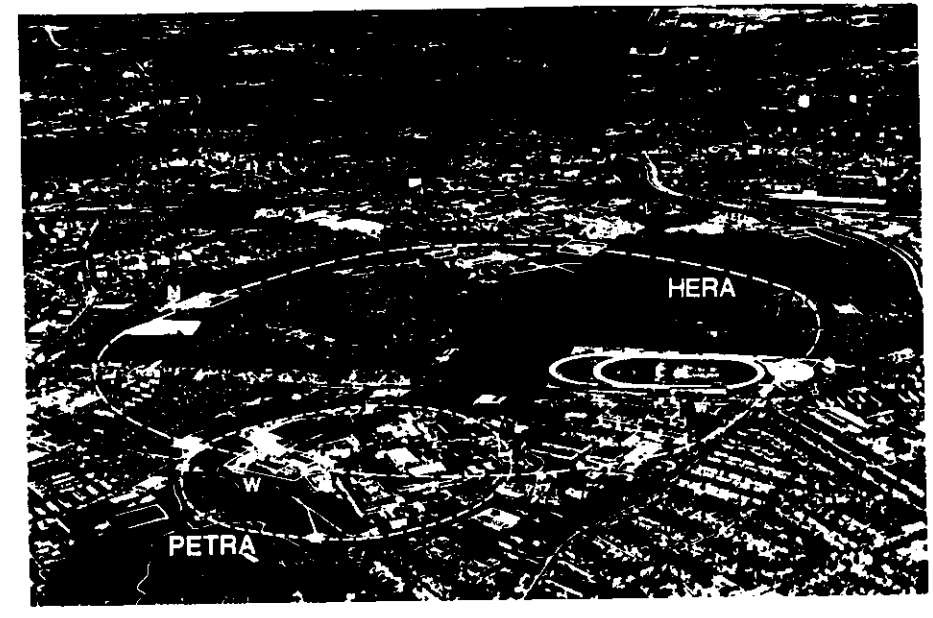


Figure 2.1: *Aerial photograph of HERA in its location, Bahrenfeld in the city of Hamburg.*

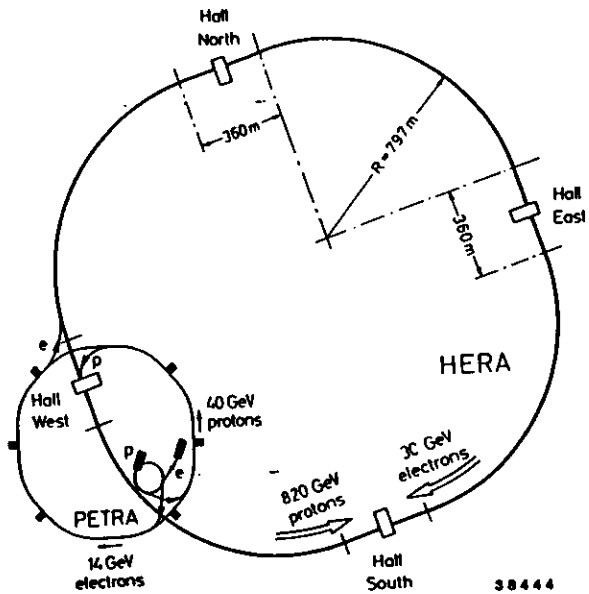


Figure 2.2: *The HERA storage ring at DESY. The beam acceleration and injection facilities as well as the location for the experiments can be seen.*

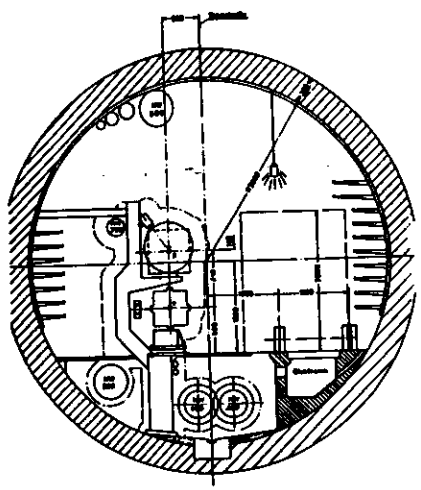


Figure 2.3: *Cross section of the HERA tunnel. The proton ring is located above the electron ring. Also shown are the supply lines for He and cooling water.*

Parameter	proton ring		electron ring	units
Nominal energy	820		30	*GeV*
c.m. energy		314		*GeV*
Q^2_{max}		98400		$(GeV/c)^2$
Luminosity		$1.5 \cdot 10^{31}$		$cm^{-2}s^{-1}$
Polarisation time			28	*min.*
Number of interaction points		4		
Crossing angle		0		*mrad*
Free space for experiments		± 5.5		*m*
Circumference		6336		*m*
Length of straight sections		360		*m*
Bending radius	588		608	*m*
Magnetic field	4.65		0.165	*T*
Energy range	300–820		10–33	*GeV*
Injection energy	40		14	*GeV*
Circulating currents	160		58	*mA*
Total number of particles	$2.1 \cdot 10^{13}$		$0.8 \cdot 10^{13}$	
Number of bunches		200		
Number of buckets		220		
Time between crossings		96		*ns*
Emittancy (ϵ_x/ϵ_y)	0.71/0.71		3.4/0.7	10^{-6} m
Beta function (β^*_x/β^*_y)	10/1.0		2/0.7	*m*
Beam tune shift (Q_x/Q_y)	0.0026/0.0014		0.023/0.026	
Beam size at crossing σ^*_x	0.27		0.26	*mm*
Beam size at crossing σ^*_y	0.08		0.07	*mm*
Beam size at crossing σ^*_z	11		0.8	*cm*
Energy loss per turn	$1.4 \cdot 10^{-10}$		127	*MeV*
Critical energy	10^{-6}		111	*keV*
Max. circumf. voltage	0.2/2.4		260	*MV*
Total RF power	1		13.2	*MW*
RF frequency	52.033/208.13		499.667	*MHz*
Filling time	20		15	*min.*

Table 2.1: *Parameters of the HERA collider.*

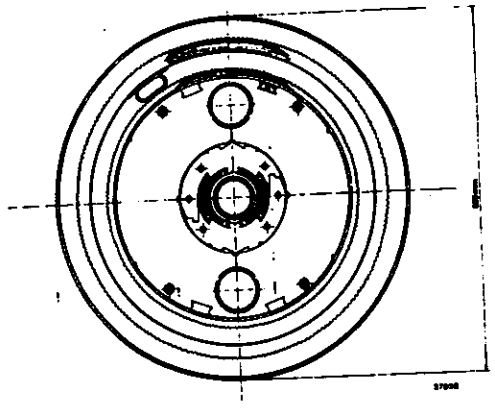


Figure 2.4: *Section through a HERA superconducting dipole. It illustrates the superconducting coils surrounding the beam pipe and how the coils are clamped by aluminum collars which in turn are reinforced by the cold iron yoke contained in a cryostat with superinsulation.*

The design of the HERA magnets profitted from the pioneering work at FNAL[1] and lead to a novel concept. Figure 2.4 shows a section through a superconducting dipole.

The energy lost by the electron beam due to synchrotron radiation is restored by RF cavities which are traversed by the beam. The frequency for the RF system at HERA (see Table 2.1) is the same as that used in DESY and PETRA, namely $500\,MHz$. For electron beams below $30\,GeV$, HERA will be equipped with cavities previously used at PETRA. Above $30\,GeV$ superconducting RF cavities must be used. Note that beam polarization time for electrons at $35\,GeV$ is 12 min compared to 43 min at $27\,GeV$, running at high energies is therefore desirable since possible electron polarization will be an important additional experimental tool at HERA.

The energy loss of the proton beam due to synchrotron radiation is negligible. Conventional cavities and klystrons have been developed. The frequency of the RF system will vary between $52\,MHz$ at injection to $208\,MHz$ at $820\,GeV$. Actually the magnet tests have shown that bending fields above $5.65\,T$ can be achieved so that it will be possible to reach $1\,TeV$ proton energies.

The electron and proton beams running in different vacuum pipes come together at four points in the HERA tunnel. The collisions are performed head on (zero degrees crossing) which forces the introduction of additional quadrupoles very near the experiments to deflect the last angle. This trajectory change of the electron beam generates a large amount of synchrotron radiation surrounding the interaction points against which the experiments have to be shielded.

[1] Fermi National Accelerator Laboratory.

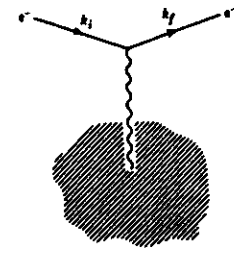


Figure 2.5: *Electron scattering by a charge cloud is a way to explore the structure of the cloud.*

To obtain the desired luminosity of $\sim 1.5 \cdot 10^{31}\,cm^{-2}sec^{-1}$ the beams, at HERA, have to be multiple bunched since the number of particles which can be stored together in a beam bunch is limited by the beam-beam tune shifts and is $\sim \mathcal{O}(10^{13})$. The number of bunches is also limited by the size of the ring so that their length does not occupy more than 30% of the bucket length in which case the RF-noise leads to a loss of the beam [1]. Both electron and proton beams are bunched. It is planned to have 220 equidistant buckets per beam out of which 200 will be filled with particle bunches. The remaining twenty buckets will be used by the experimental and accelerator groups for background studies. Four intersecting points are foreseen in HERA and experimental halls have been built surrounding two of them. The North Hall will house the H1 detector and the South Hall the ZEUS experiment. Interesting reactions can take place when two filled buckets cross at an intersection point, which happens every $96\,ns$.

2.2 Physics at HERA

2.2.1 Introduction

Electron proton scattering has played an important role in unraveling the structure of the nucleon. "Photographing" an object by scattering an electron beam off it is a very well known technique in physics. Suppose that we want to determine a charge distribution as that given in figure 2.5, which could be the electron cloud in an atom for example. Here it is necessary to measure the angular distribution of the scattered electron and compare it to the cross-section for scattering electrons off a point charge

$$\frac{d\sigma}{d\Omega} = \left(\frac{d\sigma}{d\Omega}\right)_{point} |F(q)|^2 \tag{2.1}$$

where q is the momentum transfer between the incident electron and the target, $q = k_i - k_f$. For a static target it can be easily proven that the proportionality factor, which is also known as the target form factor, is simply the Fourier transform of the charge distribution $\rho(x)$ being probed namely

$$F(\mathbf{q}) = \int \rho(\mathbf{x}) e^{i\mathbf{q}\cdot\mathbf{x}} d^3x \tag{2.2}$$

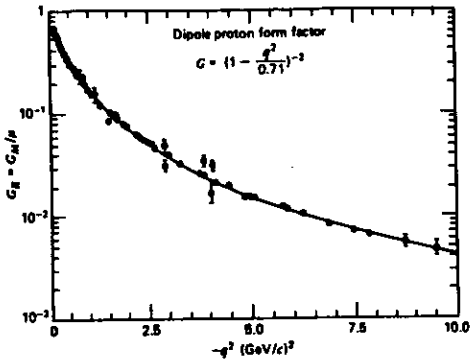


Figure 2.6: *Proton form factor as function of q^2.*

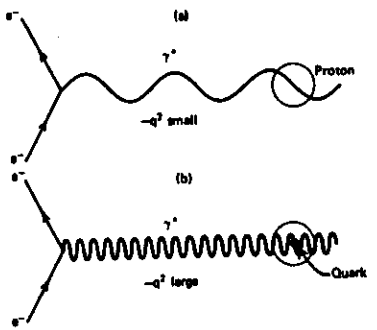


Figure 2.7: *Shorter wavelength photons can be used to investigate in detail the structure of the proton.*

If |q| is not large, we can expand the exponential and obtain

$$F(\mathbf{q}) = 1 - \frac{1}{6}|\mathbf{q}|^2 < r^2 > \tag{2.3}$$

In this way the average radius of the proton charge distribution was measured at SLAC to be around $0.8\,fm$, |2| see figure 2.6.

If one wishes to take a more detailed look at the proton one would simply illuminate it with a shorter wave length photon (see figure 2.7).

One thus expects that if $\lambda \approx \frac{1}{\sqrt{-q^2}} \ll 1fm$ one would be able to resolve the structure within the proton.

This large $Q^2 = -q^2$ limit is called the deep inelastic regime (DIS Deep Inelastic Scattering). Because of the large energy transfer to the target, the proton will break up as illustrated in figure 2.8. Notice that in the lepton (upper) vertex we have already

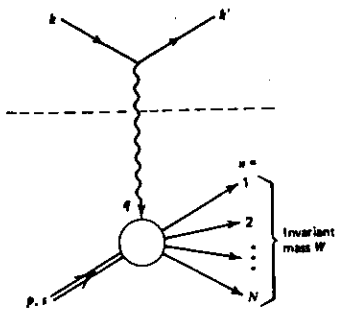


Figure 2.8: *Proton debris for $ep \to eX$.*

taken into account the fact that according to lepton number conservation the outgoing lepton can also be a neutrino.

Because the mass of the hadronic system X, denoted by W, is in general larger than that of the proton M, two kinematical variables are needed to describe deep inelastic scattering. In addition to Q^2 one uses the variable ν defined as

$$\nu = \frac{p.q}{M} \tag{2.4}$$

the following simple relation being held

$$W^2 = (p+q)^2 = M^2 + 2M\nu + q^2 \tag{2.5}$$

In figure 2.9 we show the kinematic regime open to HERA. The black dot at the left hand corner represents the region which could be explored should there exist a $1\,TeV$ muon or neutrino beam available at FNAL. Clearly HERA allows DIS studies in a domain defined by a scale beyond that of electroweak unification.

It is common to replace ν and Q^2 by the following two dimensionless variables

$$x = \frac{Q^2}{2p \cdot q} = \frac{Q^2}{2M\nu} \tag{2.6}$$

and

$$y = \frac{p \cdot q}{p \cdot k} \tag{2.7}$$

where k is the incident electron four momentum. These two kinematical variables are restricted to vary in the interval (0,1). In the rest frame of the target proton ν is simply the energy loss at the lepton vertex i.e.

$$\nu = E - E' \tag{2.8}$$

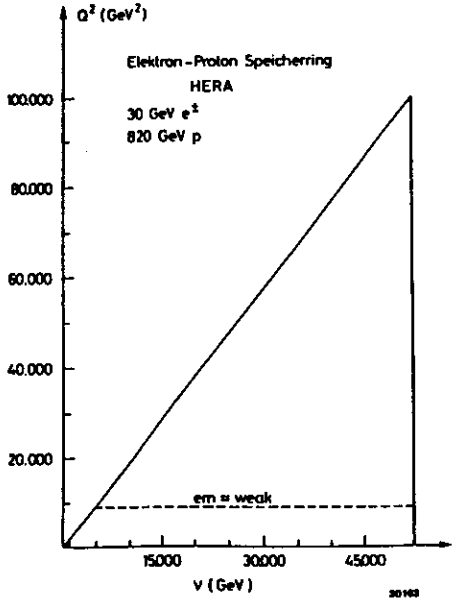


Figure 2.9: *Kinematic range available at HERA [1].*

and y is ν relative to or in units of the incident electron energy namely

$$y = \frac{E - E'}{E} \tag{2.9}$$

The variable x has also a simple interpretation, namely that of the fraction of the proton momentum carried by the struck quark. We will come back to this point later.

To lowest order in perturbation theory the diagram describing ep scattering in the deep inelastic region is given in figure 2.10. The resulting event topology can be understood in the following way: an electron impinging on a proton interacts with one of the

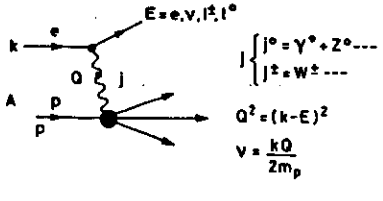


Figure 2.10: *ep deep inelastic scattering lowest order diagram.*

quarks inside the proton via a neutral (γ/Z) (NC) or a charged ($W^{\pm}$) (CC) spacelike current. As a result the "struck" quark originates a "jet" of hadrons, usually known as the "current jet", while the "spectator" partons will give rise to a "fragmentation jet" which will tend to follow the incoming proton direction. In contrast, the "current jet" and the scattered lepton will emerge on opposite sides of the beam axis, balancing each other in transverse momentum.

The differential cross-section for left (L) and right (R) handed initial state electrons is given by

$$\frac{d^2\sigma(e^{\mp}_{L,R}p)}{dxdQ^2} = \frac{4\pi\alpha^2\mathcal{P}^2(Q^2)}{x}\{y^2xF_1^{L,R}(x,Q^2)+(1-y)F_2^{L,R}(x,Q^2)\pm(y-\frac{y^2}{2})xF_3^{L,R}(x,Q^2)\} \tag{2.10}$$

The functions $F_{1,2,3}^{L,R}(x,Q^2)$ are called the *structure functions* of the proton. The propagator $\mathcal{P}(Q^2)$ is of the form

$$\mathcal{P}^2(Q^2) = \begin{cases} \frac{1}{Q^4} & \text{single } \gamma \text{ exchange} \\ \frac{1}{(Q^2+M_Z^2)^2} & \text{single } Z_0 \text{ exchange, } (M_Z \text{ - mass of the Z boson}) \\ \frac{1}{Q^2\,(Q^2+M_Z^2)} & \gamma - Z \text{ interference term} \\ \frac{1}{(Q^2+M_W^2)^2} & \text{single } W^{\pm} \text{ exchange } (M_W \text{ - mass of the W boson}) \end{cases}$$

The explicit forms of the propagators given above teach us that rates at HERA will be dominated by NC low Q^2 events. For Q^2 values of the order or larger than the weak boson masses squared, both the rates for NC and CC events are comparable. Expected production rates in the (x,y) plane are shown in figure 2.11.

One of the important measurements at HERA will be the precise determination of the structure functions mentioned above, in particular their dependence on Q^2. In the quark parton model it can be shown that these three structure functions do not depend on both scalar variables x and Q^2 but rather on the ratio between them. However when colour radiative corrections are taken into account, the presence of diagrams in which the struck quark emits a gluon either before or after the interaction with the current coming from the lepton vertex, introduces an explicit dependence on Q^2 which is actually logarithmic. HERA will allow to perform these structure function measurements in a range in Q^2 from 10^2 to $4 \cdot 10^4\, GeV^2$.

2.2.2 The quark content of the proton

In the parton model the cross section for ep scattering can be viewed as the coherent sum of the corresponding cross sections for an electron over the various types of quarks inside the proton, see figure 2.12.

Let us denote by $f_i(x)$ the probability that quark of type i carries a fraction x of the proton momentum, see figure 2.13.

They should be obviously subject to the normalization condition

$$\sum_i \int dx\; x\; f_i(x) = 1 \tag{2.11}$$

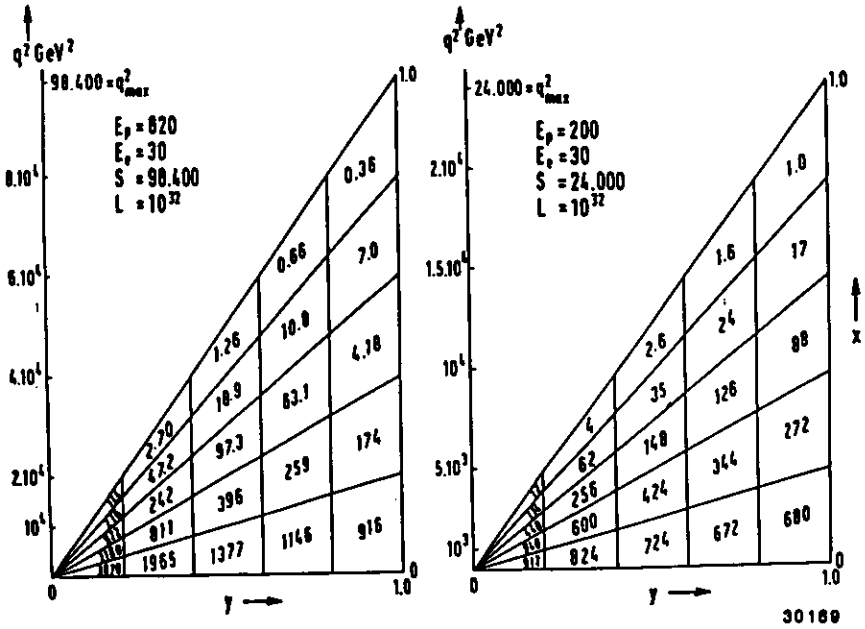


Figure 2.11: *Production rates at HERA for $e^- + p \to \nu + X$ over the kinematic range. The units are events per month for the given energies and luminosities with unpolarized electrons.*

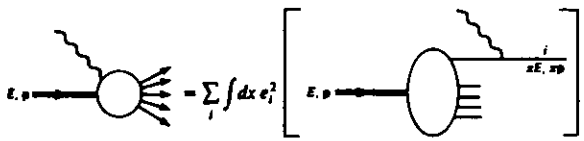


Figure 2.12: *Partitioning of ep scattering cross sections as sum of eq cross section.*

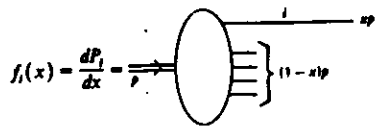


Figure 2.13: *Fractional momentum of a quark and normalization condition.*

Then the structure functions introduced above can be written as

$$F_1^{L,R}(x,Q^2) = \frac{1}{2}\sum_q \{f_q(x,Q^2) + f_{\bar{q}}(x,Q^2)\} A_q^{L,R} \tag{2.12}$$

$$F_2^{L,R}(x,Q^2) = 2xF_1^{L,R}(x,Q^2) \tag{2.13}$$

$$F_3^{L,R}(x,Q^2) = \sum_q \{f_q(x,Q^2) - f_{\bar{q}}(x,Q^2)\} B_q^{L,R} \tag{2.14}$$

These equations reflect the fact that in leading order only the quarks in the proton contribute to the cross section. In particular Equation 2.13 is known as the Callan-Gross relation [3] and is a consequence of the spin $\frac{1}{2}$ nature of quarks. The interpretation of $F_2(x)$ is simple, namely its integral over x should equal the fraction of the incident proton momentum carried by charged quarks.

The coefficients $A_q^{L,R}$ and $B_q^{L,R}$ are

$$A_{q\gamma}^{L,R} = e_q^2 \tag{2.15}$$

$$A_{q\gamma Z}^{L,R} = -2(v_{eZ} \pm a_{eZ})e_q v_{qZ} \tag{2.16}$$

$$A_{qZ}^{L,R} = (v_{eZ} \pm a_{eZ})(v_{qZ}^2 + a_{qZ}^2) \tag{2.17}$$

$$A_{qW}^{L,R} = (v_{eW} \pm a_{eW})(v_{qW}^2 + a_{qW}^2) \tag{2.18}$$

$$B_{q\gamma}^{L,R} = 0 \tag{2.19}$$

$$B_{q\gamma Z}^{L,R} = \mp 2(v_{eZ} \pm a_{eZ})e_q a_{qZ} \tag{2.20}$$

$$B_{qZ}^{L,R} = \pm 2(v_{eZ} \pm a_{eZ})^2 v_{qZ} a_{qZ} \tag{2.21}$$

$$B_{qW}^{L,R} = \pm 2(v_{eW} \pm a_{eW})^2 v_{qW} a_{qW} \tag{2.22}$$

As usual we have denoted by e_q the charge of the quark in units of the electron charge and the weak coupling constants can be written in the standard electroweak model **ref** in terms of the Weinberg angle θ_W and the third component of the weak isospin assignments, namely $T_{3f} = \frac{1}{2}$ for neutrinos, u, c and t quarks and $T_{3f} = -\frac{1}{2}$ for electrons, d, s and b quarks, as follows

$$v_{fZ} = \frac{T_{3f} - 2e_f sin^2(\theta_W)}{sin(2\theta_W)} \tag{2.23}$$

$$v_{fW} = \frac{1}{2\sqrt{2}sin(\theta_W)} \tag{2.24}$$

$$a_{fZ} = \frac{T_{3f}}{sin(2\theta_W)} \tag{2.25}$$

$$a_{fW} = \frac{1}{2\sqrt{2}sin(\theta_W)} \tag{2.26}$$

Measuring the structure functions for electron-proton and positron-proton scattering for various initial state lepton helicities will allow the unfolding of the quark momentum distributions for specific flavors or flavor combinations.

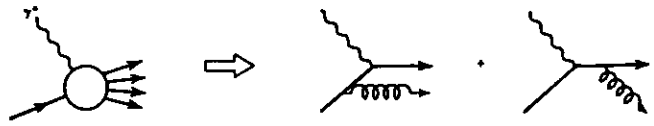


Figure 2.14: *Gluon coupling to scattered quark.*

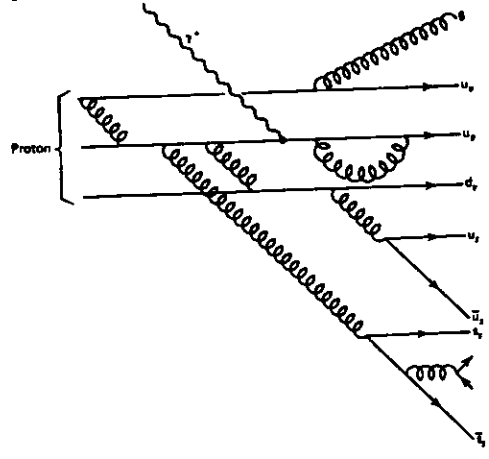


Figure 2.15: *Proton constituents: valence quarks, gluons and slow debris from $q\bar{q}$ pairs.*

2.2.3 The gluon content of the proton

As we already mentioned in the previous section the variation of the structure functions with Q^2 is due to the fact that the struck quark momentum fraction x can change because a gluon coupling to it can take some of its momentum away as shown in figure 2.14.

We know that quarks inside the proton have to be subject to strong forces which override the repulsive forces between them of electromagnetic nature. It is believed that these forces arise due to the exchange of gluons as illustrated in figure 2.15.

In fact existing data on structure function measurements at low energies [2] indicate that

$$\int dx F_2^{ep}(x) = 0.18 \tag{2.27}$$

$$\int dx F_2^{en}(x) = 0.12 \tag{2.28}$$

gluons inside the proton carry roughly 50% of the proton momentum.

It is also necessary to consider the possibility of a constituent gluon fusions with the current associated to the lepton vertex giving rise to the production of $q\bar{q}$ pairs,

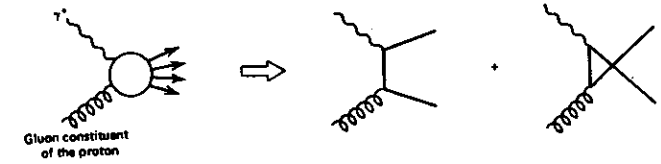


Figure 2.16: *Gluon fusion with current from the lepton vertex.*

as pictured in figure 2.16. Notice that these diagrams are of $\mathcal{O}(\alpha\alpha_s)$ and therefore are suppressed with respect to those discussed before which are of $\mathcal{O}(\alpha)$. Because the strong coupling constant, given to leading order by

$$\alpha_s(Q^2) = \frac{12\pi}{11N_c - 2N_f \ln \frac{Q^2}{\Lambda^2_{QCD}}} \tag{2.29}$$

where $N_c = 3$ is the number of colours, $N_f \leq 6$ is the number of open flavors and Λ_{QCD} is the scale parameter in QCD, is large, these corrections can be sizeable. As discussed before, these corrections induce a logarithmic dependence of the structure functions on Q^2. The parton momentum distributions inside the proton satisfy evolution equations which in certain domains in the plane (x, Q^2) can be written as [4]

$$\frac{df_q(x,Q^2)}{dQ^2} = \frac{\alpha_s(Q^2)}{2\pi}\int_x^1 \frac{dx}{x}\{f_q(z,Q^2)P_{q\to q}(\frac{x}{z}) + g(z,Q^2)P_{g\to q}(\frac{x}{z})\} \tag{2.30}$$

$$\frac{df_{\bar{q}}(x,Q^2)}{dQ^2} = \frac{\alpha_s(Q^2)}{2\pi}\int_x^1 \frac{dx}{x}\{f_{\bar{q}}(z,Q^2)P_{q\to q}(\frac{x}{z}) + g(z,Q^2)P_{g\to q}(\frac{x}{z})\} \tag{2.31}$$

$$\frac{df_g(x,Q^2)}{dQ^2} = \frac{\alpha_s(Q^2)}{2\pi}\int_x^1 \frac{dx}{x}\{f_q(z,Q^2)P_{q\to g}(\frac{x}{z}) + f_{\bar{q}}(z,Q^2)P_{q\to g}(\frac{x}{z})\} \tag{2.32}$$

The functions $P_{a\to b}(z)$ can be interpreted as the probability that parton a gives rise to parton b with a fraction z of its original momentum. These equations are named after Altarelli and Parisi.

The shape of the parton distributions as a function of x is not predicted by the standard model. Qualitative arguments lead us to expect that the parton distributions look like those plotted in figure 2.17. What the standard model tells us is that once the parton distributions have been measured at a given value of Q_0^2 then their behaviour at any other value Q^2 can be obtained from equations 2.30-2.32. Measurements of quark structure functions at present available energies are shown in figure 2.18. Their behaviour conforms to the expectations in figure 2.17. Notice that in Equation 2.30-2.32 we have introduced the gluon structure function. The gluon structure function dominates at very small values of x. While present experiments were limited to $x \geq 0.1$, HERA will be be able to explore the region $10^{-4} \leq x \leq 10^{-1}$. In this region the Altarelli-Parisi equations to which we referred above are not expected to be valid any more. Thus HERA will offer the possibility to experimentally extract for the first time the gluon density distribution inside the proton. Furthermore it will offer the possibility to quantitatively test the evolution in Q^2 of these parton densities.

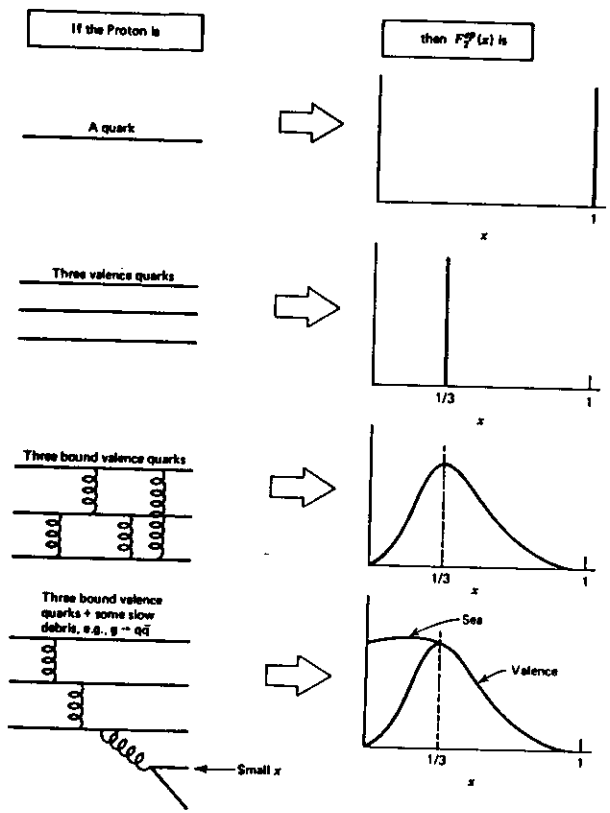


Figure 2.17: *Structure function shapes for different assumed proton compositions. Figure from [2].*

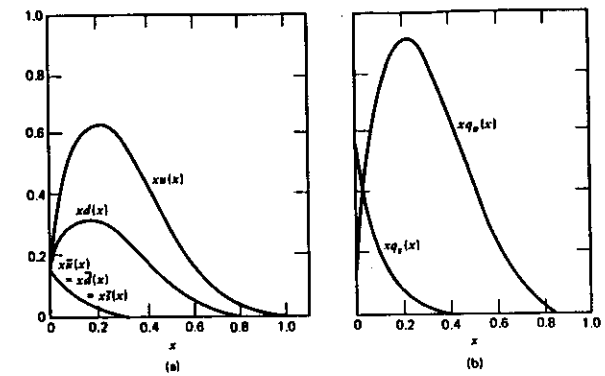


Figure 2.18: *(a) Quark structure functions obtained with deep inelastic scattering data. (b) Contributions from the total valence and sea quark. Figure from [2].*

Although as discussed above current boson - gluon fusion processes are of $\mathcal{O}(\alpha\alpha_s)$, because of the singular behaviour of the gluon density at very low x values, the cross-sections for $q\bar{q}$ pairs are large. This mechanism represent a copious source of heavy quarks. For the sake of comparison let us recall that the cross section for $b\bar{b}$ production at HERA is as large as that in e^+e^- annihilation on the Z_0 pole at LEP. Moreover the cross section for $c\bar{c}$ production at HERA will be two orders of magnitude larger. This will possibly allow for searches of rare charmed meson decays. In particular the $W - gluon$ fusion is a source of $t\bar{b}$ pairs with rates measurable up to top masses close to the W mass. The angular and energy distributions for heavy mesons at HERA are presented in figures 2.19 and 2.20.

The cross section for top production through the boson-gluon fusion mechanism as a function of the top mass is shown in figure 2.21. A summary of their cross sections is presented in Table 2.2

A way to extract the gluon density is to measure $F_L(x, Q^2)$, the longitudinal structure function, given by

$$F_L(x, Q^2) = F_2(x, Q^2) - 2xF_1(x, Q^2) \tag{2.33}$$

At small x: $(2 \cdot 10^{-3} \leq x \leq 5 \cdot 10^{-2})$ and high Q^2 the gluon distribution in the proton can be approximately given by

$$xg(x, Q^2) = \frac{3}{5}\, 5.9\{\frac{3\pi}{4\alpha_s} F_L(0.4x, Q^2) - \frac{1}{2} F_2(0.8x, Q^2)\} \tag{2.34}$$

2.2.4 Tests of the standard model

After having shown the expected rates for NC and CC as well as for boson-gluon fusion events, it is clear that HERA offers the opportunity to test the standard model in a spacelike regime complementary to the timelike processes currently being tested at

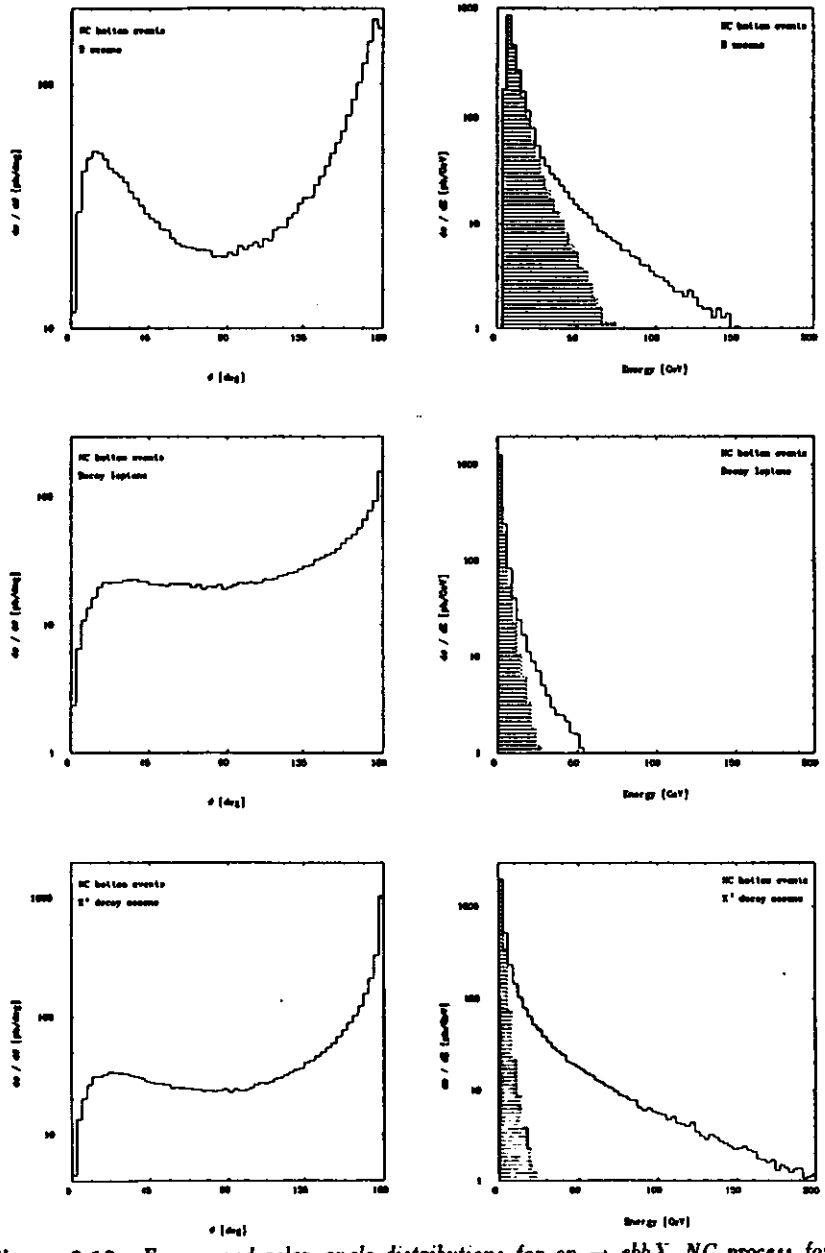


Figure 2.19: *Energy and polar angle distributions for $ep \to ebb\bar{X}$ NC process for different products at HERA energy $\sqrt{s} = 314\,\text{GeV}$. After a beam pipe cut of* 100 mrad *the distributions are the shaded areas. Figures from [5].*

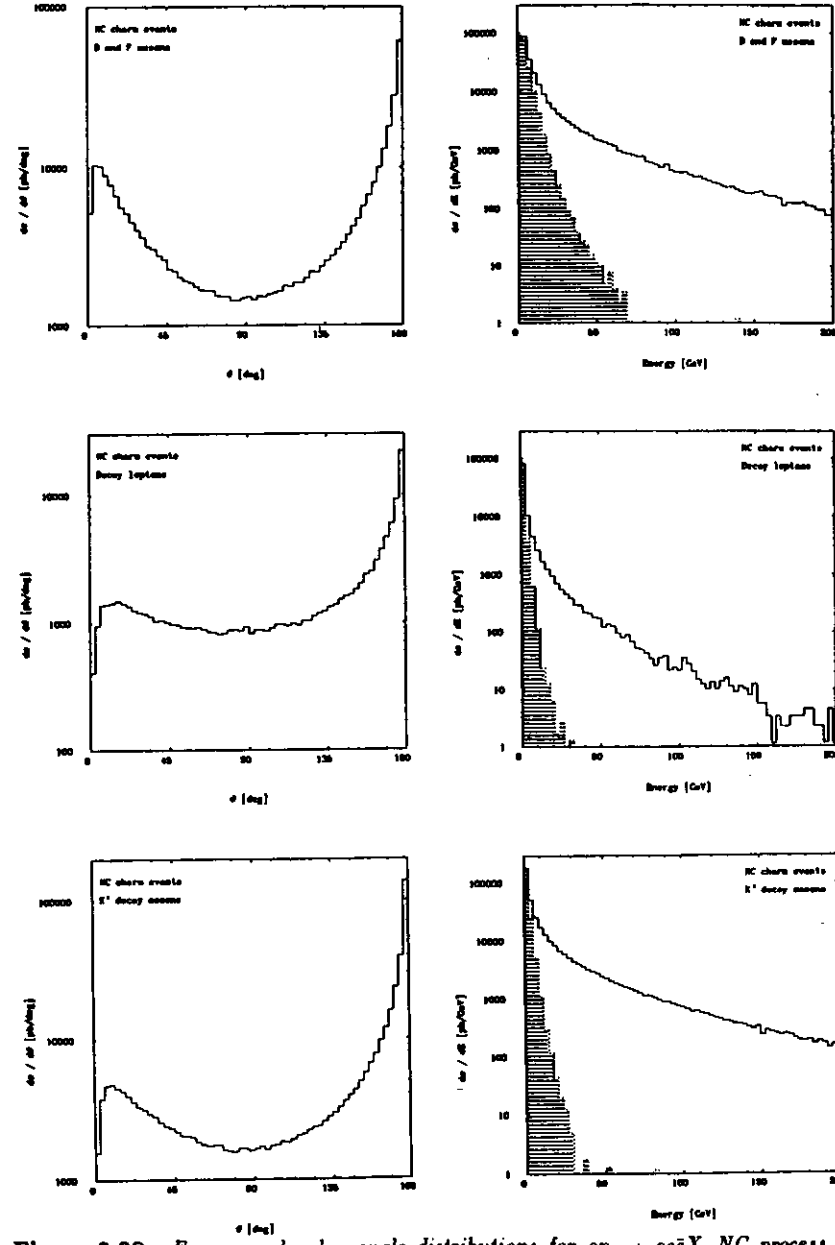


Figure 2.20: *Energy and polar angle distributions for $ep \to ec\bar{c}X$ NC process for different products at HERA energy $\sqrt{s} = 314\,\text{GeV}$. After a beam pipe cut of* 100 mrad *the distributions are the shaded areas. Figures from [5].*

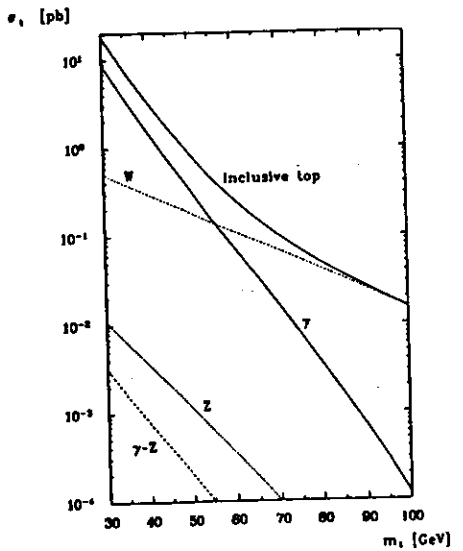


Figure 2.21: *Cross section for top production through boson gluon fusion as a function of the top's mass, Figure from [6].*

$\sigma(ep \to cX)$ [pb] at HERA ($m_c = 1.5$ GeV)								
	CC			NC $c\bar{c}$				inclusive
e^-p	$c\bar{d}$	$c\bar{s}$	$c\bar{b}$	NC	γ	Z	γ-Z	$c + \bar{c}$
BGF	0.46	8.2	0.012	5.1×10^3	5.1×10^3	0.60	4.7	1.0×10^4
e^-p	$\bar{d} \to \bar{c}$	$\bar{s} \to \bar{c}$						
QPM	0.26	3.3						3.6
e^+p	$d \to c$	$s \to c$						
QPM	0.75	3.3						4.1

$\sigma(ep \to bX)$ [pb] at HERA ($m_b = 5$ GeV)								
	CC			NC $b\bar{b}$				inclusive
e^-p	$u\bar{b}$	$\bar{c}b$	$\bar{t}b$	total	γ	Z	γ-Z	$b + \bar{b}$
BGF	$\leq 0.96 \times 10^{-3}$	0.012	0.13	4.2×10^3	4.2×10^3	0.35	0.59	8.4×10^3
e^-p	$u \to b$							
QPM	$\leq 0.56 \times 10^{-2}$							$\leq 0.56 \times 10^{-2}$
e^+p	$\bar{u} \to \bar{b}$							
QPM	$\leq 0.12 \times 10^{-2}$							$\leq 0.12 \times 10^{-2}$

$\sigma(ep \to tX)$ [pb] at HERA ($m_t = 60$ GeV)								
	CC			NC $t\bar{t}$				inclusive
e^-p	$t\bar{d}$	$t\bar{s}$	$\bar{t}b$	total	γ	Z	γ-Z	$t + \bar{t}$
BGF	$\leq 0.14 \times 10^{-3}$	$\leq 0.62 \times 10^{-3}$	0.13	0.09	0.09	0.4×10^{-3}	0.6×10^{-4}	0.31
e^-p	$\bar{d} \to \bar{t}$	$\bar{s} \to \bar{t}$						
QPM	2×10^{-3}	8×10^{-3}						1×10^{-2}
e^+p	$d \to t$	$s \to t$						
QPM	4×10^{-3} QPM	8×10^{-3}						1.2×10^{-2}

Table 2.2: *Cross sections for heavy quark production at HERA : Charm (top), Bottom (middle) and Top ($m_t = 60$ GeV) (bottom) [5].*

LEP. HERA opens up kinematical regimes which enlarge by two orders of magnitude in both Q^2 and x those previously explored at fixed target deep inelastic experiments. In particular some of the QCD tests, those related to scaling violations in the structure functions and the determination of the gluon structure function, will count among the precision tests of QCD in this coming decade. The accuracy to which one hopes to determine Λ_{QCD} is around $\pm 40\,MeV$ for $\Lambda_{QCD} = 200\,MeV$ (previous measured accuracy is $\pm 200\,MeV$).

Of particular interest will be the possibility of testing the chirality structure of the standard model by studying deep inelastic electron proton scattering with polarized electrons. For instance the cross section for right handed electrons on protons proceeding via CC should be zero.

2.2.5 Beyond the standard model

As an alternative to the discussion presented in the previous sections, one could also consider the rates discussed before as backgrounds when looking for departures from the standard model [7]. It is not our aim to give here an exhaustive discussion of all the possible theoretical scenarios and their experimental verification at HERA. We would like to simply summarize that HERA will be able to

- search for right handed currents if the masses of the associated intermediate bosons are below 500-600 GeV,
- search for extra $Z's$ ($W's$) if their masses are below 500 (200) GeV,
- search for scalar leptons if their masses are below 150 GeV,
- sense quark/lepton substructure scales of order 3-5 TeV,
- detect s-channel e-p effects up to masses of the order of the kinematical limit $\sqrt{s} = 314$ GeV.

2.3 ZEUS: a detector for HERA physics

A brief description of the components of the ZEUS detector will be given. A section along the beam axis is presented in figure 2.22 and perpendicular to it in figure 2.23.

ZEUS is a general purpose detector for HERA. It's design is a result of the physics foreseen at HERA. In particular the measurement of the kinematic variables Q^2, x, y over a very large range and with great precision, both for NC or CC events puts an emphasis on calorimetry. The precision measurement of the energy of jets containing charged and neutral components over the full solid angle coverage allow detailed measurements to be made including calculations of missing momentum corresponding to neutrinos (CC reactions). The calorimeter information is enhanced by tracking and particle identification measurements carried out by other detector elements. From the interaction point towards the outside following detectors and systems can be seen :

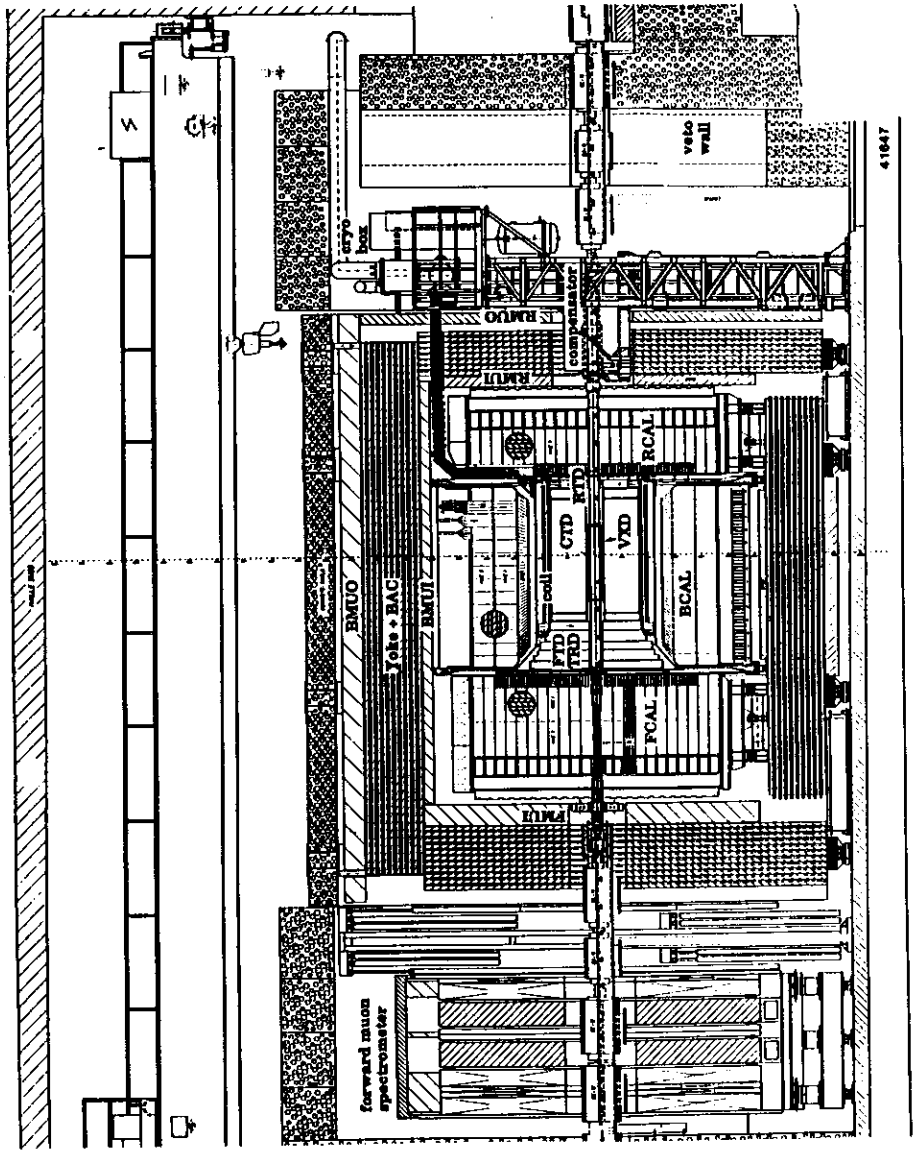


Figure 2.22: *Section across the ZEUS detector parallel to the beam axis.*

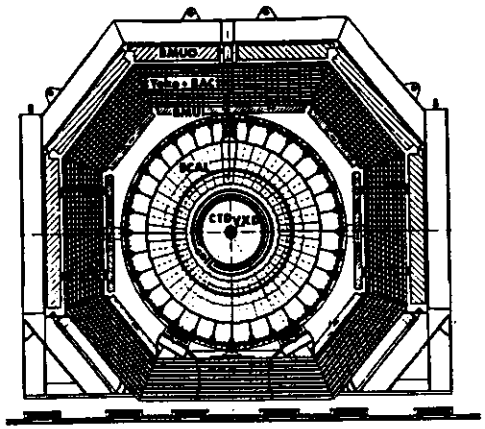


Figure 2.23: *Section across the ZEUS detector perpendicular to the beam axis.*

- the vertex detector (VXD),
- the central tracking detector (CTD),
- the forward tracking detector (FTD),
- the transition radiation detection (TRD),
- the rear tracking detector (RTD),
- the high resolution calorimeter (CAL),
- the muon detector complex (MUO),
- the backing calorimeter (BAC),
- the veto wall (VETO).

Also part of the detector but not shown in the figures :

- the hadron-electron separator (HES), placed inside the high resolution calorimeter,
- the leading proton spectrometer (LPS), placed along the beam line in the proton beam direction.
- the luminosity detector (LUMI), located also down along the beam line but in the direction of the electron beam to detect electrons and photons scattered at very small angles.

Several pieces of hardware are needed additionally even if they do not contribute data to the detector. We have :

- a superconducting solenoid surrounding the CTD area and producing a uniform field of $1.8\,T$ which allows charged particle momentum measurement to be performed simultaneously to tracking,
- a superconducting coil (the compensator) mounted around the beam pipe cancels the effect of the main coil on the beams $\oint Bdl = 0$. Both of these magnets need a liquid He supply which is delivered by the feedbox placed near-by. The feedbox obtains the He from the general supply for the superconducting magnets of the proton ring,
- an iron yoke to provide a return path for the magnetic flux and which surrounds most of the detector elements. It is used as support for mounting several subdetectors. The structure is made of layers of iron which act as the passive material for the backing calorimeter (BAC). It also serves as a filter for the muon spectrometer system.
- an additional magnetized iron toroid system is used in the muon detector in the proton direction,
- in the Rucksack, a 3 story high building placed beside the detector, is located most of the electronics needed to readout all the subdetectors as well as the trigger systems. Cables run from the detector components to the racks in the Rucksack and are carried by a drag chain which permits moving the detector and the Rucksack separately.

The subdetectors group together into functional units which will be briefly reviewed for their functionality and performance.

2.3.1 Tracking devices

The tracking system is shown in detail in figure 2.24

The main objectives of the tracking system are

a) reconstruct all charged tracks with the best possible momentum resolution,

b) use of dE/dx measurements as particle identification tool and

c) detect secondary vertices resulting from meson decay and heavy flavour production.

Additionally this information will be used in the trigger processing of the entire detector. For optimal use the tracking system, like the calorimeter, must cover as much of the solid angle as possible. The CTD covers the region 15° to 164°, the FTD and RTD cover 7.5° to 28° and 159° to 170° respectively.

The CTD chamber is organised in 9 superlayers each made of 8 levels of sense wires. They form a cylinder. The superlayers are arranged with different stereo angles (0°,

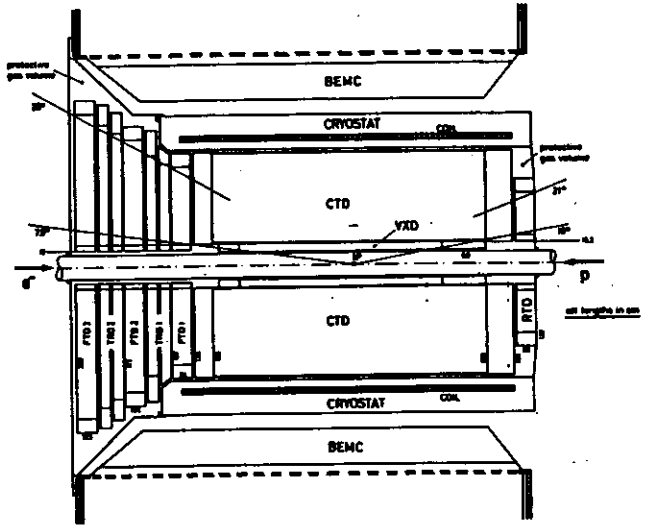


Figure 2.24: *Layout of tracking chambers. Shown are the VXD, CTD, FTD, RTD and TRD. The CTD is enclosed in the volume of the superconducting solenoid placed in the cryostat. Also to be seen is the EMC part of the barrel part of the high resolution calorimeter.*

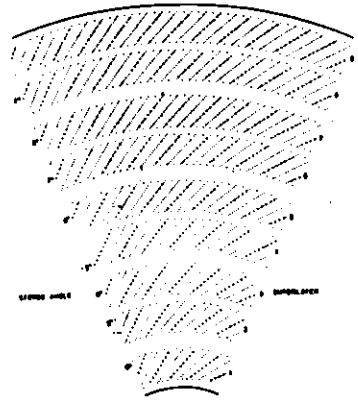


Figure 2.25: *Section through the CTD wires at the outer planes. The thick points are the sense wires, the fine points represent the field wires.*

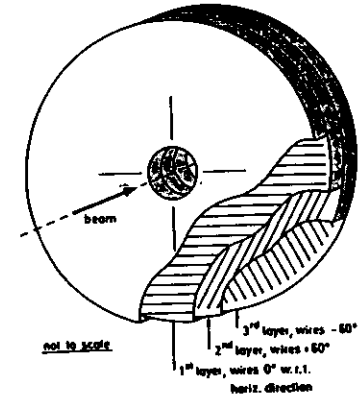


Figure 2.26: *Three chambers with wires at 60° form the FTD system.*

$\pm 5°$, 7°) relative to the beam axis to provide z-position resolution. A section across a CTD chamber sector can be seen in figure 2.25.

The front part of the central volume is tracked by the FTD system which is made up of 3 chambers with wires running at 60° angles and placed perpendicular to the beam. Figure 2.26 shows a diagram of these three planes. On the rear direction only one chamber makes the RTD.

Additionally, the TRD chambers serve to separate particles with equal momenta but with different rest-mass on the basis of the transition radiation they emit when traversing the surface between materials of different dielectric constant. The chambers are organised as many radiator planes interleaved with a tracking plane to detect the radiation. Four of these chambers are placed in two groups in between the FTD chambers. The separation achieved is typically less than 5% hadron misidentification for 90% electron efficiency between 1 and $30\,GeV$.

All these chambers are of the same type, drift chambers filled with an Ar/C_2H_6 50/50 mixture bubbled through ethanol. The combined resolution of the CTD and FTD is plotted in figure 2.27

The most central part in figure 2.24 is the vertex detector (VXD) which allows to improve vertex pointing to the CTD tracks including the detection of any secondary vertices. Its functioning principle is a combination of a drift and "time expansion" chamber which occupies only $16\,cm$ radius around the beam pipe and provides with 12 layers of wires a position resolution of $\sim 50\,\mu m$ (varying with the polar angle and the energy) and a two track separation of $500\,\mu m$.

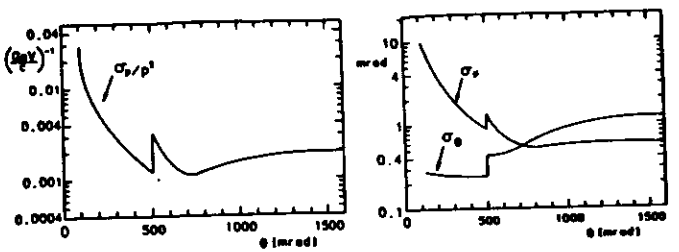


Figure 2.27: *The momentum resolution is shown as function of the polar angle for the ensemble of the central tracking devices (left). On the right, the position resolution on polar angles (σ_θ) and azimuthal angles (σ_ϕ) is plotted. The peaks in the curves come from the frames of the FTD chambers in the transition region to the CTD.*

2.3.2 The calorimeter system

To measure the energy of both charged and neutral final state particles a calorimeter system will be used at ZEUS which comprises two parts. The high resolution calorimeter will measure the energy and position of the particles with the best possible precision across the whole solid angle of 4π. The readout of this device is the main subject of this document and the detector itself is described in the next chapter. It achieves a resolution in the energy of hadrons of $\sigma_E/E \simeq 35\%/\sqrt{E}$ and for electrons and photons of $\sigma_E/E \simeq 17\%/\sqrt{E}$.

Additionally the Backing calorimeter (BAC) is installed to measure the energy leaking out of the high resolution calorimeter for high energetic jets. It consists of proportional chambers in aluminium profiles placed in between the iron plates of the yoke which acts as the passive material. It achieves an energy resolution of $\sigma_E/E \simeq 100\%/\sqrt{E}$. It can also detect muons crossing the drift chambers and determine their momenta by measuring three points in their trajectory.

The distinction between electromagnetic and hadronic energy depositions can be achieved thanks to the longitudinal segmentation of the calorimeter. However to increase the electron/hadron separation several planes of silicon detectors are placed inside the high resolution calorimeter at a depth of the maximum development of the electromagnetic showers. Two planes are foreseen in the forward region and one each in the rear and barrel parts. The HES has a small granularity ($3 \times 3\,cm^2$ pads) and can recognise electromagnetic shower components in jets.

2.3.3 Muon detectors

The muon detector system is divided into the forward (FMUON), barrel (BMUON) and rear (RMUON) parts.

The BMUON and RMUON consist of two sets of two limited streamer tube chambers separated by aluminum frames. One set is placed inside and the other one outside the iron yoke. The magnetization of the yoke allows to measure the momenta of the particles (muons) which are not absorbed in the calorimeter.

The FMUON is made up of five planes of limited streamer tubes, four planes of drift chambers and a time of flight counter. They can be seen in figure 2.22 with the labels LT1 to LT5, DC1 to DC5 and TOF. Additionally to the iron yoke, in the forward direction two magnetized toroids (with conventional coils) provide "bending power" increasing the momentum resolution for high energetic muons.

The momentum resolutions thus achieved are $\sigma_p/p = 23\%$ at $p = 100\,GeV$ in the forward direction and $\sigma_p/p = 30\%$ at $p = 20\,GeV$ in the barrel and rear detectors. The system contributes to a more precise determination of the momenta of the muons independently of the central tracking system and play a crucial role in the trigger system to recognise background events from beam-gas interactions or cosmic muons.

2.3.4 The small angle detectors

Far away from the interaction point, two detector systems detect particles which come out of the interaction at very small angles. On the proton direction, 40 to $80\,m$ away from the interaction point, the leading proton spectrometer made up of 5 planes of silicon microstrip detectors can detect particle impacts with a precision of $25\,\mu m$. The main object of this system is to detect the leading proton scattered at a very small angle after some deep inelastic reactions. For these events a full containment is thus achieved.

On the other side, in the direction of the electron beam, the luminosity monitor detects electrons and photons scattered at very small angles. The detection of an electron and a photon the energy of which sums up to the energy of the primary electron tags Bremsstrahlung events at very small angles ($< 0.5\,mrad$) which are used to monitor the luminosity at the interaction point.

The energy of the electron is measured with a lead-scintillator calorimeter placed placed at about $36\,m$ from the interaction point beside the electron beam. Inside the calorimeter, Si pads will additionally detect the position. The photon's energy is measured also with a lead-scintillator calorimeter placed at a distance of $\sim 108\,m$ from the interaction point near the proton beam. In front of it a carbon filter will protect it from synchrotron radiation.

Both detectors can be moved away from the beam pipe during injection and acceleration to diminish the radiation damage.

Chapter 3

Calorimetry: Principles and the ZEUS Solution

The importance of high precision calorimetric measurements has been presented in the previous chapter. Now, a more detailed discussion will follow on how the energy detection mechanism in calorimeters occurs for different particle types. The construction principles of the ZEUS calorimeter are also described in this chapter.

3.1 Sampling calorimeters

Calorimeters, currently used in high energy physics experiments are either "homogeneous" or "sampling". *Homogeneous* calorimeters consist of a single material, such as Lead glass, NaI, BGO, etc. This material acts as an absorber in the sense that the incident energy is degenerated by shower processes and as a detector since Čerenkov or scintillation light produced by the constituents of the shower process produce a measurable signal. *Sampling* calorimeters separate the tasks of absorber and signal production and detection. Typical absorber material is Fe, Cu, Pb or U. Examples of detector materials are scintillating plastics which produce detectable signal in the form of light or liquid argon or silicon in which cases the revealing mechanism is the ionization charge which can be collected electrically.

Of course, as we want the detectable signal to be proportional to the absorbed energy, the two materials have to be quite intimately associated so that a sum of fractions of the deposited energy can be seen by the active detector. Several realizations of this grouping can be imagined and some of them have been physically realised at different calorimeters. The ZEUS calorimeter concept chose the so-called "sandwich" type structure, where alternate layers of different materials perform a stepwise process of shower development and signal generation. Stacking enough layers of the two materials is necessary to ensure a complete deposition of the energy carried. The energy and type of particles which have to be detected determine the size of the calorimeter once both material types and their relative thicknesses have been fixed.

The primary particles incident on the calorimeter interact in various ways with

the materials making up the detector and generate secondary particles of lower energy which in turn interact with the material giving other particles. The original incoming particle produces in this way a so-called "shower" or "cascade" in which the energy carried is "degraded" and part of it is detected. The process of the shower generation being of statistical nature and the physical development of it set limits to the energy detection precision. Also the principle of alternating materials leads to a "sampling" of only a fraction of the energy in the active parts adding additional uncertainties to the energy measurement, the *sampling fluctuations*. The *sampling fractions* are different for different sorts of particles, indicating distinct calorimetric efficiency.

Two types of showers can be distinguished : the *electromagnetic* and the *hadronic* showers, the latter type including fractions of the first sort.

3.2 Electromagnetic showers

3.2.1 Shower generation

Several mechanisms contribute to the energy loss mechanism for electrons and photons incident on matter. However at high energies the fraction of energy lost per unit of depth of material is almost energy independent and only due to Bremsstrahlung and pair creation. The secondary particles produced in the cascade carry successively less energy until they reach the range where several effects are important. If the whole cascade is absorbed, the energy deposited equals that of the primary particle.

For electrons or positrons the main process occurring at high energies is the Bremsstrahlung, radiation of photons on the field of nuclear charge . In the sub-GeV range, other processes like Møller and Bhabha scattering and ionization take place. Positrons in addition suffer annihilation. Ionization is in fact the dominant phenomenon and the reason that all secondary particles finally get absorbed. Figure 3.1 shows the different cross-sections for these processes and their dependance on energy in the case of a lead absorber.

In the case of photons (see figure 3.2) the main process at high energies is the pair production of e^+e^- while for energies lower than $10\,MeV$, the Compton and the photoelectric effects are dominant.

At high energies ($> 1\,GeV$), the absorption can be characterised in a material-independent way by the so-called *radiation length*, X_0, of the substance. It is defined as the material thickness to be travelled by an electron so that it looses on average 63.2% of its energy through Bremsstrahlung. The average energy as the particle traverses matter is :

$$E = E_0 e^{-\frac{t}{X_0}} \tag{3.1}$$

where :
$t\,[cm]$ is the thickness of the material,
$E_0\,[MeV]$ the energy of the incident electron,
$X_0\,[cm]$ the radiation length.

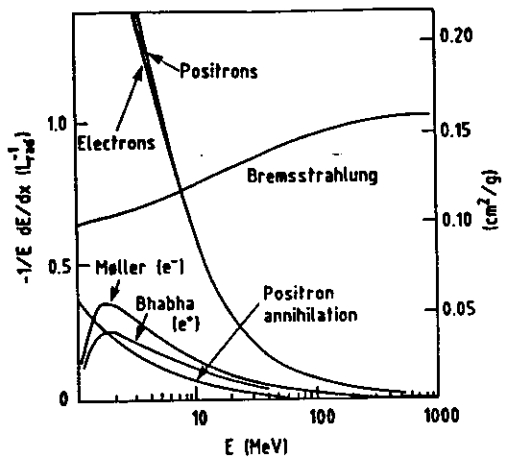


Figure 3.1: *Fractional energy loss in lead for electrons and positrons as function of their energy [8], per radiation length (left scale), per* g/cm^2 *(right scale).*

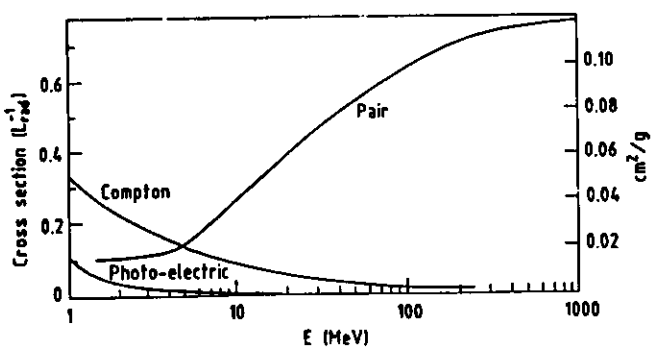


Figure 3.2: *Cross section of photons in lead as function of their energy [8].*

Material	Z	A [g]	$\rho\left[\frac{g}{cm^3}\right]$	$\rho X_0\left[\frac{g}{cm^2}\right]$	$X_0[cm]$	$\epsilon_0[MeV]$
Polystyrene	< 3.4 >	-	1.060	43.8	41.3	~ 80
Al	13	26.98	2.70	24.01	8.89	48.8
Fe	26	55.85	7.87	13.84	1.76	24.3
Pb	82	207.19	11.35	6.37	0.56	7.8
U	92	238.03	18.95	6.00	0.32	~ 6

Table 3.1: *Values of the Radiation Length X_0 and critical energy ϵ_0 for some materials.*

The radiation length can be computed using [9]:

$$\frac{1}{\rho X_0} = 4\alpha\frac{N_A}{A}\frac{Z(Z+1)r_e^2\ln(183Z^{-1/3})}{1+0.12(Z/82)^2}\left[\frac{cm^2}{g}\right] \tag{3.2}$$

where :

α	is	the fine structure constant,
A	the	atomic mass of the material in [g],
Z	the	atomic number of the material,
N_A	the	Avogadro number,
r_e	the	classical electron radius in [cm],
ρ	the	density of the material in $\left[\frac{g}{cm^3}\right]$.

Equation 3.2 can be approximated [10] by :

$$\rho X_0 \simeq 180\frac{A}{Z^2}\left[\frac{g}{cm^2}\right] \tag{3.3}$$

which is good to better than 20 % for $Z > 13$.

At low energies the dominant energy loss is no longer due to radiation but to collisions. The *critical energy* ϵ_0 of the material is the energy at which both losses, Bremsstrahlung and ionization are equally important. It represents the limit where the growth of the shower stops and it starts dissipating its energy. Its value is given approximately by [10]:

$$\epsilon_0 = \frac{550}{Z}[MeV] \tag{3.4}$$

This approximation is accurate to 10% for $Z > 13$. For some materials the values of X_0 and ϵ_0 can be found in table 3.2.1 [11].

A very simplified model of shower development can provide insight into (electromagnetic) calorimetry assuming that the only dominant processes at high energies are Bremsstrahlung for electrons and pair production for photons and these are described by asymptotic formulae.

An electron entering material with an energy E much bigger than the critical energy ϵ_0, after having crossed one radiation length of material X_0 will have lost 63% of its

initial energy into photons by Bremsstrahlung. We can say that on the average the photon and the electron will carry each half of the original energy, $E/2$. After another radiation length of material, the photon will create an e^+e^- pair and the electron will emit another Bremsstrahlung photon. The energy of the four particles existing is on the average $E/4$. The multiplication process proceeds. When the electrons reach an energy below ϵ_0 they will be completely absorbed by collisions and the shower terminates. The model is equally valid if the shower is started by a photon except for a shift in depth.

The number of particles doubles each radiation length. After t units of radiation length, the number of photons and electrons $N_{e,\gamma}$ is :

$$N_{e^-+\gamma} = 2^t \tag{3.5}$$

where t is the depth, now in units of $[X_0]$. The mean energy ϵ of each particle of course goes inversely :

$$\epsilon = \frac{E}{N_{e,\gamma}} = E \cdot 2^{-t} \tag{3.6}$$

where E is the energy of the incident electron or photon $[MeV]$.

The depth, in units of radiation length, where their mean energy ϵ equals the critical energy ϵ_0, is where the shower reaches its maximum spatial spread and is :

$$t_{max} \simeq \frac{\ln E/\epsilon_0}{\ln 2}[X_0] \tag{3.7}$$

At t_{max} the shower development and the number of particles reach a maximum. Further in the calorimeter, the energy left over is deposited by ionization.

The total distance covered by all the particles of the shower is called the average *total track length* $< T >$; in units of X_0 it is equal to the number of particles of the shower.

As the showering process occurs, a small part of the energy is lost by ionization and is proportional to the total track length because each high energetic particle of the shower deposits an amount of energy per unit length independent of the energy it carries :

$$E_{visible} = E_{ionization} \propto < T >= \frac{E}{\epsilon_0}. \tag{3.8}$$

This linear relation between the incident energy and the total track length or the energy loss by ionization makes calorimeters useful devices.

In general not the whole track length T will be detectable, but only a fraction of it T_d will give some signal which can be seen. $T_d < T$ because only shower particles carrying more than a certain threshold energy η are detectable.

$$< T_d >\simeq F(\eta) < T >= F(\eta)\frac{E}{\epsilon_0}. \tag{3.9}$$

It is necessary to know the longitudinal extension in order to ensure containment of the shower within the calorimeter. Naturally, due to the statistical nature of the shower development, total containment for practical calorimeter dimensions cannot always be achieved. Experimental and calculational information [8] parametrize the longitudinal energy deposition to reach 98% in a length :

$$(L_{98\%}) \simeq t_{max} + 4\lambda_{att} \tag{3.10}$$

where $L_{98\%}$ is the depth at which 98% of the energy has already been deposited. The quantity λ_{att} comes from the exponential decay of the shower (following $e^{-t/\lambda_{att}}$) after having reached the maximum. λ_{att} results to be quite energy independent but material dependant and can be characterised also in radiation length units : $\lambda_{att}[X_0] \simeq (3.4 \pm 0.5)$ [8].

The important fact we learn from Equations 3.7 and 3.10 is that the depth of a shower, i.e. the depth of the calorimeter we need to contain and measure, grows only *logarithmically* with the energy. Thus for example ZEUS can have a calorimeter which measures 400 GeV jets as well as particles in the sub-GeV range and still keep it's size reasonable.

3.2.2 Energy resolution

The processes of energy deposition, detection and readout in a calorimeter have been shown to have a statistical nature. The relative precision of the energy measurement is :

$$\frac{\sigma(E_{visible})}{E_{visible}} \tag{3.11}$$

where $\sigma(E_{visible})$ is the standard deviation of the distribution of measured values.

Intrinsic fluctuations

Two kinds of uncertainties enter into the measurement of the energy. First, as we have seen, the showering is in itself an statistical process. Also Landau fluctuations occur due to ionization processes with high energy transfer to the electrons of the detector material which leads to asymmetric spectra for the deposition at high energies. They are however not quantitatively significant for the case of the ZEUS calorimeter. A description can be found in [10,11].

From equation 3.9 we know that the mean track length which is detected $< T_d >$ is proportional to the energy of the incident particle. The energy deposited is first proportional to the number of particles produced but also to the number of particles detected N_d. N or N_d are large numbers results of many different causes and based on the large number theory they will follow normal distributions. The standard deviation of N normally distributed events goes as the square root of N. This means :

$$\frac{\sigma(E)}{E} \sim \frac{\sigma(N_d)}{N_d} = \frac{\sqrt{N_d}}{N_d} = \frac{1}{\sqrt{N_d}} \sim \frac{1}{\sqrt{E}} \tag{3.12}$$

Equation 3.12 represents the lower limit in the precision of the measurement of energy, the *intrinsic fluctuations*. The best homogeneous electromagnetic calorimeters made

of scintillating crystals or noble liquids are indeed limited by this statistical fact and achieve energy resolutions of the order of $\sigma_E/E \simeq 1\%/\sqrt{E}$ or better [8].

Sampling fluctuations

If instead of a homogeneous we use a sampling calorimeter, the particles produced in the showering will only contribute to the visible signal when they cross the active medium of the calorimeter. In a sandwich sampling type device like the ZEUS calorimeter, the average detectable total track length is sampled regularly at a distance of d radiation lengths separating two active layers. This means that the number of particles which are really observed is reduced to :

$$N_{sampled} \simeq \frac{< T_d >}{d}. \tag{3.13}$$

Substituting equation 3.9 :

$$N_{sampled} \simeq F(\eta)\frac{E}{\epsilon_0 \cdot d} \tag{3.14}$$

In an equivalent way to equation 3.12, $N_{sampled}$, which is normally distributed due to the hypothesis that the number of crossings behave as independent factors, has also a relative precision inversely proportional to the square root of $N_{sampled}$.

$$\frac{\sigma(N_s)}{N_s} = \frac{1}{\sqrt{N_s}} \tag{3.15}$$

This means the sampling of the average detectable total track length results in an additional degradation of the energy measurement. From equations 3.14 and 3.15 results :

$$\left(\frac{\sigma_E}{E}\right)_{sampling} = 3.2\% \cdot \sqrt{\frac{\epsilon_0\,[MeV]}{F(\eta)} \cdot \frac{d\,[X_0]}{E\,[GeV]}} \tag{3.16}$$

A more accurate description of the real shower includes a term accounting for the transverse development of the shower. The particles do not cross $d\,[X_0]$ of material before being sampled again in the next active layer as we mentioned in equation 3.13, but travel transversally with a certain angle traversing in fact

$$d / \cdot \cos\theta \cdot$$

radiation lengths of matter. The term $< \cos\theta >$ represents a mean value of the deflection angle of the tracks measured from the shower axis.

This transversal spread is characterised by the quantity called the Molière radius ρ_M, which is a material independent quantity equivalent to the radiation length X_0 for the depth. The Molière radius describes the average lateral deflection of electrons of energy ϵ_0 when they traverse one radiation length of material. The shower is contained in a cylinder of radius $R = 2 \cdot \rho_M$.

For elements with $Z > 13$ the Molière radius ρ_M can be approximately calculated to a 10 % precision by :

$$\rho_M \simeq 7\,\frac{A}{Z} \tag{3.17}$$

Monte-Carlo calculations give the following parameterization for $\cos\theta$ [10] :

$$< \cos\theta > \simeq \cos\frac{21MeV}{\pi \cdot \epsilon_0} \tag{3.18}$$

With equation 3.18, the sampling fluctuations contribute to the resolution of the energy measurement in equation 3.16 with :

$$\left(\frac{\sigma_E}{E}\right)_{sampling} \geq 3.2\% \cdot \sqrt{\frac{\epsilon_0\,[MeV]}{F(\eta) \cdot \cos\left(\frac{21}{\pi \cdot \epsilon_0}\right)} \cdot \frac{d\,[X_0]}{E\,[GeV]}} \tag{3.19}$$

The only method to diminish this contribution once the materials making the calorimeter have been fixed is to decrease the layer thickness d. In an obvious way, this increases the amount of energy which is really sampled, statistically reducing its variation.

The analytical estimations of the sampling fluctuations are however not very precise and valid only for light materials and reasonably thick layered calorimeters. If thinner layers are used, the model hypothesis of independent shower development does not hold any more.

Other fluctuations

Another important contribution to the degradation of the energy resolution is added by the instrumental construction of the calorimeter and the readout mechanisms of the signals. For example leakage due to constructively finite calorimeter depth, deteriorates the resolution (see [8]). Non uniformities in the signal collection or in the construction of the calorimeter also show up as degradation in the resolution.

For most calorimeters a further statistical contribution due to the conversion into electrical current or voltage for signal processing adds again to the uncertainty in the signal. The ZEUS calorimeter is instrumented with photomultipliers, and there the process of electron generation at the photocathode originated by incoming photons is also in itself of statistical nature. Of course, the contribution of the photostatistic to the global energy resolution is diminished if the amount of light increases. The light generation, transport and collection system at ZEUS is therefore subject to strict criteria with the aim of achieving a maximum possible efficiency. The contribution of photostatistics to the electromagnetic energy resolution at ZEUS is measured [12] to be around[1] $10\%/\sqrt{E}$.

Non-uniformities and other non-ideal features do not scale inversely with the square root of the energy but add in a constant way to the resolution, dominating at high

[1] In the hadronic part of the calorimeter, the amount of light produced is larger and thus the effect of photostatistics is reduced $\sim 7\%/\sqrt{E}$.

energies. The aim of the ZEUS calorimeter construction is to keep all these contributions at the 1 % level. All the contributions to the resolution of the electromagnetic energy at ZEUS are expected, in the whole energy range it has to cover, to add to a maximum of :

$$\left(\frac{\sigma_E}{E}\right)_{electromagnetic} \simeq \frac{17\%}{\sqrt{E}} \oplus 1\%. \tag{3.20}$$

As it will be shown from calibration results this has been essentially achieved.

3.3 Hadronic showers

Particles subject to the strong interaction, i.e hadrons, also produce showers when entering a calorimeter though the shower development is different to the electromagnetic showers previously described.

In contrast to electromagnetic cascades which are dominated by Brehmsstrahlung and pair production processes with very large cross-sections, many channels compete in the development of *hadronic showers*. A fact which produces larger variations in the deposited and visible energy.

The main hadronic shower development is given by inelastic scattering of particles with the nuclei of the absorber material. This and other processes occurring are more complicated to describe than the factors governing an electromagnetic shower where analytical analysis, even if under restrictive conditions, is possible and excellent Monte-Carlo simulation tools (e.g. EGS) exist. Modelling hadronic showers is difficult and calculations are only possible with Monte Carlo methods and parametrized experimental results. Here, only a brief description of the phenomena leading to the hadronic shower will be described. A detailed explanation is given in [11] and the calculational methods are described in [13,14,15].

The hadron's energy is lost in inelastic collisions and carried away by some of the nucleons or secondary produced hadrons. If their energy is larger than the nuclear binding energy, they leave the nucleus predominantly in a forward direction and collide with neighbouring nuclei repeating the process. In some $10^{-22}s$ this process is terminated because the particles coming out of the collision can no more leave the nuclei. After this a second step follows where γ-quanta are produced when the nucleons are deexcited. These on their turn produce electromagnetic showers which deposit energy in the active layers by ionization.

If the absorber is uranium, in addition fission can occur and as a product low energy (few MeV) slow neutrons appear.

In total some 300 different reactions occur in the propagation of a hadronic shower, each contributing comparable amounts to the global process. Event to event statistical fluctuations and the relative importance of competing visible energy production processes set limits to the possible resolutions achievable for hadron energy measurement.

To describe hadronic showers in a material independent way, the quantity λ, the nuclear interaction length is introduced in a similar way to the radiation length for electromagnetic showers.

3.3.1 Compensation in hadronic showers

The part of deposited energy which is rendered visible in the calorimeter is typically smaller for hadronic than for electromagnetic showers. This is mainly due to a larger amount of the hadronic cascade energy lost in intranuclear inelastic collisions and nuclear binding energy. In addition with passive materials of high A, many neutral particles[2] are generated in the cascade and these produce less signal in the active medium.

This fact leads to smaller visible signals for hadrons than for electrons of the same energy. The so-called e/h ratio is smaller than 1. The consequence is that the electromagnetic part of the hadronic shower yields larger signals than the pure hadronic part, resulting in a larger spread in the global measured response. The effect of fluctuations in the ratio of pure hadronic to electromagnetic signal produced by a hadronic shower upon the total measurement can be minimized by achieving an e/h ratio equal to one. This case is the so-called *compensation* of the signals.

Using uranium as passive material [16] helps in compensating the losses in the hadronic shower. For the electromagnetic part of the shower (neutral pions decaying into photons), the uranium will absorb a larger fraction of the energy and the signal in the active medium will be smaller. On the other hand for the hadronic part, the low energy neutrons are not affected by the uranium [17]. They interact with the hydrogen atoms in the active material (large cross-section for neutrons) and produce signal in the readout.

The amount of electromagnetic reduction and neutron amplification is set by the ratio of absorber to active material [15,13] :

$$R_d = \frac{Thickness\ of\ absorber\ layer}{Thickness\ of\ active\ layer} \tag{3.21}$$

so that compensation[3] is reached. For the ZEUS calorimeter, Monte Carlo calculations and diverse test calorimeter measurement have finally set a ratio of $3.3\,mm$ of uranium vs. $2.6\,mm$ of scintillator as the dimensions to be used.

Besides the intrinsic fluctuations in the hadronic shower formation, the sampling principle also applies to this deposited energy, and only a fraction of it will be detected. This adds sampling fluctuations also in the hadronic energy resolution and measurements show that they are larger than in the case of electromagnetic showers.

Also instrumental limitations, like the finite depth of the calorimeter or the unavoidable non uniformities in the construction add to the experimental resolution. As in the case of electromagnetic cascades they do not necessarily scale in a $1/\sqrt{E}$ way and thus limit the performance at high energies.

For the ZEUS calorimeter calculations predict and prototype tests result in a resolution for the measurement of energies of hadrons of :

$$\left(\frac{\sigma_E}{E}\right)_{hadronic} \simeq \frac{35\%}{\sqrt{E}} \oplus 2\% \tag{3.22}$$

a quantity which has also been achieved as calibration measurements show.

[2] The amount of π^0s is also increasing with energy giving a non-linearity in the readout signal.
[3] In fact "overcompensation" ($e/h < 1$) can be obtained if a large DU thickness is chosen.

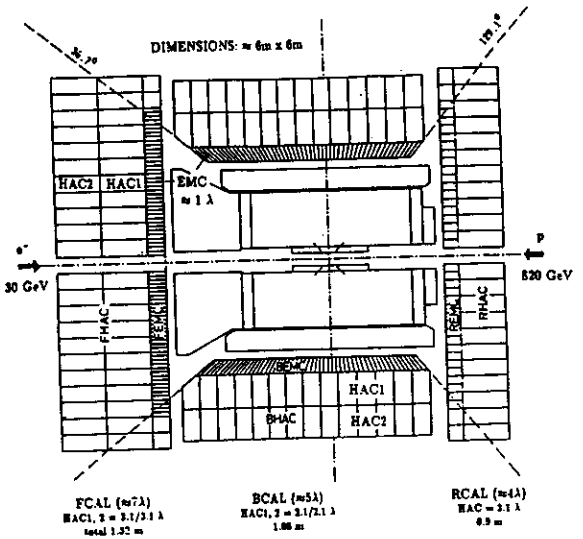


Figure 3.3: *Mechanical division of the ZEUS high resolution calorimeter.*

3.4 The ZEUS calorimeter

The calorimeter for the ZEUS detector is one of the most advanced detectors for high energy physics experiments. The ZEUS collaboration has developed a device which (almost) hermetically surrounds the interaction point and which has an energy resolution for hadrons at the limit of the achievable.

The detector itself as well as the techniques used to construct it will be described.

3.4.1 Segmentation

The ZEUS calorimeter covers 99.8% of the solid angle in the proton direction (forward) and 99.5% in the electron direction (backward). The size and weight of the calorimeter, mainly governed by the necessary depth to absorb the full energy of the showers which can be produced at the $e-p$ collisions, forces a modular construction and installation.

It is divided into three components shown in figure 3.3, covering portions of the polar angle θ:

- the forward calorimeter (FCAL) for θ between 2.2° and 39.9°,
- the barrel calorimeter (BCAL) extends between $\theta = 36.7°$ and 129.1°,
- the rear calorimeter (RCAL) between $\theta = 128.1°$ and 176.5°.

The structure of all the parts is similar. The inner most part forms the electromagnetic calorimeter (EMC) with a depth of $\sim 25\ X_0$ (equivalent to $1\,\lambda$).

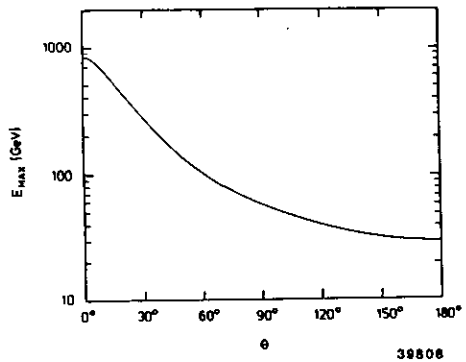


Figure 3.4: *Maximum jet energy as function of the polar angle [7].*

The rest of the matter builds the hadronic calorimeter (HAC). It's depth varies depending on the polar angle to cope with different maximum energy showers (see figure 3.4). In the forward region it is $\sim 6\,\lambda$ deep while in the rear it has $\sim 3\,\lambda$ and $\sim 4\,\lambda$ in the barrel yielding a total depth of 7, 4 and 5 λ respectively.

The EMC part is readout as one section in depth while the HAC part is divided into two sections, HAC1 and HAC2 which are readout separately throughout the whole calorimeter.

However the size and direction of the segmentation in the transverse sense varies across the regions. For example the central parts of the FCAL have EMC sections with dimensions of $5 \times 20\,cm$ ($5 \times 10\,cm$ in the RCAL) which are arranged parallel to the beam direction, this means they are non-projective to the interaction point. In the external regions where the sections overlap with the BCAL, the segmentation is $20 \times 20\,cm$ and is also non-projective. In the BCAL, the EMC segmentation is $\sim 5 \times 24\,cm$ but the sections are arranged projectively to the interaction point. The divisions in the hadronic calorimeter are typically $20 \times 20\,cm$ and are non-projective over the whole calorimeter.

The calorimeter is divided into 24 modules for the FCAL, 32 for the BCAL and 24 for the RCAL. The FCAL and RCAL modules are blocks of several meters height (2.2 to $4.6\,m$), $20\,cm$ width and depth varying between 70 and $152\,cm$ (in their active area). An isometric view of one of them is shown in figure 3.5.

The BCAL modules are all equal and have a trapezoidal section between 24 and $45\,cm$ and each one covers a wedge of 11.25° in azimuthal angle. Their length is $3.2\,m$. One of the modules is drawn in figure 3.6.

All the modules have a gap in their EMC sections (at $\sim 4X_0$) (two gaps exist in the FCAL at ~ 4 and $\sim 7X_0$) where one scintillator plane and one U-plate have been left out to leave space for a plane of silicon pads detectors to improve the hadron-electron separation (see [18]).

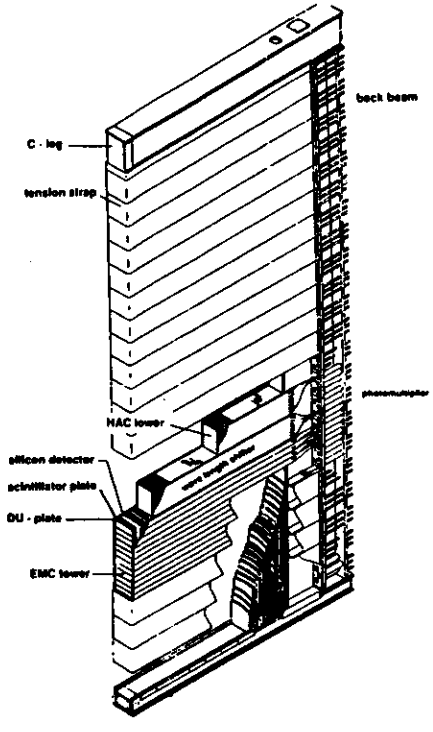


Figure 3.5: *Isometric view of a FCAL module. The different hardware elements can be seen.*

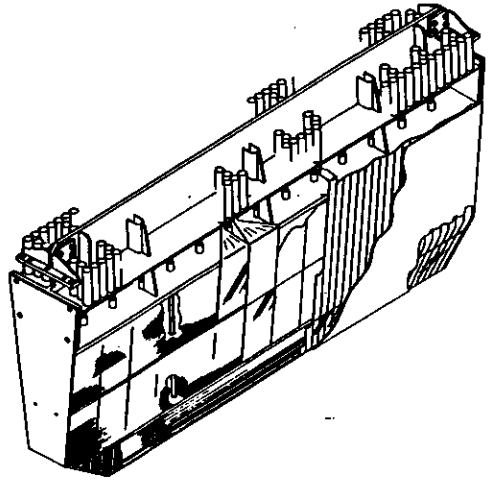


Figure 3.6: *Artist view of a BCAL module.*

3.4.2 Module construction

The high precision design for the whole calorimeter forces some unusual constructional features to be adopted for all the 80 modules and their components.

Uranium plates

The optimum energy resolution of $35\%/\sqrt{E}$ for hadron showers is made possible by a e/h ratio of 1. This is achieved for a ratio of thicknesses of $3.3\,mm$ of depleted uranium (DU)[4] and $2.6\,mm$ of scintillator of the SCSN-38 type.

The DU plates are fully encapsulated by a stainless steel foil to protect the scintillator from large radiation doses which would quickly reduce it's light yield and shorten the calorimeter's lifetime. Also the steel case is a security factor mainly against fire damage of uranium and radioactive dust contamination caused by handling.

The size of the plates varies from module to module. For FCAL and RCAL they are $< 20\,cm$ wide and have lengths up to $4.6\,m$. In the BCAL their width increases as they are placed further away from the interaction point, each plate subtends the same transverse angle.

Several new techniques had to be developed to produce the longest plates (up to $4610\,mm$) and to achieve and monitor the tolerances in the thickness to $3.3 \pm 0.2\,mm$ and other dimensions.

The plates are held apart by spacers of $5 \times 10\,mm^2$ ($5 \times 6\,mm^2$ for EMC) area and $3.9\,mm$ thick placed every $20\,cm$ along the sides of the modules.

[4] 98.1% U^{238}, 1.7% Nb, 0.2% U^{235}.

Scintillator

In between the DU plates are placed the scintillator tiles. A small part of the particle shower's energy is converted into visible light through a scintillation process. The material has been chosen to be a cast scintillator on polystyrene base (see figure 3.8-(a)) because of several factors like aging and radiation stability, high light yield and long attenuation length for light relative to the size of the tiles.

The tiles have a thickness of $2.6 \pm 0.2\,mm$ and different areas depending on their location inside the modules, from $5 \times 20\,cm$ in the FCAL EMC section to $24 \times 42\,cm$ in the HAC2 BCAL sections. They have all their edges polished and are individually wrapped in special white paper which is printed with a black and white pattern to improve the uniformity of the light response. This correction pattern affects the amount of UV light which is reflected and yields a uniformity of the local light yield from around 7% to 2% across the whole surface of the pieces.

The opposite edges of the tiles are open so that light can escape to the optical transport system. Both sides are open so light is simultaneously readout on the left and on the right sides. This eliminates part of the fluctuations due to the readout and provides some redundancy as well as spatial resolution. Tests have shown that in average 3.3 photoelectrons are produced in each layer of the material when read from both sides for a minimum ionizing particle crossing the calorimeter.

Also a rigorous quality control during manufacturing is necessary. The thickness of the raw scintillator material is mapped, and tiles are cut accordingly. Then they are individually weighted to determine their final thickness and given a location in the modules' interior so that thicknesses add up as close as possible for different sections.

All the tiles (except 2 every 4 in the EMC) have cutouts in their corners to leave room for the spacers. The spacer and cutouts represent less than 1% of dead space inside the modules

Optical transport

The light leaving the scintillator tiles is collected on the sides of the modules by $2\,mm$ thick sheets of a plastic material called wave length shifter (WLS) which receives the light with the wavelength leaving the scintillator and transports it at another wavelength.

The scintillation light produced by the shower of particles, crosses a small air gap and enters the WLS bar. The base material of the WLS is polymethyl methacrylate (PMMA), and is doped with a fluorescent dye, for several reasons [18] chosen to be Y-7. The light is absorbed by the dye molecules and reemited by fluorescence in a longer wave length (blue light is transformed into green).

Thus the light produced by all the scintillator tiles of one calorimeter section is added and measured together. The WLS bars carry the light all the way out to the back of the modules but only the surface directly opposite to the scintillator of the section to be readout actually receives light. The rest is wrapped in reflecting material so that no light gets lost. Figure 3.7 shows cut out of a module (FCAL) where the DU, scintillator

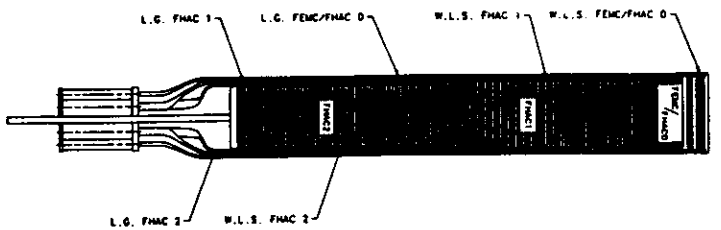


Figure 3.7: *Light readout arrangements. The uranium plates interleaved with the scintillator tiles as well as the WLS bars are shown. Note the gaps in the EMC part of the module, they leave space for the hadron-electron separator silicon detectors. (Figure from [19]).*

and WLS plates can be seen.

Figure 3.8 shows the emission and absorption spectra of the different optical components. For the materials and concentrations chosen enough radiation resistance for several years of operation, taking annealing effects into account, has been proven. Some UV absorbent is also added in the chemical mixture so as to reduce the Čerenkov light produced by particles traversing directly the WLS plates, which cannot be distinguished from the real scintillating light due to the absorption-fluorescence emission mechanism. This effect is specially important if the particles cross the bars longitudinally, and accounts to a big extent to the non-uniformities between adjacent calorimeter modules.

As in the case of the scintillator, a tight uniformity is required. It is achieved by using different concentration of dye on the longest plates and by having a correction pattern stamped on the back reflector which reduces the quantity of reflected light A 2% uniformity is achieved with all these precautions.

By internal reflections, the light is transported to the photomultiplier photocathode over distances varying between 0.25 m and 1.65 m depending on the calorimeter module and section.

Module assembly

For the FCAL and RCAL the DU plates and the scintillator tiles are stacked together onto a C-form frame which supports the ends of the DU plates. The diverse WLS needed to readout the different calorimeter section are mounted together in stainless steel cassettes which are attached at the sides of the stacks. The whole ensemble is held together by flexible stainless steel straps of $0.3\,mm$ thickness and ca. $20\,cm$ width. They are held and tensioned at the back beam of the module's frame [19].

For the BCAL modules a T-beam frame supports the stacked plates of the HAC sections with tensioning rods. The EMC section is strung with thin wires to a stainless

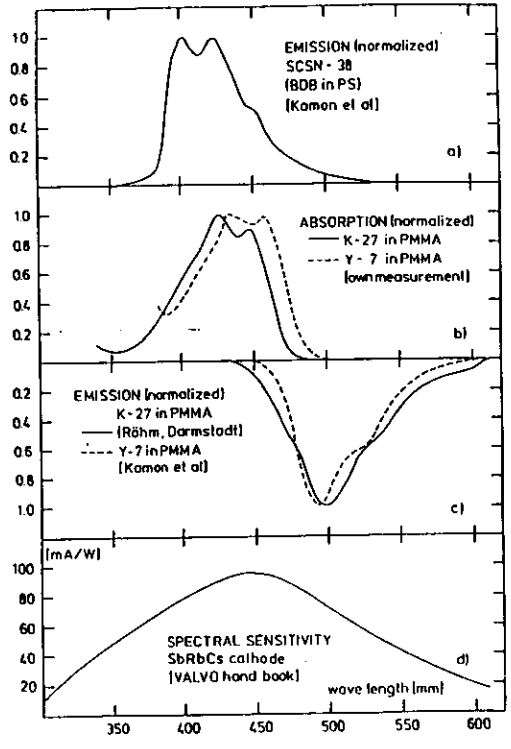


Figure 3.8: *Emission and absorption spectra of scintillator and WLS materials.*
a) Emission spectrum of SCSN-38 scintillator;
b) Absorbtion spectrum of K-27 and Y-7 in PMMA;
c) Emission spectrum of K-27 and Y-7 in PMMA;
d) Spectral sensitivity of a SbRbCs photocathode..

steel plate which is part of the frame.

3.4.3 Mounting

The entire calorimeter is made up of ca. 10.000 DU plates and around 240.000 scintillator tiles. The total construction weights around 700 tons and has ca. 12.000 readout channels.

The 80 modules have to be mounted together in the ZEUS detector.

The BCAL modules are mounted on two so-called *spokes wheels*, large aluminium disks which support also other detector components (see figure 2.22). These disks can be rotated at installation time to insert the one module at a time from above.

The FCAL and RCAL modules are mounted on platforms resting on the iron yoke of the detector, called *cradles*. They stand on the bottom side of their C-frame and are bolted to the cradles and in between them at the top of the backbeams.

In order to avoid major radiation damage to the optical components or the electronics and to ease installation, the cradles are split in two parts which can move by ca. 40 *cm* to the sides of the beam line. This will happen every time HERA is doing machine development or beam injection. Enough room is available inside the iron yoke so that the sideways movement can occur while remaining closed.

The straps, spacers, WLS and other mechanical components needed introduce dead space and non-uniformities. However, due to the construction method (straps tying the plates instead of rods holding them together) only about 6 to 7% of the space represents dead material.

Some precautions have been taken to improve the uniformity of the calorimeter across the modules' boundaries. The BCAL modules are tilted by 2.5° relative to a radius vector to the interaction point so that the boundaries are non-projective.

Also in between all the modules lead sheets will be installed. This helps to reduce the Čerenkov light produced when particles cross the WLS and which boost the measured signal producing large (up to 20%) non-uniformities when scanning across the boundaries. Thus the non uniformities are kept in the worst cases (0° incidence) at a level below 10%. Measurements have shown that 2.5 *mm* of lead in between the modules are needed.

3.4.4 The conversion of light into electric signal

The light collected by the WLS along all scintillator tiles in one calorimeter section is guided to the light sensitive cathode of a phototube installed in the frame of the calorimeter module. In order to couple the flat WLS to the round photocathode some forming is necessary. Out of the flat surface, strips are cut, bent and glued together so that a rectangular cross section contacts to the glass side of the photocathode.

The photomultipliers have quite tight specifications, the main ones are:

- 10 stage multiplication providing high gain (10^5 at 80% of the maximum voltage),

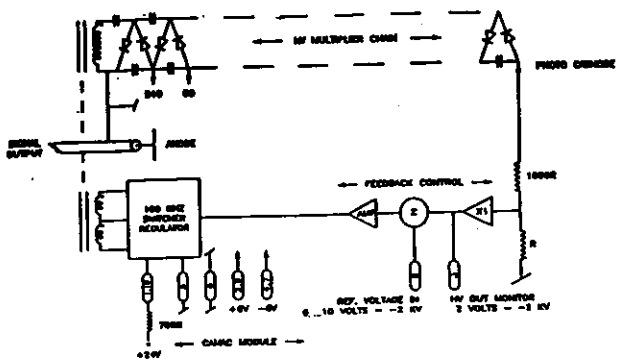


Figure 3.9: *Scheme of the Crockroft-Walton cascade generator to produce the high voltage at the dynodes of the PMTs. The regulator plus the HV chain are packed onto a base of a similar diameter as the PMT. The supply and control are located in a unit placed nearby the modules.*

- small nonlinearity ($\pm 2\%$ up to $100\,mA$ pulse anode current),
- small dark current and noise ($\sim 0.1\,nA$ at $20°C$),
- stable gain over short periods (hours) ($\pm 3\%$).

The tubes for the HAC sections are of the Hamamatsu R-580 type, with a photocathode diameter of $34\,mm$. The space constraints for the electromagnetic tubes in the FCAL only, are much tighter and only very small tubes are possible. Valvo's XP-1911 are used, they have an diameter of only $19\,mm$ (photocathode $14\,mm$).

The high voltage at the dynodes of the PMTs is produced by active bases using a "cascade multiplicator" following the principle of the Crockroft-Walton generator (see figure 3.9). They are based on a ladder of capacitors to increase the voltage on escalating dynodes, separated by diodes to hold it and rectify the voltages to DC. The base-PMT as a unit receives a low supply DC voltage (typically 15 V) and returns a monitor signal proportional (1000:1) to the high voltage at the cathode. A coaxial cable comes out with the anode signal. The main advantage of this type of base is a much reduced power dissipation, 0.1 W at the base against 1 - 2 W of usual resistive bases. Also no HV[5] cables are needed, a quite important security feature for installation when tons of uranium are building the calorimeter.

The supply voltage and the return monitor signals connect both to a computer governed controller unit placed inside the detector, at the sides of the calorimeter, distant at the most $5\,m$ from the tubes.

A typical energy deposition in the calorimeter results in a current signal out of the PMT anode with a typical width of $20\,ns$ for electrons ($30\,ns$ for hadrons) like in

[5] High Voltage

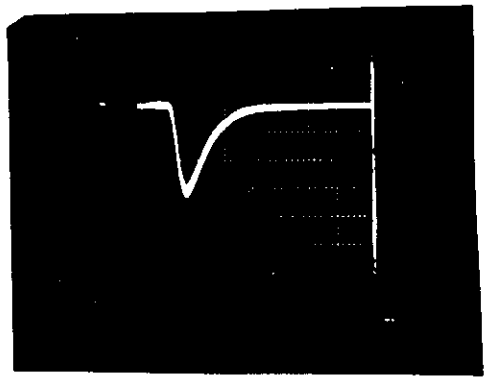


Figure 3.10: *Typical shape of a PMT (Valvo XP-1911) pulse for electrons. (20 ns/div, 200 mV/div). The rising edge of the signal is mainly given by the PMT response (plus capacitive load of cables ...) while the falling edge is due to light decay in the scintillator, WLS ....*

figure 3.10.

Most of this current (AC signal) is dumped onto a terminating impedance while some small fraction of it enters the diverse channels of the calorimeter electronics and is thus the starting point of the rest of this document.

Chapter 4

Readout for the ZEUS Calorimeter

After having presented how the ZEUS calorimeter is constructed in order to produce the best possible energy measurements, now the electronic system used to actually quantify the signals will be described.

4.1 Calorimeter information

Two quantities are required from the calorimeter. The first is the measurement of the "total"[1] energy deposited in the calorimeter by the incoming particles, where the amount should be known as the sum of quantities of the independent subcalorimeters (EMC, HAC1, HAC2) and sections. In combination with the tracking devices for the charged particles and on its own for the neutral ones, the calorimeter is used for position and angle measurements and electron identification. Finally, we want a precise determination of the time the particles reached the calorimeter.

The signal we obtain is the charge arriving at the anode of the PMT. The measurement of the energy of the incoming particles is possible due to the fact that the measured charge is proportional to the deposited energy. As discussed in the previous chapter, a large effort has been invested in achieving this proportionality independent of the amount of energy and the localization of the deposition inside the calorimeter.

In a simplified way it can be considered as a series of constants of the diverse efficiencies and gains of the readout chain being applied on the incoming energy (arbitrary symbols) :

$$Q_{anode} = g_{pmt} \cdot \epsilon_{wls} \cdot \epsilon_{scintillator} \cdot \alpha_{sampling} \cdot \gamma_{visible} \cdot E_{in}$$

The risetime of this current is very short, typically a few nanoseconds, and happens a constant time (the transit time in the PMT) after the particles crossed the calorimeter, so it can be used to determine the time of the energy deposition even if small variations in time-of-flight, scintillator and WLS light response produce an smearing of the signals.

[1] "Total" understood in the sense of the sampling calorimeter where only a fraction of the energy is detected.

4.2 Boundary conditions for the readout at ZEUS

The electronics for the readout of the ZEUS calorimeter must fulfill several requirements :

- cover the full dynamic range of energies which can be originated at HERA collisions;
- provide an energy measurement with the required segmentation. The noise factor should not be dominating in comparison with other noise sources;
- resolve the timing of the energy deposition to about $1\,ns$ or better, mainly for rejection of comic rays and other background;
- implement the calibration method of the calorimeter with the DU radioactivity to better than the 1%;
- cope with the $96\,ns$ bunch crossing time of HERA with minimum dead time;
- provide information for the different levels of the trigger system within the required time windows.

Some of these constraints introduce novel factors in the electronics with methods and solutions being used for the first time in experimental high energy physics. A description in some detail follows.

4.2.1 Dynamic range

The kinematics of the HERA machine determine the energy range to be seen in the ZEUS Calorimeter. The upper limit will occur in the forward, proton, direction where energies up to $400\,GeV$ (see figure 3.4)[2] will be deposited in the electromagnetic part of the calorimeter. On the other hand, minimum ionizing particles like muons will deposit (in the EMC) the equivalent of $300\,MeV$ electron energy. These small signals are important for calibration and diagnoses purposes[3]. We require them to be measured with an accuracy of 3 to $5\,MeV$ resulting in a mean digitization signal around channel 100. Compared to this value, the $400\,GeV$ signals are around $1.5 \cdot 10^5$ times bigger. Thus the required dynamic range is equivalent to roughly 17 bits.

[2] In the immediate neighbourhood of the forward beam pipe jets can reach even 700 or $800\,GeV$ though not the full energy will be deposited in one section.

[3] Another reason for having a precision level below $10\,MeV$ is the need to add ~ 12000 signals to get the total energy in the calorimeter. As the energy depositions are localised in "clusters", most of these signals will be zero and a wrong measurement of these would yield a large systematic error in the final result.

4.2.2 Noise and DU radioactivity

The electronics intrinsic noise has to be kept small so as not to dominate on the energy resolution of the calorimeter. Also coherent noise from external sources has to be suppressed. The limit is given be the signals produced by the DU-radioactivity.

Short cables joining the PMTs' output to the input of the electronics are a necessity to keep the pickup small. This leads to first stage electronics being mounted in the direct neighborhood of the PMTs, e.g. in the calorimeter's backbeam.

On the other hand calorimeter studies [20] have shown that the signals produced by the natural radioactivity can be used as an excellent tool to monitor the calibration of the calorimeter. Therefore its mean value has to be measured with $\sim 1\%$ precision. This is achieved by integrating the signal over a larger time interval.

4.2.3 Timing

The determination of the time at which the energy deposition occurred in the calorimeter is an information necessary in order to be able to screen out signals coming from backgrounds like cosmic rays. The required precision is of the order of $1\,ns$ as real signals can come in integer multiples of the bunch crossing time, $96\,ns$ and a good rejection of off-time events[4] is needed. The PMT signal appears a constant time after the $e-p$ interaction has happened, dependant mostly on the type of phototube and its high voltage.

4.2.4 Bunch crossing time

In HERA electrons and protons can collide every $96\,ns$ giving thus a high luminosity.

The bunch crossing time is on the same scale as the detector response time. Events signals can thus overlap in time producing a degradation of the information.

The quantity of $96\,ns$ is several orders of magnitude below the bunch crossing times of existing colliders but already longer than others being planned.

This fact is one of the most innovative and challenging of HERA, and certainly the most novel one what concerns detector readout.

4.2.5 Triggering

The aim of a detector at HERA is to observe the physics processes occurring in an $e-p$ interaction. However, the interesting events are only a small fraction of all those taking place. Backgrounds come from the electron beam, e.g. synchrotron radiation; from the proton beam, e.g. beam-gas interactions; and from photoproduction or other sources like cosmic rays. These background sources have different rates, but can add up to an order of magnitude of $100\,kHz$ [21] while interesting events represent 2-3 Hz rate.

[4] With $\sim 1\,ns$ time resolution one can in principle determine the direction of particles and check if they were originated at the interaction point.

There is certainly no system which can record such an amount of information[5] for later analysis and in any case one needs to notice that an event (no matter if interesting or background) has indeed occurred to proceed with the recording.

The device which recognizes if an event has taken place is called the trigger logic, in this case a whole trigger system. In fact it also discriminates at least a sizeable fraction of the background events and rejects them. An example of a trigger process is the missing transverse momentum (P_T) trigger where the P_T of all the particles produced at the interaction is measured and added up. A non zero P_T sum is interpreted as a signature of an interesting event which should be recorded. The measurement does not need to be performed with ultimate accuracy and the non-zero result has only to be incompatible with the experimental error.

A trigger decision can be taken in a very fast way. This however would not be very selective and in a high background environment, of the selected events, still only a small fraction would be of interest. A more discriminating trigger decision needs longer time as we also want to keep all (or nearly all) of the interesting events, i.e. have a high (99%) trigger efficiency.

An efficient and selective trigger combining information from several of the ZEUS subdetectors clearly cannot be produced in the time remaining until the next bunch crossing [22] so that the calorimeter information, in the same way as the information from all the other components, has to be stored while the triggering process concludes.

At ZEUS, the trigger process [23] is divided into three steps (First, Second and Third Level triggers) each one operating upon decreasing number of events with increasingly detailed information and tools. They reduce the event rate to approximately $1\,kHz$, $100\,Hz$, and $3-5\,Hz$ respectively.

4.3 Pipelining

The storage of signals while the trigger process is operating typically acts as a FIFO[6] system which can also be seen as a "pipeline" where the information is introduced on one side at a constant rate, $96\,ns$, and continuously pushed forward to leave place for new data.

If the trigger decision is positive, the data must be recovered from the pipeline; if this is not the case, it will just drop out at the end.

The solid state implementation of pipelines looks more like a cyclic ring buffer which is continuously being overwritten until it is stopped and readout by a trigger.

Here, the *pipelining* concept is mentioned for the first time and though it is not a new concept in readout at physics experiments[7], it is the first time such a wide use of

[5] The amount would be equal to the rate times the size of each event
i.e. $\mathcal{O}(100)\,kHz \times \mathcal{O}(100)\,kBytes = \mathcal{O}(10)\,GBytes/second$.

[6] First In First Out

[7] In fact most particle physics experiments require a pipeline to hold the data while it's being decided if it is worth keeping or not. Usually the pipeline are the cables themselves which carry the readout signal and which are made longer than necessary. Of course with $5\,ns$ of delay per meter of expensive

pipelining techniques is necessary.

4.4 Typical solutions for readout

All the subdetectors of ZEUS have the same time constraints for their readout :

- $e - p$ interactions and other beam related events like beam gas, can occur synchronously at every bunch crossing, i.e. in $96\,ns$ time intervals;
- background events like comics are asynchronous;
- triggering (a process needing one order of magnitude more time than the beam crossing) is needed to reduce the data recording rate. During this time the information has to be stored to avoid dead time losses.

They also share the events they want to see, all coming from the same $e - p$ collision.

However they differ in the type and dynamic range of the signals. For example the energy range of the collisions' products maps into a 17 bit analog charge range (plus a timing information) in the calorimeter, while it might be a digital (1 bit) information for another component which only detects a hit or the absence of it and does not want or need to know its intensity. Another example is the different time the signals need to arrive at their front end electronics, while for the calorimeter this is some nanoseconds, it can be hundreds of nanoseconds of drift time in the gases of some tracking chambers.

These different requirements lead to different readout methods. As an example of a solution for readout, a brief description of the readout electronics for several of the tracking chambers used in the ZEUS detector will be given [24]. One can regard it as an alternative to the concept adopted for the calorimeter.

The signal coming from the wires is amplified and shaped locally then transmitted to the Rucksack (50 m) to a receiving amplifier which also reshapes it again. The signal is then sampled and digitized by an 8 bit range flash analog to digital converter (FADC) every $9.6\,ns$. Several points in the risetime of the signal are thus recorded and with it precise timing (equivalent to hit coordinate) measurements. The result of these digitizations are written into fast random access memories (RAM) implemented in ECL devices, with a depth of 1024 steps. This digital storage pipeline thus holds the history of the past $9.8\,\mu s$ of the detector signals. A very quick analysis of some "hit flags" gives a first information on tracks to the triggering system. Upon the receipt of a trigger the relevant data is passed to another RAM bank and the pipeline storage RAM starts again to be written at location zero.

This front-end electronics concept fulfills the requirements of tracking detectors : high speed, low noise, 8 bits dynamic range, calibration. This system has some important implications :

high quality cable this is only a possible solution if the number of channels is not very large and the trigger delay is in the ns range.

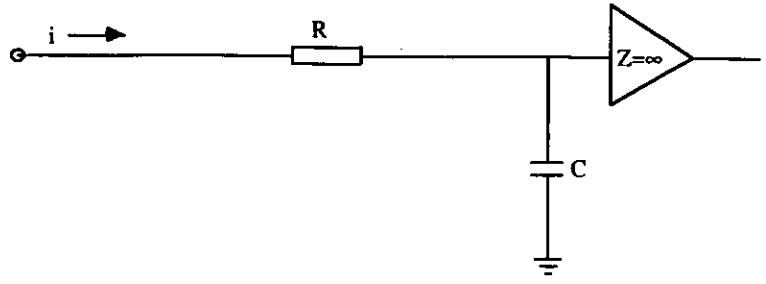


Figure 4.1: *Integrating network formed by a resistor and a capacitor.*

- the localization of the electronics far away from the detector means that at least one cable per readout channel has to be carried over a long distance, this is expensive and requires large space;
- one FADC is needed for every channel, which is also expensive and consumes a lot of power;
- fast RAM is a cheap and simple pipelining method, but typically also quite power consuming[6];

The different demands for calorimetry require different solutions.

An alternative concept, the one used in the ZEUS calorimeter will be presented in the next section.

4.5 Analog measurement methods

The calorimeter information arrives to the electronics in the form of a current signal with a width of several ns and with an amplitude into $50\,\Omega$ varying from some mV to many volts (see figure 3.10).

4.5.1 Analog measurement of charge

The electric measurement of the integral of a pulse current is in principle simple, one inputs it into a network of a capacitor in series with a resistor as in figure 4.1, and when the current reaches zero, the capacitor has a stable voltage which can be measured. The final capacitor voltage is independent of the resistance if enough time is allowed:

$$V_c = \frac{1}{C} \cdot \int i\,dt$$

The voltage can be measured e.g. by the Wilkinson method, discharging the capacitor at a constant current, and counting the time this takes with a fast (e.g. $20\,MHz$) scaler.

[6]Typical consumption of a board with FADCs, RAMs and control is $100\,W/16$ *channels*.

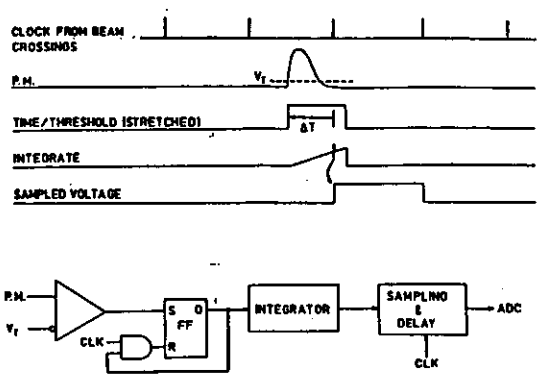


Figure 4.2: *Conventional method of measuring the arrival time of a signal.*

This apparatus called the integrating ADC is the standard method used in high energy physics [25].

The measurement for high resolution high rate requirements is however not as simple as this. The integration of the current through a capacitor poses two problems. First by integrating the current, we lose the timing information. Second, the process of discharging the capacitor even if the counting is performed fast takes of the order of $100\,\mu s$ which is too long to prepare the capacitor for the next incoming current (from the next particle interaction).

Another method to measure the stored voltage is to use a sample and hold circuit in front of a conventional successive approximation ADC[9]. The problem arises when the voltage is already in HOLD state, the capacitor has to be discharged, if not, the next current will be integrated on top. This action, the so-called restoration of the baseline is the main problem if it has to be performed to a high precision.

An intermediate solution is to add a differentiating stage to the integrating network so that once the voltage has reached the top, the baseline is restored by the differentiation. The whole electronics network is called *shaper* due to the fact that it 'shapes' the incoming signal into another one where the peak represents its integral, but returns the output to zero after a short time. The actual measurement of the voltage is performed by a sample and hold device which points at the peak of the shaped signal.

4.5.2 Analog measurement of time

A typical method to measure the timing of a signal relative to a clock is shown in figure 4.2. The arrival of the signal from the detector (when surpassing a threshold V_T) causes the start of a ramp, the voltage of which is measured (e.g. sampled and held) at

[9]Using a FADC here is also a possible solution.

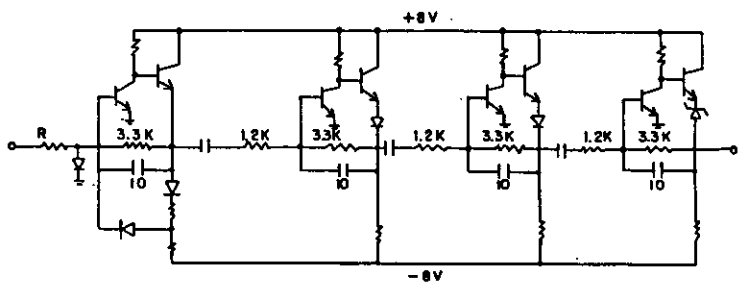


Figure 4.3: *Four stage circuit used to shape the PMT's signal.*

the arrival of the following clock edge. This voltage is thus proportional to the difference in time between the arrival of the detector signal and the next clock.

This method however requires some extra electronics for every channel, the comparator, ramp generator and sample and hold device. Also the linear ramp has to be reset, a problem similar to the integrating ADC charge measuring setup.

An alternative method to this will be presented in the next section.

4.6 Analog solutions at the ZEUS calorimeter

The analog electronics for the ZEUS calorimeter is built around the shaping and sampling principle [26,27,28] which has been shortly presented in the previous section and along with its physical implementation will be discussed now.

4.6.1 Shaping-sampling method for charge and time measurement

As discussed above, the information extracted from the detector signal will be charge and time. Other information embedded in the detector signal, like for example, the exact pulse form [29], though possible to study, will not be covered in this document.

The typical pulse coming from deposited energy in the calorimeter at the output of the photomultiplier has the shape shown in figure 3.10. Measuring the integral of this signal gives the charge produced.

The shaping method used for the ZEUS calorimeter integrates and differentiates the signal recursively four times using a circuit shown in figure 4.3 with equal time constants. The peaking time of such a shaping network[10] [30], occurs at N-1 (N being the number of integrations/differentiations) times the time constant used, in our case

[10]The analytical descriptions of these networks are typically presented as response to a Dirac-δ signal, i.e. their transfer function. We use them however with other input signals with a small but finite width. The output would be in fact the convolution of the input with the transfer function.

$3 \times 33\,ns$. The shapes of the signals at the different stages are shown in figure 4.4. We then take measurements of voltage at several points along this signal so that we are capable of reconstructing the height and time of the signal. The charge information is contained in the height of the peak, so we could try to sample at the peak of the signal.

Jitter error might however occur due to shifts in time between the clock we use to sample and the signal itself. A better jitter robustness of the shaping-sampling principle can be achieved if we take two samples on the signal instead of one. Taking them on opposite sides of the peak and adding them, can compensate the error introduced by the jitter as long as the interval between samplings remains constant. A jitter free number is obtained from a combination of the two samples weighted with the slopes of the pulse on each side. This number is also proportional to the input charge.

It is also necessary to take a height measurement of the samples relative to the baseline so that any low frequency coherent noise which might add to the signal is cancelled out as it adds to both the baseline and the pulse samples.

As for the time measurement, what we need is instead of a jitter insensitive algorithm another method which gives a quantity with big dependence on time shifts. We can combine also the two samples taken, but instead of adding them, we can take their ratio or difference and here the time shifts will not compensate but will be emphasized.

Further discussions on reconstruction methods to calculate the charge and time, can be found in Chapter 7.

However efficient this shaping-sampling scheme might be, it is nevertheless a compromise as it degrades the speed of the detector. The detector delivers a very fast signal lasting for a very short time (see figure 3.10) whereas the shaped pulse (figure 4.4) is longer than the $96\,ns$ HERA bunch interval. Thus signals from adjacent bunch crossings will overlap resulting in degraded performance. The principle seems therefore to be in conflict with the collision rate and its viability is only due to the fact that the probability of two interactions in one beam crossing (or in two successive ones) giving energy in one calorimeter cell is low. By measuring the baseline before the pulse, pile-up events can be recognised and if required rejected.

4.6.2 Analog range

The constraints mentioned in section 4.2.1 yield a dynamic range of $1.5 \cdot 10^5$ equivalent to ~ 17 bits. Commercially available fast analog to digital converters have usually a 12 bit range. There exist some devices with larger ranges (16 bit), but their low speed makes them impossible to use in experiments.

The solution adopted at ZEUS foresees the division of the full dynamic range into two parts, one of them covering low energies up to $20\,GeV$ with high precision and the other one the full range with coarser energy bin-size. The splitting occurs at the shaping unit. Two shaper networks are used each one with a different gain, accomplished by having different input impedances. So when the low energy range saturates we still can

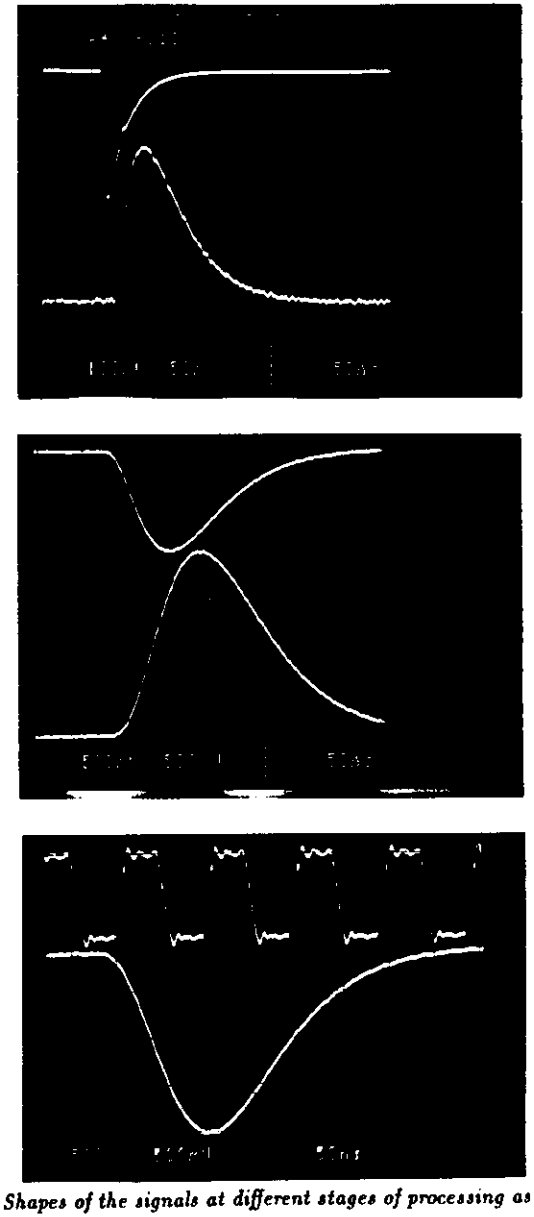


Figure 4.4: *Shapes of the signals at different stages of processing as measured on nodes of the circuit of figure 4.3.*

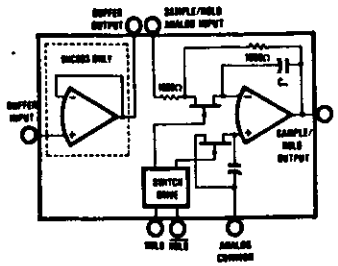


Figure 4.5: *Schematics of a commercial Sample and Hold device.*

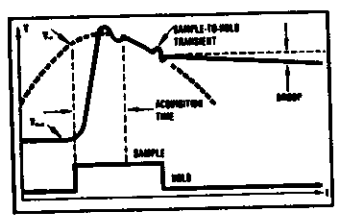


Figure 4.6: *Track, Sample and Hold voltages.*

digitize the signal at the other range. The intercalibration of the two ranges is done at the overlapping energies. This splitting doubles the amount of channels to readout. Note that the simplest electronics resolution could follow a $\sqrt{E}$ rule as the precision of energy measurement goes with this function, as we have seen. However a non linear scale is a very difficult method to work with (e.g. for pedestal subtraction).

4.6.3 Analog pipelining

The need for storing or delaying the analog signal by the amount of time required to reach a trigger decision has been discussed. In section 4.4, a typical *digital* solution for pipelining was presented. Some features were shown which concluded why this concept would not be a feasible solution for the pipelining of the ZEUS calorimeter.

An *analog* solution for pipelining will be presented, the heart of it being an analog pipeline VLSI[11] integrated circuit. As discussed in section 4.6.1, also a device is needed which samples the shaped signal at several points so the best solution is the combination of the two functions, a system which samples the signal and stores the sample for several microseconds.

A sample and hold device is basically no more than a capacitor connected to the input with a switch as shown in figure 4.5. When the switch opens, the capacitor holds

[11] Very Large Scale Integration

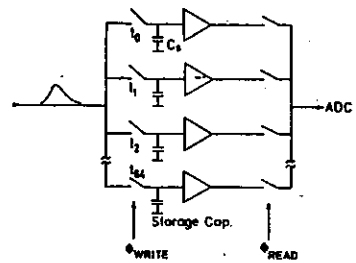


Figure 4.7: *Schematic of an analog pipeline (following [31]).*

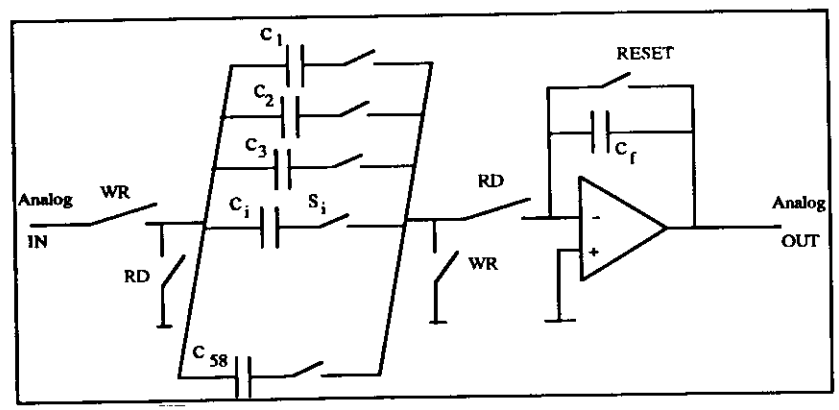


Figure 4.8: *Schematic of the ZEUS analog pipeline circuit.*

the voltage between its plates at that moment as seen in figure 4.6. If the capacitor has no leakage of its charge to ground, the switch has an infinite off resistance, and the buffer downstream has also an infinite input impedance, the capacitor will hold the sampled voltage forever. Real devices can hold the charge several milliseconds without losing more than 1% of it. With a series of switches and capacitors and addressing each one after the other, we can have a set of samples on the signal and keep them for the needed time until we want to read them out. The organization could be like the one shown in figure 4.7.

The real pipeline for the ZEUS calorimeter is an ASIC[12] which actually follows this principle but has all the storage cells connected to the same readout operational amplifier. It is wired in a negative feedback loop. Its scheme can be seen in figure 4.8. When sampling the analog signal, the input is connected to the series of capacitors, but

[12] Application Specific Integrated Circuit, equivalent term to *full custom* device.

only one of them has at a time its other plate connected through a closed switch to a defined voltage (ground) so that current can flow and the capacitor charges up. The other capacitors are floating and hold the charge received on previous samples.

The charging of the capacitor takes place through a connection line and two closed switches, all of which represent an equivalent resistance R and capacitance in the path of the current. The circuit is then not different than the one drawn in figure 4.1. The capacitor charges with the time constant $R \cdot C$. Due to this fact, to make sure that it reaches the voltage held at its input, it should not be disconnected before a time of several time constants has passed. In practice, this time constant is quite small (few nanoseconds) because the capacitor is small ($1\,pF$) and the whole resistance represents a few kΩ. This, along with other problems in the design of the circuit will be discussed in the next chapter.

Switching from one capacitor to the next results in sampling the input at several points in time. The total depth of this 'memory', which is equivalent to the 'length' of the pipeline or the amount of delay is given by the number of cells times the time used to switch from one cell to the next, i.e. the number of cells divided by the switching clock frequency.

The analog pipeline concept was pursued for the ZEUS calorimeter since the beginning, however alternative pipeline devices were considered [32] and prototypes were built [33]. The switched capacitor principle was the one followed mainly because of its simplicity as well as better performance (specially better linearity and smaller power consumption) and superior radiation hardness of the first test circuits.

4.6.4 Analog buffering

In addition to the problem of pile-up presented in section 4.6.1, which happens in the detector at input time into the pipeline, a second timing conflict exists when exiting the pipeline.

When a trigger decision is positive the information from the calorimeter, stored in the pipeline, has to be read out and digitized for further analysis. Of course, only the relevant part of the pipeline has to be digitized, but for the process of reading out the information the pipeline's input is disconnected from the shaper output. During this readout time the electronics is not sensitive to the detector output and any information produced there is lost. This is called the 'dead-time' of the calorimeter although it is due to the electronics and has to be avoided or at least minimized.

The amount of dead-time is given mainly by the digitization time of one voltage sample, which for the required (see section 4.2.1) 12 bits, is around $1\,\mu s$. This value has to be multiplied by the number of voltage samples we need to digitize[13]. Of course, the dead-time is only relevant if compared to the time between triggers. Considering

[13]Strictly speaking the time length of the pipeline has to be included in the deadtime since the readout of one event clears the rest of the memory

the expected $1\,kHz$ rate at ZEUS and the 8 samples to be digitized, we come up with approximately $8\,\mu s$ compared to $1000\,\mu s$, which is below 1%. However this is achieved only if every channel is equipped with one ADC device, which is unrealistic due to the number of channels and their costs. Thus this 1% has to be multiplied by the ratio of ADC devices to readout channels, for the ZEUS calorimeter this ratio is 1:12. This gives a deadtime of $12 \times 8\,\mu s \simeq 100\,\mu s$ which represents a factor of 10% which is no longer acceptable and requires extra electronics to reduce it.

A buffer system should provide an intermediate storage during processing for the relevant data so that the pipeline can be restarted again. It has to be an analog device to save the digitization time and it has to be cheap so that every channel can be equipped with one. The storage has to hold at least the number of samples we later want to digitize during the time of this digitization. The solution adopted is an implementation with the same principle of the switched capacitor sample and hold circuit as in the pipeline using as many cells as we want to digitize. This is called the *analog buffer*.

Upon receipt of a trigger the cells containing the information of the event which originated it are readout into the buffer cells. After this, in parallel to the readout and digitization of that information, the main pipeline can be restarted so that the detector output is again sampled and stored thus decreasing the deadtime to the amount required to transfer the samples from the main pipeline to the analog buffer. This analog transfer occurs also approximately[14] at a speed of $1\,\mu s$ per cell, so the 1% deadtime with the mentioned trigger rate of $1\,kHz$ can be maintained. As there is one buffer per pipeline channel, the transfer time is independent upon the number of channels and so at $1\,kHz$ trigger rate the deadtime is no more determined by the ratio of ADC devices to channels although at higher rates this would be again a limiting factor.

4.6.5 Analog multiplexing and DU current measurement

As already commented, due to several reasons (power, cost, cable space ...) it is not realistic to have one ADC device digitizing every readout channel. Thus the need to connect several analog channels to one ADC arises. This function is performed by a component called *multiplexer* which switches several inputs to one output, the switching control signal being a set of addresses giving a channel number in some code or an incrementing clock to step through the input channels. Typical commercial characteristics of multiplexers include few hundred Ω on-resistance, $T\Omega$ off-resistance and $\mathcal{O}(10)\,ns$ switching time.

The natural solution for the analog readout at ZEUS is to couple the multiplexing device with the intermediate analog buffer in a monolithic component which takes care of the analog signal after the trigger has happened. The analog buffer-multiplexer chip is a second ASIC which has been developed for the ZEUS calorimeter.

[14]In fact the reading of the pipeline is performed at a rate of $1.7\,\mu s$ to allow a final settling of the operational amplifier in the pipeline and reseting of the feedback capacitor (see next chapter).

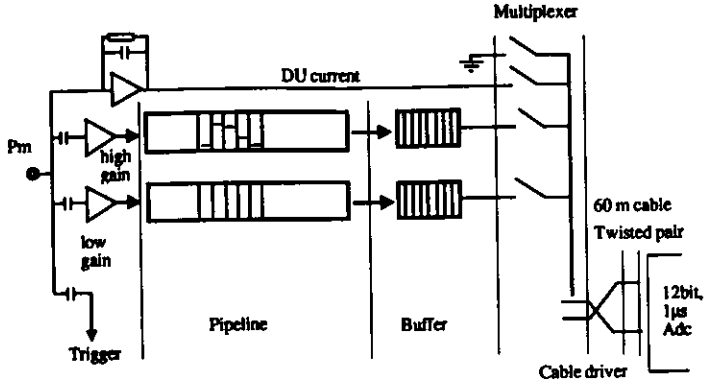


Figure 4.9: *Schematics of the complete analog chain.*

The entire analog chain is shown in figure 4.9 including the part used in measuring the DU current.

4.6.6 DU current

The uranium noise (UNO) is due to low energy photons and electrons originated at the DU plates and emerging out of the steel cladding which surrounds them. These particles enter the scintillator and produce light which cannot be prevented. Measurements [34] model these pulses as having a mean rate of $\sim 2\,MHz$ in the EMC ($10\,MHz$ in the HAC) and an exponential energy distribution with a mean value of $6,7\,Mev$. The rates and the mean energy vary with the cladding thickness.

To use these signals as a calibration tool for the calorimeter sections, the signal is averaged with a time constant ($20\,ms$) much larger than the rate so that single measurements give a precision better than 1%.

It has been shown [26] that this noise does not degrade the performance of the shaping-sampling scheme for charge and time measurement.

A current to voltage converter integrates the current with a time constant of 20 ms. This voltage is sent to the ADC through the same multiplexer as the sampled voltages in the pipeline. The precision of the conversion depends on the tolerance of the integrating resistor R_{DU} which is of 0.1%.

4.7 Triggering the analog electronics

The trigger system, in order to reach a decision, receives part of the detected signal in the calorimeter. It also has to accept information from other detector components [23]. This trigger evaluation takes some time $\mathcal{O}(\mu s)$, therefore the trigger process itself has also to be constructed as a pipeline accepting incoming information every $96\,ns$ and performing every step with at least this repetition rate.

Part of the current (5%) produced by the calorimeter PMTs is directed to the input of this trigger system where initially an analog sum of currents is performed resulting in an addition of deposited energy in different sections of the calorimeter, still retaining some geometric resolution. These sums are digitized by FADCs operating at $10.4\,MHz$ with 8 bit precision placed in the Rucksack [35].

The calorimeter is subdivided into 16 regions, and at this level by hard-wired digital operations [36] several processes are performed and a total of 0.5 kB of data is produced:

- the quantities E (energy), E_x (transverse x-energy), E_y (transverse y-energy) are calculated for the electromagnetic and hadronic sections.
- some coarse calculation of the energy is performed for portions of the calorimeter regions. Both the portions as well as the threshold values are programmable.
- a quick analysis takes places to determine if isolated leptons can be identified.

The fact that the trigger system accepts data every $96\,ns$ and that the calculation of all the above mentioned quantities lasts[15] for about $1\,\mu s$, means that at any given moment data from the last ten beam crossings are in the system. This data is being clocked through the different stages at least at a rate of $10.4\,MHz$ which is also a good example of a pipelined system. Note that the trigger system is a dead-time-less device, it never stops accepting input information.

These quantities mentioned above, calculated for every region, are passed for global analysis and regional comparison to a processing system which calculates and records some meaningful global information like the total number of isolated muons, total electromagnetic energy deposition.

This global system accepts the first analysis results from every component arriving in a synchronized way so that they all refer to the same beam crossing. The output of this global trigger (GFLT[16]) is a logical ACCEPT signal, generated a fixed time ($4.6\,\mu s$) after the bunch crossing it refers to.

A positive ACCEPT causes the calorimeter and every other component to read out the part of the pipeline corresponding to the bunch crossing required.

Monte Carlo predictions foresee that the rate of the first level trigger is around $1\,kHz$. However, most of these events will be beam-gas interactions, uninteresting for physics.

4.8 Digital processing

Upon leaving the front end electronics the information from the calorimeter has to be digitized and additional filtering is necessary.

[15] In addition to the calculations, time is required for the analog to digital conversions and some trigger logic. In total the calorimeter first level trigger needs a total of $2.2\,\mu s$ after the crossing occurred to pass its conclusions to the GFLT [22].

[16] Global First Level Trigger

4.8.1 Digital conversion

When the transfer of the samples from the pipeline is finished, the buffer device is set to the read state and all (or only part of) the voltages taken along the shaped pulse kept in the buffer cells are put out through the multiplexer part and driven with a push-pull cable driver circuit through $\sim 60\,m$ of twisted pair cable to the Rucksack. Here, the complementary voltages are received on the so-called "digital cards" by a differential amplifier whose output is connected to an ADC chip. This device digitizes the voltage at the input with 12 bit precision at a rate of $1\,MHz$. The conversions are written into successive RAM locations.

There is a one to one connectivity between buffer-multiplexer chips and ADC chips.

4.8.2 Digital operations

The raw digitized information written into the RAM is picked up by a Digital Signal Processor (DSP), a fast microprocessor specially conceived to perform few simple operations at very high speed. The DSP applies corrections to the measurements which are necessary because of the imperfections of the pipeline and buffer discussed in the next two chapters.

Furthermore, following the guidelines presented in section 4.6.1, the DSP also performs a combination of the samples, also quite simple operations, and calculates the energy deposited as seen by each phototube and the arrival time of the signal at each channel. This information is written into memory for use by the second level trigger (SLT).

4.8.3 Calorimeter Fast Clear

The First Level Trigger discussed in section 4.2.5 is a process which is performed in a pipelined fashion. Every $96\,ns$ a step of the action has to take place so that no event piling occurs. This condition and the $2.2\,\mu s$ time constraint limit of course the possibilities of the FLT. In order to keep the rate at the estimated $1\,kHz$ for the SLT a dedicated system called the Calorimeter Fast Clear [37] is foreseen.

The Fast Clear system is a hard wired custom built digital processor. It receives digital data produced by the FLT FADCs and applies a cluster searching algorithm operating in parallel over the regions of the calorimeter.

This analysis is performed while the calorimeter's control system is shipping the analog data from the buffers to the ADCs and being digitized. The digitization of the analog data takes $\sim 108\,\mu s$ so if the Fast Clear system can decide after some tens of microseconds that the event is not worth any further analysis, there is no point in finalizing the conversions. This saves dead time introduced by the digital processing and work to the SLT. When the search process is finished the type found for the event is passed to the GFLT box which decides if to issue or not the ABORT operation.

The Fast Clear system needs more or less time to reach a decision depending on the

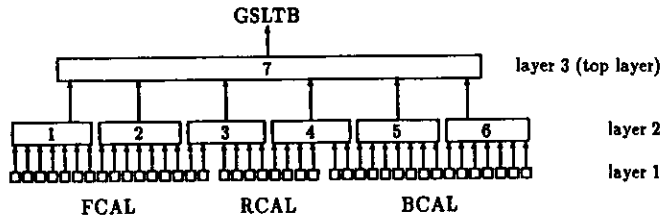


Figure 4.10: *Layout of the readout and second level trigger network. Each box represents one 2TP-VME module.*

type of the event and the number of clusters. For a beam gas event it is predicted to last between 19 and $23\,\mu s$.

4.8.4 Second Level Trigger

The energies and times generated by the DSP are quantities related to each PMT. Decisions on possible physics of events have to be taken on the basis of the whole calorimeter or even combining the information coming from several subdetectors. After the analysis performed by the FLT, the Second Level Trigger (SLT) [21] and Global Second Level Trigger (GSLT) [38] take their decisions with the full precision information.

The calculation of this information is performed in a three level network of transputers in VME modules (2TP-VME)[17].

The memories into which the DSPs write the calculated energies and times are readout by one of the two transputers of the 2TP-VME module. The information is passed to the other transputer which then calculates its part of the energy sums and clustering data. These transputers form the level 1 of the SLT network. They communicate to other transputers (level 2) which perform the operations at the calorimeter section (FCAL, BCAL, RCAL) level. A transputer module (level 3) connected to those in level 2 produces the final global numbers and communicates them to the GSLT. Figure 4.10 shows the layout of the readout and trigger network.

The SLT produces the following information :

- $E_{transverse}$ and $E_{longitudinal}$ (transverse and longitudinal energy sums),
- E_x,E_y (vector transverse energy sums in the x and y directions) as well as P_T (total missing transverse momentum),
- The number of clusters, defined by a significant amount of energy grouped on some contiguous sections of the calorimeter. For every cluster data like the type

[17] A transputer is a special sort of microprocessor with optimised connectivity produced by the INMOS company. At ZEUS, the transputers will be supported in the 2TP-VME board which houses two T800 transputers. This board has been developed by NIKHEF (Amsterdam).

(electromagnetic, muon or hadronic), the position and size of the cluster and the energy deposited in EMC and HAC sections is compiled. From Monte Carlo simulations the number of clusters is expected to be 2 to 5 for the average event.

The rate after the filtering of the GSLT is around 100 events per second, a reduction factor of 10 compared to the FLT is achieved.

4.8.5 Third level trigger

The rate of events coming out of the second level trigger is still much too high for any storage mechanism, 100 Hz with an event size of 150 kB, produce 15 MB of data every second.

The rate which can feasibly be recorded or sent to the main computer is 3 to 5 events per second. To reduce the number of events coming from the GSLT a more detailed analysis called the the Third Level Trigger (TLT) [39] has to be performed. This analysis is similar to the basic offline code classifying the events and performing global event reconstruction. After forming the complete event with the *EventBuilder* (EVB)[18][40], data is distributed to a set of processors working in parallel each one handling one event.

If the analysis yields the result that the event is worth keeping, the TLT system ships the data to the main computer where it is stored.

[18]The event builder is basically a programmable switch network which connects the readout of the different subdetectors to the TLT processors.

Chapter 5

Custom electronic components

As it has been shown in the preceding chapter, the specifications mainly in precision and dynamic range to be achieved in the ZEUS calorimeter imply an analog solution for the intermediate storage of the readout signals. The samples are stored in an analog form for the span of the delay needed for triggering.

Thus, the heart of the analog part of the electronics is made up of two integrated circuits, the analog delay line and the buffer-multiplexer. These two components are custom made for the ZEUS experiment and their construction, description, properties and testing will be the subject of this chapter.

The development was carried out in collaboration with the Fraunhofer Institute of Microelectronic Circuits and Systems[1] and the Nevis Laboratories[2] and references [41,42,43] document the design issues of the circuits, their evolution and results of the project.

5.1 Principles of (ideal) signal sampling

Figure 5.1 shows an ideal switch with an storage capacitor for waveform sampling. We will assume the switch is a *linear time-variant device* this means its resistance is only dependant on a control signal $V_s(t)$ called the sampling signal and not on its input $V_i(t)$ nor output $V_o(t)$ signals. Further on in this chapter we shall see how this can be almost achieved with real components.

As any component, the switch has a transfer function $h(t)$ which defined as the response to the unit impulse (a Dirac-δ function). An arbitrary input can be obtained by summing an infinite number of impulses of area equaling the input. The linearity of the device allows us to obtain its response as the sum of the responses to the impulses by applying the superposition theorem.

Let $u(t)$ be the unit impulse, an arbitrary input function $i(t)$ may be written as the

[1] Fraunhofer Institute of Microelectronics and Systems, Finkenstr. 61, D-4100 Duisburg 1, FRG. Contact persons are B. Hosticka and J. Möschen.

[2] Nevis Labs., Columbia University, New York, USA.

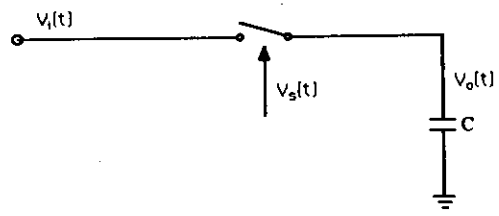


Figure 5.1: *Ideal analog switch with sampling capacitor.*

sum of many impulses weighted with $i(t)$:

$$i(t) = \int_{-\infty}^{+\infty} u(t-\tau) \cdot i(\tau)\, d\tau \tag{5.1}$$

and $h(t)$ the response to $u(t)$, the output $o(t)$ of this linear time invariant system is the convolution of the input with the transfer function :

$$o(t) = \int_{-\infty}^{+\infty} h(t-\tau) \cdot i(\tau)\, d\tau = i(t) * h(t)$$

This can be understood as a system with "memory" which "remembers" the output produced by the signal which entered it τ time ago and adds it together to the rest of its memory.

In our case seen in figure 5.1, we have $i(t) = V_i(t)$, $o(t) = V_o(t)$. If we say our switch is ideal, it has zero resistance when closed and it opens at $t = t_s$ then its transfer function is an impulse at t_s: $h(t_s - t) = \delta(t_s - t)$, so :

$$V_o(t_s) = \int_{-\infty}^{+\infty} \delta(t_s - \tau) \cdot V_i(\tau)\, dt = V_i(t_s) \tag{5.2}$$

which is no more than having sampled the input at t_s.

A non ideal switch will have an arbitrary transfer function w_s so :

$$V_o(t_s) = \int_{-\infty}^{+\infty} w_s(t_s - \tau) \cdot V_i(\tau)\, dt = w_s(t_s) * V_i(t_s) \tag{5.3}$$

but in the same way as equation 5.1 it can be written as :

$$V_o(t_s) = \int_{-\infty}^{+\infty} [w_s(t) * V_i(t)] \cdot \delta(t_s - t)\, dt. \tag{5.4}$$

This represents the conclusion that a non-ideal but linear switch can be considered as equivalent to a filter with response $w_s(t)$ followed by an ideal switch as shown in figure 5.2.

If the frequency of the input signal is much slower than the sampling time, at equation 5.3 the input signal can be considered constant and therefore can be removed from

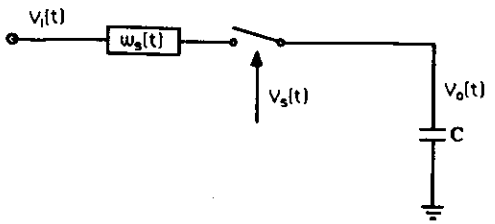


Figure 5.2: *Equivalent circuit to a real linear switch.*

the integral. Then the sampled signal is proportional to the input voltage even in the non-ideal but linear case

$$V_o(t_s) = V_i(t_s) \int_{-\infty}^{+\infty} w_s(t_s - t) \cdot dt \propto V_i(t_s).$$

Later it is shown how the realization of switches with real components performs with respect to the ideal switch. We will see that real switches are not linear time invariant systems because the input enters into the transfer function. However models with e.g. stepwise linear time invariant transfer functions can be implemented [44].

Sampling theory supports the choice of the sampling and shaping frequency used by the ZEUS calorimeter. In fact Shannon's sampling theorem [45,46] forces a sampling rate of double that of the maximum frequency in the input signal in order not to have aliasing[3]. As we saw in the previous chapter, the PMT signal is integrated and shaped so as to have a width (i.e. a smaller frequency, FWHM $\sim 200\,ns$) such that two successive samples ($96\,ns$ apart) are taken on opposite sides of the peak.

5.2 Integrated electronics

Analog systems using fast sampling techniques are not new in high energy physics experiments. Based on discrete components, large systems [47,48] have been used in experiments at SLAC and PETRA with good performance (12 bit precision with $20\,MHz$ sampling). However, power consumption and packing density make this approach inviable at the present generation of experiments.

Only integrated circuit techniques allow for a reduction of size, cost and power consumption of the electronics. This has gained importance in the 80's, starting with the readout of silicon microstrip detectors [49,50]. The first devices included signal integration, shaping and multiplexing. Further integration of signal processing functions has been required by the construction of new detectors with higher density and precision requirements and made possible by the development of integrated circuit technology.

[3] In sampling theory the term *aliasing* describes the process of spectral overlap by which a function can not be recovered from it's sampled data form and occurs because either the signal is not bandwidth-limited to a finite range or the sampling rate is too low.

For example, at SLAC, for the readout of drift chambers [51], the "Microstore" or "Analog Memory Unit (AMU)" was developed in the mid eighties [31,52]. The AMU samples and stores drift chamber wire signals keeping many samples on a pulse for precise pulse timing measurements. By using slow readout of the stored signals high precision digital conversion can be achieved. The ZEUS calorimeter group followed some of the concepts adopted in the AMU.

Usual integrated circuit technology can be divided into bipolar and field effect technologies. The later is dominated by the metal- oxide- semiconductor (MOS) technique though junction field effect transistors (JFET) play an important role in low-noise applications. Bipolar technology has its advantages, it is faster and devices have higher transconductance. MOS technology shows decisive qualities important for our application :

- the fabrication process is simple and well developed,
- very high integration of devices can be achieved,
- MOS transistors have very high input impedance,
- power consumption is low,
- noise is low (though JFETs perform better here),
- implementations of switches show almost ideal properties,
- integrated capacitors can be very precisely defined,
- it is possible to combine digital and analog circuits on the same piece of silicon.

5.3 Realization of components for an analog storage unit

The realization of the analog delay line requires mainly[4] two components : capacitors and switches. MOS techniques provide several alternatives for their fabrication which will be described in the following sections.

5.3.1 Capacitors

Fabrication of capacitors on an integrated circuit is a well controlled process using the standard MOS techniques : n or p doping, oxidation, polysilicon or metallization which also are needed for transistor production.

Two types of capacitors, shown in figure 5.3, are the most widely used in analog sampling applications. In both cases silicon oxide makes up the dielectric medium. The

[4] Operational amplifiers are also needed. They are basically made of transistors and the one used is briefly covered in section 5.5.3.

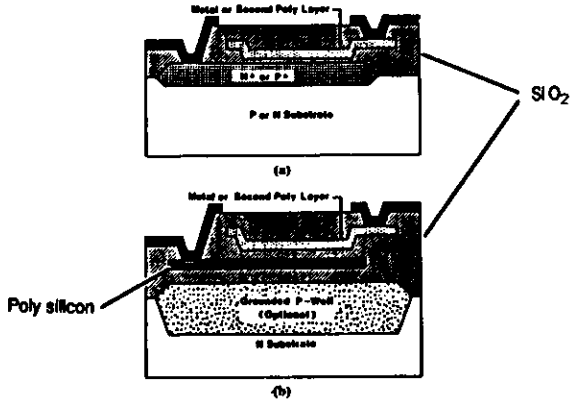


Figure 5.3: *MOS capacitors types :(a) gate- oxide- channel (b) polysilicon- oxide- polysilicon [53].*

first one (see figure 5.3-(a)), called a gate-oxide-channel type [54] or metal over active area, has the top plate made out of polysilicon or metal, the bottom plate is an n-doped region on the p-substrate or vice-versa. The other type (figure 5.3-(b)), polysilicon-oxide-polysilicon or double poly type, has the bottom plate also made from another polysilicon layer.

The characteristics of both types will be outlined. For a gate-oxide-channel capacitor :

- the fabrication is easy and requires no additional steps or masks than the ones necessary for the production of transistors. The bottom plate n-region is created at the same time as the implantation of the n-channel of the transistors.[5]
- the thin oxide making up the dielectric medium is grown on (n-doped) single crystalline silicon and this process is controllable and reproducible. This results in good oxide quality and voltage strength.
- the isolation of the bottom plate from the bulk is a reverse biased $p-n$ junction. Leakage current can flow through this junction and thus stored charge will leak to the bulk. Also such a reverse biased junction has a voltage dependant parasitic capacitance. It has a non-linear characteristic which can represent 5 to 20% of the nominal capacitance. A compromise in the n-doping of the bottom plate must be reached : with the n-doping the parasitic capacitance increases but the leakage current decreases.

[5]This is in general true though in the process used at ELMOS (Dortmund, FRG) the oxide providing the dielectric media was 70 nm thick in contrast to the 40 nm of the standard gate oxide for the transistors and thus required an extra mask.

- Typical values of capacitances per unit area are between 0.4 and $0.48 \cdot 10^{-3} pF/\mu m^2$ (see [54])[6].

For a polysilicon-oxide-polysilicon capacitor :

- the fabrication requires one more mask for the second polysilicon areas.
- the thin oxide has to be grown on polycrystalline material; this diminishes its quality and reproducibility and has to be made thicker. Additional processing steps are also necessary for its production.
- no leakage currents exist as the bottom plate is fully isolated from the substrate.
- the parasitic capacitances still exist, but are smaller (10%) and not voltage dependant.
- The capacitance per unit area is somewhat smaller than the previous type, 0.24 to $0.32 \cdot 10^{-3} pF/\mu m^2$ [54] due to the larger thickness of this grown oxide[7].

There exists independent of the capacitor type a parasitic capacitance from the top plate to the substrate associated with the circuits connected to it, however its value is less than 1% of the nominal capacitance. Also in both cases the biggest uncertainty in the capacitance value comes from the geometric definition of the capacitors due to mask tolerances and oxide thickness variation across the wafer. Variation up to 20% in absolute value of the capacity are usual [53]. Furthermore, for both types a voltage coefficient in the range of $-50\,ppm/V$ and temperature dependence of 20 to $50\,ppm/°C$ enter in the capacity value [54].

However all these effects are very similar for two capacitors if they are placed near each other on the wafer. If their areas are also similar, also the edge effects are of the same magnitude. The solution for high precision devices is to design the circuit to depend on the ratio of capacitors and not on their absolute value making tolerances cancel. If the ratio of capacitances should be other than 1:1 the big capacitor is usually made of several units of the small one so as to have proportional geometric properties. The precision which can be reached in the ratio of any two different capacitors to a third one (*matching*) is around 0.5% (for 1:1, $1\,pF$) in both technologies though this depends on the absolute value of the capacitance. Both of these effects can be seen in figure 5.4.

5.3.2 Transistors

MOS transistors[8] have the basic structure shown in figure 5.5 which shows an NMOS transistor. On application of a positive voltage on the gate with respect to the substrate,

[6]The mentioned process using 70 nm of capacitor oxide thickness achieves $\sim 0.6 \cdot 10^{-3} pF/\mu m^2$.

[7]The process used at IMEC (Leuven, Belgium) with this technology achieves with $70-90$ nm capacitor oxide thickness $0.35 \ldots 0.45 \cdot 10^{-3} pF/\mu m^2$.

[8]MOS transistors are also called metal- oxide- semiconductor- field- effect- transistor, MOSFET, due to the functioning principle of controlling the conductivity of the channel by creating a field under the gate with the application of a gate voltage.

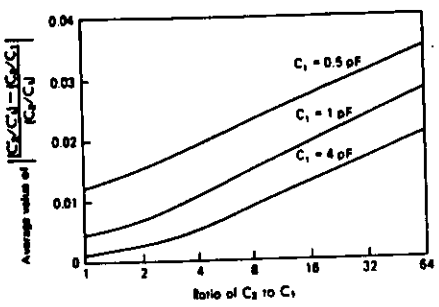


Figure 5.4: *Capacitor matching as function of the capacity ratio and the absolute capacity value [54].*

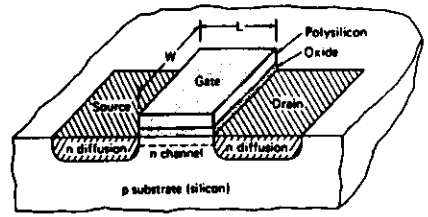


Figure 5.5: *Basic structure of a n-channel MOS transistor.*

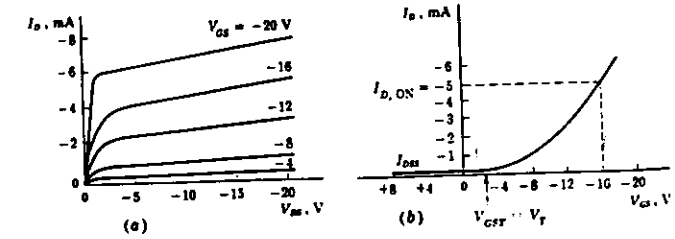


Figure 5.6: *(a) Characteristic curves and (b)Transconductance curve for a p-channel transistor (V_{DS} = 10 V): V_{DS}: drain-source voltage, V_{GS}: gate-source voltage, I_D: drain current, V_T threshold voltage. Only the linear region on the left side of (a) (small V_{DS}) is the one used for switching.*

the region under it is emptied from the majority positive carriers (it is a p-doped region) and a channel, n-channel is created between the source and the drain and the flowing of current is thus *enhanced*. This is the so-called *enhancement* n-channel type transistor. If the basis substrate is n-doped, the drain and source are p-diffusion areas, then the gate voltage has to be negative so that current flows through the p-channel. This would make a p-channel transistor.

If a lightly doped area (n-doped for n-channel transistors) is implanted in one of the process steps on the channel area, this channel conducts even with zero voltage on the gate (relative to the substrate) and a negative voltage (for n-channel devices) has to be applied on the gate to cut the conduction by depleting the channel from majority carriers. Such a device is called *depletion* transistor.

The characteristic and transconductance curves for a PMOS transistor are shown in figure 5.6.

The substrate making up the wafer where the structures are created is common to all of them and is doped with one type of impurity, donor or acceptor ions, leading to n- or p-type substrate. The transistors one can construct on them have a channel of the reverse type (n-channel on p-substrate and p-channel on n-substrate). However, in the same way the ion implantation provides for the doping of source and drain, it also can be used to create on some areas a *"well"* (also called tub) of opposite doping than the substrate where devices of the same channel type as the original substrate can be made. Figure 5.7 shows two transistors a n-channel and a p-channel connected as an inverter. This technique is called CMOS[9].

CMOS processes have been widely developed in the last years and are dominating most digital applications due to the simplicity of the CMOS inverter shown in figure 5.7 and the low power consumption, because current only flows when the transistors are switching.

The gate is made out of polysilicon on top of the gate oxide leading to the so-called CMOS-silicon gate process, or directly metal, the CMOS-metal gate process.

[9]standing for Complementary MOS

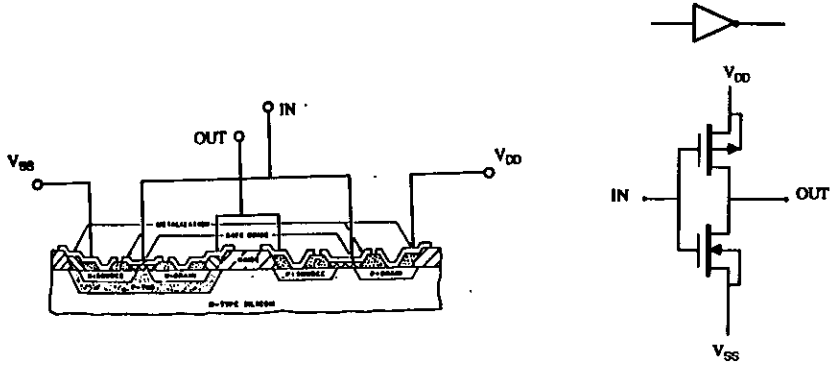


Figure 5.7: *CMOS inverter made up of a n- and a p-channel transistors.*

Technology integration achieving minimum features sizes with visible (ultra violet) light for photolithography under 1 μm is commercially available while research processes exist which use X-rays from synchrotron radiation for illumination to achieve further feature size reduction.

Because of the availability of the process and due to some other advantages which will be discussed further on, CMOS technology with 2.5 μm minimum feature size has been used for the design and manufacturing of both the analog pipeline and the buffer-multiplexer integrated circuits.

5.4 Switching devices

Integrated capacitors and their fabrication has been commented on in section 5.3.1. In figure 5.1 the second element needed is a switch.

5.4.1 Features of a switching transistor

Any of the transistors presented in section 5.3.2, p- or n-channel, either depletion or enhancement devices can act as a switch which is open or closed between the source and the drain depending on the voltage applied on the gate. However, this switch is not ideal according to the discussion of section 5.1 with zero resistance when closed and instantaneously opening to infinite resistance, with both properties independent of the voltage to be switched. A model for a "real" transistor is shown in figure 5.8. The main parameters in figure 5.8 and their values are the following :

- R_{on} is derived from the dependance of the drain current I_D on the applied voltages [54] :

$$I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T - \frac{1}{2} V_{DS}) \cdot V_{DS} \tag{5.5}$$

which is valid for $0 < V_{DS} < (V_{GS} - V_T)$ that is in the active region, and where

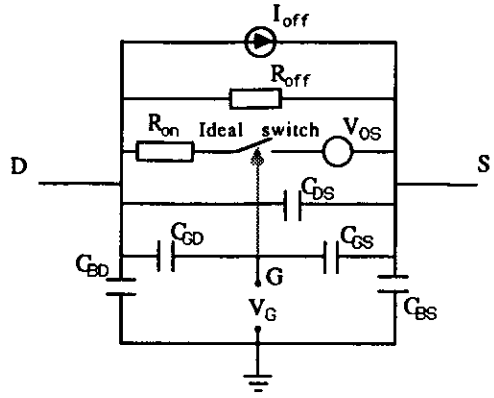


Figure 5.8: *Equivalent diagram for a "real" switching transistor [54].*

- μ is the mobility of the channel $\left[\frac{cm^2}{V \cdot sec}\right]$,
- C_{ox} the capacitance per unit area of the gate oxide $\left[\frac{F}{cm^2}\right]$,
- W and L the dimensions, Width and Length of the gate channel of the transistor $[cm]$,
- V_{GS} the gate-source voltage,
- V_T the threshold voltage of the transistor, i.e. the V_{GS} below which the transistor is considered to be an open circuit ($I_{DS} < 10^{-9} A$),
- V_{DS} the drain-source voltage, and which is considered to be small.

This expression is valid for a n-channel transistor, an equivalent one can be obtained for the p-channel.

The resistance of a device is the proportionality factor which relates a small variation of the current to the voltage drop on its terminals. So if we differentiate expression 5.5 while $0 < V_{DS} < (V_{GS} - V_T)$ we have :

$$R_{on} = 1 / \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T - V_{DS})} \tag{5.6}$$

for a n-channel transistor, and

$$R_{on} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (-V_{GS} + V_T + V_{DS})} \tag{5.7}$$

for a p-channel device. In both cases the resistance depends on the voltage we want to switch, a fact which causes a non-linearity. To control the switch a gate-source voltage several times bigger than the threshold is used and typical R_{on} values range from several kΩ to $\mathcal{O}(100)\,\Omega$ or less, decreasing for large values of $\frac{W}{L}$.

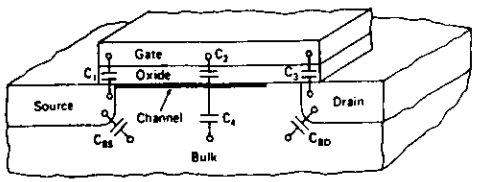


Figure 5.9: *Parasistic capacitances of a MOS transistor.*

- R_{off}, the resistance of the switch when open, can also be obtained by differentiating the equation of the I_D when $(V_{GS} - V_T) < V_{DS}$:

$$I_D = \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \tag{5.8}$$

  which gives 0 if $V_{GS} = V_T$. In fact R_{off} is in the $10^{12}\ \Omega$ range and can be considered ideal.

- The current source I_{off} represents the leakage current through the transistor when open. It is mainly due to the subthreshold current in the weak inversion mode and is in the pA range. This current is strongly temperature dependant doubling every $10\,°C$.

- The voltage source V_{OS} representing the voltage offset on the terminals when the switch is open even with no current, can be neglected.

- Diverse parasitic capacitances are associated with the different junctions. They are shown in figure 5.9.

  Their effect is quite important because their magnitude is several percent of the actual storage capacitors. Their value and dependencies can be parametrized [54].

  C_{GD} and C_{GS} represent the effect known as *feedthrough* or CFT[10] by which the operation of the switch modifies the voltage at the signal path due to sharp rising or falling edges in the control voltage applied at the gate. Their existence comes from the overlapping of the gate with the diffusion areas of drain and source and also from the coupling through the gate oxide. At least a part of their value, not associated with geometry is given by the functioning mode of the transistor. A quantification of the error induced on the output is not easy and several approximations have to be made. A modeling can be found in [54]. In a first approximation it depends on the source voltage and is proportional to the gate area WL [42] :

$$V_{CFT\ error} = -\frac{WLC_{ox}}{2C_S}(V_H - V_S - V_T) \tag{5.9}$$

[10] Clock feed trough, CFT

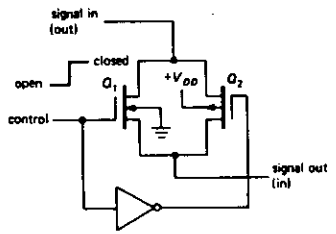


Figure 5.10: *CMOS transmission gate.*

  where C_S is the storage capacitance, V_H the high level gate signal (to have the switch closed) and V_S the source voltage.

  The capacitors to the bulk (C_{BS} and C_{BD} in figure 5.8) are normally due to reverse-biased junctions and as parasitic must also be taken into account. Their magnitude is thus also voltage dependant.

The dynamic range of the analog signal we want to switch is limited. If the gate is at the full supply voltage (positive supply V_{DD} for NMOS devices or the negative V_{SS} for PMOS), the transistor will be on until the analog voltage reaches the supply minus the threshold voltage. But as it does approach (see figure 5.6), the transistor starts turning off and a non-linearity appears. The analog voltage has to be kept well below the supply so that V_{GS} is far enough to the right side of figure 5.6-(b).

Due to all the factors considered, a simple transistor can be only used as a switch for high precision applications if corrections are taken for the non-ideal aspects.

5.4.2 Transmission gate

CMOS technology provides the possibility to overcome at least some of these imperfections with a switching device known as a transmission gate shown in figure 5.10 and which is the usual implementation of an analog switch.

The transmission gate is made with two complementary transistors switched in parallel. By applying clock signals of opposite polarity to the gates one can achieve :

a) that depending on the input at least one of the transistors conducts, that means the switch is closed, or

b) setting both transistors in a non-conducting state providing an open switch.

In comparison to the single transistor a transmission gate requires at least twice the area and also complementary control clocks. However several advantages encourage the implementation of switches with transmission gates. Namely :

- The dynamic range of the analog signal the switch can transmit in the ON state is increased over a factor of 2. It will be no more limited to well below the supply

because as one transistor starts turning off, the other one is fully on so the switch still conducts. If the signal is within the gate clock levels, both transistors are ON.

- The R_{on} can be calculated as the parallel resistance of the n-channel transistor with the p-channel :

$$R_{on}^{transmission\ gate} = \frac{R_{on}^{p} \cdot R_{on}^{n}}{R_{on}^{p} + R_{on}^{n}}. \tag{5.10}$$

Using equations 5.6 and 5.7 their parallel resistance with equation 5.10 is :

$$R_{on} = \frac{1}{([\mu C_{ox}\frac{W}{L}]_n + [\mu C_{ox}\frac{W}{L}]_p)(V_G - V_T) - ([\mu C_{ox}\frac{W}{L}]_n - [\mu C_{ox}\frac{W}{L}]_p)V_{signal}} \tag{5.11}$$

with the assumptions

$V_T^p = -V_T^n = V_T$, independent of the bulk voltage

the clocks are of equal but opposite amplitude $V_G^n = -V_G^p = V_G$.

From the mobility of the channels we have

$$\mu_n \simeq 3 \cdot \mu_p \tag{5.12}$$

So for a transmission gate where the transistors dimensions relate as

$$\left[\frac{W}{L}\right]_p = 3\left[\frac{W}{L}\right]_n \tag{5.13}$$

its ON resistance is independent of the analog signal to be switched, something which is desirable for a switch as R_{on} is not zero. In fact the resistance is typically small (e.g. in our design for $(W/L)_n = 6/4$, $(W/L)_p = 10/2.5$ it results $R_{on} \sim 2\,k\Omega$). When combined with the usual storage capacitors of $1\,pF$ this leads to charging times in the ns range.

- The clock pulses applied to the gates of the NMOS and PMOS transistors have opposite polarities. Through the parasitic capacitances C_{GD} and C_{GS} of figure 5.8, the feedthrough appearing on the analog signal is of opposite sign and although not totally, tends to cancel out. The cancellation is not perfect as :
  - the C_{GD} and C_{GS} are not necessarily exactly equal for the n- and the p-channel transistors,
  - the switching does not occur exactly at the same time with exactly equally sharp pulses. This is mainly due to the different mobilities of the two channel types (see equation 5.12).
  - one of the gate control signals is derived by inverting the other one so at least a delay and an edge form change appear.

The dependence of the CFT on the gate area in equation 5.9 implies that the best possible canceling of the CFT induced voltage error for a transmission gate occurs if the complementary transistors have equal area :

$$[W \cdot L]_p = [W \cdot L]_n \tag{5.14}$$

which basically corresponds to equal capacitance.

In fact the offset comes to be one order of magnitude smaller in the case of a transmission gate than for a single switching transistor [42].

Equations 5.13 and 5.14 lead to the following relation for the size of the transistors forming the transmission gate :

$$L_n = \sqrt{3}L_p \qquad and \qquad W_n = \frac{1}{\sqrt{3}}W_p. \tag{5.15}$$

Due to these three reasons, transmission gates are always used to implement switches when the space on the silicon permits it.

5.5 Other components

Besides capacitors to store charges and switches to isolate them from the input or output, some additional components are necessary for a functioning analog delay line.

5.5.1 Digital control

A control section is necessary to generate the right sequence of signals to operate the switches so that a set of sampling devices works as a delay line. The functionality we want to achieve is the following :

1. The analog memory is a device where signals can be stored and retrieved hence a control is needed to determine the function expected, write into the memory or read from it.
2. For both, read and write functions, no random access to the cells is necessary. The charge samples to store will always be resident on contiguous cells. This requires only the input of an external control that defines the switching from one cell to the next.
3. The device should work with the minimum number of external signals and generate the rest internally.

These requirements imply the usage of several auxiliary circuits internal to the device.

The second point can be implemented with a shift register connected in ring configuration where only one "true" state (or logical "1") is shifted through so that one cell is selected at a time.

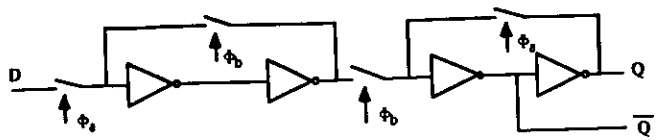


Figure 5.11: *Scheme of a CMOS-Flip-Flop operated by two non-overlapping clocks.*

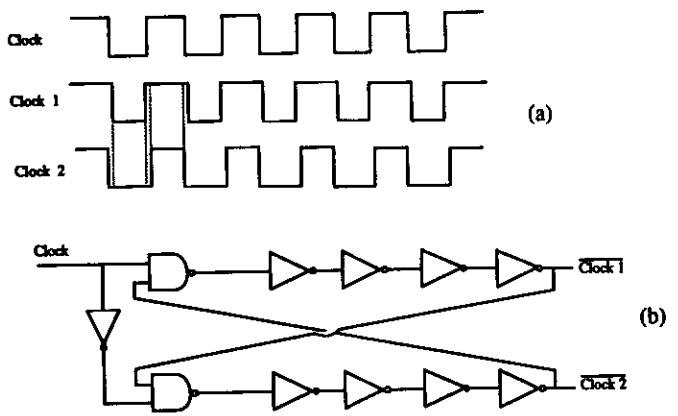


Figure 5.12: *(a) Two phase non-overlapping clocks signals. (b) Circuit to generate them out of a one phase clock.*

The shift register is made from CMOS-flip-flops using two non-overlapping clocks. A scheme of a CMOS-flip-flop can be seen in figure 5.11. This implementation has been used because the number of transistors needed is about half the number used in conventional flip-flop versions.

On figure 5.11 Φ_a and Φ_b are two opposite non-overlapping clock signals that make the circuit at all feasible. The information at the D-input is taken over at the rising edge of Φ_a and gets out to Q and $\overline{Q}$ with Φ_b. Figure 5.12-(a) shows two non-overlapping clock signals.

The generation of a two-phase non-overlapping clock is done starting from an external single phase signal and takes place also inside the integrated circuit so as to follow feature number 3. The circuit that produces the non-overlapping two-phase clock is drawn in figure 5.12-(b) and guarantees the non-overlapping of the signals with the delays in the inverters. In fact the amount of non-overlapping is given by the number of inverters on each branch.

A way to initialize the shift register must also be provided. An INITialize signal could be supplied externally, but following point 3 it can also be generated internally

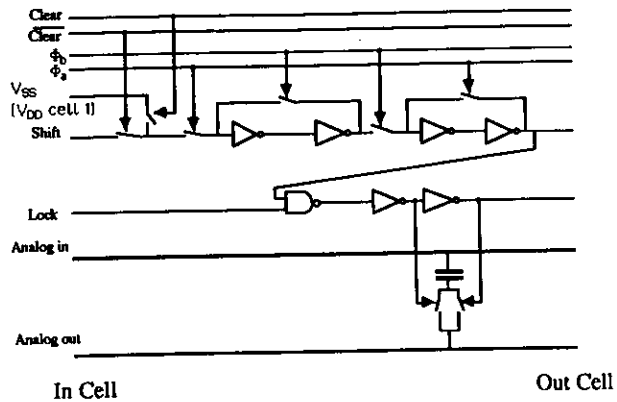


Figure 5.13: *Storage cell with digital control.*

when the mode of operation changes from Read to Write. When this happens, another auxiliary circuit issues a CLEAR signal with the edge of the next clock, and all the CMOS-flip-flops are cleared except for the first one which gets a logic "1". The writing process thus starts always at cell number 1 and by counting the number of clocks we can determine at any moment which part of the pipeline we are using.

Also some mechanism has to make sure that two sampling cells are never selected simultaneously. This is of course usually not the case but cannot be taken for granted at switching time. This feature is usually called the *"break-before-make"* function. The circuit therefore includes an additional gate on every cell connected to the flip-flop of the preceding one so that the switch only opens if the previous cell is already deselected.

With this additional LOCK-path, the whole cell with its digital control is represented in figure 5.13.

5.5.2 External signal interface

As we have seen in section 5.4, the gates of the single transistors or the transmission gates switch on the application of clock signals with amplitudes as big as the supply voltages V_{DD} or V_{SS}. Typical values of the supply are ± 5 Volts which is a large swing for digital signals.

In order to simplify the coupling to the rest of the electronics, the digital control signals for the pipeline are applied as complementary levels and received inside with a comparator which swings its output from V_{DD} to V_{SS} on a difference of $\pm 25\,mV$ on its input pins. Thus the inputs are TTL or ECL compatible by fixing one of the inputs to a constant voltage. In the ZEUS calorimeter front end electronics signals are applied as ECL-$\overline{\text{ECL}}$ levels.

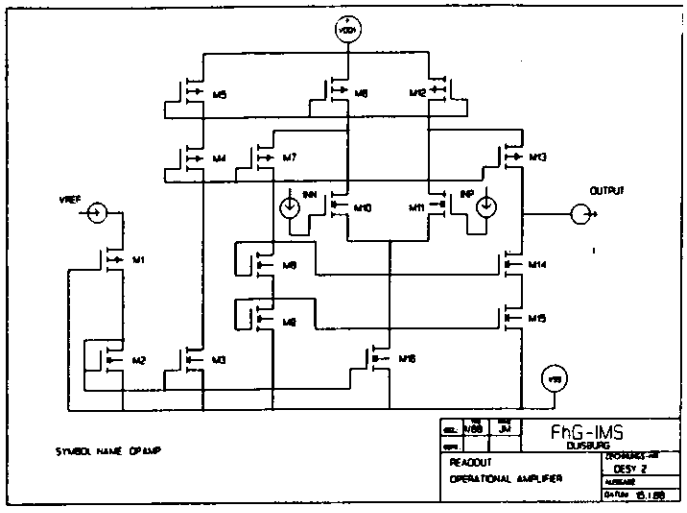


Figure 5.14: *Operational amplifier circuit.*

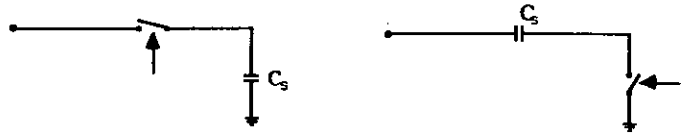
5.5.3 Operational amplifier

To readout the capacitors a low output impedance, high open loop gain operational amplifier is used to drive the voltage off-chip. It is compensated by the load capacitor at the output node. It is connected in a negative capacitive feedback loop and because of its high gain all the charge is transferred to the feedback capacitor. The circuit making the amplifier can be seen in figure 5.14.

The design of operational amplifiers is a subject in itself. We will only give the main requirements, all of them achieved in the custom design of the op-amp.

- Gain ($> 65dB$ open loop)
- Linearity in the required signal range
- Noise (Signal to noise ratio $> 80dB$)
- Power dissipation ($< 15mW$)
- Settling time ($< 500ns$ to 0.1% of end value)

An input for the reference current has been carried to an external pin. It is labeled V_{REF}. By varying the current going into this node, the speed and drive capabilities of the operational amplifier (at a cost of larger power consumption) can be influenced. Typical values of I_{REF} used are $50\,\mu A$ per op-amp which is achieved at $V_{REF} \sim 1.3\,V$ over ground.



(a) Layout 1 (b) Layout 2

Figure 5.15: *Alternative connectivity for a sampling element.*

For the full description of the operational amplifier performance and its construction see [42].

5.6 Component interconnection

The elements necessary to the construction of an analog storage unit have been described in the preceding sections for their ideal and non-ideal characteristics. Several interconnections are however possible for the same circuit functionality. So both the connections and the layout should be such that non-ideal qualities of the components have the smallest effect on the charge we want to store.

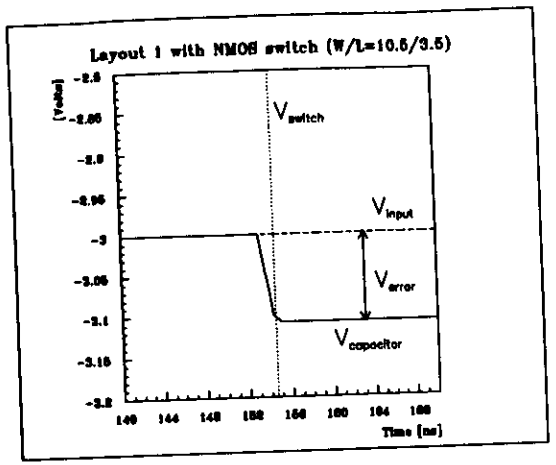
A sampling element has been shown in figure 5.1 with its non-ideal realization in figure 5.2. The scheme shown in figure 5.15-(b) is also a possible setup to store on capacitor C_S a voltage sampled from the input signal V_i at the time the switch opens. Which layout presents more advantages? Or where do the imperfections of the single components show smaller effects on the whole device?

The non-ideal model of a switching transistor presented in section 5.4.1, or other equivalent ones, can describe in mathematical form the characteristics of the devices. However when interconnected with other components a model yields a set of several differential equation with difficult (if any) analytical solution.

Much more powerful is the computer simulation of these mathematical models and solution with iterative methods. Several programs exist for simulation of MOS circuits, SPICE [55] being the most widely used. Results of simulations performed in order to find the optimum layout will be shown. The program BONSAI [56] has been used for this purpose. More extensive simulations, also of other parts of the circuit can be found in [42]. There, the optimum transistor sizes have been determined and will be used here to simulate alternative layouts.

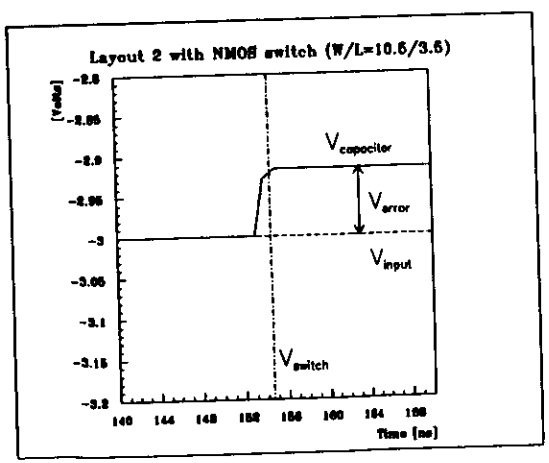
The two possible switch-capacitor layouts of figure 5.15-(a) (referred to as layout 1) and figure 5.15-(b) (layout 2) have been simulated and program outputs are shown in figures 5.16 to 5.19. Switches have been implemented with both single transistors (NMOS) and CFT optimized transmission gates following equations 5.15. The parameters used for the simulation are the following :

- The capacitor is always $1\,pF$,



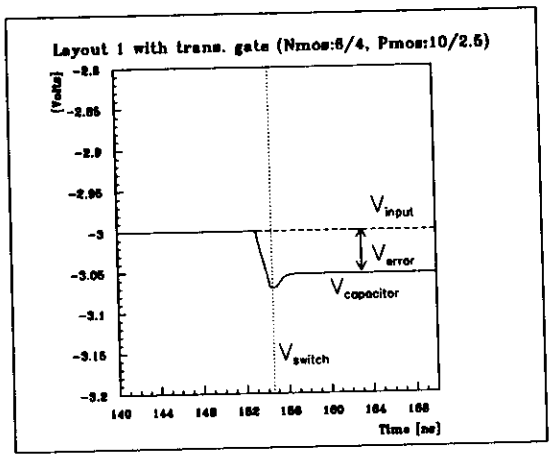
$V_{input}(V)$	V_{error} (mV)
-4.0	118
-3.0	109
-2.0	99
-1.0	88
0.0	84

Figure 5.16: *Simulation of sampling element type 1 with NMOS transistor as switch.*



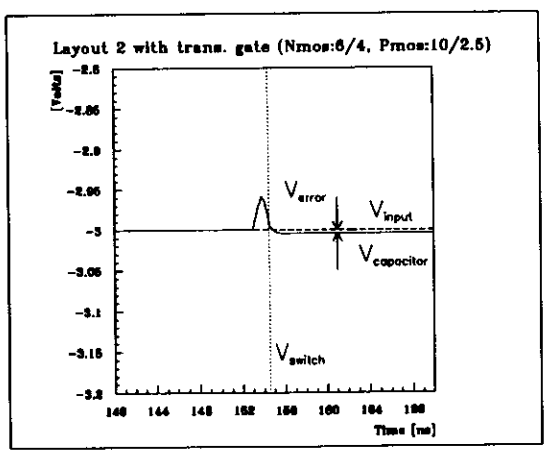
$V_{input}(V)$	V_{error} (mV)
-4.0	84
-3.0	84
-2.0	84
-1.0	84
-0.1	84

Figure 5.17: *Simulation of sampling element type 2 with NMOS transistor as switch.*



$V_{input}(V)$	V_{error} (mV)
-4.0	62.6
-3.0	52.8
-2.0	29.5
-1.0	6.8
0.0	-9.2
1.0	-32.2
2.0	-49.5
3.0	-67.8
4.0	-83.4

Figure 5.18: *Simulation of sampling layout 1 with optimized transmission gate switch.*



$V_{input}(V)$	V_{error} (mV)
-4.0	4.7
-3.0	4.7
-2.0	4.7
-1.0	4.7
-0.1	4.7
0.1	4.7
1.0	4.7
2.0	4.7
3.0	4.7
4.0	4.7

Figure 5.19: *Simulation of sampling layout 2 with optimized transmission gate switch.*

- $V_{SS} = -6\,V, V_{DD} = +6\,V$,
- The gate(s) are operated with the full voltage swing $\pm 6V$,
- The switching pulse edges have a rise/fall time of $2\,ns$,
- The parasitic capacitances are dimensioned as expected for the technology used,
- Inverters have been implemented as in the real pipeline (NMOS: $W/L = 3.5/3.5$, PMOS: $W/L = 10.5/3.5$),
- The diffusion areas are $10\,\mu m$ wide,
- The operational amplifier (for the readout simulations) has been replaced by an ideal voltage controlled voltage source with gain of 10.000 in order to speed up the simulations.

The main results out of the simulations are :

- Layout 1 shows a dependence of the error voltage due to CFT on the analog signal even if the switch used is a transmission gate and it is in the $100\,mV$ range equivalent to a few percent of analog signals up to $-4\,V$ (see figures 5.16 and 5.18). This fact results from equation 5.9 where in this case the V_{Source} is V_{Signal}. The tables in figures 5.16 and 5.18 can be interpreted as a constant error plus a part increasing linearly with the input signal.
- Setup 2 has a CFT induced error independent of the analog signal (in this case the source is tied to ground which makes V_{err} in equation 5.9 constant), and as expected when using transmission gates, the CFT is an order of magnitude smaller than for simple transistors. The value comes out to be ca. $5\,mV$ (see figures 5.17 and 5.19).
- When the switch is open, the variation of the analog signal should not change the voltage sampled in the capacitor C_S. However this effect known as *signal feedthrough* (SFT) exists and is due to the non-ideal but real existence of parasitic capacitances C_{BD} and C_{BS}. It is shown in figure 5.20 for setups 1 and 2 with open switches and V_{input} varying as a step function.

  In setup 1 no SFT shows up as the open switch isolates C_S from the input, even if it is in parallel with C_{BD}. In setup 2 however with an open switch, C_S and C_{BS} form a capacitive divider and C_S sees part of the variation of the analog signal. The exact value of C_{BS} and with it the amount of signal feedthrough depends on the overlap of the gates with the diffusion areas [42]

Layouts 1 and 2 seem therefore to be equally unsuited for a sampling operation. Only an appropriate layout for the readout of the signal allows setup 2 not to be affected by signal feedthrough. These interconnections are shown in figure 5.21 and the simulation results can be seen in figure 5.22. In figure 5.21 C_{BS} of the switch is drawn. At storage time C_S and C_{BS} act as one capacitor, as they do at read time. All their

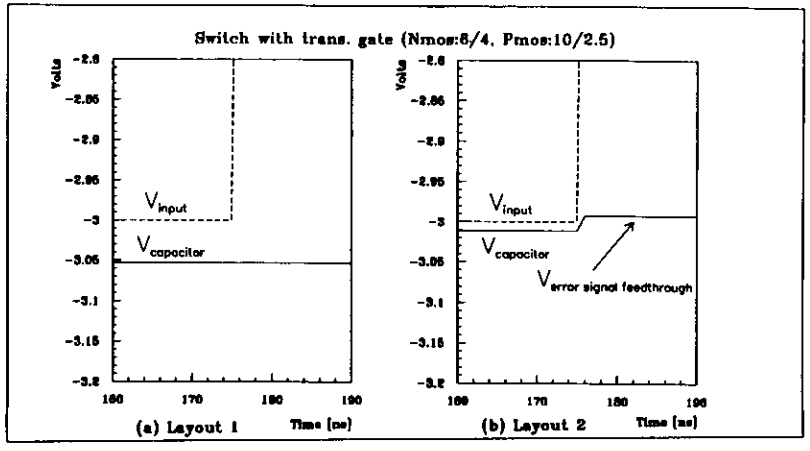


Figure 5.20: *Signal Feedthrough of sampling elements of figure 5.15 (a) and (b) due to the parasitic capacitances from the bulk to the signal path. V_{input} is set as a step function from -3 to $0\,V$.*

charge is transferred to the feedback capacitor C_F and the signal feedthrough error is compensated.

As comparison another possible layout is shown in figure 5.23 and simulated output in figure 5.24 shows that this layout does not compensate signal feedthrough.

5.7 Device specifications and component size

The layout to be used follows the design of one channel shown in figure 5.21, and for one cell can be seen in figure 5.25. The values of the different elements have been chosen after extensive simulations to obtain the required performance.

The specifications required for the analog delay line are compiled in Table 5.1. They determine the final election and sizing of the different components in the circuit.

The area occupied by the capacitors in first order determines the size of the chip and with it the achievable integration. The larger the capacitor, the more charge we are moving around and thus better signal-to-noise ratio and smaller the error in matching (see figure 5.4). However this also increases the charging time of the circuit. In section 5.3.1 we commented on typical capacitances per unit area. The size of the capacitors as already mentioned has been chosen to be $1\,pF$. To achieve $1\,pF$ of capacity with a technology which yields $\sim 0.6 \cdot 10^{-3}\,pF/\mu m^2$, approximately an area of $1600\,\mu m^2$ or a square of $40\,\mu m \times 40\mu m$ is needed which is a compromise value between all the factors, and also a typical production size.

For the switches, the following facts are to be taken into account :

- Switches S1 and S4 for storing and S2 and S5 for reading out are operated by the

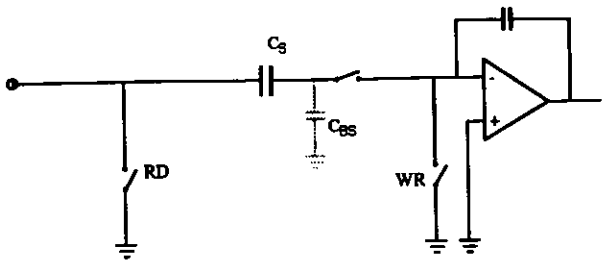


Figure 5.21: *Sampling element with readout connections.*

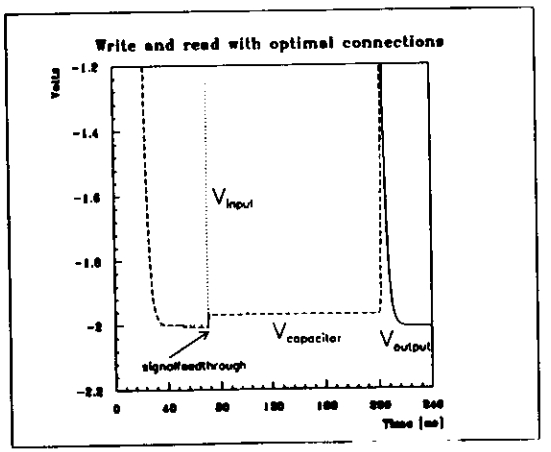


Figure 5.22: *Simulation result of sampling element with readout stage. At t = 20 ns the WR switch is closed and C_S charges up. At t = 50 ns the sampling switch is opened to the hold state. CFT is induced. At t = 70 ns the analog input goes to 0 V producing SFT.*

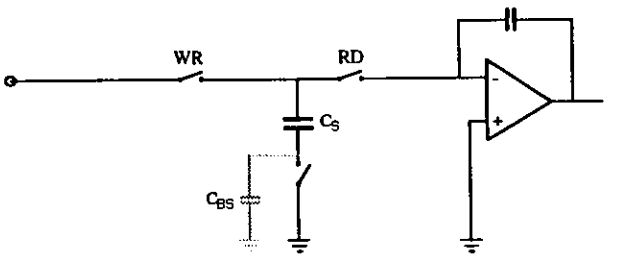


Figure 5.23: *Unsuitable layout for signal feedthrough compensation.*

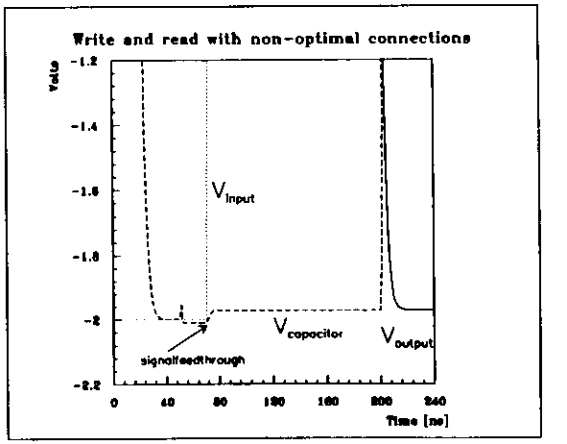


Figure 5.24: *Simulation result of figure 5.23.*

		Units
Analog input signal	0 ...-4	Volts
Analog output signal	0 ...-4	Volts
Signal to noise ratio	> 72	dB
Number of cells	58	
Cell matching difference	< 0.4	%
Charging time constant	< 4	ns
Switching jitter between cells	< 1	ns
Switching jitter between channels	< 1	ns
Non-Linearity	< 0.25	%
Discharging time constant	> 1	second
Read frequency	1	MHz
Write frequency	> 11	MHz
Supply voltage	± 6	Volts
Dissipated power per channel	< 50	mW
Channels per chip	4 to 8	
Temperature stability	< 200	*ppm/°K*

Table 5.1: *Specifications for an analog delay line circuit.*

external $\overline{\text{RD}}$/WR. When they change state all S3 except one, $S3_i$, are open. This one gets corrupted anyway so this fact and also the range of the analog signal (negative unipolar) makes it possible to use NMOS transistors for these switches. Their size should be big enough so as not to influence the charging time constant. $\frac{W}{L}$ has been chosen to be $\frac{200}{3.5}\,\mu m$. Figure 5.26 shows simulation results for different sized transistors.

- Switches S3 and S6 have to be operated while the analog information, input or output, is being transferred and have to be optimized for minimum CFT induced offsets. The external signal CLK switches $S3_i$ off and $S3_{i+1}$ on.

  They are implemented as transmission gates following relations 5.13 and 5.14 and the chosen sizes are $[\frac{W}{L}]_n = \frac{6}{4}\,\mu m$ and $[\frac{W}{L}]_p = \frac{10}{3.5}\,\mu m$.

- Switch S5 is held open while storing samples on C_S and is also operated by the $\overline{\text{RD}}$/WR signal. While from the functional point of view its existence is not necessary, it separates all the transmission gates at each storage cell from the node of the operational amplifier.

- For reading out the charge sampled in C_S, it is transferred to the feedback capacitor C_F. After the amplifier has settled and the output voltage has been passed further down the chain (to the analog buffer or to an ADC), C_F's charge is cleared by closing S6 long enough for the charge to disappear. The external signal RESET operates S6. Although optimized, this operation introduces a fixed CFT volt-

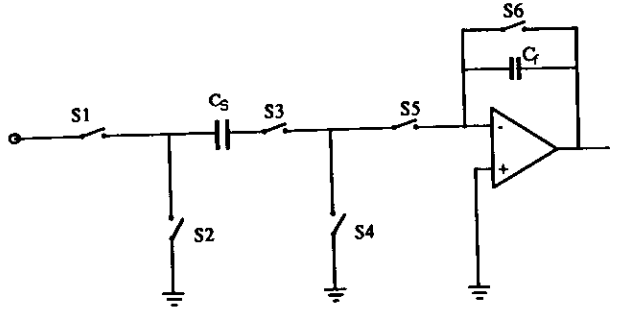


Figure 5.25: *Layout of one full delay line channel.*

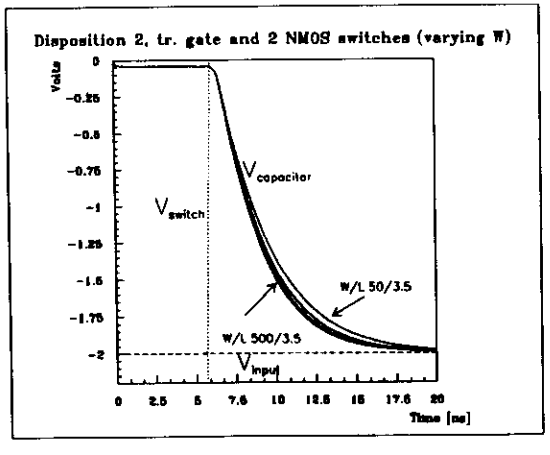


Figure 5.26: *Capacitor charging curves for different transistor sizes.*

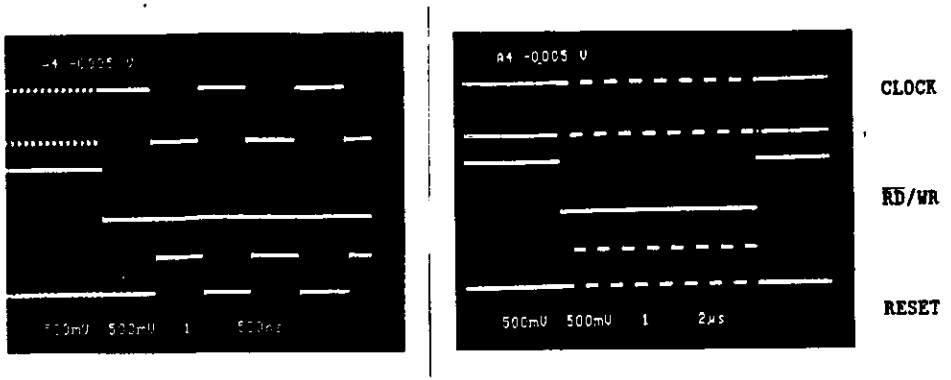


Figure 5.27: *Control signals for analog pipeline operation. On the change from* WRITE *to* READ*, the* CLOCK *changes from* $10\,MHz$ *to* $1\,MHz$*. Then 8 samples are read and transferred to the buffer (see also the* $1\,MHz$ RESET *signal). When this is done, the pipeline is again restarted in Write mode with* $10\,MHz$ *clocks.*

age offset in the capacitor which adds to the sampled voltage on the next cell ($\sim 15\,mV$).

Figure 5.27 shows a scope photograph of the control signals to operate the analog pipeline.

5.8 Layout on silicon

Once the electrical design of an integrated circuit has been finished the construction is mainly a geometrical problem. A set of masks defining the zones for the technological processes has to be produced. Each mask determines the areas where a particular step occurs, e.g. metallization, doping, oxidation, threshold implantation.

The choice of a $2.5\,\mu m$ technology is given mainly by a mixture of factors like the S/N ratio, the speed and the maximum analog signal we want to use.

A wide range for the analog signals implies large supply voltages to the transistors. In order to hold these voltages, the minimum feature size cannot be too small otherwise breakdown will occur. However, larger transistors imply larger parasitic capacitance which slow down the signals ($frequency \propto 1/L^2$) [57] and allow only smaller clock frequencies. So a compromise has to be found. Needing a V_{DD}, V_{SS} of $\pm 5\,V$, to have good linearity up to $-3\,V$, with the $2.5\,\mu m$ transistors[11], we are almost at the limit of the specifications for maximum voltage.

The frame for the layout is given by the *design rules* of the technology used. For the process used for series production typical design rules are given in Table 5.2.

[11]The smallest transistors we have in the pipeline are $2.5\,\mu m$ devices in the transmission gates and

CMOS technology, Epi wafer, n-tub, single metal, single poly	Value	Units
Threshold voltage V_T n-mos	+1	Volts
Threshold voltage V_T p-mos	-1	Volts
Polysilicon width	≥ 3	μm
Poly-poly distance	≥ 3	μm
N-mos gate length	≥ 3.5	μm
P-mos gate length	≥ 2.5	μm
Metal width	≥ 4	μm
Metal-metal distance	≥ 3.5	μm
Contact holes	3×3	μm^2
Overlapping with contact hole	≥ 1.5	μm
Overlapping active-metal	≥ 2.5	μm
Gate oxide thickness	~ 40	nm
Capacitor oxide thickness	$\sim 60 - 70$	nm
Active-active distance	≥ 4.5	μm
P-area - tub distance	≥ 7.5	μm
Bond pads	130×130	μm^2
Bond pitch	≥ 200	μm

Table 5.2: *Main design rules of the CMOS process used.*

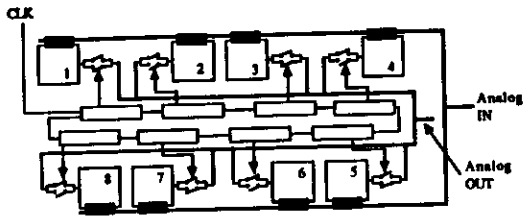


Figure 5.28: *Layout of the test chip storage channel (8 cells).*

Both the pipeline and the buffer-multiplexer circuits are products of a full custom design. This means the placing and interconnection of the components have been optimised so as to have a most efficient use of the silicon area without undermining the properties of the circuit.

How important the placing of the diverse components is and how it affects the features of a circuit will be shown with an example extracted from experience.

Before a full design of the 4-channel, 58-cell pipeline circuit was tackled, a test chip with one channel and 8 cells of storage was designed and put into silicon [42,58]. The idea was to demonstrate the viability of an analog storage unit operating at $10\,MHz$. The design included all the features of the full pipeline plus additional ones (e.g. random cell access for reading) to perform exhaustive tests on this device.

The main fraction of components in the circuit are the storage cells with its local part of the shift register as shown in figure 5.13. This structure has to be repeated 58 times per channel and represents the largest area of the circuit; it is therefore essential that the layout of this cell be optimized. The size of any of the devices (and with it the area) is a parameter determined as we have shown, by the specifications of the circuit. The designer has however the choice how to place them.

The largest component in the cell is certainly the capacitor ($40\,\mu m \times 40\,\mu m$). Compared to this the transistors of the analog switch are small (e.g. $10/2.5\,\mu m$ channels[12]).

Figure 5.28 shows how the components for the storage cell were placed in the design of the test chip for the 8 cells. A substantial asymmetry can be observed between the two rows of cells and even among those in the same row. Cells 1, 3, 6, 8 have their analog switches on their right, while the others have it on their left. Also the paths carrying the signals for the gates are not equivalent for all cells, for cells 2, 4, 5 and 7, the path with the gate signal overlaps with the path carrying the analog input, while for the other cells this overlap does not exist. As a consequence of this, the coupling of the signals when switching is different from cell to cell.

This coupling, added to effects like clock feedthrough can be observed if we write $0\,V$ in all the cells and read them out. The output is what we call *pedestals* of the

$3.5\,\mu m$ in the inverters

[12]The width of the active areas is usually $10\,\mu m$ this means on a $10/2.5\,\mu m$ device they occupy $10\,\mu m \times 10\,\mu m = 100\,\mu m^2$.

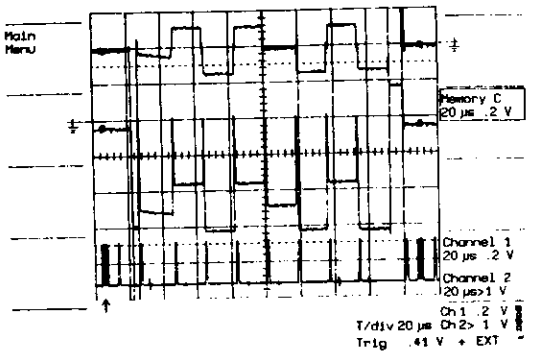


Figure 5.29: *Pedestals for the test chip (top trace), output for* 1 V *(0.5 gain) DC input (middle trace) and Clock signal (bottom trace).*

different cells (see next chapter, section 6.3.3). In the case of the test chip the pedestal differences amount to over $300\,mV$ between cells as is shown in figure 5.29 (top trace).

All main properties of the pipeline concept have been measured on the test chip [58]. Only after that, the design of the full pipeline chip was attempted. The redesign for the real pipeline cared for high symmetry in the cell layout. The location of the components is shown in figure 5.30.

However the two row structure for the storage cells makes four corners appear as asymmetries in the layout, a fact that has important consequences as we will see in the next chapter. The pedestal values can be seen in figure 6.6 and show a much improved pattern.

The two row scheme is maintained for two reasons :

- the pipeline operates in a ring form, i.e. the next cell after the 58th is cell number 1,
- the dimensions of a chip should not exceed certain typical manufacturing dimensions and a line with 29 cells yields a size of $\sim 4.5\,mm$ which already counts to the large chips[13].

Typically, the silicon crystals are made square, so the dimension of $4.5\,mm$ has also been chosen transversally. This fact forces (or allows) us to have an integration level of 4-5 channels/device.

Additionally to the repeated cell structure, other components are needed. The large S1, S2, S4 and S5 switches as well as the operational amplifier with its feedback capacitor and the Reset switch are placed to the right of the repeated storage cells. On the periphery, near the bonding pads are the input comparators for the control signals as

[13]The size of the silicon crystals is the main factor entering an equation that gives the yield (and with it the costs) of the production. For $4.5 \times 4.5\,mm^2$ a yield of $\sim 50\%$ is expected. This is also the experience from production batches.

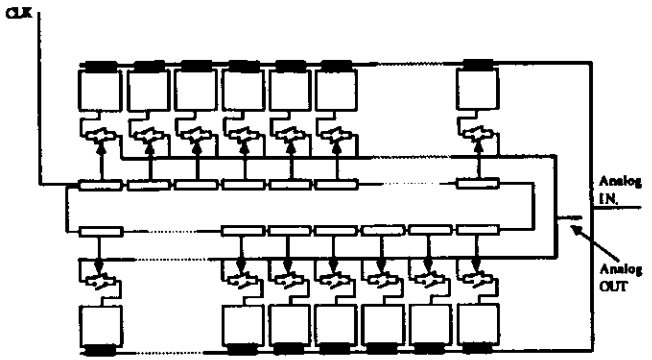


Figure 5.30: *Storage cell layout in pipeline chip.*

well as the two phase non-overlapping clock generation circuits. The symbolic scheme can be seen in figure 5.31 while a block drawing of the physical layout is shown in figure 5.32. For completeness figureb:pipeph shows a full plot of the pipeline.

5.9 Buffer-multiplexer circuit

The second ASIC developed for the ZEUS Calorimeter readout electronics is the *buffer-multiplexer* chip. Its function has been described in the previous chapter.

The development was started once the good functioning of the delay line was established. Its design profits from the pipeline design and it uses most of its circuit elements. Also the specifications are similar to the pipeline circuit, though the writing speed is no longer required to be above $10\,MHz$. Only $1\,MHz$ is needed. As the naming of the chip indicates, the device consists of two separate parts which are discussed as follows.

5.9.1 Buffer subcircuit

The buffer has been introduced to reduce the readout deadtime. It stores the information in the same way as the pipeline.

The difference lies in the number of cells. As explained in chapter 4 we only need to keep three samples of the shaped signal to reconstruct the calorimeter's information, time and energy. The length of the buffer was fixed to 8 cells. This provides either extra baseline measurements (to check that no pulse pile up has occurred) or more samples to determine the pulse shape on the later falling edge.

The circuit and the control signals are similar to figures 5.25 and 5.27. Some differences in construction exist. Integration is different: one buffer channel is made up of 8 cells and one chip contains 12 channels. The capacitors used are $2\,pF$ because the charging time allowed is larger (smaller writing frequency).

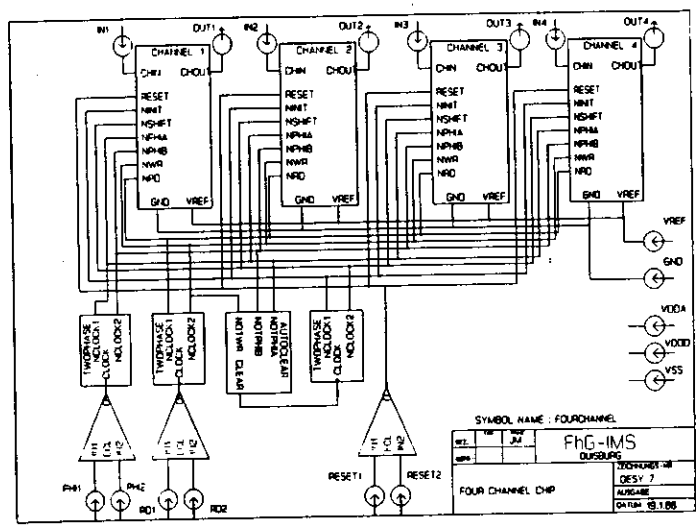


Figure 5.31: *Symbolic layout of the full analog pipeline chip.*

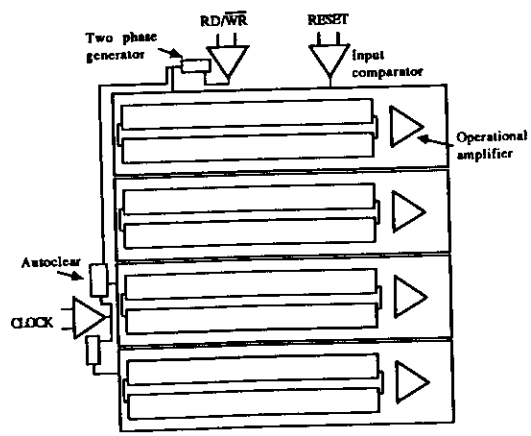


Figure 5.32: *Physical layout of the full analog pipeline chip.*

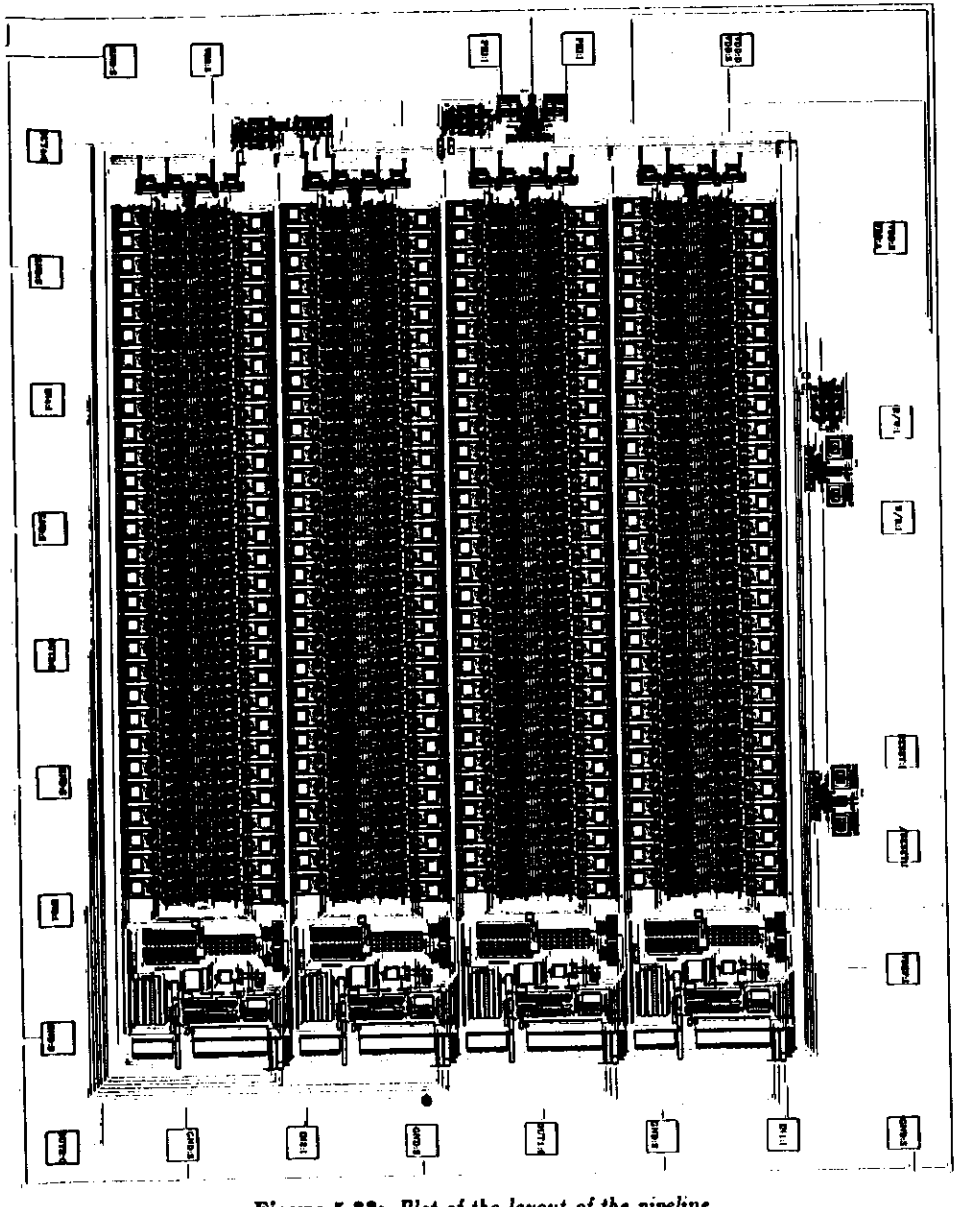


Figure 5.33: *Plot of the layout of the pipeline.*

Also different is the existence of a first "dummy" cell which is normally selected if the circuit is not enabled and which is not readout. Its existence is necessary as the usual state of the buffers is to be waiting for first level trigger decisions compared to the pipelines' usual functioning which are being continuously clocked through the cells. These large stand-by times could charge up the selected cell with pickup voltage which would add to the real analog sample introducing a varying pedestal. Also this dummy cell is the one which is selected at the time of switching from write to read and in the same way as in the pipeline its' charge gets cleared.

All the buffer channels get written simultaneously, in the same way as the pipeline. The reading on the other hand is performed serially one channel after the other driving each sample to the ADC. For this, the digital control in the buffer includes an additional enable path which drives all the shift registers of all the channels when the cells are being written, but only the selected one when reading out the information.

5.9.2 Multiplexer section

A multiplexer is a system that connects several voltage nodes with a further one, one at a time, under control of a select signal. In our case always consecutive nodes are selected, no random access is necessary. The select signal is called increment (`INC`) and each pulse of it selects the next node.

The connection is performed through analog switches. They are implemented as transmission gates. As in the pipeline switches, the control is carried out by a shift register, implemented also with CMOS-flip-flops. Only one "true" state is clocked through and a lock path provides for break-before-make operation so that two nodes are never simultaneously connected to the output.

The integration adopted features on one chip (ca. $20\,mm^2$ of silicon also), 12 inputs multiplexed to one output and further 13 inputs to a second output, while the shift register operates all 25 inputs. The connections are such that the nodes of the first 12 inputs are the outputs of the operational amplifiers of the 12 analog buffers while the other 13 have direct paths to external pins where DC voltages can be connected. The last of the 13 channels is meant to be the baseline signal which determines the chip's output when it is in a stand-by state. Figure 5.34 shows a functional block diagram of the buffer-multiplexer chip.

The digital control system is somewhat more complicated. The multiplexer shift register and one of the 12 other shift registers for the selected buffer have to be operated simultaneously. Additional enable signals have to be generated and the initialize operation has to be performed for all the paths. The circuitry is however basically equivalent to the pipeline. The control signals have the same input comparator so as to be received differentially. The non-overlapping two-phase clock generation is also necessary and performed in the same way as for the pipeline. Figure 5.35 shows the signal sequence required to operate the device.

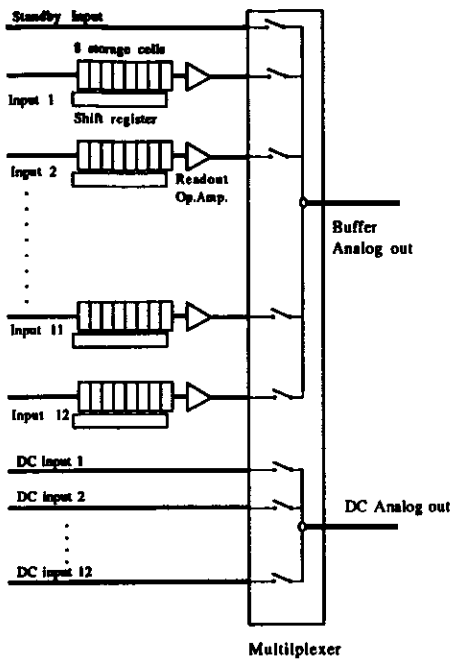


Figure 5.34: *Buffer-multiplexer global block diagram.*

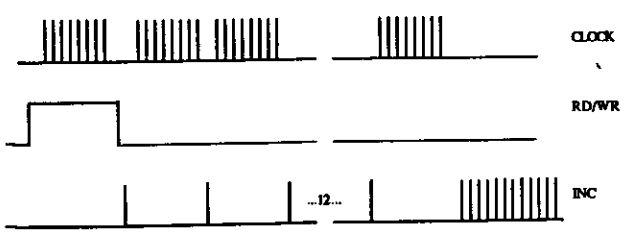


Figure 5.35: *Control signals to operate the buffer-multiplexer chip.*

Chapter 6

Device testing and quality control

The design and production of both the analog pipeline and the buffer-multiplexer chips has been carried out specially for the ZEUS calorimeter readout electronics, both are *full-custom* integrated circuits.

As a new research product the working concept needs to be proven and stability measurements have to be performed. Finally the whole electronics chain has to be tested, calibrated and checked for overall system reliability.

This chapter will cover the test of the chips[1] as stand-alone devices, while the electronics chain as an ensemble will be discussed in the next chapter.

6.1 Testing

In the previous chapter, the external control signals required for the operation of both chips have been described (see figures 5.27 and 5.35). The first step required for testing the devices, is their correct operation with the adequate sequence of control signals.

6.1.1 Device control signal generation

In order to test the devices to investigate their functionality and characteristics, more flexibility is required than the controls for operation in ZEUS. Generating the control signals with a computer which can be reprogrammed in an easy way provides a means of testing the devices under different conditions. However testing under realistic conditions requires the generation of high frequency signals, e.g. the clock period being nominally $96\,ns$ and it has to be proven that the circuit does work at higher frequencies. Testing equipment with this performance is commercially available but at high costs. An intermediate solution is the generation of signals of lower frequency with the computer. These control some auxiliary electronics operating with higher speed signals. This provides both flexibility and realistic conditions.

[1] The discussion will be centered on the pipeline chip where the requirements to be met are more stringent. The apparatus and the tests can and have been applied to the buffer-multiplexer chip as well

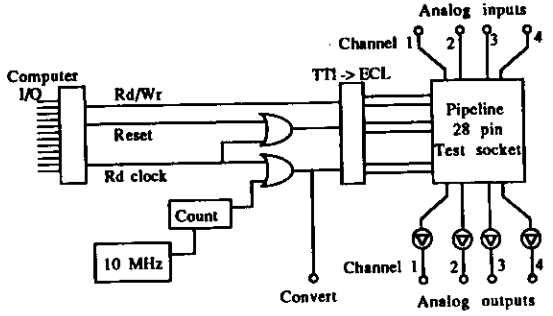


Figure 6.1: *Symbolic layout of the auxiliary board for the analog pipeline test. Note that the main electronics circuitry in implemented in TTL logic and the control signals are interfaced to the chip as ECL levels.*

6.1.2 Test computer elements

The equipment available for testing is centered around a VME-bus [59] based computer with several additional boards connected to it through the bus. The boards used include a CPU[2] based on the Motorola 68020 microprocessor; terminal, mass storage and network interfaces; a 12 bit, 4 channel, $\pm 10\,V$ analog range DAC[3]; a 12 bit precision, $3\mu s$ fast, 16 analog inputs, ± 5 or $\pm 10\,V$ range ADC board and several digital I/O[4] boards.

The main interface for generation of control signals, the I/O boards[5] have 4 registers, 8 bit wide each, which are mapped to the CPU's memory and interface to the output world as TTL voltage levels. They can be used as input or output registers by simple software changes.

6.1.3 Auxiliary electronics

The analog pipeline as shown in figure 5.27 requires 3 control signals: the clock (PHI), the switch between read and write (RD/$\overline{\text{WR}}$) and the RESET.

When writing in the cells, the clock has a frequency of $10.4\,MHz$. An auxiliary board (see figure 6.1) houses a $10.4\,MHz$ free running TTL quartz oscillator. This signal is gated with the RD/$\overline{\text{WR}}$ coming from one of the output pins of the I/O module and is applied to the chip only when WR="1". The number of PHI clocks is counted with a fast counter register and when the count reaches the preset number (from 0 to 255 which can also be set from the I/O port) the fast clocks are blocked in front of the pipeline and the writing process is stopped. At this moment a level is sent back to the computer via another pin of the I/O board.

[2] Central Processing Unit
[3] Digital to Analog Converter
[4] Input/Output
[5] Type XYCOM, XVME-200.

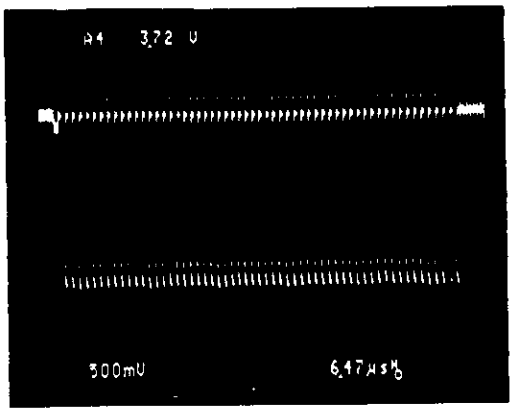


Figure 6.2: *Pipeline output for a DC input of -2.0 Volts.*

The read process then starts. A chain of pulses is sent under computer control and arrive at the chip as clock signals for the read phase. In ZEUS the reading is performed at $1\,MHz$ rate. The RESET signal runs also at $1\,MHz$ but only when reading the cells. In the test system this does not happen with $1\,MHz$ rate since the analog information is digitized with the ADC (BB-AD950) which takes 3 μs to produce the 12 bits.

6.1.4 Testing the functionality

In the initial tests, DC voltages are applied at the pipeline's inputs. The outputs are buffered with unity gain high input impedance buffers so as to avoid excessive load of the CMOS op-amp integrated in the pipelines and to allow the signal to be seen on the oscilloscope and ADC. Figure 6.2 shows a typical scope photograph of the output of a pipeline when the input is -2.0 Volts. Only the signal of 57 cells is seen, the last cell gets corrupted when switching from write to read. The length of the pipeline is in practice only 57 cells.

6.2 Quality control

The production of integrated circuits is a complicated process. Commercial production yields remain well below 100%. The yield depends on the size of the crystal and the clean room conditions. For the pipeline chip ($5 \times 5\,mm^2$ of silicon) the estimated yield is around 40 to 50%.

To minimize packaging costs which can contribute to a large extent ($\sim$ 50%) to the chip's cost the devices have to be tested before the packaging occurs. This is the so-called *wafer* test. It is performed on special "prober" machines which contact the

circuit's bonding pads with very thin needles and apply supply voltages and control signals. The functionality is proven by measuring the currents and output signals. The inputs are normally connected to voltage or current sources which can be controlled by the test computer, the outputs through multiplexers to high precision ADCs. The circuits not satisfying certain quality criteria are marked[6]; the good dyes[7] are bonded and encapsulated into 28 pin PLCC[8] packages for surface mount. First devices were delivered in ceramic chip carriers. Tests (pedestal, gains) were performed to work out the influence of the type of carrier. No obvious reason was found which would have required the use of expensive ceramic carriers.

The quality control tests performed by the manufacturing company were :

1. Supply current (I_{SS})
2. Leakage current of inputs
3. Reference voltage for nominal op-amp reference current
4. Output of every cell for $0\,V$ input (pedestal)
5. Output of every cell for $-2\,V$ input (gain)
6. Rough linearity check for negative input voltages

In figure 6.3 some distributions are shown for the quantities described, for all the dyes contained on one wafer. The acceptance limits set are also drawn.

6.3 Parameters to measure

The measurements on wafer cannot provide full diagnostics for a device. In addition to the functionality tests done by the manufacturing company, several other test are performed after packaging to verify if the performance is within the specification.

The circuit is designed to allow amplitude and time measurements. These measurements are influenced by several parameters (noise, offset, gain, non-linearity, switching jitter), which result in effective noise on the measured quantities.

In this section these measurements will be described in detail and results will be shown.

6.3.1 Noise

Signal processing for particle detection is subject to several sources of uncertainties [60,61] and as a result "noise" appears on the measured quantity. In the chain the signals must go through, the "noisiest" component is the one which dominates the final

[6] usually called *inked*, as a drop of coloured wax is dropped on the faulty crystals.
[7] The single crystals are also called *dyes*.
[8] Plastic Leaded Chip Carrier.

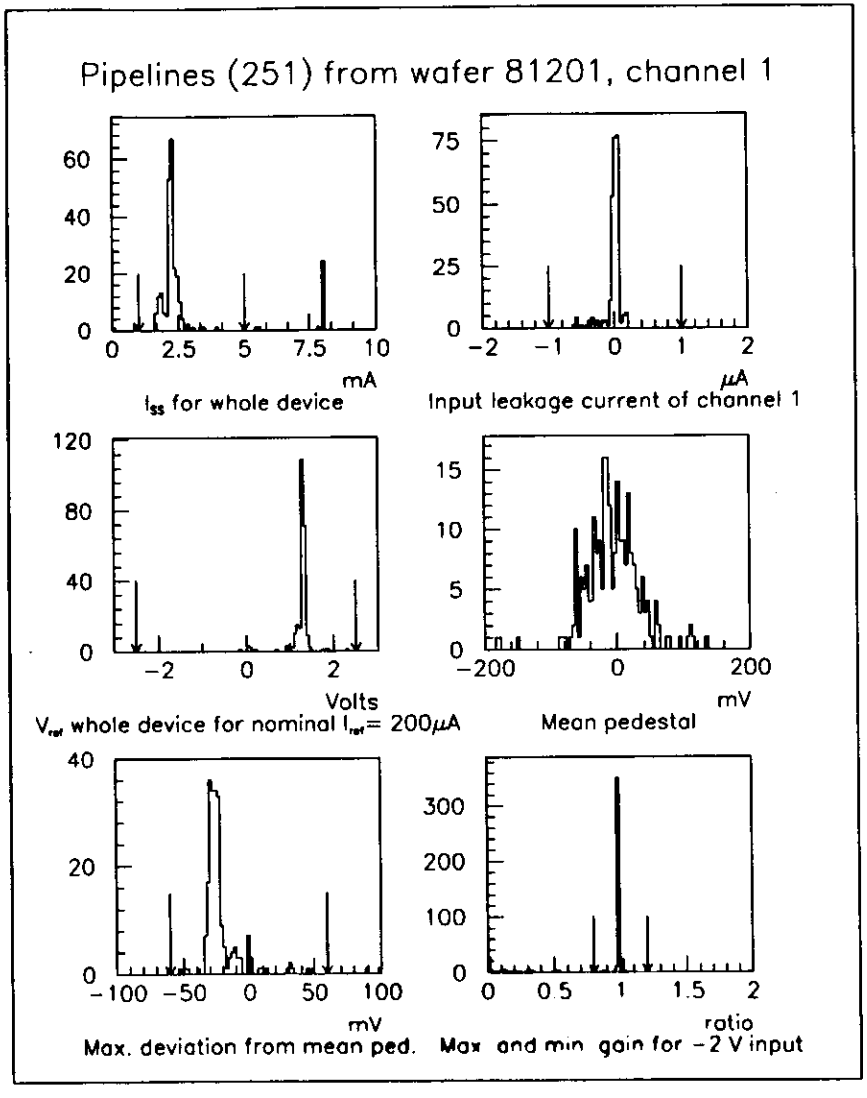


Figure 6.3: *Distribution of test parameters for all 251 pipelines produced on one wafer and acceptance limits. The values shown correspond to one pipeline (1st) channel of each dye.*

noise of the whole measurement. The analog pipeline, a potential noise source with its switches and operational amplifiers should not be this limiting factor.

The noise measurement is performed by repeatedly measuring the output of the pipeline for a "noise free" constant input and analyzing the distribution of this quantity. The standard deviation of this distribution is the quantity we define as noise.

Figure 6.4 shows distributions representing several noise measurements. Figure 6.4-(c) shows the ADC binning limit. The noise seen is constant, around $0.5\,mV\ rms$, independent of the output signal. For a maximum output signal of -4 V, the noise is 8000 times smaller. The Signal to Noise ratio is therefore 8000:1 or $78\,dB$.

In the ZEUS calorimeter electronics, signals of up to -2 Volts will be digitized with 12 bit precision. This means that only 1 count in 4000 will be resolved.

The noise measured when the pipelines are connected to the calorimeter modules will be shown in chapter 8.

6.3.2 Maximum operating frequency

The design of the circuit was such that it should operate at a writing frequency a little above $10\,MHz$. Increasing this frequency results in functional failure at around $18\,MHz$. The reason for this failure was not determined.

The read frequency is limited by the speed of the operational amplifier. It needs $500\,ns$ to reach the end value to within 0.1%, and $500\,ns$ to have the voltage at the feedback capacitor cleared, the operating $1\,MHz$ is the upper limit of operation. Figure 6.5 shows a scope photograph of this reading process.

6.3.3 Pedestal offset

The clock and signal feedthrough and crosstalk mentioned in section 5.4.1 or 5.4.2, are seen as output signal when zero volts are applied at the input. They result in offset voltages (*pedestals*) which have to be corrected when using the circuit. Results are shown in figure 5.19.

Some effects like the CFT are equal for all the cells if all the switches are identical. Others however, depend strongly on the the circuit's topology. Figure 6.6 shows the values of pedestals for one chip (4 pipelines) as measured in the test setup. The asymmetries of the layout mentioned in section 5.8 can be seen when measuring pedestals.

While the mean value of the pedestal is very sensitive to the setup used to provide signals to the pipeline, the exact socket used, the connection of the signal lines to the chip, etc., the relative cell to cell variation is setup independent. Manufacturing tolerances, like mask alignment also cause differences from chip to chip. As explained in Chapter 4, these channel to channel pedestals are measured (on the front-end cards), stored and subtracted from the actual measured quantities. Because of these systematic edge effects, the pedestal of every cell has to be stored, 58 numbers per pipeline, instead

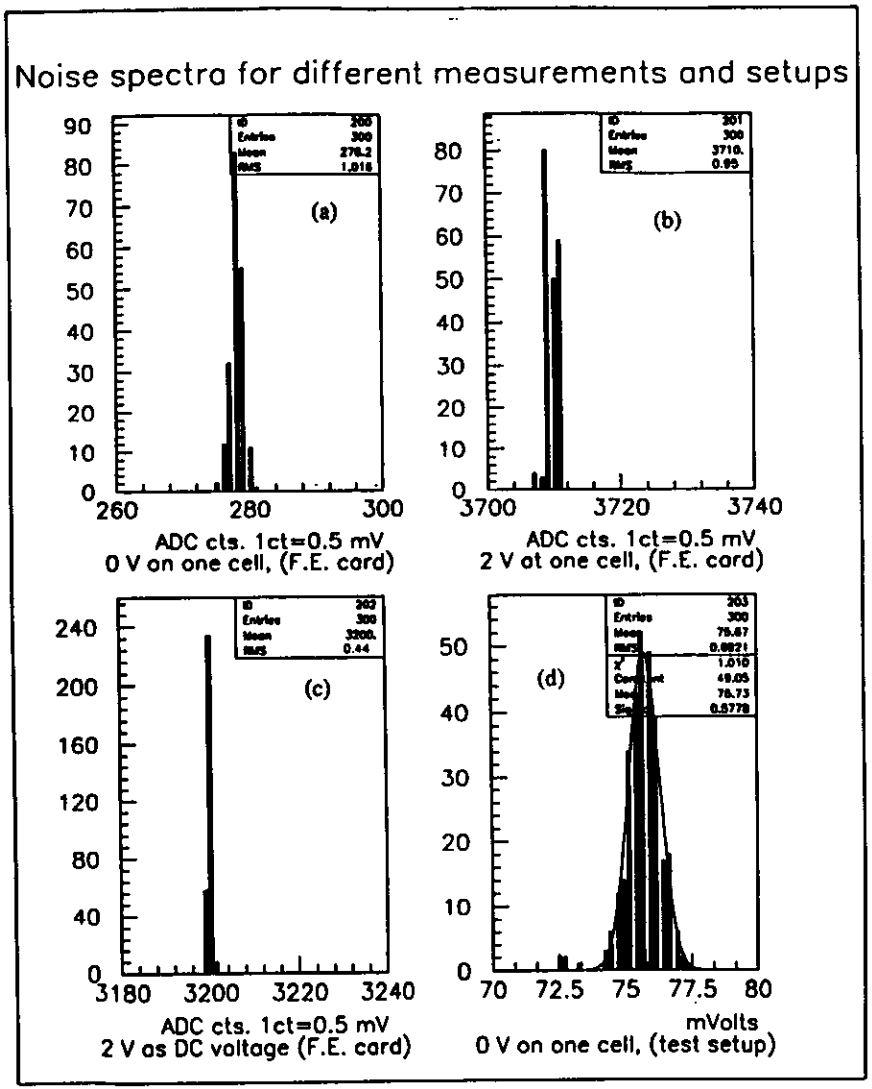


Figure 6.4: *Distributions for noise measurements: (a) Zero volts at one pipeline cell as measured with a front end card, (b) −2 V at one pipeline cell as measured with a front end card, (c) −2 V DC directly at the ADC to show ADC resolution, (d) Zero volts at one cell as measured with test setup and high resolution ADC (0.24 mV/ADC channel).*

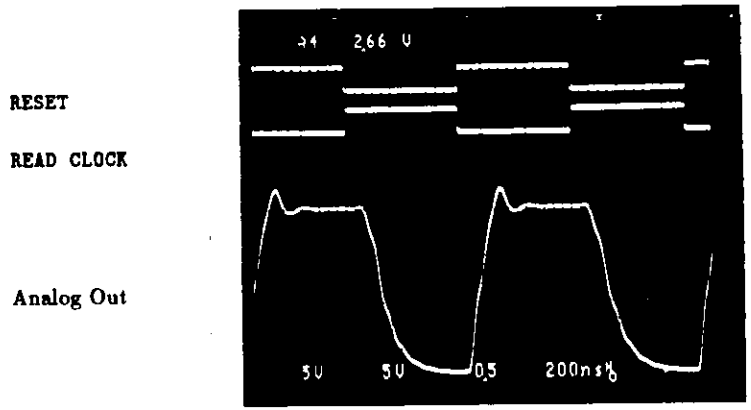


Figure 6.5: *Oscilloscope photograph from a cell reading and reset process.*

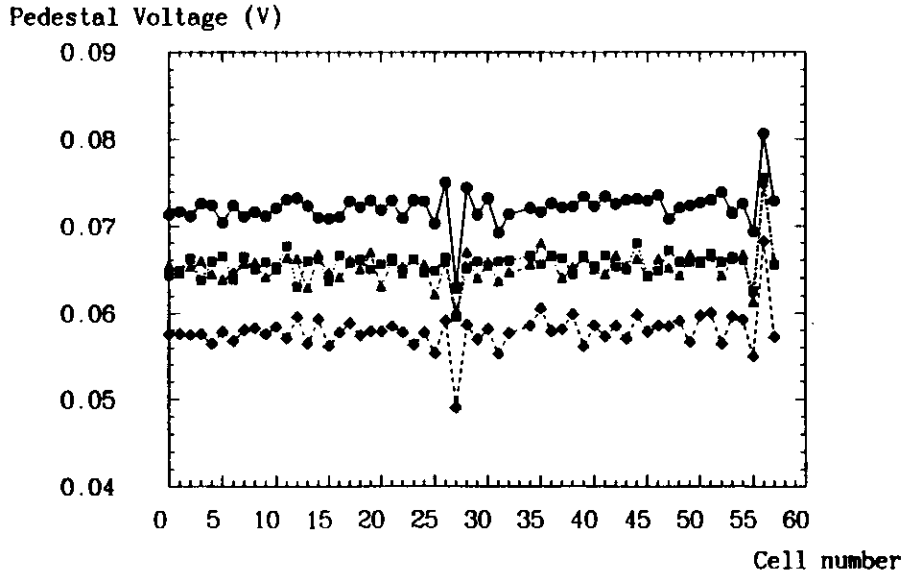


Figure 6.6: *Cell number vs. pedestal voltage for four pipelines in one chip.*

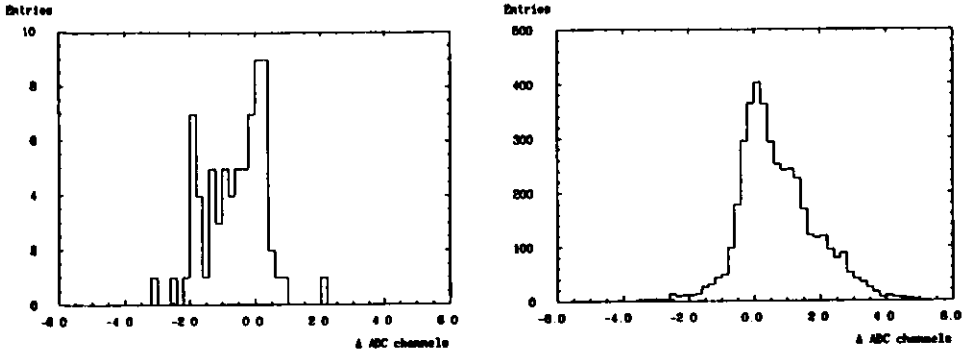


Figure 6.7: *Variation over 3 months of the pedestal of the first cell for 72 pipelines (left); the pedestal of the 57 other cells relative to the first one for the same 72 pipelines (right). 1 ADC count* $\sim 0.5mV$.

of only one global offset which was the aim when the design was started[9]. If this were not done, the structure coming from the asymmetry would cause major errors mainly due to the fact that all the pipelines in the calorimeter are run synchronously. When a trigger starts the readout, in all the channels the same cells are used and millivolt ($\sim 10mV$) errors would be added around 13000 times. This is clearly not acceptable.

. Since the pedestals are mainly dependant on geometrical design factors they should be constant in time. Measurements have shown that this is true.

In figure 6.7 the difference between data taken 3 months apart as measured on cards attached to a calorimeter module in a test-beam stand are shown.

6.3.4 Cell gain and matching

In section 5.3.1 we explained how capacitors are built in MOS circuits. We also saw that the absolute value of capacitance could not be predicted to better than 20 or 30%. However the relative precision of two close by capacitors of the same value can be expected to be around 0.5%. In the layout adopted for the pipeline the ratio output signal to the input (*gain*) is ideally determined only by the proportion of the storage capacitance to the feedback capacitance. To optimize the cell to cell matching all 58 storage cells have been set very close together. The aim was a uniformity better than 1 part in 256 (or 0.4%) (see table 5.1).

As in the pedestal case, the gain of a cell is correlated to its cell number as shown in figure 6.8. It can be seen that within one pipeline the maximum difference between two cells is ~0.8% and the r.m.s. is around 0.5%. This is more than the quoted achievable value for capacitor matching and is attributed to technology limitations.

[9]Other possible solutions would be to leave out events using the corner cells or use a constant for all the cells and additionally two more for cells 29 and 58.

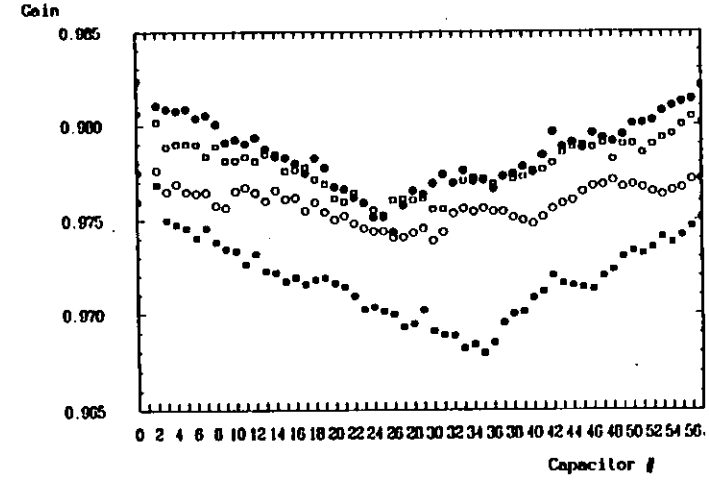


Figure 6.8: *Cell gain vs. cell number for the 4 pipelines in one chip. This is a typical case but also chips without the two row structure exist.*

The gain follows the two row structure of the pipelines cells, increasing or decreasing as we move to the left or to the right. An attempt was made to correlate it to variations of the thickness of the thin oxide which makes up the dielectric medium of the capacitors (see section 5.3.1), but no significant correlation was found and the thickness was checked to be equal to better than 0.5%.

Similarly to the pedestal case, the specification of 0.4% matching has not been achieved; the ~0.8% difference obtained would degrade the calorimeter performance so again digital, cell to cell, corrections are necessary. The gains are measured, stored and applied to the measurements. Instead of one global gain per pipeline 58 different gain numbers are necessary. Here too the gain is a geometry related factor, thus these quantities are constant in time as shown in figure 6.9 for pipelines mounted on a test-beam stand.

6.3.5 Non-linearity

Another important parameter required from any component used in the calorimeter readout is a very good linearity. If a variation in the input of any apparatus does not induce a proportional variation in the output the whole measurement process gets further complicated. The quantity we use to describe how linear a device is, is actually its *non-linearity* and the specification gives a maximum number which should not be exceeded. Figure 6.10-(a) shows how the non-linearity is defined. It is actually the deviation from the straight line that goes through zero (once the pedestal has been subtracted) and the maximum signal used. In figure 6.10-(b) the limits required in the specification are drawn.

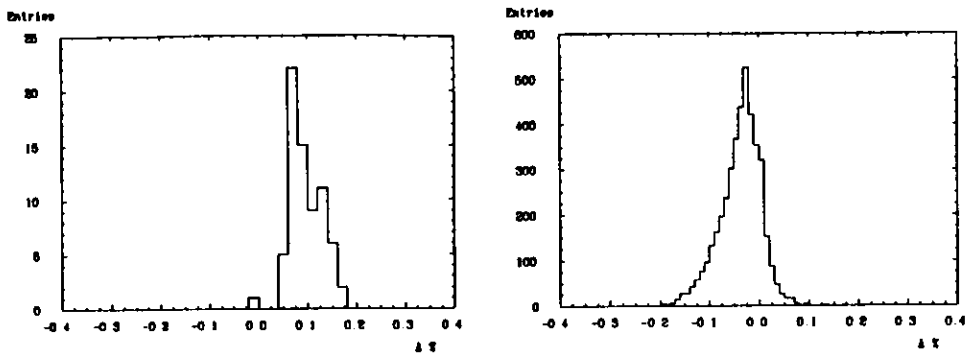


Figure 6.9: *Gain variations over 3 months : (left) of the first cell for 72 pipelines; (right) the gain of the 57 other cells relative to the first one for the same 72 pipelines.*

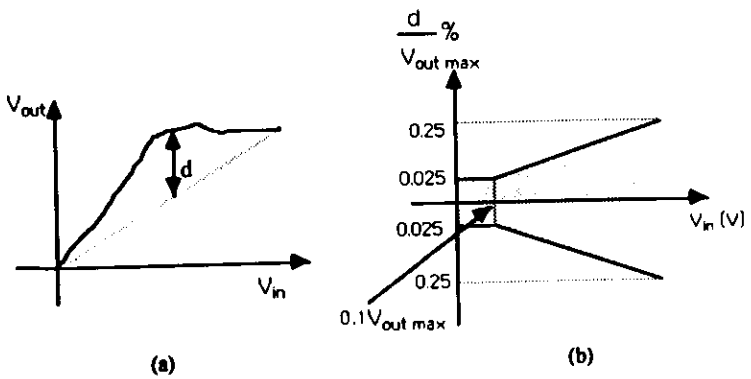


Figure 6.10: *(a) Definition of non-linearity and (b) limits required.*

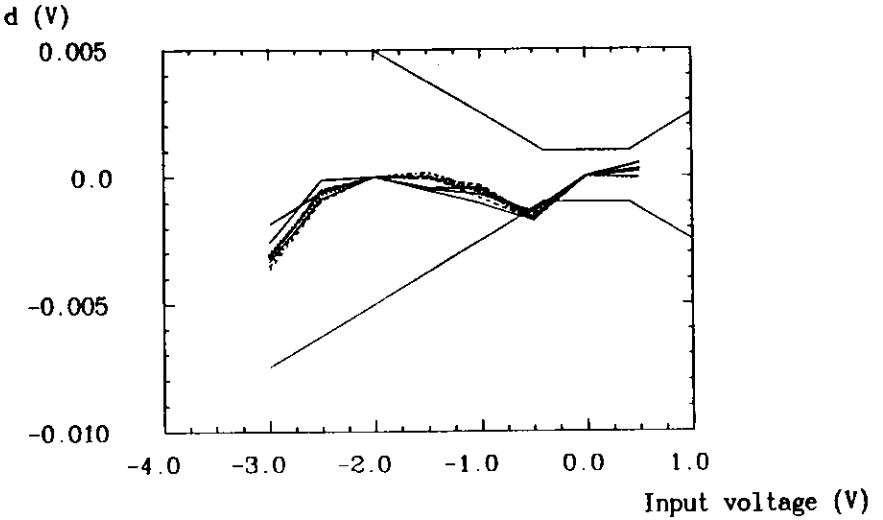


Figure 6.11: *Non linearity for several capacitor of one pipeline.*

In figure 6.11 the non-linearity measured for several cells of different pipelines is plotted. As can be seen it is basically within the specification required for the range used.

The fact that large NMOS transistors are used to implement the global Read/Write switches (see section 5.7), gives the circuit a certain bonus for negative analog signals. If the voltage to store is positive, the V_{GS} of the $n-$channel devices decrease, and so does the transconductance[10] (see figure 5.6). This shows up as an increased non-linear behaviour for large positive signals.

The performance shown of non-linearity smaller than 0.25% allows us to see the circuit as ideally linear in the required range and not needing any further correction. One offset and one gain numbers cover the behaviour of every cell[11].

6.3.6 Charging time constant

In order to be able to store an analog sample in one storage cell and switch to the next one to sample the next voltage, the charging process has to be fast enough. In fact we want to operate the pipeline at $10.4\,MHz$, so in $96\,ns$ we have to switch from one cell to the next and assure that it has reached the charge corresponding to the input voltage.

The process of storage is basically the charging up of a capacitor through a resistor. The resistor represents the ON-resistance of the sampling switch plus the resistances of the other switches in the path of the signal (see section 5.7). This loading process

[10] or the R_{on} resistance of the switch (see equation 5.6)

[11] As a comparison, the "AMU" of SLAC shows a gain non-uniformity of 1.5% plus some curvature in the response which needs a third term in a correction fit to get a resolution better than 10 bit [52].

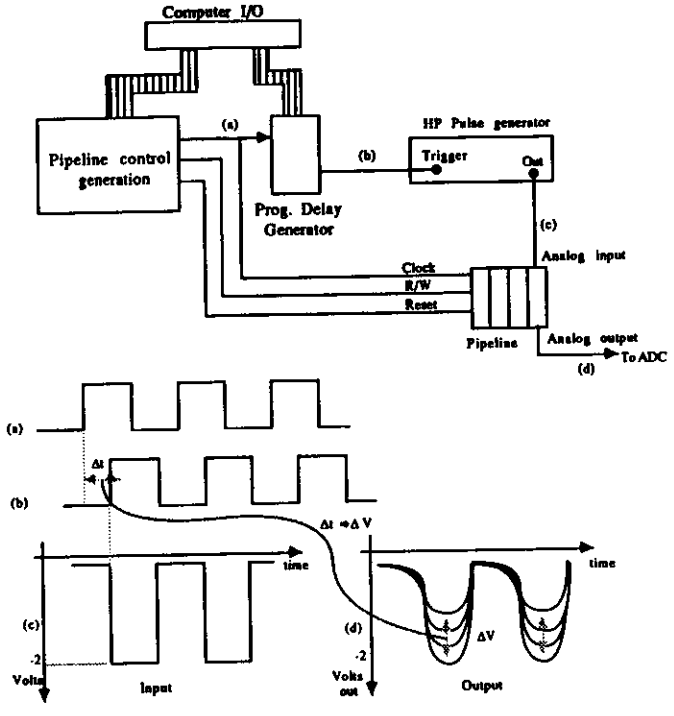


Figure 6.12: *Setup and signals used for time constant and sampling jitter measurement. Note that the sensibility of the test is* $\Delta t \rightarrow \Delta V \sim 200\,\mathrm{mV} \rightarrow 1\,\mathrm{ns}$.

follows an exponential function whose time constant has been simulated to be $\sim 4\,ns$, see figure 5.26.

To measure the parameter we apply a voltage step at the input and measure the output function by shifting in time the voltage step relative to the clock signal which operates the switch.

This process is shown in figure 6.12 with the setup used to generate it. The same sampling clock is used to trigger a programmable pulse generator where the delay (Δt) between the input and the output can be set by the computer to fractions of nanosecond. The output pulse is then fed into the pipeline. The generator used in the measurements has a slew rate of $1\,V/ns$, so the step has a rise time around $2\,ns$.

If we plot the measured output voltage against the delay Δt we obtain the charging curve of the capacitor, and with it the pipeline's time constant. This is plotted in figure 6.13.

The time when the output reaches 63.2% ($1 - 1/e$) of its end value, is by definition the time constant of the circuit. We have calculated that the finite rise time of the input

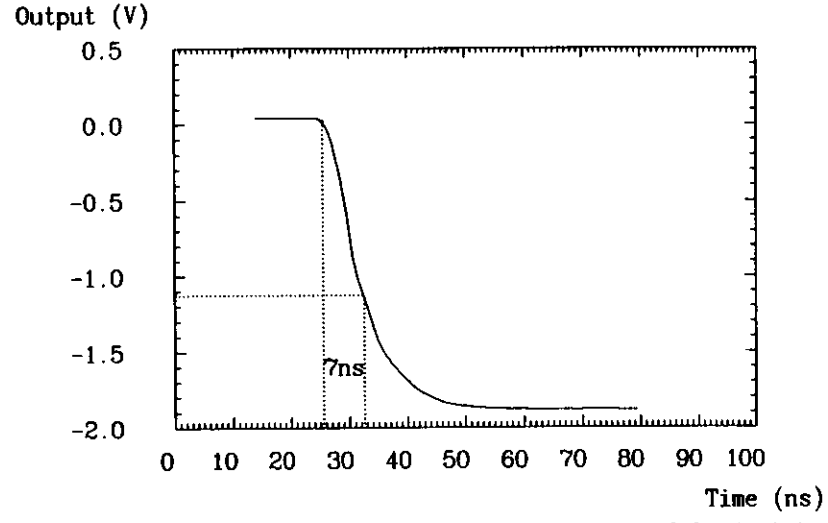


Figure 6.13: *Charging curve of one capacitor. The time constant of the circuit is* $\sim 6\,\mathrm{ns}$. *It is obtained incremented by* $\sim 1\,\mathrm{ns}$ *due to the slewing of the input step.*

signal results in an increment of $\sim 1\,ns$ in the time constant of the output.

The measurement shows a bigger time constant (typically $7\,ns$ and therefore $6\,ns$ for an ideal step input) than the simulated value ($4\,ns$). This difference comes from effects in the real circuit which are difficult to simulate, for example, the input signal does not only see the storage capacitor of the selected cell, but also in parallel the parasitic capacitances from all the other 57 cells even if they are open circuit as mentioned in section 5.6 for the signal feedthrough.

Small variation in charging time from cell to cell might occur. This is however not very important as we give more than $15 \cdot \tau$ time to the cell to charge up.

Note that the charging time acts as a delay on the input signal. In fact we sample the signal which was at the input some small time before. To estimate the effect we calculate the voltage at the capacitor (V_C) in an RC network, figure 4.1, for a linear input $V_{in} = k \cdot t$. The differential equation which gives the voltage at the capacitor

$$\tau \cdot \dot{V}_C + V_C = k \cdot t$$

has the solution $V_C = k \cdot t - k$ which means that the sampled voltage is decreased by the slope of the input signal, in the case of our shaped signal $\sim 0.02\,V$.

Our reconstruction algorithm (see section 7.4.1) however compensates for this slewing effect as it adds samples on the rising and falling sides weighting them with their slopes. The slewing errors compensate.

6.3.7 Switching jitter

Different charge samples of the input are stored in different sampling elements inside the pipelines. These sampling elements have physically different switches which may open at different phases relative to the external sampling clock. If this is the case, the sampling interval is no longer a constant.

Assuming that the input clock signal PHI is of ideal constant period, the differences in switching time have two origins :

- the switches can have different trigger voltages at which they open, due for example to variations of the threshold voltage among the transistors. This characteristic affects the sampling because the voltage edges driving the gates are not infinitely steep.
- the time delay of the paths carrying the complementary clocks signals that drive the shift register is different among the cells mainly due to increasing capacitive load coming from the path itself and from the parasitic capacitances of transmission gates connected to it.

A computer simulation and estimation is difficult (see [42] pp.108-110). The switching jitter has been measured using a technique similar to that in section 6.3.6.

By shifting in time a voltage step input we determine the delay from the moment we apply the CLK signal to the when the output starts to rise, which accounts for the transit time through the input receiver and the shift register flip-flops. This quantity tells us when we are really sampling. To be more sensitive to any variation instead of using the time the output starts to change, we use the time when it reaches half of the step end value. The setup used is the same one as for the charging time measurement (see figure 6.12).

Figure 6.14 shows the quantity switching time delay (t_i transit time from now on) as defined above for all the cells in 4 pipeline channels. It can be seen that within one pipeline, which is what matters for a constant sampling interval, the difference from cell to cell is not bigger than $0.25\,ns$, a remarkable performance. This would result in less than a 0.2% error in the measurement of charge. These quantities are representative for all the pipelines. Thus good performance on the stability of the sampling interval is insured.

For the four pipelines on one chip, and for different chips, t_i can be seen on table 6.1, where the figure quoted is the mean of the 58 cells. One can see that the pipelines in one chip have similar transit times, while for different chips, the differences are larger (see figure 6.15). This fact is not so disturbing since the charge reconstruction algorithm presented in section 7.4.1 is tolerant to this kind of shifts up to some limit. Other elements in the readout chain (e.g. PMTs) have similar uncertainties.

6.3.8 Others

Several other properties have been measured, to check that the performance is acceptable. Figure 6.16 for example shows a scope plot of how the operational amplifier in the

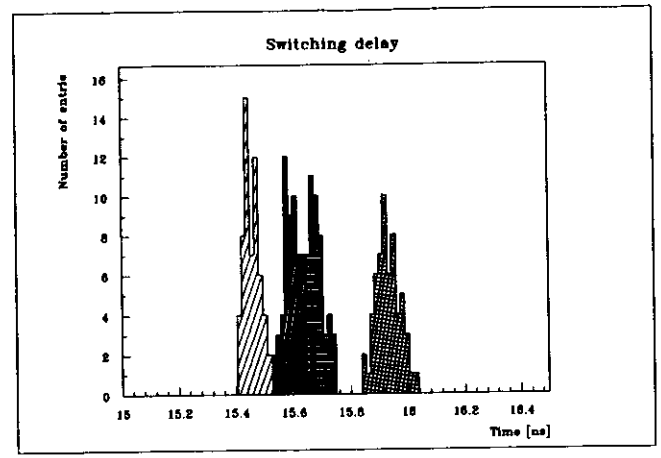


Figure 6.14: *Switching time delay for all the cells in the four pipelines of one chip. Each shaded area represents one pipeline. Within one pipeline the cells have switching delay equal to within* 0.25 ns. *The precision of such measurements is better than* 0.1 ns *and is given by how well we can measure a sample in the middle of the voltage step : we obtain* 1 V *with rms 1% equivalent to* 0.05 ns.

Pipeline number	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	13.5	18.0	17.4	16.5	18.8	16.7
2	13.3	18.0	17.3	16.2	18.6	16.4
3	13.3	17.9	17.4	16.4	18.8	16.6
4	13.4	18.1	17.5	16.2	18.8	16.5

Table 6.1: *Mean transit time through different pipelines.*

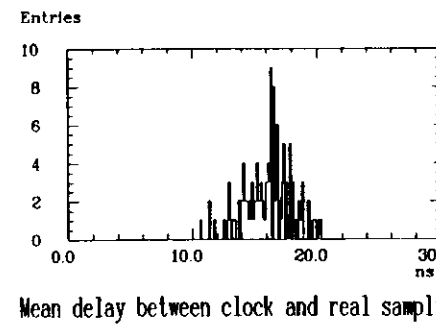


Figure 6.15: *Distribution of transit times for 150 different pipeline chips. The plotted value is the mean of the four pipelines. The maximum differences among chips is* 10 ns *while the standard deviation of the distribution is* $\sim$ 2 ns.

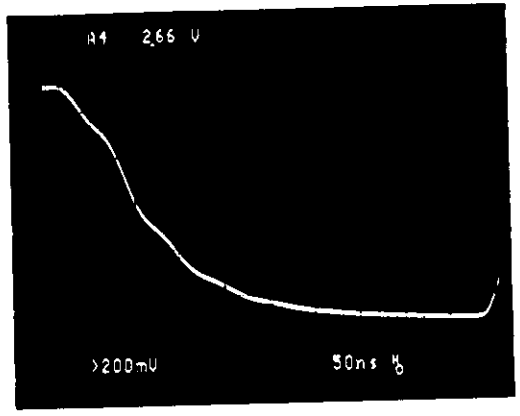


Figure 6.16: *Oscilloscope photograph showing settling of pipeline's op-amp.*

pipeline reaches its end value. It can be seen (though difficult in this photograph) that after $500\,ns$, the value does not diverge more than 0.1% from the final level. The speed of the operational amplifier can be regulated with the reference current we fix from the outside. Typically we use $50\,\mu A$ I_{ref} per amplifier.

Figure 6.17 shows the droop rate of the capacitors. On the photograph the loss of charge of the feedback capacitor while reading without applying a reset signal, is estimated at $\sim 1\,mV/ms$. The droop rate of the capacitors when they are disconnected cannot be seen in the picture but has been measured to be $\sim 2\,mV/s$. These figures are certainly on the safe side when operating the pipeline at MHz speed.

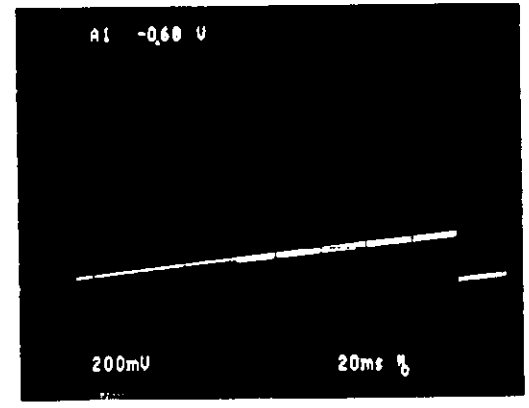


Figure 6.17: *Oscilloscope photograph showing the discharging of the capacitors. Note the time scale* ms.

Chapter 7

Readout implementation

The concept for the readout of the ZEUS calorimeter has been presented in chapter 4.

A first working environment has been implemented and used for data taking for several months. It is used for the calibration of FCAL and RCAL[1] modules with a particle test beam at CERN. Parallel test are being performed at FNAL for the BCAL modules. These modules are the ones which will be used in the ZEUS experiment. Previous tests performed with prototypes of the modules [12] and prototypes of the electronics [62,33] served to optimize the calorimeter construction and test the readout concepts.

The aim of the test beam effort is to understand the response of the different calorimeter sections to different types of particles and determine the precision of the overall calibration.

For the test beam experiments, the complexity of the readout is a fraction of that of the full calorimeter in the ZEUS experiment at HERA. However most of the systems and ideas used are the final ones and have been tested here for the first time in a real experimental environment.

This chapter will give a detailed description of the readout for the ZEUS calorimeter including concepts in software and hardware. Divergencies of the test beam setups from the final implementation will also be described.

The experimental setup for the tests performed at CERN and some results obtained are discussed in the next chapter.

7.1 Analog readout of the calorimeter modules

The principle of the ZEUS calorimeter, from the energy deposited by particles to the electric signal generated by the photomultipliers, has been described in chapter 3. Here the electronics for the analog readout of the PMTs will be described.

[1]The forward and rear parts of the ZEUS high resolution depleted uranium calorimeter will be referred to generically as the FCAL throughout this chapter.

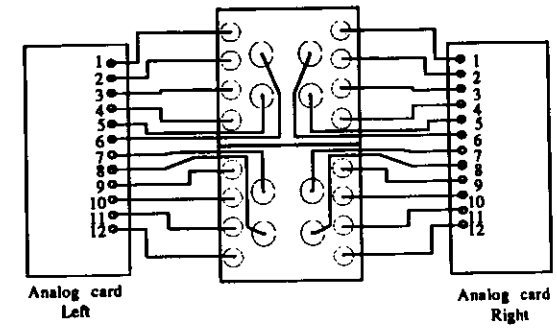


Figure 7.1: *Typical connectivity of PMTs to Frond end cards.*

7.1.1 Analog Front-End Cards

Signal cables ($\sim 2m$, $50\,\Omega$) connect the PMTs to the analog front-end cards. These cards are designed and built following the concepts explained in chapter 4. As discussed there, their heart pieces are the two custom integrated circuits described in chapter 5, the analog pipeline and the buffer-multiplexer chips.

The module segmentation packs 12 PMT channels on each analog card with two analog outputs feeding two different ADCs, each one carrying multiplexed information of 6 PMTs. This is a natural division due to the tower structure of figure 3.7. The connectivity is shown in figure 7.1. It keeps the readout of left and right calorimeter sides on separate front end cards and thus provides some redundancy in case of failure.

Figure 7.2 shows a scheme of one card. The components are listed below.

- Twelve coaxial *connectors* receive the cables from the PMTs. The current signal is resistively split and connected to :
  - the termination, resistor R_0 and capacitor C_0,
  - the high gain pulse measuring circuit with capacitive coupling (R_H),
  - the low gain pulse measuring circuit with capacitive coupling (R_L),
  - the trigger output with capacitive coupling (R_T).
  - the DC integrating network.

  The values of the components are chosen so that the global impedance at the end of the PMT cable is $50\,\Omega$ and all the networks have identical time constants (though the trigger output has a different time constant which is cancelled at the input of the trigger sum cards).

- Twelve *shaper* subcircuit boards. They are built with hybrid technology on ceramic substrate, with copper plating on the back side to form a ground plane.

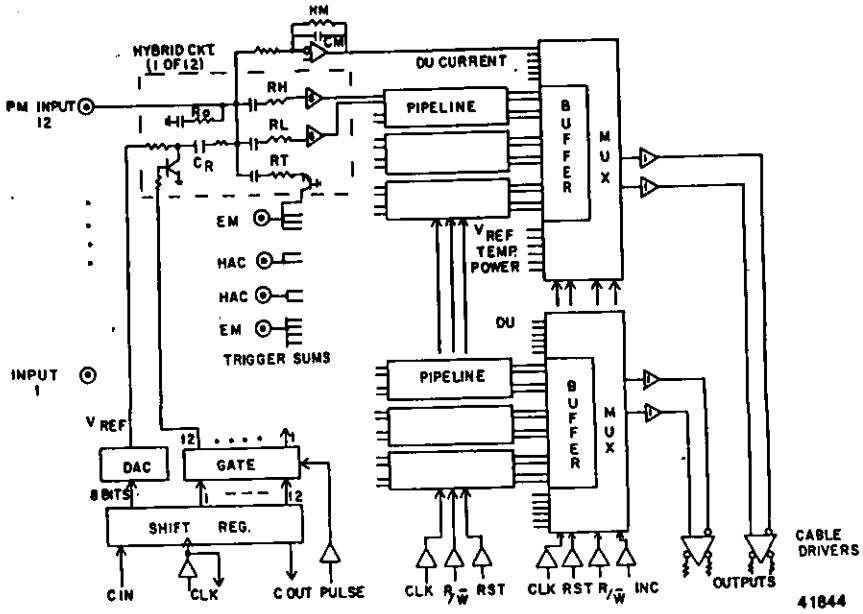


Figure 7.2: *Schematics of one analog front-end card.*

The components include laser trimmed thick film resistors. On these hybrid are placed the current splitting networks. The two shapers circuits covering different energy ranges as explained in section 4.6.2 are mounted back to back.

RC networks mounted onto the shaper boards with fast analog switches provide the possibility to *inject charge* directly into the main signal paths, as if it came from the PMTs' anodes. The leading edge of the pulse is a fast signal produced by the discharge of the capacitor when it is connected through the analog switch to ground. The trailing edge is implemented to be similar to the decay of the light signal coming from the calorimeter.

The amount of charge injected can be set by a semi-DC voltage level which charges the capacitor and which is generated in the calibration subcircuit (see below). The capacitor is dimensioned to $22\,pF$ and is made up of two capacitors in parallel; one of them can be trimmed so that all the injectors are equal to 0.2%.

- The *Trigger outputs* from the shapers are grouped on the main board to perform analog current sums. Transistors separate the channels so that no coupling occurs. Four different sums[2] are performed and carried to coaxial connectors for output. These outputs are further connected to analog trigger sum cards where several

[2]Channels 1+2+3+4, 5+6, 7+8, 9+10+11+12 give the electromagnetic and hadronic sums (for FCAL and BCAL).

towers are added together. After a $60\,m$ cable to the Rucksack the digital trigger system starts (see section 4.2.5).

- Twelve *operational amplifiers* connected as current to voltage converters using 0.1% precision resistors and with a time constant of $20\,ms$ provide the measurement of the semi-DC current from the PMTs caused by the uranium radioactivity. The fact that the DU current is much larger[3] than the dark current from the PMTs and that the time constant used for the integration allow single measurements with precisions of 1%.

- The *analog pipelines* sample and store the output of the shapers, one pipeline channel for the high gain channel, another one for the low gain. One chip thus serves two phototubes.

- Their outputs are connected to the *buffer-multiplexer* chips. Two buffer-multiplexer chips cover the 12 PMT channels of the analog card. The 12 external DC multiplexer inputs are connected to :

  - 6 DU integrators to send out the DC voltage proportional to the UNO current,
  - 2 ground signals to readout the ground level on the analog cards. This is the reference for the other signals,
  - a voltage signal generated by a *precision voltage* source of 5 Volts which is split with a 0.1% accurate resistive divider down to 1.67 Volts. It serves to convert ADC counts to volts taking into account the whole analog chain of cable driver, cable and ADC,
  - a precise fraction (2/5) of the voltage which is used to load the capacitor of the charge injector,
  - the voltage from a temperature sensor on the card.

  These voltages can thus be brought to the ADCs for digitizing.

- Differential *receiving circuits* accept incoming ECL-$\overline{\text{ECL}}$ control signals for pipeline and buffer-multiplexer control.

- A *calibration subcircuit* constructed as a hybrid inserted onto the main board supports an 8 bit DAC chip, which is used to set the DC voltage to drive the charge injectors. In addition through an analog switch, the DC voltage can be connected directly to the inputs of the pipelines, providing the means to test the pedestals and gains of the storage cells as described in section 6.3.3 and 6.3.4. Through a resistive laser trimmed precision divider it is connected to one of the DC multiplexer inputs. This allows absolute charge injection calibration as it gives a feedback of the amount of charge injected.

  The DC voltage can also be connected to the DU integrators for calibration.

[3]Note that the specification for the PMTs is to have a dark current $\leq 0.1\,nA$ (doubling every $7°C$) and the DU current amounts to $100\,nA$ in the EMC sections and $500\,nA$ in the HAC sections.

- A *shift register chain* made up by 3, serial in-parallel out, 8 bit deep devices, linked as a daisy chain. They are also daisy chained with neighbouring cards through serial-in and serial-out channels. A clock running parallel to the data, shifts it from card to card through the whole calorimeter. It provides two functions :
  - Setting individual bits in the register allowing pulsing of the corresponding charge injectors. Firing all of them simultaneously serves to calibrate the readout system up to an equivalent energy of $\sim 20\,GeV$. Pulsing some of them simulates energy deposits in the calorimeter following given patterns, isolated particles, jets, ... mainly in order to check the performance of the trigger system.
  - Further shift register bits set the DAC and also define the path the DC voltage is connected to, directly to the pipelines or to the charge injectors.

  The signals for the charge injectors are generated on the assertion of an external PULSE originated in the control system which enables the parallel output of the shift registers.
- A separate *blocking signal*, MODE, disables the functioning of the whole shift register chain.
- Two *cable driver* subcircuits, also constructed as hybrids inserted on the main PCB, drive the analog output signals from the buffer-multiplexer chips through 60 meters of twisted pair cable to the ADC cards. This is a high performance device mainly due to its excellent linearity. The signals, typically ranging from zero to -2 Volts are sent down as complementary pair (-1 and $+1\,V$ and centered around $0\,V$) and a differential amplifier receives them in front of the ADC chip.
- Several fixed *voltage regulators* supply the diverse components with the necessary voltages : $\pm 5\,V$ for the custom circuits and the digital components, $\pm 8\,V$ for the shapers and cable driver hybrids. The input voltages used are $\pm 11\,V$. The regulators are screwed to the back of the card which is covered by two $1.5\,mm$ sheets of aluminium to carry away the heat. The cards on their turn are fixed to a cooper cooling beam cooled by circulating water.

The total power consumed in the card is about $16.6\,W$ of which $5.9\,W$ is dissipated by the regulators.

The signal lines connecting an analog card to the rest of the system are shown in figure 7.3-(a) where the analog card is shown as a black box. All except the PMT and the trigger connectors[4] are placed on a multiwire flat ribbon Input/Output (I/O) connector. The arrangement of this connector can be seen in figure 7.3-(b).

7.1.2 Front-End control signal generation

Except for the PMT signals which come from the calorimeter, all the input signals in figure 7.3 are control signals which have to be generated. They have to be brought to

[4]These have their own coaxial mini connectors type Sealectro™.

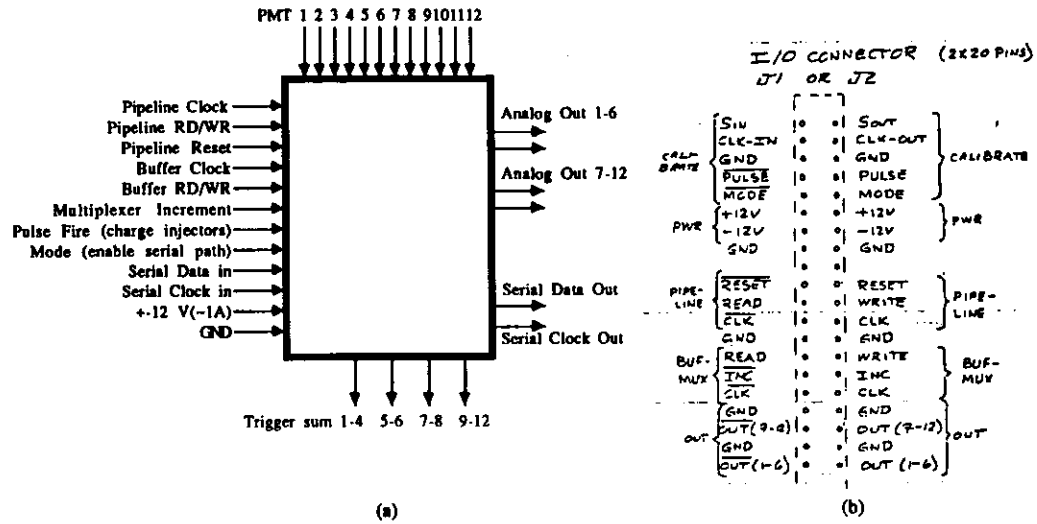


Figure 7.3: *(a) Signals connecting to an analog card, (b) Input/Output connector linking an analog card to the control and DAQ system.*

the I/O connector of the analog cards. The whole ensemble is a relatively sophisticated system which is described in the following sections.

The generation is performed by several control units, electronic cards built as NIM[5] units. At **ZEUS** they will be placed in a crate in the rucksack, 60 meters away from the calorimeter modules. At the **CERN** test-beam the crate is placed in the control hut, also 60 meters away from the module.

From their functionality, the control signals form natural groups. These are generated by different modules which do however have to interchange some signals. A description of the modules as for their external connectivity is given here. All these control modules are linked in between them with several coaxial and flat ribbon cables. They form a whole as shown in figure 7.4.

Pipeline controller module

It generates the control signals for the pipeline chips : READ/$\overline{\text{WRITE}}$, CLOCK and $\overline{\text{RESET}}$[6]. These leave the unit as NIM logical levels. The circuit that produces them is a set of shift registers, flip-flops, counters and gates, all ECL components. It requires several pieces of information which it obtains from the neighbouring modules in form of logical ECL levels. From the rest of the system it obtains :

- the basic synchronization clock, $10.4\,MHz$;

[5]Nuclear Instrument Module

[6]This signal though generated in the pipeline controller module, is not used as it can be produced on the analog card (see relation 7.1).

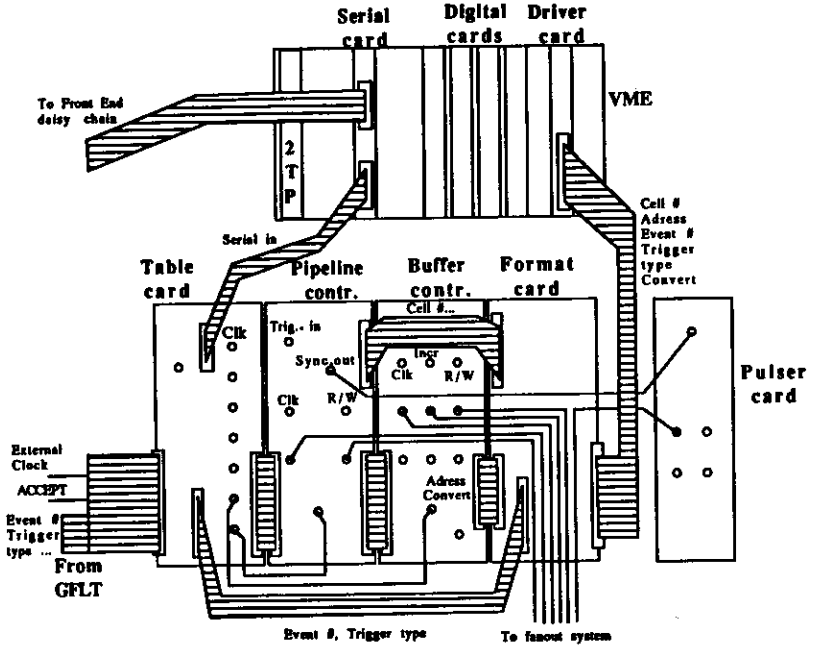


Figure 7.4: *Control modules for calorimeter electronics and interface to the data acquisition system and their connectivity.*

- a trigger signal. The usual working state of the front end is that signals are continuously being written into the pipelines with 10.4 MHz sampling clock. The mode is switched from write to read triggered by an event and the interesting pipeline samples are passed onto the buffers. This process is initiated by a trigger signal, which arrives from the GFLT ACCEPT signal (see section 4.2.5) in the **ZEUS** environment and from the selected particle trigger described in section 8.1 for the **CERN** test stand.

- several signals to synchronize the pipelines with the buffer operation;

- various numbers, in form of binary parallel signals, providing diverse counting data, e.g. how many cells to read out or how many cells have to be skipped after a trigger is received to find the interesting samples.

Various other signals apart from the 3 pipeline controls are produced. They link this controller to the other cards. For example a `pipeline BUSY` signal or the actual `cell number` where the analog signal is being stored or retrieved, are required to interface to the rest of the system.

A further important signal is also generated on this module, the `PULSE` signal is produced when a trigger arrives and is synchronized with the 96 ns clock. The synchronization can in addition be forced to happen when a certain cell number is reached. The final concept at **ZEUS** includes an additional *pulser card* to perform this duty.

Buffer controller module

It produces in the same way as the pipeline controller, NIM signals for the buffer-multiplexer chips on the analog cards. These are : `READ/`$\overline{\texttt{WRITE}}$, `CLOCK` and `INCREMENT`. The `RESET` for the feedback capacitors at the buffer's output operational amplifiers is produced locally on the analog cards with the logical operation:

$$\texttt{RESET} = \overline{\texttt{CLOCK}} \cdot \texttt{READ} \tag{7.1}$$

and is not handled by the controller.

It also produces the `CONVERT` signal, which is channeled to the ADCs and defines the exact time when the analog output voltages are to be digitized. In a similar way to the pipeline controller, some additional signals link this module to the rest of the control system. Sample count or synchronization signals, including the 96 ns clock come from the pipeline controller. Also `Buffer BUSY` or `Cell number` are also generated and passed on. The `Address` of the memory where the samples have to be stored once digitized, is produced here.

7.1.3 Auxiliary modules for control

In addition to the two modules that generate the control signals for the pipelined system, several others are needed.

Pipeline test module or Table card

This module does not produce any control signal but acts as an interface to the trigger and data acquisition system. The *Pipeline test module* is used at the **CERN** test facility (and other test setups), while the final version of control electronics for **ZEUS** will use the so-called *Table card*[7].

On this card, the $96\,ns$ clock is generated (internal mode, e.g. at **CERN**) or received (external mode, at **ZEUS**) and regenerated for further distribution to the rest of the control system.

The Table card provides the interface between the GFLT and the calorimeter control system. On a 17 pair flat cable it receives from the GFLT the following data [63]:

Pair #	Assignment
0	reserved
1	test enable
2-4	test trigger type
5-6	readout type - system control
7-8	readout type - crossing ambiguity
9-11	readout type - component dependent
12	abort flag
13	accept flag
14-16	reserved

The test trigger type is ony valid if the test enable is set while the readout type and the abort flag require the accept flag to be set. The system control bit field is interpreted as follows :

value	meaning
0	normal readout
1	off beam trigger
2	test trigger
3	initialization

The Table card is downloaded with tables of data which relate the signals from the GFLT to information used in the readout control, e.g. from the crossing ambiguity the table produces and passes to the pipeline controller the number of cells to skip and to the format card the position of the baseline sample.

The computer system links to the control electronics by means of this module through several serial channels. Thus information like the number of cells to be readout (e.g. for test triggers) can control the operation of the readout system. From the Table card this data is made available to the pipeline controller, format and pulser cards, either in a parallel data form or by further connecting the serial channels.

[7] These two units will be referred to in this document as **Table card**. It should be understood as *Table card* in **ZEUS** and *Pipeline test module* at **CERN**.

Serial card

The module placed in the the data acquisition system which communicates with the Table card is the *serial card*. It is a VME unit (see section 7.2.2) which can be accessed by the data acquisition system.

Its hardware consists mainly of several FIFO registers into which this "serial" information is written. On the reception of a "send" command, the data words in the FIFO are sent under control of a $1\,MHz$ clock produced by an on-board quartz crystal. Bits are sent in a serial way one bit at a time, most significant bit first through a level converter. Both the data and the shifting clock, originally TTL logic levels are transformed into ECL-$\overline{\text{ECL}}$ signals and sent on twisted pair cables off from the board.

Eight FIFO channels are available on each serial card. They can be written individually and upon the SEND command, if any data is in the FIFO, clock pulses are produced and the bits are sent. Thus sets of different lengths may be shipped out. The 8 channels are completely equivalent and can be connected to any part of the system. At the **CERN** test stand, one such card exists and four channels out of the eight are used. In **ZEUS** several serial cards will be necessary. The channel numbers given below are the ones used at **CERN**. The information pieces are as follows:

- Channel 2 is connected to the general signal distribution system and is daisy chained on the right half of the module. The data is carried through the shift registers of the analog cards (see section 7.1.1). For each analog card, three bytes are sent:

  1. The 7 LSBs[8] determine the voltage set by the DAC on the calibration subassembly. 0000000 is maximum voltage ($5\,V$ at DACs' output), 1111111 represents minimum voltage. The voltage is applied to the charge injectors. The MSB[9] determines (when "0") whether a fraction (2/5) of the DAC's output voltage should also be directly connected to the pipeline's input to measure pedestals or gains. This precision voltage is also applied to the input of the DU integrators to have a calibration of their offset and gain.
  2. Any set bit in the first 6 LSBs enables the firing of the charge injectors on the PMT channels $7 \ldots 12$. The actual firing is done on the receipt of a PULSE signal.
  3. Ditto, but for PMTs $1 \ldots 6$.

  A total number of bytes equal to three times the number of analog cards in the daisy chain must be written to the FIFO.

- Channel 3 is exactly the same, but connects to the daisy chain on the left side of the module.

  In **ZEUS** channels 2 and 3 from several serial cards will feed all the daisy chains of front-end cards in all the modules.

[8] Least Significant Bit
[9] Most Significant Bit

- Channel 4 connects directly to the Table card. In the operation at **ZEUS** tables are downloaded. They are described in detail in [63].

  For the operation of the pipeline test module as used at the **CERN** test beam, three bytes are sent via this serial channel :

  1. Bit 4 of byte 1 provides control for the generation of a synchronized signal which can be used as **PULSE**. The rest of the byte is not used.
  2. The 6 LSBs define the number of cells which have to be counted after the reception of a trigger before the reading of the pipelines starts. This is a crucial number which reflects how long the trigger system needs to produce a decision after the signal arrives in the calorimeter pipelines. It is further explained below.
  3. The 3 LSBs determine the number (maximum of 8) of samples which will be readout into the buffer and to the ADCs. The 4th bit (if "1") forces the readout of the DC multiplexer positions of the buffer-multiplexer chips. The 4 MSBs are not used.

  The example of beam triggers at **CERN** will be used to clarify the aim of byte 2 and why it needs to be under computer control.

  A beam particle at the **CERN** test (see section 8.1) is detected by a coincidence of signals from scintillation counters on its path. About $1\,ns$ later it hits the calorimeter and deposits its energy producing scintillating light in the layers, which appears after a transit and rise time (e.g. $20\,ns$) as a charge signal at the output of the PMTs. The signal is integrated, shaped and samples are stored in several contiguous pipeline cells. After this, the signal returns to zero but the sampling and storing process continues on the subsequent cells.

  The signals from the counters travel on 30 meters long ($150\,ns$) coaxial cables to the hut. There, they are discriminated on a threshold and logically combined with fast electronics which also needs a few hundreds of ns. Finally a trigger is produced and it reaches the pipeline test module about $1\,\mu s$ after the particle hit the calorimeter. At $10.4\,MHz$, this corresponds to 10 pipeline cells which in the meantime have been written. The interesting information now has to be readout. To achieve this, the next 58-10, i.e. 48 cells should be skipped, then the pipeline is set into read mode, the buffer set into write mode and as many clocks as samples required are sent. Skipping cells is done by writing into them at $10.4\,MHz$. As we have seen the number of cells to skip depends on the trigger timing and is thus most conveniently set from the computer.

  In **ZEUS** this number will be small (from 0 to 10) because the GFLT decision takes up the whole length of the pipeline.

- Channel 5 connects to the pipeline controller unit although the cable from the serial card plugs into the Table card. The purpose of this data is to permit test triggers so that well defined cells in the pipelines can be readout for example to determine the individual cell pedestals as will be shown in section 7.3.2. The input

  triggers are delayed until a certain cell is reached in the count. Four bytes are sent and they order as follows:

  1. Bits 1-8 allow setting a programmable delay generator and shift in time the PULSE signal relative to the sampling clock to perform studies like in figure 6.12 or pulse shape analysis.
  2. Not used
  3. Bits 1-8 is the number of rotations of the trigger synchronization, i.e. how many times the whole pipeline must be clocked through before the trigger is released. This feature is in fact rarely used.
  4. Bits 1-6 set the cell number to which the trigger should be synchronized to. Bit 7 disables this synchronization feature. Bit 8 disables the synchronization with the number of rotations. Having both conditions disabled is the usual running mode for beam data taking.

- Channel 6 will be additionally used at **ZEUS**. Bits defining the delay between the buffer read signals and the convert edges will be needed. Their use is explained in the next Section. Four bytes are foreseen.

- Channel 7 will also be used at **ZEUS** to direct the serial information going to the analog cards on the modules. One byte of serial data is sent to the fanout system (see section 7.1.4). The 7 LSBs of the byte define to which calorimeter module should the serial data for the daisy chain of analog cards (at **CERN** channels 2 and 3) be sent to. Setting the MSB will activate all the fan outs and the same serial data will be sent to all the modules of the whole calorimeter. This will be the usual operation mode. The individual loading will be only used to test triggering schemes.

Table 7.1 shows a summary of the information sent through the serial links.

Format card

Several pieces of information either generated or available at the NIM controller units of section 7.1.2 have to be readout into the data acquisition system. They are an integral part of the data and should accompany it to the final storage. The following quantities have to be integrated in the data stream:

1. *Cell number* where the first readout sample was stored. The following samples are in consecutive cells. This data serves as address to the table where the correction constants for the pipelines' cells gains or pedestals are stored. Note that this number is conceptually different than the cell number mentioned in the previous section where it is been set (not read from) on the controllers for calibration purposes.
2. *GFLT Bunch Crossing Number*, is produced by the GFLT box and fed into the Table card. In **ZEUS** it identifies the bucket at which the trigger was generated.

Serial Channel connected to	Byte	bits : Function
Right front-end daisy chain	1	1-7 : DAC value (0=maximum) 8 : DC to pipeline (if "0")
	2	1-6 : Fire Charge injection PMTs 7-12 7-8 : Not used
	3	1-6 : Fire Charge injection PMTs 1-6 7-8 : Not used
Left front-end daisy chain	1	1-7 : DAC value (0=maximum) 8 : DC to pipeline (if "0")
	2	1-6 : Fire Charge injection PMTs 7-12 7-8 : Not used
	3	1-6 : Fire Charge injection PMTs 1-6 7-8 : Not used
Pipeline controller	1	1-8 : PULSE delay (units of $0.5\,ns$)
	2	1-8 : Not used
	3	1-8 : Rotation number to synchronize
	4	1-6 : Cell number to synchronize 7 : Disable cell synchronization 8 : Disable rotation synchronization
Table card used as pipeline test module	1	1-3 : Not used 4 : Enable sync. Pulse out 5-8 : Not used
	2	1-6 : Number of cells to skip before read 7-8 : Not used
	3	1-3 : Number of samples to readout 4 : Readout DC values (UNO ...) 5-8 : Not used
Format card	1	1-8 : Convert delay FCAL
	2	1-8 : Convert delay BCAL
	3	1-8 : Convert delay BCAL
	4	1-8 : Convert delay spare
Fanout system	1	1-7 : Module addr. for daisy chain data 8 : All modules receive serial data

Table 7.1: *Serial data sent on the different channels to control the readout, control and distribution system. Note that the two channels connected to the daisy chains have to be loaded with 3 bytes times the number of cards connected on the chain. For the serial data used to load the Table card and their meaning see [63].*

This is used to associate the calorimeter information with the data coming from other subdetectors.

3. *FLT Number*, a count number increased for every accepted event. It is generated by the GFLT and starts with 1 at the beginning of a new run.

4. *Readout type*, produced by the GFLT. It indicates the type of the event e.g. normal trigger, test trigger ...

5. *Cell address*, called bits A0 ... A6 coming from the buffer controller. This number is sent to the RAM memories address pins, where the ADC chips write the encoded output (see section 7.2.1).

At **ZEUS** all this data is readout through the *format* card[10], another NIM unit sitting beside the controllers, and where flat multiwire cables bring the data from the table, pipeline and buffer controller modules. This card synchronizes the data and sends it multiplexed to another unit plugged in the VME crate of the digital aquisition system, the "driver" card described below.

The format card performs another function. The CONVERT signal generated in the buffer controller unit, is passed to the format card. It has to be further sent onto the digital system and end up at the "encode" pin of the ADC chips.

Different sections of the calorimeter have different length analog paths to the digital system, thus the convert signals must be delayed accordingly. The digital cards grouped by criteria given in section 7.1.5 digitize sections of the calorimeter. Groups of crates thus receive different CONVERT signals. Programmable delay generators[11] delay the convert signals by an amount set digitally, shifting by a few nanoseconds per bit. Four of these delay generators exist, each one requires 1 byte. These are downloaded from one serial channel on the serial card.

Pulser card

The *Pulser* card is used at **ZEUS** to handle the test triggers. It receives serial data which allows the data acquisition system to modify its response to test triggers. From the GFLT (through the Table card), when a test trigger is scheduled, it obtains the test trigger type (3 bits). This is received $2.112\,ms$ [64] before the test trigger is actually issued and allows to prepare for the test.

The pulser card will be used to perform charge injection runs or laser runs in the empty buckets of HERA, so as to have a good monitoring of the whole readout of the calorimeter.

[10] At the **CERN** test stand only the cell number is readout into the data stream. The number can be accessed at a flat multiwire connector on the front of the pipeline controller. It is passed as ECL levels directly driven from the counter registers. This means the number is cyclically changing when the data taking is running. Only when a trigger occurs and the pipeline readout is initiated, the binary count remains fixed. At this moment, the pipeline READ/$\overline{\text{WRITE}}$ signal changes state, from write to read. An auxiliary home made board is used and both the cell count and the pipeline READ/$\overline{\text{WRITE}}$ signal are translated to TTL logic levels and sent to the VME crate connected to the data acquisition system.

[11] Type AD-9500.

Driver card

The *"driver"* card introduced above provides the way to incorporate all the auxiliary data into the VME environment[12]. One of these is plugged into each crate of the digital system. Flat multiwire cables link them to the format card.

It incorporates a VME bus slave interface. The signals coming from the format card, among them the CONVERT are driven to the bus, through VME's private lines on connector J2, rows A and C and made available to the digital cards.

On two lines, information is passed back to the NIM controllers. The digital system sets a BUSY line to "1" when too many triggers have arrived and the information has not been processed. BUSY is also issued while the startup of the digital system is performed. It is transmitted back down to the GFLT processor and disables further triggers.

Also an ERROR line is activated if the digital system detects a serious problem during data processing. This is also passed down to the format card and requests the generation of an initialize signal from the GFLT. From the GFLT this INIT signal returns to the digital system via the whole control modules which also get reset.

7.1.4 Control signal distribution

The signals generated by the controller system described above have to be brought to the analog front-end cards. These are placed directly on the backbeam of the calorimeter modules.

At ZEUS, the control signals have to be distributed to 80 modules grouped in three different families, FCAL, BCAL and RCAL, with sizes ranging from 2 meters to over 4 meters height, and each one with up to 252 channels of readout. All of them are equipped however with nearly identical analog cards which require the same control signals.

Two types of signals can be distinguished :

- The so-called *fast* signals which carry timing information on their transition edges and which have to be distributed to the whole calorimeter with a time difference not larger than $2-3\,ns$ and be stable in the sub-ns level. The two signals in this family are the Pipeline CLOCK and the PULSE for the charge injectors.

- The *slow* signals are not so time sensitive and can be distributed with differences of up to $20\,ns$. The rest of the signals belong to this group, namely : Pipeline RD/$\overline{\text{WR}}$, Buffer RD/$\overline{\text{WR}}$, Buffer CLOCK, Multiplexer INCREMENT, MODE of operation (i.e. calibration or run mode), Serial Data and Serial Clock.

[12] At the CERN test stand a XYCOM XVME-200 digital I/O module which can operate up to four 8 bit registers as digital TTL inputs or outputs is used. Among other features, it can also read one word (two bytes) when a control signal has a transition from "1" to "0" or the other way around. This function is used in this case, and the cell number is latched into a register on the transit of the pipeline READ/$\overline{\text{WRITE}}$ signal. The value remains there, until the computer control reads it out and includes it into the event data.

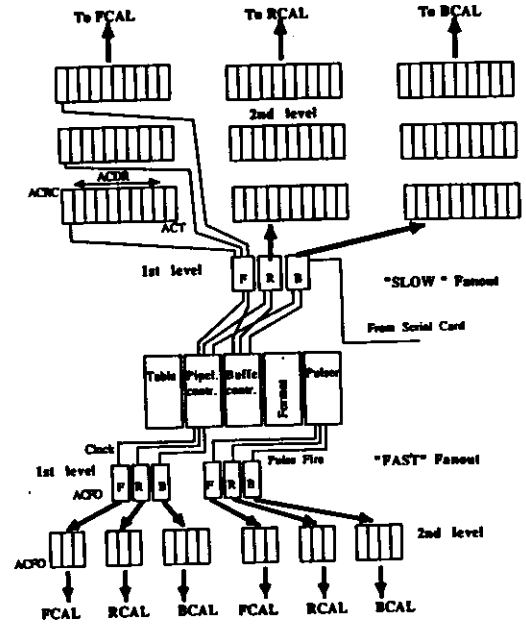


Figure 7.5: *Distribution of control signals to the calorimeter modules.*

Different paths are implemented for the fast and for the slow signals. A scheme of the distribution system is shown in figure 7.5. The distribution paths run as follows :

1. One set of controller units produces the signals for the whole calorimeter. These are placed in a NIM crate on a rack in the rucksack of ZEUS. The serial data and clock come from the serial card(s) from a VME control crate.

2. The number of calorimeter modules to be supplied with signals requires fanouts to multiply the signals. The signals are available four times as single NIM at the output of the controllers.

   For the fast signals a fanout card called the ACFO exists. It features two 1:4 fanouts also configurable as a single 1:8 fanout. The inputs are single NIM signals while the outputs are sent as push-pull NIM-$\overline{\text{NIM}}$ levels. For each one of the fast signals three outputs from the controllers connect to three ACFOs for the FCAL, RCAL and BCAL. From these, a second level of fanout with a total of 20 ACFO[13] cards provides one set of signals per calorimeter module.

   For the slow signals three outputs from the controllers connect to 3 modules, for

[13] 6 are required for the 23 FCAL modules, other 6 for the 23 RCAL modules while 8 are needed for the 32 BCAL modules.

the FCAL, RCAL and BCAL. The channels from the serial cards are plugged also into these modules. In these units the signals are regenerated as NIM-$\overline{\text{NIM}}$ levels and are grouped onto a 25-pin D-connector which is available four times in each unit. For the second level of fanout a bus system is used. It is implemented by having the first level outputs connected to a receiving card (ACRC) which is plugged to a bus where up to 8 drivers cards (ACDR) generate the signals for 8 modules on identical 25-pole D-connectors. The bus is terminated with a terminator card(ACTC). Each ACDR generates one set of signals which is connected to one calorimeter module. Four of these buses are required for each FCAL, RCAL and BCAL.

The whole fanout system occupies 6 NIM crates and is located in a neighbouring rack to the controllers.

3. From the fan outs the signals have to be carried to each module. The fast signals are carried differentially (NIM-$\overline{\text{NIM}}$ levels) on a pair of coaxial RG58 cable which are cut to equal timing.

   Delay cables between the fanouts equalize the different distances to the different regions, forward, barrel and rear so that all front-end cards handle the same event with the same timing.

   The slow signals are also sent differentially as NIM-$\overline{\text{NIM}}$ levels, but on twisted pair shielded cable, with 25-pole D-type connectors on each side.

4. These cables end on the bottom of the F/RCAL modules and on one side of the BCAL modules. Here the fast signals are again fanned out on equal length twisted pair cables; the slow signals are sent on flat multipairs. For the fast signals one signal per distribution board (see below) is generated. For the slow ones only a 1:2 fanout is necessary, for right and left on the modules.

5. At the FCAL and RCAL modules, distribution boards connected in daisy chain bring the slow signals along the backbeam of the modules. The distribution board is built as a bus into which 3 analog cards can be plugged. These boards have equal length connections to the fast signal fanout on the bottom of the module. Also the power connections for the front-end enter these distribution boards. There is one daisy chain for the right and one for the left half.

   At the BCAL modules, the signal distribution is a little different since no distribution bus exists. The signals are carried by groups of cables from the side of the modules to boards fixed onto the backbeam of the modules and here the analog cards are plugged.

6. At the end of the daisy chains, small boards provide for the correct termination of the signals.

The power supplies providing the $\pm 11\ V$ for the analog electronics are placed $80\,m$ away from ZEUS and distributed to each module. Only DC power is fed to the inside of the iron yoke to avoid $50\,Hz$ noise.

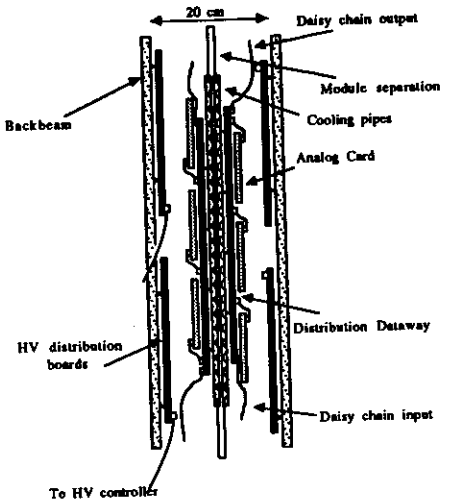


Figure 7.6: *Mounting of distribution system at an FCAL backbeam.*

Figure 7.6 shows a view of an FCAL or RCAL backbeam[14]. All the boards necessary for signal distribution, plus the analog cards are shown. Also the HV distribution system is shown. All the analog electronics is grouped at the top and the bottom half of the modules. This is possible because the packing density on the cards is bigger than the PMT readout. This allows the delicate CMOS electronics to be kept away from high radiation areas and thus reduces the dose.

7.1.5 Analog information path

From the analog cards where charges proportional to the deposited energy are stored, the information has to be brought to the digital system in the Rucksack.

Each buffer-multiplexer chip on the analog card serves 6 PMTs. The outputs of the 3 cards on a distribution boards (6 differential signals) are grouped on the bottom of the modules onto multiple twisted 24-pair cables with 50 pin D-type connectors to cross the 60 meters to the Rucksack. In the Rucksack the cables end on a mixing panel[15] where the individual pairs are arranged according to the regions defined by the second level trigger of the calorimeter (see section 4.8.4). The analog signals are eventually received

[14]The signal distribution system used at the CERN test experiment is similar to the concept to be used at ZEUS. However, no large fanout system is needed as we are only controlling one module. Also the distribution boards have been placed on an electronics beam on top of the modules so as to have better access to the PMTs.

[15]At the CERN stand, only three ADC cards with two ADC chips on them are available. An analog multiplexer switched the three towers, the one where the beam is pointed at and the two at the sides, to the ADC cards, one ADC chip digitising the PMTs of the right side, the other one those at the left side of the tower.The multiplexer is controlled from the data acquisition system.

by differential amplifiers which pass the received voltage difference to the ADC chips. Each analog cable pair ends on one of the ADC chips.

7.2 Data acquisition

The whole readout of the calorimeter has to proceed with digital analysis and storage. The analog signals have been shown to end up at the ADCs. Different stages of the digital system will be discussed here.

7.2.1 Digital conversion

The digital conversion of the analog pulse samples is performed in the so-called "digital" card, in contrast to its counterpart, the analog card.

For the **ZEUS** readout[16] the *digital cards* provide 4 ADCs on one 280 mm × 6U[17] board, one slot wide, complying to the VME standard. Up to 18 boards will be plugged into one crate, and several racks filled with these crates located in the rucksack will be needed to readout the whole ZEUS calorimeter. Figure 7.7 shows the schematic parts of a digital card and their interconnection. They are described below.

- The *differential amplifiers* receiving the complementary analog signals have already been mentioned. They are connected so as to have a gain of 5.

- The main component in the system is the *analog to digital converter chip*[18], a device with 12 bit precision, up to $1\,MHz$ digitizing rate with low power consumption ($1.3\,W$).

  This chip uses a two pass technique to perform the conversion. An on-chip integrated sample and hold amplifier holds the input signal for the time needed to complete the conversion. The input voltage is first measured with 7 bit precision by a flash converter and latched into a register. These bits provide the input to a fast digital to analog converter, the output of which is compared by a differential amplifier to the analog input. This difference is converted again by the flash converter, yielding the least significant bits. These bits are also latched and a digital correction logic combines the two 7 bits results into a 12 bit word.

  The entire process needs about $650\,ns$, after which the sample and hold circuit is set into "track" mode following the input with full accuracy after $180\,ns$. $170\,ns$ are needed to start the conversion and cover all the internal delays. Externally

[16]The digital cards used at **CERN** are of a different type than the ones used at **ZEUS**, actually they are a first prototype in the development towards the final design and operate $1\,MHz$ conversion rate, implementing digital signal processing and on board memory, all under VME control. Their functionality is quite general as requirements were not yet determined in detail at the time of development.

[17]One Unit of rack space is equal to $44.45\,mm$.

[18]type DATEL ADS-112, 0 to 10 Volts range, 24 pin hybrid component, packed in a ceramic dual in line case.

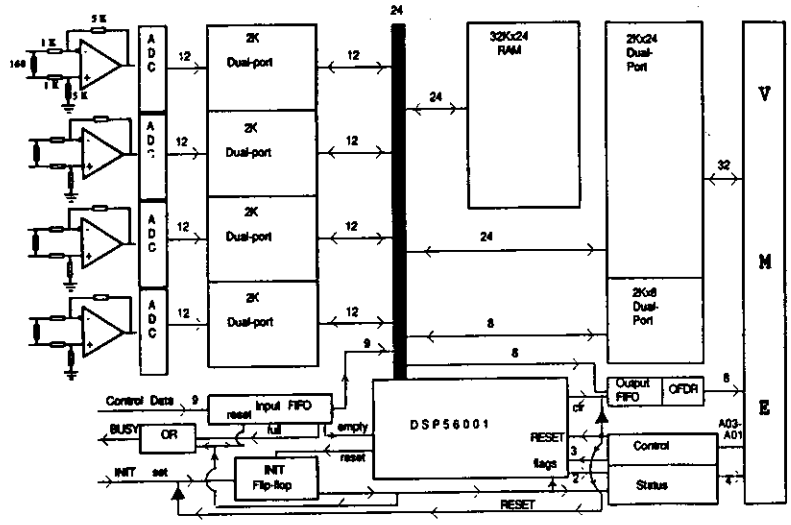


Figure 7.7: *Scheme of a "digital" card.*

seen, the convert pulses can be applied every $1000\,ns$, making out of this device a full $1\,MHz$ ADC converter.

- The digital output of each converter is written into a dual ported, 12 bit wide, 2k deep *RAM*.

  The address where the digitized data is written is generated in the buffer controller card (see section 7.1.2) and arrives at the address pins of this RAM bank. In fact only the lower 7 bits[19] (A0-A6) giving the address within one event are produced in this way. The next event is written into the next "page" by changing the upper 4 address bits. A maximum of 16 events fit in this memory.

  Using RAM chips instead of FIFO registers which would not require addressing information leaves some flexibility in the system e.g. for aborting an event while it is being digitized (with the calorimeter fast clear system, see section 4.8.3).

- A *fast FIFO* receives on private lines of the VME backplane the information needed to process the event, e.g. the trigger number or the pipeline cell number where the first sample was stored, which get in this way incorporated into the digital data stream. A BUSY signal is generated if this FIFO gets filled. This can be due to too many GFLT ACCEPT signals or too slow processing of the information on the calorimeter SLT system.

[19]Note that an ADC has to convert a maximum of 108 (6 PMTs × 2 gain ranges × 8 samples + 12 DC values) samples per event which can be covered by 7 bits.

- An additional 32k deep 24 bit wide *RAM* also exists on each card. The primary aim of this memory is to keep the calibration constants for the pipeline and buffer-multiplexer chips (see section 6.3.3 and 6.3.4). Programs to perform these corrections as well as those needed to apply the charge and time reconstruction algorithms are also stored there. Details of how this happens will be discussed in section 7.4.1.

- The heart and intelligence of the digital card reside in a *Digital Signal Processor* (DSP) of the type Motorola DSP56001, a one chip special purpose microprocessor specially suited to perform digital operations on data in a parallel way. It is a 24 bit wide processor with a $100\,ns$ instruction cycle. It includes 512 words of on-chip memory to keep programs and intermediate variables.

- A *local 24 bit wide bus* connects the input RAM, the input FIFO, the output FIFO and the storage RAM to the DSP. In the typical procedure the DSP :

  a) fetches the digitized data from the input RAM,

  b) reads the FIFO to determine the pipeline cell number of the first sample,

  c) reads the data RAM to get the corresponding calibration constants and

  d) performs the operations given by the program residing (at least partly) on its on-chip RAM.

  The following results are produced :

  - Charge and time of deposited energy for the individual channels. This needs a previous decision whether to use the high and/or the low gain range based on the recognition of saturation.
  - Corrected or raw samples for off-line analysis, if required or if the DSP decides the reconstruction is dubious.
  - Right/Left, EMC/HAC energy sums for SLT processing.
  - Data quality control information like checks for pile-up.
  - Control information like trigger number, cell number ...

- These results are written on a further *dual-ported RAM* memory connected to the internal bus. From here they can be accessed via the VME bus by the controller in the crate. In this case it is a 32 bit wide 4K deep RAM which is accessed as a combination of a 24 bit and an 8 bit registers when written from the DSP, and as 32 bit registers when seen from the VME bus.

- The results corresponding to one event are grouped into a so-called page, the index number of which is written at the end of the calculations on an *output FIFO*, also accessed through the VME bus by the crate controller.

- *Additional control and initialization registers* complete the components on the digital card.

The digital cards represent distributed intelligence on the readout system. With one digital card serving 24 PMT, more than 500 DSPs give to the ZEUS calorimeter $\sim$ 5000 MIPS[20] processing power at the lower levels of the readout chain. Calibration runs, detector performance checks and data reduction calculations are available for sophisticated triggering.

Thanks to their programmability the system remains flexible, allowing for quick response to changing running conditions as well as full control for debugging phases.

7.2.2 VME control and readout

The digital cards and other modules as mentioned are connected onto a VME bus. A way has to be provided to control these units and send their information to higher levels in the chain.

VME is a standard [59] for a bus providing connection between different modules within a crate, with well defined protocols. Typically a VME crate is controlled by a processor of the Motorola 68000 family which acts as the crate "master", steering the other modules in the crate, usually "slaves" by writing into some of their control registers and getting information out of them by reading from their memory banks or registers[21]. The VME standard does not provide however directives to connect several crates.

For the readout of the ZEUS calorimeter a novel solution has been adopted. The crate control is performed by a *transputer*[22] [65] which allows easy intercommunication to other transputers placed in other crates. The communication is achieved through serial channels, called *links*[23] of which each transputer has four.

The transputers and their connections form a tree network so that the readout data can be passed on for storage. The decision to use transputers for the readout was conditioned by the fact that the network for the calorimeter SLT is implemented with transputers [21,66,38]. The SLT starts by reading out the energy information from the digital cards so a simple solution was to let the transputers perform the rest of the readout and pass on the data.

The transputers are placed in the "2TP" modules [67], a special development of NIKHEF for the ZEUS calorimeter. The 2TP modules contain a VME interface, two (thus 2TP) T800 transputers (X and Y), $4\,MB$ of local RAM each and $0.5\,MB$ of triple ported RAM which can be accessed by both transputers and from the VME bus.

[20] Mega Instructions per Second

[21] All the interfaces, electrical, mechanical, software ..., between masters and slaves, are well defined parts of the VME standard.

[22] A transputer is a 32 bit microprocessor chip of the RISC (Reduced Instruction Set Computer) type. These processors execute only simple instructions, but this in a very fast way as opposed to usual microprocessors which can carry out sophisticated instructions with very flexible addressing capabilities, but need a level of intermediate decoding called microcode from where the hardware can execute the operations. Their performance is comparable to the most recent processors of the 68000 family (e.g. 68030).

[23] The links are DMA channels which receive/send data in serial form. They achieve speeds of $1\,MByte/s$.

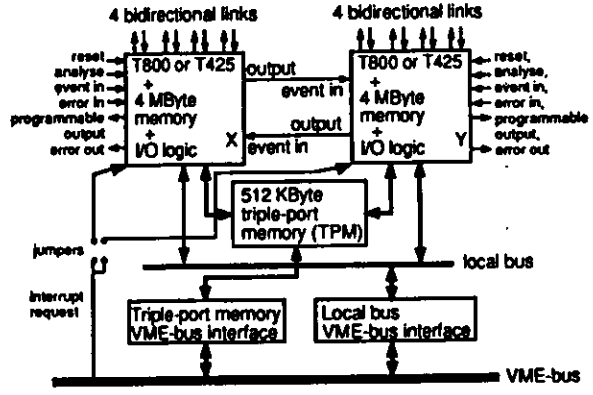


Figure 7.8: *Scheme of a "2TP", two transputer VME module.*

Figure 7.8 shows a scheme of such a unit. The 2TP board is plugged in as crate master in the digital cards' crates. The digital cards call for readout when they are finished with processing an event.

When a digital card is finished with the processing it drives a line in the J2 VME connector to "1". As soon as all the cards are finished the last digital card[24] in the crate provokes an interrupt on the VME bus and the transputer of the SLT network reads the calculated energy sums [66]. Then the trigger process operates and if the event is accepted, the complete event is readout by the other transputer and passed to the readout network.

VME control and readout for the CERN test beam

The readout used at the CERN module calibration experiment is less sophisticated.

However it was decided that this calibration experiment should also be the field test of some of the components which were foreseen for ZEUS. A first version of the 2TP board in a small preproduction series in a 2 slot wide version had been produced and these have been successfully used in the test beam. This 2TP board performs the readout of the ADCs and crate control [68]. It also reads the rest of the modules in the VME crate[25].

The 2TP board is connected through one link of transputer X to the main data taking computer, a DEC Micro Vax 3500. The other transputer, Y, in a parallel process handles the trigger, performs the actual VME bus reading of the ADCs and other modules and monitors the hardware. It passes the events with a certain buffering to the X transputer

[24]This function on the "last" card is actually achieved by hardware jumpers so that all the cards are constructively identical.

[25]These are : A XVME-200 (replacement for the driver card), Krauss-Maffay VME E/A (to control the LED light injection system), the CES-8210 VME to CAMAC interface (to read out the CAMAC crates into the main data stream) and the Trigger box (a home made module to interface to the fast trigger system and which also provides some facilities for the input and output of signals).

which before sending the data on the link packs several events together building the so-called superevents and formats them in ZEBRA[26] banks.

The fact that an event has occurred and converted data is available at the ADC board's RAM is communicated to the 2TP board also via an interrupt line of the VME bus. This interrupt is however generated not by the ADC cards themselves like at ZEUS, but by another module residing in the VME crate, the *trigger box* unit. This unit receives the signal produced by the fast electronics. After some delay, the readout task performs the readout of the ADC's RAM via the VME bus.

All these tasks are running on the transputers in a parallel way, a mode for which these processors are specially suited. Each process is activated by external events (like an incoming trigger, or a 'data send' command from the Vax) or by an internal scheduler which distributes the processing power of the central unit.

7.3 Calibration methods

In the preceeding sections we have discussed all the parts needed to readout the calorimeter, both at the CERN test stand and at ZEUS. Concepts and implementations in hard- and software have been shown.

With the tools available, the calibration of the calorimeter modules has to be performed at CERN with well identified particles, so that later on at ZEUS, particles of unknown characteristics can be correctly recognised and measured.

Prior to the calibration of the calorimeter modules themselves, a calibration of the readout electronics has to be performed. This is mandatory for two reasons,

1. uncalibrated or insufficiently adjusted electronics will ruin the performance of the best constructed module;
2. all the modules have been calibrated with the same set of electronics and they will be equipped at ZEUS with other cards.

In this section a detailed description will be given of the method used to calibrate the electronics.

7.3.1 What to calibrate ?

There are quite a few parameters given by the electronics which enter in the response of the calorimeter which have to be considered.

1. The gain of a PMT is a function of the voltage on the cathode and its dynodes. The relation between the voltage V and the gain G is described by :

$$\log G = \log B + C \cdot \log V$$

[26]ZEBRA is bank format and I/O package used in experimental high energy physics developed at CERN by DD.

Two constants are needed, *the factor B and the exponent C* of the logarithmic relation. These quantities are measured on a separate measuring stand prior to the mounting on the modules[27]. Other quantities like dark current are also systematically measured as acceptance criteria for the PMTs.

2. The PMT signal is shaped. The components making up the shapers are 1% components. A *gain* and possibly a *shape* calibrations for each scale range are needed. The shaper is very linear and its gain is given by one number, however if needed, a second degree correction will cover the nonlinearity of the PMT and shaper set. The shape is in a simplified way described by two numbers, the slopes of the rising and falling edges.

3. The samples of the shaped pulse are kept in the analog *pipeline*. Here they are subject to *pedestal and gain* distortions as function of the cells where the samples are stored. These two quantities have to be calibrated out for each cell of both gain channels. It has been shown that the nonlinearity of the analog pipeline is such that two quantities, gain and offset are sufficient to describe the behaviour of each cell over the whole range used.

4. After a FLT trigger decision, the selected samples are transferred to the analog storage cells on the buffer-multiplexer chip. The voltages are again affected by different *gains and offsets of the buffer cells*.

5. From the buffer, the samples are multiplexed out to the ADCs. They are sent differentially over 60 meters of cable, driven by the cable driver subcircuit. The *gain of the drivers, cables and ADCs* can be combined to one number, which converts digitized ADC counts to volts on the buffer cells. The voltage is measured relative to a baseline value, obtained by digitizing the ground through one of the DC multiplexer channels.

6. The long cables cause, due to unavoidable capacitive load, long settling times thus some voltage from large samples can affect the following ones. This can be considered as a *sample-to-sample crosstalk* which should be corrected. It affects also DC measurements like DU noise currents. The effect is certainly very small thanks to the implemented readout order.

7. The current generated by the uranium radioactivity is measured as a voltage over a high precision (0.1%) resistor with an operational amplifier connected as a current to voltage converter. However different channels can have different *offsets* due to different operational amplifiers or ground connections.

All these quantities affect the signal readout from the calorimeter and have to be measured in order to cancel them out of the real signals.

[27]The parameters can also be determined once the phototubes are mounted on the modules, by measuring the DU current vs. different settings of the HV.

7.3.2 Calibration scheme

The tools discussed in section 7.1.1 can be used for the determination of the quantities above mentioned.

ADC scale calibration

The precision voltage generated on the analog card is connected to one of the DC inputs at both buffer-multiplexer chips of each analog card. Also the electrical ground on the card is connected at another one of the DC inputs. When the DC multiplexer positions are readout, the difference in ADC counts[28] is defined to be equal to the precision voltage (2.0 V at the CERN cards, 1.67 V at ZEUS). The constant k giving the conversion scale is :

$$k = \frac{A_{prec} - A_{ground}}{V_{prec}}$$

Pedestal calibration

The determination of the pedestals and gains of the different cells of the pipeline and analog buffer is more complicated. It is not possible to measure the signals directly at the output of the pipelines as the samples have to pass the buffers. The tool available for measuring pedestals and gains is the DC voltage from the DAC which can be connected to the inputs of the pipelines.

In fact what we measure is a combination of the pedestals and gains of the cells in the pipeline and in the buffer. There is such a combination for every pair of pipeline and buffer cells. Connecting a voltage V_{input} to the pipeline input and storing it in cell i of the pipeline and cell j of the buffer yields at the output a voltage V^{ij}_{output} :

$$V^{ij}_{output} = V_{input} \cdot c^p_i \cdot c^b_j + V^p_i \cdot c^b_j + V^b_j \tag{7.2}$$

with c^p_i the gain of pipeline cell i, c^b_j the gain of buffer cell j, V^p_i the pedestal of pipeline cell i and V^b_j the pedestal of buffer cell j.

For any combination of i (1 ... 58) and j (1 ... 8) two correction constants (a slope and an offset) would be produced resulting in a total of $58 \times 8 \times 2$ numbers, in fact twice that number for every PMT channel are needed because each one has a high and a low gain pipeline.

This number however can be reduced as the gains of the buffer cells are all very similar[29] (at the 0.25% level). Thus equation 7.2 simplifies to

$$V^{ij}_{output} = V_{input} \cdot c^p_i \cdot c^b_j + (c^b \cdot V^p_i + V^b_j)$$

Now for $V_{input} = 0\,V$, we measure at the output the sum of the pedestals $c^b \cdot V^p_i$ and V^b_j.

[28]From now on, quantities designed with V will be meant to represent voltages, while quantities with A stand for the voltages converted into ADC counts.

[29]We will suppose the buffer gains to be one, however this does not lessen generality.

This simplification[30] allows us to separate the 58×8 numbers into 58 and 8 which we store. We readout sets of eight cells, each time starting at a further pipeline cell $(1 \ldots 8,\ 2 \ldots 9,\ \ldots,\ 58 \ldots 7)$. We measure a set of $58 \cdot 8$ offset values which we can split into $58 + 8 + 1$ as follows. If we call h_{ij} the measured value for zero volts input through pipeline cell i and buffer cell j, we can refer all the h_{ij} to e.g. h_{11} and store only the following quantities :

$$\begin{aligned} \delta^0 &= h_{11} \\ \delta^p_i &= h_{i1} - h_{11} \quad (i = 1 \ldots 58) \\ \delta^b_j &= h_{1j} - h_{11} \quad (j = 1 \ldots 8) \end{aligned}$$

which amount[31] to 67 instead of 464.

Now for any pipeline and buffer cell combination we can recover

$$h_{ij} = \delta^0 + \delta^p_i + \delta^b_j$$

and thus correct V_{output} to get

$$V_{input} = V_{output} - h_{ij} = 0\,V$$

Gain calibration

The same scheme can be used for the gains. This time an input voltage of $-2\,V$ is applied at the input to the pipelines.

We divide the output, corrected for the pedestals, by the input we apply, this yields the linear gain values. The $gain_{ij}$ we measure as before in groups of 8, each time starting at one further pipeline cell. Of course all the measurements are performed relative to ground :

$$gain_{ij} = \frac{h_{ij}^{-2\,V\ input} - h_{ij}^{0\,V\ input}}{A_{reference\,(-2\,V)} - A_{ground}}.$$

Note that the voltage we are applying to the pipelines' inputs is simultaneously measured through one of the DC multiplexer channels $A_{reference}$ as is the voltage of the card's ground.

As above we keep the quantities relative to cell combination 1,1 :

$$\begin{aligned} g^0 &= g_{11} \\ g^p_i &= g^0/g_{i1} \\ g^b_j &= g^0/g_{1j} \end{aligned}$$

and from here we reconstruct each

$$gain_{ij} = \frac{g^p_i \cdot g^b_j}{g^0}.$$

[30] The error we make is $O(0.1\,mV)$.

[31] Per definition δ^p_1 and $\delta^b_1 = 0$ so in fact only 65 not 67 is the number of constants.

To correct a measured sample, we must know its ordering position in the readout, this determines the buffer cell j where it came from, and we must also know the pipeline cell i where it was first stored (see section 7.1.3).

The measured sample is corrected by :

$$h^{ij}_{corrected} = \frac{[h^{ij}_{measured} - (\delta^0 + \delta^p_i + \delta^b_j)] \cdot g^0}{g^p_i \cdot g^b_j}$$

for which only two tables of 1+58+8 numbers are necessary.

Shaper gain calibration

To calibrate the shapers we inject a known amount of charge at their input and measure it at the output by reconstructing it from the samples.

The amount of charge injected is the product of the capacitor in the charge injector times the voltage set from the DAC. The capacitance is $22\,pF$ and the maximum voltage is $5\,V$, so some $110\,pC$ can be injected. This is approximately equivalent to the energy deposit of $20\,GeV$ electrons. This saturates the high gain channel of the electronics, but is only $\sim 1/20$ of the maximum signal in the low gain channel. This does not provide a precise calibration of the low gain channel. The laser injection system is used for this as will be shown in section 7.3.5.

In fact we perform this charge injection at two or more DAC values. The amplitude calibration for the shapers is obtained from the ratio of differences of measure to injected charge. This takes care for offset problems by the injection[32]. The two values of charge injected are, of course, at both ends of the scale.

For shaper channel i, the calibration for the amplitude is :

$$a_i = \frac{Q^1_{injected\,i} - Q^2_{injected\,i}}{Q^1_{reconstructed\,i} - Q^2_{reconstructed\,i}}$$

which simultaneously serves as a way to set an absolute charge scale to the measured (or reconstructed) values. The way to calculate $Q_{reconstructed}$ from the h is explained in section 7.4.1.

The $Q_{injected\,i}$ is determined by measuring the DAC reference voltage $A_{reference\ DAC}$. We calculate

$$Q_{injected}[\mathrm{pC}] = ((A_{reference\ DAC} - A_{ground})[\text{ADC counts}] \cdot k\left[\frac{\mathrm{V}}{\text{ADC counts}}\right]) \cdot 22[\mathrm{pF}]$$

which is common to channels 1 to 6 (one value) and 7 to 12 (a second value) because the $A_{referenceDAC}$ is only measured twice per analog card.

One could also apply a more sophisticated method where several values of charge are fitted with for example a polynomial, this would take care for non linearities at the shaper (or the charge injector) but it has been shown not to be necessary.

[32] Setting 0 Volts on the DAC still injects some charge into the shaper, at least the feedthrough of the trigger pulse produces a non-zero signal.

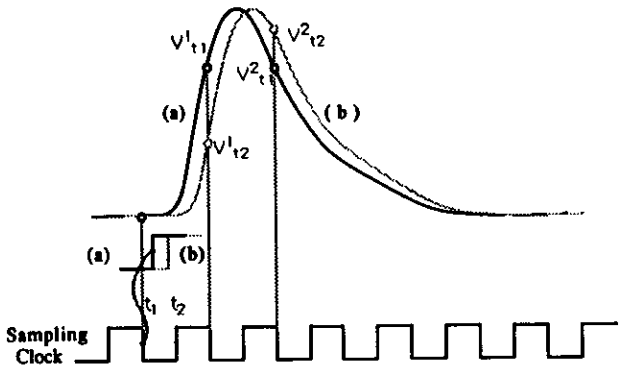


Figure 7.9: *Method to measure the slopes of a shaped pulse.*

Shaper slope calibration

If we want to determine the slopes of the pulse to describe the shape, at least two points have to be measured on each side.

As explained in section 7.1.2, we use a signal synchronized with the `sampling CLOCK` to trigger the injectors, this guarantees fixed points on the input pulses. By delaying this `PULSE` signal relative to the clock which generated it, we can find a timing such that the samples have approximately equal height on the two sides of the peak (see figure 7.9-(a)).

By incrementing or decrementing this delay by a known small quantity (e.g. $5\,ns$), we will get samples at position (b) on the pulse and we can easily calculate the corresponding slopes which we usually normalize to the charge of the injected pulse :

$$s_{up} = \frac{V^1_{t_2} - V^1_{t_1}}{(t_2 - t_1)Q_{inj}} \tag{7.3}$$

$$s_{down} = \frac{V^2_{t_2} - V^2_{t_1}}{(t_2 - t_1)Q_{inj}}. \tag{7.4}$$

The runs are performed only for a fixed set of cells, applying the pedestals and gains corrections makes the measurements independent of the position in the pipeline.

Integrator offset calibration

To determine the offset of the current integrating circuit I^{offset}_{UNO}, the HV of the PMTs is turned down (to $400\,V$) so that their gain is reduced by several orders of magnitude and standard UNO measurement is taken reading out the DC positions of the multiplexers.

This amount of current is subtracted from the normal UNO current measurements :

$$I^{real}_{UNO} = \frac{V^{measured}_{UNO}}{R^{DU}} - I^{offset}_{UNO}$$

Cable pileup calibration

The amount of cable pileup can be determined by looking at the change of the ground levels when varying the preceeding voltage in time on the cable. This is implemented in an already hardwired fashion on the card as the ground voltage is connected not to one, but to two DC inputs of each buffer-multiplexer chip. The first one is almost constant since it comes directly in time after the last sample of the last buffer channel, which can be set to zero. The second ground comes directly after the DC input which is connected to the DAC reference voltage on the card, which can be varied from 0 to -2 V and the variations induced on the accompanying ground measurement show the pileup. A linear relation is assumed and the pileup constant f results :

$$f = \frac{A^2_{ground} - A^1_{ground}}{A_{reference} - A^1_{ground}}$$

and a sample "i" is corrected for cable pileup from the previous one by :

$$S^{corrected}_i = S^{measured}_i - f \cdot S_{i-1}.$$

7.3.3 Implementation of the calibration

To measure all the quantities described in the previous section, several runs of data taking have to be performed. They require different settings for the electronics which are commented below. All the serial data settings can be found in table 7.1.

- Both the k and the f constants are easily obtained when a measurement of the DC multiplexer inputs is performed.

  Note that the control electronics does not allow the readout of DC multiplexer channels without previously reading the buffer channels. The contrary is possible, but for example at **CERN** always a complete reading is performed. On a run type called *UNO*, the buffers' data is ignored, and only the DC multiplexer positions are written in the data stream.

  In order to be able to read these DC positions, bit four of the third byte at the serial channel connected to the Table card has to be set to "1" and downloaded on the controller.

- To obtain the h_{ij} measurements to determine the pedestals, the voltage input to the pipeline should be zero. We do this in a *Pedestal* run. Here, the serial channels connected to the daisy chain have to have the first byte set to `11111110` (DAC equal to minimum and DC connected to pipelines). Then we repeat measurements varying the readout starting cell of the pipeline to have different combinations of 8 cells. This we achieve by iterating on bits 1 to 6 of byte 4 of the serial channel leading to the pipeline controller.

- The same procedure is done in a *Gain* run to obtain the $gain_{ij}$ where we now change the serial data to a high value of the DAC (e.g. `00000000`) and measure again iterating through the cells.

- The measurement of the shapers gain is performed in a *Charge injection* run. Here we trigger the charge injectors on the shaper hybrids to inject an amount of charge which can be set with the DAC. Through the serial links we load :

  1. to the daisy chain : xx111111, xx111111 to fire the 12 injectors and xxxxxxx1 DAC value to the injectors
  2. to the Table card : xxxx1xxx to allow a synchronized pulse to come out.
  3. the usual additional data like number of samples, enable cell synchronization, which one ...

  This produces charge injection before the shapers. We repeat this for two DAC settings at different scale ends.

- The *Slopes* is a two fold run, the first injects an amount of charge at the middle of the scale and measures points on the pulse with nominal delay as in figure 7.9-(a). The second run introduces a delay and measures points as shown in figure 7.9-(b).

  The serial data needed for this is the same as for a charge injection run, only the DAC value is set to typically the middle of the scale 0111111.

  The delay is introduced under computer control. At **ZEUS**, the *pulser* module (see section 7.1.2) performs this function[33].

- A *UNO400* run is taken to measure the offset for the integrated current by setting the voltage at the PMTs to $400\,V$, this means no light is seen from the uranium radioactivity. It is equivalent to a normal *UNO* run.

Other calibrations and checks

Some additional checks are performed though no calibration constants are generated.

A *DC non-linearity* run is meant to check the linearity of the readout system from the pipelines input onwards. We take a fixed set of cells and cycle through several DAC settings, measuring at each one the output samples when a DC voltage from the DAC is given as input to the pipelines. After correcting for pedestals and gains, the measured points give a measurement of the non-linearity of the system. The implementation of the runs is identical to a pedestal or gain run, only the DAC byte is changed from minimum to maximum in several steps, taking a data run at each one.

Also a *Pulse non-linearity* run is performed. It consists of a set of charge injection runs at different charge settings. After all the corrections, this data will show the non-linearity in the system following the PMT output.

A second sort of *Pile up* run is also taken in addition to measuring the variation of the ground voltage as a function of a varying reference voltage. The idea is to use the pipeline cells to measure the cable pileup. An explanation follows.

[33] At **CERN** the PULSE signal runs through a module where its path can be switched through an external cable of known length. The switching is implemented with one of the enable bits from the trigger box.

Run type	# of runs	# consts. per PMT	calibrates
DC-UNO	2	2/6	k ADC counts to volts, f cable pileup
Pedestal	58	117	δ^0, δ^p_i, δ^b_j for high and low gain
Gain	58	117	g^0, g^p_i, g^b_j for high and low gain
Slope	2	2	s_{up}, s_{down} slopes of the high gain shaper
Charge injection	2	1	a_i gain of high gain shapers
DC non-linearity	10		Non-linearity from pipeline to ADC
Pulse non-linearity	10		Non-linearity from shaper to ADC
Pileup	2		Cable pileup with pipeline samples
UNO pedestal	1	1	I^{offset}_{UNO}, PMT offset current with HV down
Random triggers	1		Check if all corrections are OK. Should yield Energy = 0

Table 7.2: *Electronics calibration runs.*

A large charge injection pulse is generated as in a pulse non-linearity run. This gives two big samples on the edges of the pulse plus some smaller ones following them. In the usual charge injection run the number of cells skipped would be such that these two values fall e.g. on the third and fourth samples.

Instead if we load on the Table card a number of cells to skip smaller by 6 than the usual one, we will obtain 7 samples on the baseline and the last one will be the big sample on the rising edge of the pulse. The next voltage which is multiplexed on the cable is the first sample of the contiguous buffer channel and due to the connectivity of the system it will be the low gain path of that same channel, and the 7 first samples will be also baseline. Looking at the variation of this first sample of the low gain channel when the pulse is fired or not also gives us information on the cable pileup.

A last check performed is the *Random trigger* run. In this case triggers are produced when no signal comes in the system. If all the corrections are properly performed, the result seen should be zero on every channel.

As a summary table 7.2 shows the runs taken and the information they yield.

7.3.4 Electronics and calibration monitoring

The electronic readout of the calorimeter modules at **ZEUS** or even of one module at the **CERN** test stand, is a complicated ensemble. A lot of equipment, hardware and software has to work reliably over long periods of time.

Some monitoring has to be performed to insure proper operation. Also some systematics in identification of misfunctioning has been developed.

A successful complete electronics calibration guarantees the functioning of the electronics. Some checks on the calibration results are performed :

- Pedestal values must fit into high-low limits ($\pm 50\,mV$).

- Gain values cannot diverge from one by more than one percent ($0.99 < g_i < 1.01$, $0.9 < g_0 < 1.1$).
- Pedestal and gain measurements must have the rms of their distributions below a certain level (rms at each cell $\leq 1\,mV$).
- The non-linearity, both DC and pulse, of the system has to be below a limit (1%).
- The pulse slopes must fall in a predefined range.
- The offset currents on the integrators have to be below a limit ($\leq 5\,nA$) and below a noise level ($< 2\,nA$ rms).

The whole procedure is however too complicated and time consuming to be performed very frequently. The constants produced are stable enough (see e.g. section 6.3.3 or section 6.3.4) so that recalibration is only necessary for longer time periods[34].

A monitoring concept is however provided by the following runs :

- The *random trigger* runs control if the calibration constants still correct for the distortion of the signals by the electronics.
- The *charge injection* runs monitor the whole chain up to the PMT. This is a integral test and if the data is as expected, a proper functioning of the chain shapers, pipelines, buffers, up to the ADCs can be validated.
- The *UNO* runs monitor the functioning of the PMTs and their gain. A correct signal from the uranium radioactivity practically assures a proper functioning of the PMTs.
- The *Laser* runs (see next section).

These monitoring runs have been taken at **CERN** every 8 hours and will be used at **ZEUS**. They allow on-line monitoring of the performance of the system and control if any part fails. Data is also available for off-line analysis for stability studies.

7.3.5 Additional calibration methods

The proper functioning of the readout electronics is a necessary condition to have a working calorimeter. However the contrary is not the case. To make sure that the calorimetric data is understood, two additional calibration systems have been built into the calorimeter modules :

- A γ-*Source* calibration system checks the performance of the calorimeter modules in a quasi-DC way.

[34] At **CERN** for example these measurements and checks are performed at the beginning of the run period when the module to be calibrated is installed.

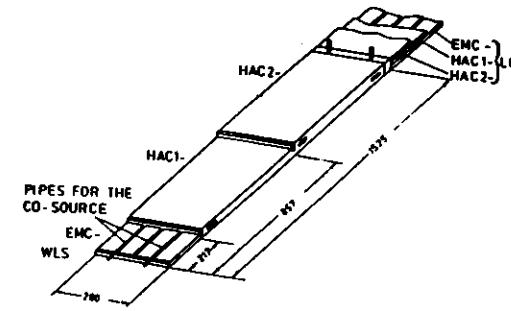


Figure 7.10: *The tubes for γ-source calibration can be seen between the EMC WLS [69].*

The γ's irradiate the scintillator tiles which are neighbouring to the source and produce a signal on top of the DU-radioactivity. Reading this out with the electronics as a usual DU measurement and correlating it with the source position, gives information about construction problems in the calorimeter modules e.g. misplaced or darkened scintillator tiles or WLS bars. These checks are performed before the modules are installed at ZEUS.

The γ-source calibration system will also provide information on aging or radiation damage of the whole optical system in the modules during the operation at HERA.

^{60}Co sources of $1.5\,mm$ diameter and a strength of $1.6\,mCi$ can be inserted and moved along the sides of the modules. Brass tubes are set in between WLS bars as shown in figure 7.10 so that the point-like sources can be moved with a computer controlled stepper motor from the top of the modules (the side in BCAL) and after a bend, along each WLS, and thus across the scintillator layers.

- A *light flasher* calibration system is also in-built into the calorimeter modules. The following properties of the readout chain can be readout and monitored :
  - PMT gain stability both on a short and long term basis;
  - Linearity of the PMT's over the whole energy range;
  - Check (linearity, timing) of the readout electronics over the whole dynamic range. Specially important here is the check of the low gain electronics channel.

  The scheme of the light flasher system is shown in figure 7.11. The light is generated by a N_2 laser and after being converted to the wavelength of the scintillator it is injected through a distribution network of optical fibers into the WLS necks near the PMTs.

  The distribution splits the laser light onto fibers which enter each module and from here it is distributed further to a fiber system running along the backbeam

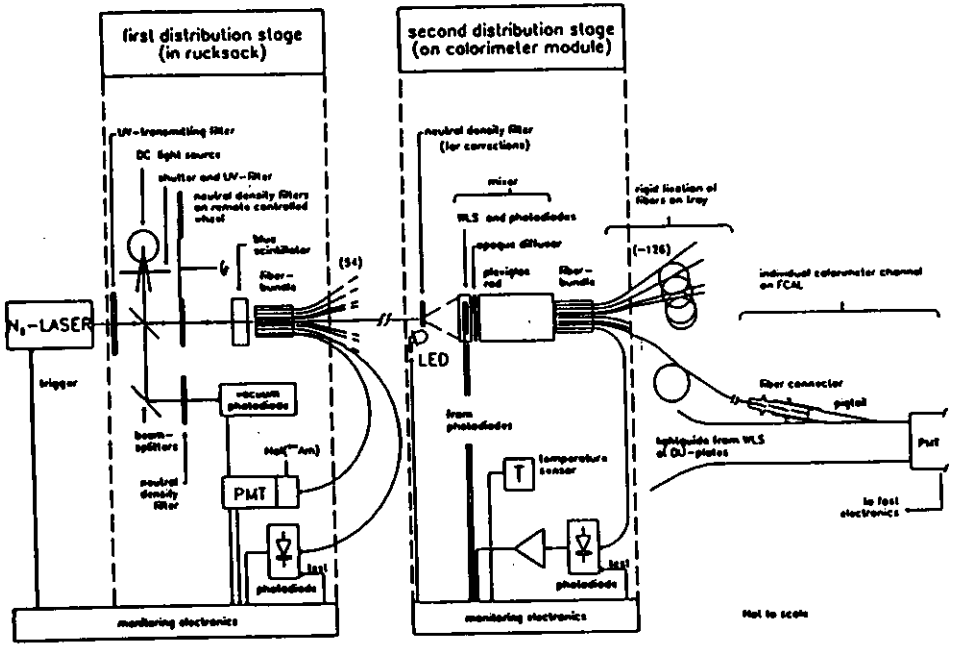


Figure 7.11: *Scheme of the light flasher calibration system [18].*

of the modules. The amount of light injected can be set with filters of different transmission values so that the whole dynamic range of the calorimeter can be scanned.

In addition at the entrance of the module[35] distribution system, light can also be produced with an LED-system[36] in a DC or pulsed way which represents a fallback solution to the laser light and serves to measure the dependance of the PMT gain as function of the its anode current.

7.4 Data reconstruction

The whole electronics and data taking process has only one aim, we want to know how much energy was deposited when and where in the calorimeter, and if possible by what kind of particles.

The voltage samples on a signal derived from the PMTs' output, with additional information like an integrated noise current are the only information linked to the deposited energy we receive. Many calibration constants have to be applied on this raw data. Data reconstruction is therefore a major part of the whole measurement.

Note that the following reconstruction result in a charge produced by the PMTs. However the absolute energy calibration, i.e. the link between ADC scale and deposited GeV can only be provided by a beam calibration as shown in the next chapter. In that sense the reconstructed pC are an intermediate unit.

It is also vital that the data reconstruction is performed in a proper way because the system is conceived such that data reduction can be achieved at the lower levels of the readout chain. This means that at some point in time when confidence exist that the reconstruction is performing properly no more the raw samples but only the reconstructed quantities will be recorded.

7.4.1 Charge reconstruction

As discussed in section 4.6.1, the current signal from the anode of the photomultipliers is shaped and sampled at fixed intervals. The charge carried by the original PMT pulse has to be recovered or reconstructed from the voltage samples.

The reconstruction algorithms will be explained on the hand of test measurements with charge injected ($\sim 55\,pC$) by the on-board charge injector into the shaping-sampling electronics.

The result of the shaping for a δ-fuction input pulse can be described by

$$V_{out} = \frac{Q}{\tau}\left(\frac{t}{\tau}\right)^N e^{-\frac{t}{\tau}} \tag{7.5}$$

with N=3, the number of stages minus one and τ, the time constant of the RC networks. This function has its peak at $t = N\tau$. The value of τ (set to $33\,ns$) is chosen such that

[35] for FCAL and RCAL modules only
[36] Light Emitting Diode

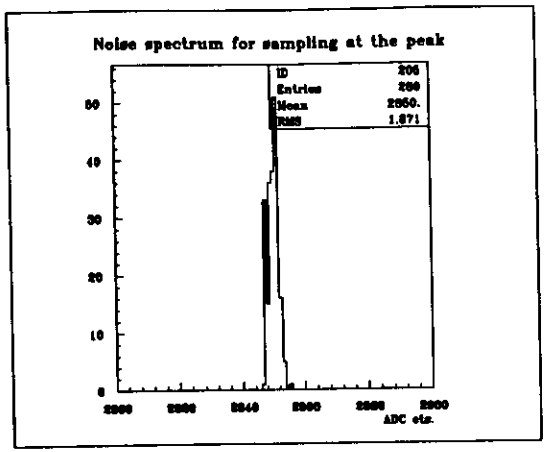


Figure 7.12: *Distribution of samples at the peak of the shaped signal. The scale shown is in ADC counts (1 ADC count* $\sim 0.5\,\mathrm{mV}$*) and the value corresponds to* $\sim 55\,\mathrm{pC}$*. The rms of the measurement is equivalent to* $0.034\,\mathrm{pC}$ *and represents a noise of 0.06% in the reconstructed charge.*

for the sampling frequency used ($96\,ns$), two samples fall on both sides of the pulse peak and the preceeding one on the baseline before the rising starts.

Note that measuring V_{out} at any t, gives a value proportional to Q, i.e. proportional to the energy deposit. We can set for example the sampling clock to take a sample at the peak of the signal. A histogram for measured heights at the peak is shown in figure 7.12.

We can also choose to sample on one side of the peak. This can be seen in figure 7.13. The noise increases more than a factor of three because any jitter in the sampling induces a variation of the sampled voltage.

As we have several samples on the pulse, each of them proportional to the charge we want to reconstruct, a linear combination of two or more of them will conserve the proportionality. We make therefore a linear combination of two samples on both edges in such a way that the amount of jitter compensates. The linear combination is inversely related to the slopes on both sides s_{up} and s_{down} :

$$Q \propto \frac{1}{s_{up}} h_1 + \frac{1}{s_{down}} h_2 \tag{7.6}$$

calling h_1 and h_2 the samples on the rising and falling edges subtracted from the baseline measurement.

If it is assured that the time between two successive samples is kept constant[37], the jitter induced error in the amplitude's measurement will go in one direction on one side

[37]With the analog pipeline constructed as has been shown in section 6.3.7, this fact is guaranteed up to effects smaller than $0.25\,ns$ equivalent to less than 0.2% error in the reconstructed charge.

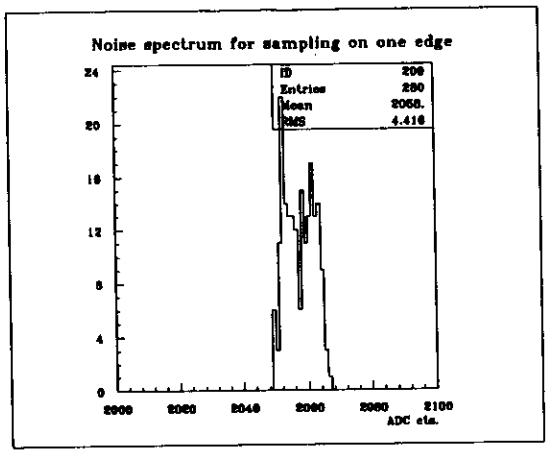


Figure 7.13: *Distribution of samples at the one edge of the shaped signal. Again the value corresponds to* $\sim 55\,\mathrm{pC}$ *but now the rms grows to 0.21% in the reconstructed charge.*

while it goes in the other for the second side.

Figure 7.14 shows a distribution obtained with measurements of samples on both sides and operated with equation 7.6.

It can also be shown that the addition of a further term to equation 7.6 including another sample divided by the pulse's slopes there, does not add precision to the measurement, on the contrary, the rms of the quantity thus calculated increases to $0.038\,pC$ or 0.07%, even more than when using only one sample on the peak[38].

The samples in equation 7.6 are measured from the baseline of the pulse. For this at least one sample has to be taken before the pulse actually starts. By subtracting the baseline value we are in fact eliminating low-frequency noise which results in a coherent shift of the baseline and the samples on the pulse. We estimate[39] the band-pass frequency at $\sim 1\,kHz$.

The principle of equation 7.6 is very simple and very efficient for charge reconstruction but assumes a triangular pulse shape which is quite valid if the sampling points lie not very far from the nominal timing. However as the sampling time varies, the shape enters curved zones and equation 7.6 delivers for the same pulse (i.e. same integrated charge) a different quantity. This deviation is easy to compute and can be seen in figure 7.15. In fact the sampling time varies if events occur asynchronous to the sampling clock.

This is the case at the CERN calibration experiment in which particles arrive ran-

[38]This can be explained by the noise of the sum of 3 similar uncorrelated distributions which is $\sqrt{3}$ times the noise of one of them. This is of course not the case here where also the third measurement is correlated, but it's noise starts to be dominant vs. the improvement it brings.

[39]On the basis of sinusoidal noise of amplitude comparable to our signal.

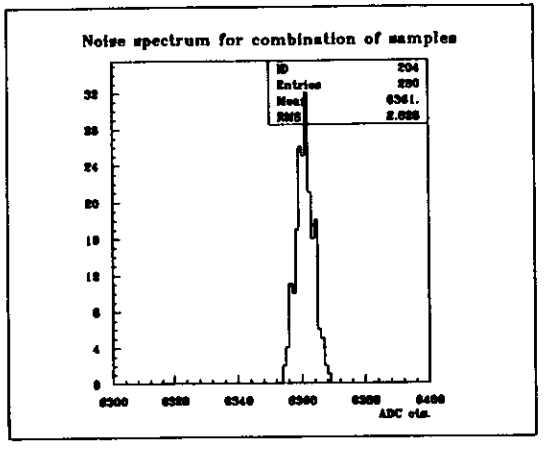


Figure 7.14: *Distribution of values following equation 7.6 with samples from both sides of the shaped signal. The same pulse of* 55 pC *is used. The rms is 2.7 channels, that is* 0.023 pC *or 0.04%. which is reduced with respect to the measurement at the pulses peak by a factor of 1.5 and approaches the 12 bit conversion limit of one unit in 4096, or 0.025%.*

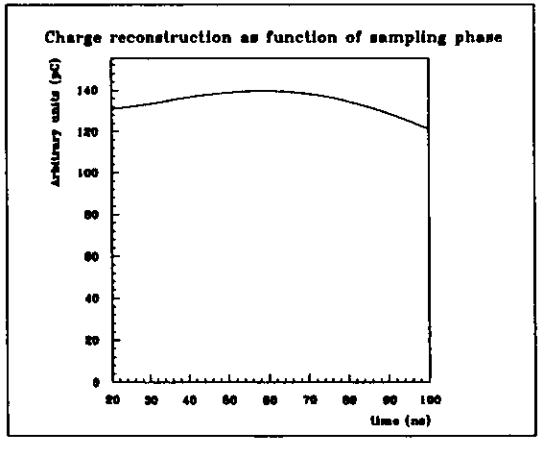


Figure 7.15: *Error in charge reconstruction due to the sampling phase variation. This result is obtained from an analytical expression of equation 7.6 derivating equation 7.5.*

domly during the 2.8 seconds spill span. Therefore two alternatives are possible. Either a synchronous trigger is defined which accepts only particles arriving in a very narrow fixed phase window, a method which yields low rate for data taking as $\sim$ 90% of the events are rejected. The alternative is to accept all the particles but measure their time relative to the sampling clock[40]. With this additional measurement one can correct the reconstructed charge with the function in figure 7.15.

An equally precise approach to the charge reconstruction can be taken by using the information in equation 7.5 defining the shape of the pulse and the relation between the samples. This procedure yields equally precise results as calculations with equation 7.6, but for asynchronous sampling needs no additional corrections, the shape of figure 7.15 being inherent to the pulse form of equation 7.5. One way to do this [70] is to extract from two samples the timing and then the amplitude at the expense of an extra determination of τ :

$$h_1 = \frac{Q}{\tau}\left(\frac{t_1}{\tau}\right)^3 e^{-\frac{t_1}{\tau}} \tag{7.7}$$

and

$$h_2 = \frac{Q}{\tau}\left(\frac{t_1+T}{\tau}\right)^3 e^{-\frac{t_1+T}{\tau}}$$

yields

$$t_1 = T\left(\frac{X}{1-X}\right)$$

with $X = \sqrt[3]{\frac{h_1}{h_2}} \cdot e^{-\frac{T}{3\tau}}$ and then enter with it equation 7.7 and obtain Q by using any one of the two samples

$$Q = h_1 \cdot \tau \left(\frac{\tau}{t_1}\right)^3 e^{-\frac{t_1}{\tau}}$$

The quantity τ is typically determined by performing a fit with the function of equation 7.5 to data coming from asynchronous beam runs.

With this method[41] and the same data as in the previous examples the quantity equivalent to $55\,pC$ is obtained also with 0.04% rms, similar to that calculated using equation 7.6. This approach delivers good results over the whole sampling phase range, however the calculation of the exact sampling time (or quantity X) is not precise if the amount of charge is small, and entering this into equation 7.5 gives a poor performance.

7.4.2 Time reconstruction

The second piece of information which is required from the calorimeter readout is the time at which the deposition of the energy occurred. As explained in the previous section the sampling at ZEUS occurs synchronously to the bunch crossing, the main data will have samples of approximately equal size on both the rising and falling edges. Those

[40] This is done by making a TDC measurement which is started with the trigger and stopped by the next sampling clock coming after it. This data is readout in a CAMAC module and gets incorporated into the main data stream.

[41] Though the method is simple as well, its implementation might be difficult in the DSP code (e.g. performing a cubic root) which is of very limited size.

signals will be defined to have an arrival time equal to zero. All the energy deposited will in fact have a time approximately equal to zero.

However, other energy depositions can take place at other random times. Among others cosmic ray muons can cause some energy signal within any section of the calorimeter. Also particles coming from the interaction of protons with the residual gas in the beam pipe might occur before the protons reach the interaction point and deposit their energy on the back side of the RCAL. This deposition occurs before the products of the main interaction reach the calorimeter.

These events can be rejected in a quite clean way by calculating their time and looking if it is compatible with the crossing of the electrons and protons.

The second method explained in section 7.4.1 makes already use of the calculation of the time which serves as input to the algorithm.

The simple scheme using only the sample information of equation 7.6 provides also a way of obtaining a precise measure of the arrival time. In contrast to the summing of the samples which is insensitive to the jitter, their difference is very sensitive to any relative shift between the signal and the sampling clock.

In fact, the variation of one of the samples on the edge, gives us the time jitter relative to a nominal sampling point defined to be $t = 0$ when both samples are equal. This variation is however larger if the size of the pulse is larger, that is the quantity is proportional to the charge :

$$t = \frac{h_1 - h_1^{nominal}}{s_{up} \cdot Q} \tag{7.8}$$

Equation 7.8 can be turned into an expression dependant on the two samples :

$$t_{sampling} = \frac{h_1 - h_2}{(s_{up} + s_{down}) \cdot Q} \tag{7.9}$$

where the slopes used are normalized to the charge as explained in equation 7.3.

In the same way as for the charge reconstruction, equation 7.9 is valid in the region around the nominal sampling, the pulse form not being straight lines anymore on the far regions. For those, also an analog shape as figure 7.15 can be analytically deduced. It can be seen in figure 7.16.

With relation 7.9, an the data used for the previous charge reconstruction examples from charge injected with the on-board charge injector a measurement of time is obtained with $0.1\,ns$ rms though due to noise this precision[42] decreases with decreasing energy.

[42]Note that this data is taken on a fixed set of cells, i.e. PULSE is produced with a cell synchronization, and only in this way is the time resolution better than the cell to cell jitter discussed in section 6.3.7 to be less than $0.25\,ns$.

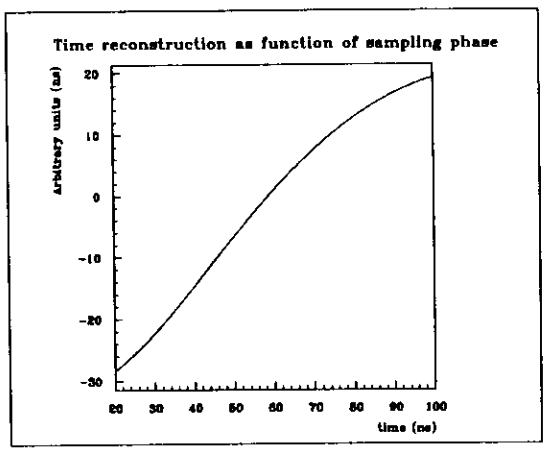


Figure 7.16: *Error in the time reconstruction due to the sampling phase variation. This result is obtained from an analytical expression of equation 7.9 using equation 7.5.*

Chapter 8

Results from FCAL module calibration

As mentioned in the preceeding chapter an experiment has been done at CERN to check the performance and calibrate with beam particles part of the modules of the forward and rear parts of the ZEUS calorimeter.

All the measurements have been performed with the pipelined electronics used in the readout of the ZEUS calorimeter. The results are based on part of the data which has been taken from one module[1] although 6 FCAL and 4 RCAL modules representing around 30% of all the FCAL and RCAL channels have been tested and calibrated [20]. The discussion is not meant to be an extensive calorimetric study. However the results show first that calorimeter readout can reliably be performed and second that the designed calorimetric performance has been achieved.

First, the experimental setup for the tests performed at CERN will be sketched.

8.1 FCAL Test beam Set-Up

The tests described in this chapter have been carried out at the X5 test beam in the West Area of the CERN Super Proton Synchrotron (SPS). The SPS operates with a period of 14.4 seconds out of which 2.4 seconds are spill time. The protons are accelerated to $450\,GeV$, extracted by a septum magnet and directed onto a target where secondary particles are produced, ($\pi^-, \pi^+, \pi^0, e^-, e^+, p^-, p^+, \mu \ldots$). A magnet spectrometer selects charged particles according to charge and momenta and transports them to the calorimeter modules. The energies available range from ~10 to $110\,GeV$.

The spectrometer is equipped with a set of detectors for particle identification, selection and triggering. Figure 8.1 shows a scheme of the counters and detectors in the particles path. There are:

- Trigger scintillation counters (B1, B2, B3, B4, B5). Counters B1 and B2 cover the entire beam. B4 is a large surface counter with a $2\,cm$ diameter hole for rejection of off axis particles and upstream interactions. Counter B5 is placed behind the calorimeter module and thus gives a signal for particles which are not absorbed in the calorimeter.

- Two Čerenkov counters ($\check{C}$) filled with He and N_2, produce signals which are used to discriminate electrons from hadrons.

- Two sets of multiwire proportional chambers (MWPC), each with two chambers, before and after the last bending magnet, provide particle tracking for precise measurements of momenta for every event.

- Two drift chambers placed near the calorimeter module allow measurement of the precise impact coordinates of the particles.

[1] Internal denomination FNL1 tested in October 1989.

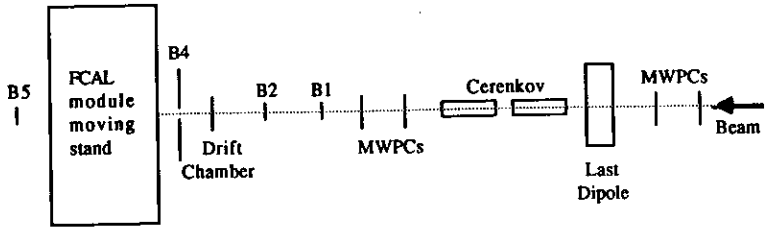


Figure 8.1: *Experimental setup at the SPS X5 beam line for FCAL calibration test.*

With these detectors the following relations can be defined:

$$\begin{aligned} BEAM &= B1 \cdot B2 \cdot \overline{B4} \\ Electron &= BEAM \cdot \check{C} \\ Hadron &= BEAM \cdot \overline{\check{C}} \\ Muon &= BEAM \cdot B5 \end{aligned}$$

Information from the trigger counters, MWPC's and Drift chambers are digitized using standard CAMAC modules. These are readout by the data acquisition computer for every particle satisfying the trigger conditions selected.

The up to 13 tons heavy modules lie on a stand which can be moved vertically and horizontally to expose every part of the calorimeter with the incident beam. The movement is performed by electric motors under computer control. A monitoring system reads back into the computer the actual position of the table. The horizontal position is measured by two axial encoders coupled to toothed wheel gears with different transmission ratios moving with the stand. The vertical encoder is a sliding ruler. Both devices give measurements with a precision of $0.5\,mm$ and deliver Gray coded binary numbers which can easily be converted into positions.

8.2 Electronics noise vs. UNO

The requirements for the signal to noise ratio for the electronics have been discussed in previous chapters. The fact that the ZEUS calorimeter uses uranium as absorber material adds the signals from the radioactivity to all the measurements performed. The noise coming from the electronics is never a dominant factor as can be seen in figure 8.2.

When no beam energy has been deposited in the calorimeter, the energy the system measures should be zero[2]. The UNO signal has been included in the pedestal as we want to measure the additional signal from the particles. This is checked with random trigger runs the result of which is shown in figure 8.3.

The current from the PMT due to the uranium radioactivity is integrated with a time constant of $20\,ms$ and can be arbitrarily chosen by setting the high voltage on the phototube's base. This determines the scale for converting charges from the PMTs (pC) to deposited energy (GeV). A value of $100\,nA$ is set so that the signals for the minimum ionizing particles, as seen in the EMC sections, appear in ADC channel 100 as discussed in section 4.2.1.

From this number, the currents from the other sections can be derived just by multiplying by the amount of DU material which contributes to the signal in each case taking into account the attenuation[3] due to different cladding thicknesses. The HV for HAC sections is set so the UNO current measured is $500\,nA$, $400\,nA$ in the case of HAC0 sections.

Of course the values which are set in practice show small variations from channel to channel because the HV really set is not exactly the demanded one or drifts occur in time. The UNO current is however measured (typically every 8 hours) and the signals from the calorimeter can be normalized to the nominal values of the currents. All the comparison from channel to channel are thus corrected for the UNO currents. This is the so-called *UNO calibration*.

8.3 Pulse form and energy reconstruction

In the test beam particles incident on the calorimeter are asynchronous with respect to the sampling clock. If we plot the 8 recorded samples against the time at which they were taken[4] we obtain the plot of the shaped pulse. Figure 8.4 shows the shape of the pulse obtained with $15\,GeV$ electrons on a PMT of an EMC section. Figure 8.5 shows as a comparison the shape obtained with events from charge injection in the front end electronics.

[2]Even if UNO are real pulses, we are not triggering on them and the method to reconstruct charge by subtracting a previous sample will yield both positive and negative charges as shown in figure 8.2.

[3]The DU plates of the HAC sections are cladded with a $0.4\,mm$ thick stainless steel foil while for the EMC plates the thickness is only $0.2\,mm$. This additional cladding attenuates the DU signal by a factor of ~ 2.6.

[4]This time is a sum of the global time of the event relative to the sampling clock as measured with the TDC plus the number of the sample times the sampling clock period.

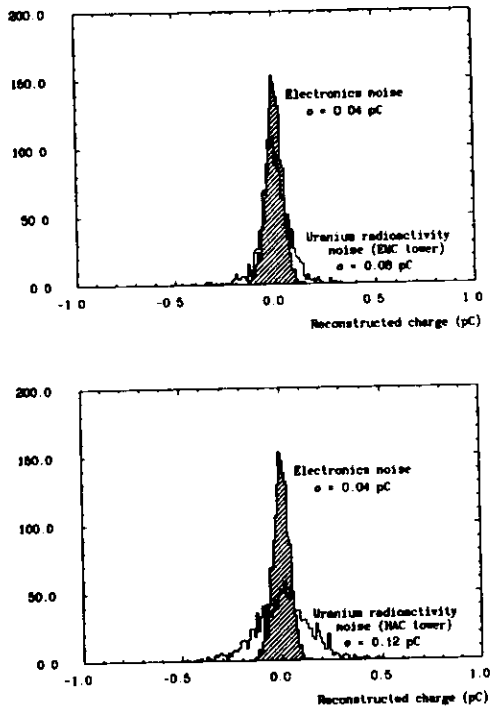


Figure 8.2: *Noise distributions from calorimeter channels (high gain readout). The data has been taken when no beam signal was present in the calorimeter. In each case one channel where no calorimeter PMT is connected is shown (shaded) against another one where EMC (top) or HAC (bottom) sections are connected. The electronics noise is $0.04\,pC$ equivalent to $8\,MeV$ per channel and is at the level at 1.5 ADC counts.*

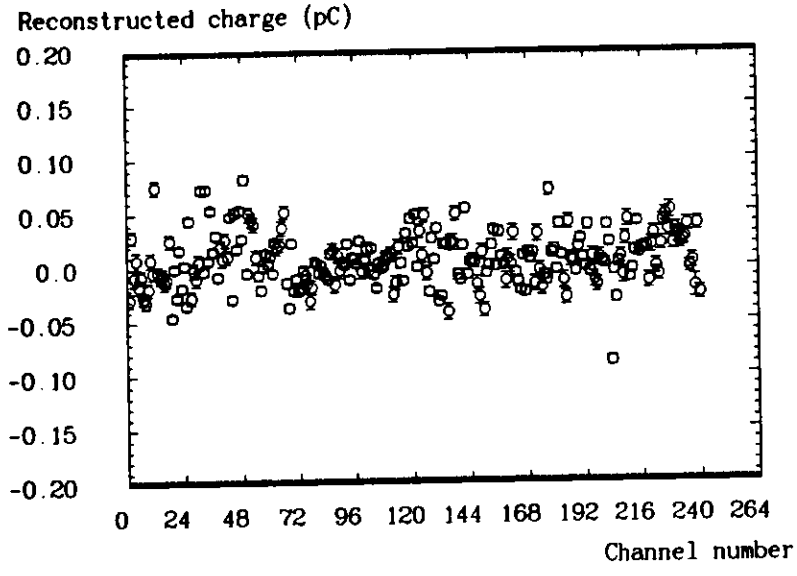


Figure 8.3: *Reconstructed charge for random triggers for all the channels of the module. The values are within* 0.05 pC *(or* $\sim 1-2$ ADCcounts*) equal to* 0.0 pC.

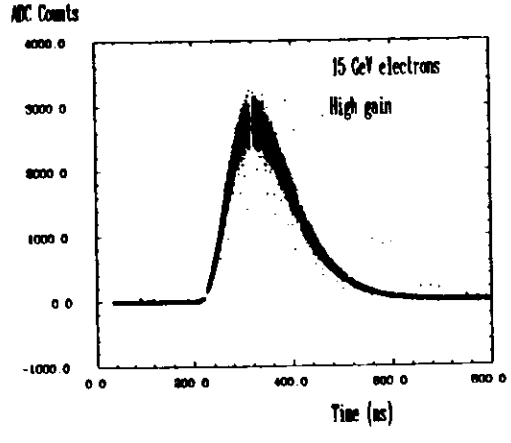


Figure 8.4: *Pulse shape obtained from electron events. The plot is obtained by taking the 8 samples of many asynchronous events and plotting them together. Note that the width of the shape is due to the calorimeter resolution. If fitted to equation 7.5,* τ *results in* $\sim$ 36 ns.

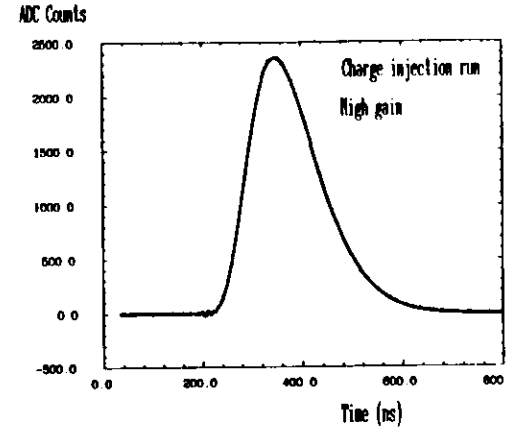


Figure 8.5: *Pulse shape obtained from charge injection events. The pulse is much better defined than the electron pulse as there is no fluctuation in the input signal. The small jitter at time* $\sim$ 200 ns *is generated by the injection system which happens at that instant. Due to this the baseline measurement used is the one taken one sample before, i.e. time* $\leq$ 100 ns. *Again a fit to equation 7.5, yields* $\tau \sim$ 38 ns.

If we want to use in the analysis the data from all the events taken with no cut on their phase, a correction curve like figure 7.16 has to be computed or deduced from the data itself. Figure 8.6 shows such a curve derived from data used for the correction of the reconstructed charge for events which are off-phase with the sampling clock.

However in order to be able to apply the curve from figure 8.6 to all the channels, their relative time differences have to be taken into account so that the maximum of the curve appears at $t = 0$, for all channels.

We define $t = 0$ when the two samples on the shape of the signal are equal height. When the pulse like in figure 8.4 comes from particles, two factors contribute to the channel to channel time shift :

- Different PMTs have different transit times. This is in general true for different types of PMTs like is the case of the FCAL modules[5]. The transit time is a function of the high voltage (V) applied on the dynodes [71], typically related to $\frac{1}{\sqrt{V}}$. This causes minor differences ($\leq 5\,ns$ between channels).
- Different sampling time in the pipelines (see section 6.3.7) between the input of the sampling clocks and the actual sampling.

This can be seen in figure 8.7. The numbers derived from this plot are used to center the shape of figure 8.6 on $t = 0$ for all channels.

[5]The EMC tubes are of the type Valvo XP-1911 while the HAC tubes are the larger Hamamatsu R-580 (see section 3.4.4).

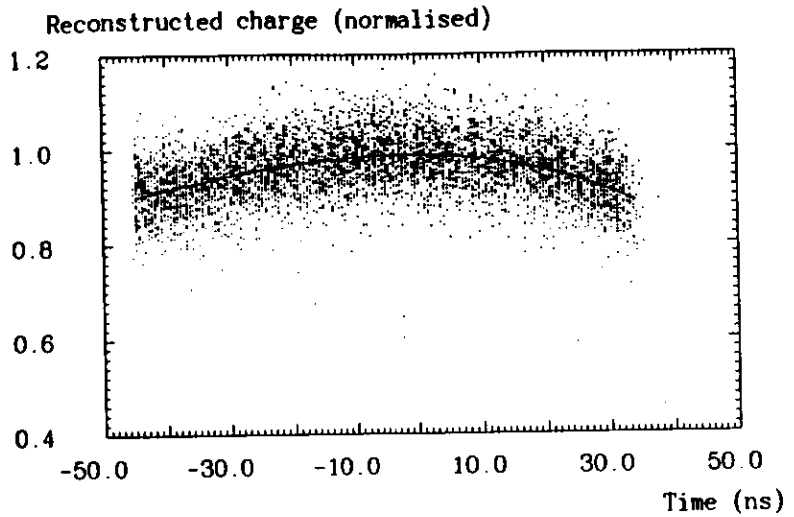


Figure 8.6: *Correction for energy reconstruction of off-phase events. The data comes from* 15 GeV *electron events. The fit is a* 4^{th} *degree polynomial. The correction is approximately valid for all energies and for all types of particles.*

8.4 Particle selection

Different types of particles have been used to calibrate the calorimeter modules. The main particle selection was done via the choice of the target and absorber in the primary beam. Also a particle selection trigger has been defined at the test beam (see section 8.1). However for an offline analysis a better selection has to be performed to have a clean sample of events with none or little contamination from misidentified particles. This can be done by applying selection cuts to the digitization measurements from the beam line detectors

The shower development within the calorimeter itself can also be used, see figure 8.8, for particle identification since :

- Muons, as minimum ionizing particles, deposit little energy in the sections where they traverse the calorimeter and none outside,
- Electrons deposit most of their energy in the strip where they hit the calorimeter and very little in adjacent strips or in the deeper hadronic sections. This is clearly seen in figure 8.8 (middle) for a sample of events taken with the electron trigger and a beam energy of $15\,GeV$. Most of the events show in fact the described conditions and will be analysed as electrons. However figure 8.8 (bottom) shows a large contamination of the electrons in a $110\,GeV$ beam with other particle types, e.g. hadrons (little energy in the incident strip and large in the rest of the

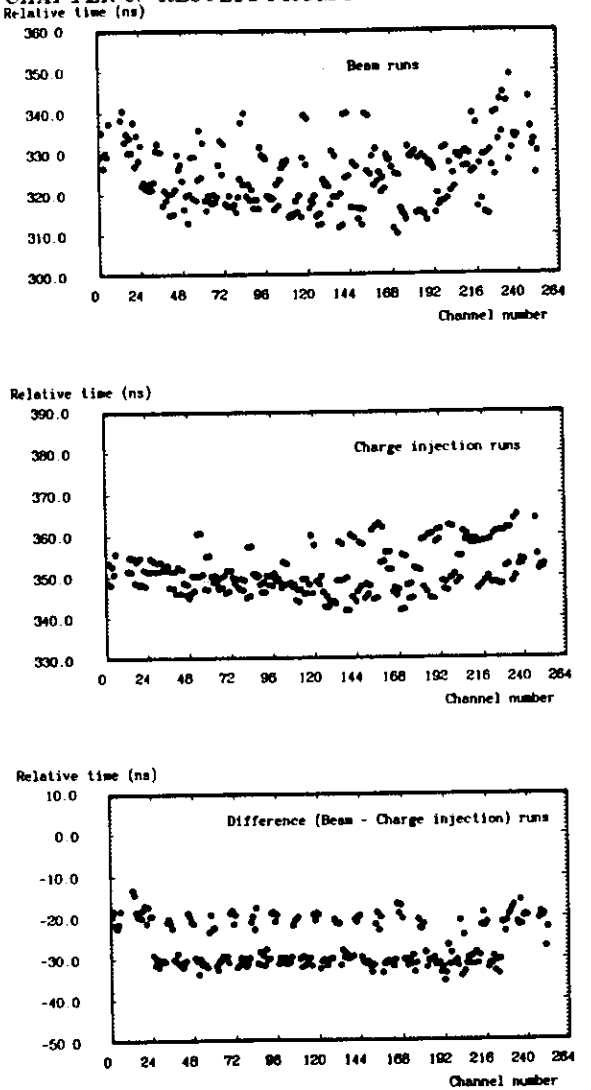


Figure 8.7: *Relative time differences between channels. The unit on the left side are* ns *but the absolute scale is meaningless. The plots show timing obtained with beam runs (top), with charge injection (middle). The bottom plot is the difference between the two others and shows a difference of* ~ 10 ns *transit time between the EMC and the HAC tubes. Note that the channels appear always in groups of two. This comes from the fact that two adjacent channels are readout by the same pipeline chip which has almost equal transit time in its four pipelines (see Table 6.1). This is clearly seen in the middle plot and with some smearing from the PMTs' high voltage, also in the top.*

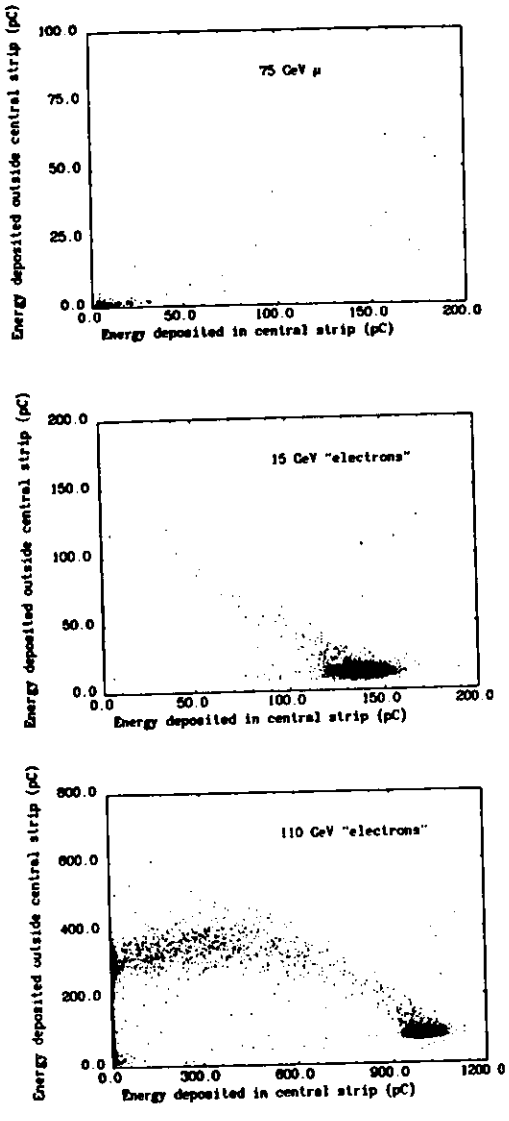


Figure 8.8: *Energy deposited in the calorimeter for different particle types displayed as correlation between the part deposited in the EMC section where the beam is incident and the rest.*

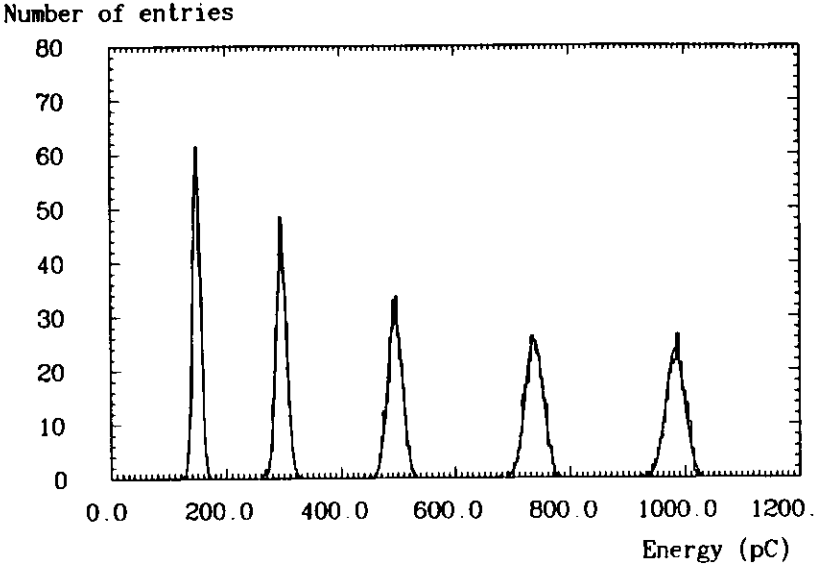


Figure 8.9: *Pulse height distributions for electrons (from left to right) of 15, 30, 50, 75 and 100 GeV with the results of gaussian fits.*

calorimeter) or muons. This indicates that the setting of the Čerenkov detector was not optimised for high energy beams.

On this basis, applying the selection for the expected energy in the central section and the rest, the criterion is used for choosing samples of particles and eliminate contamination. As an example electrons of 15 GeV were defined as particles depositing between 100 and 170 pC in the central EMC section and between 0 and 30 pC in the rest of the module.

8.5 Energy resolution for electrons

The fluctuations in the calorimeter signal discussed in chapter 3 show up as a spread in the samples of the pulse (see figure 8.4) and can be seen in the distributions of measured charge. For electrons of several energies these are shown in figure 8.9.

The standard deviation of the gaussian fits to the data is what we call the energy resolution and as theory predicts this scales with the $\sqrt{E}$ which means that the precision of the measurement *improves* with increasing energy. This can be seen in figure 8.10 where we also see that the result of the fits yield a value for the resolution of $\sim 17\%/\sqrt{E}$ for electrons as expected from the construction of the calorimeter.

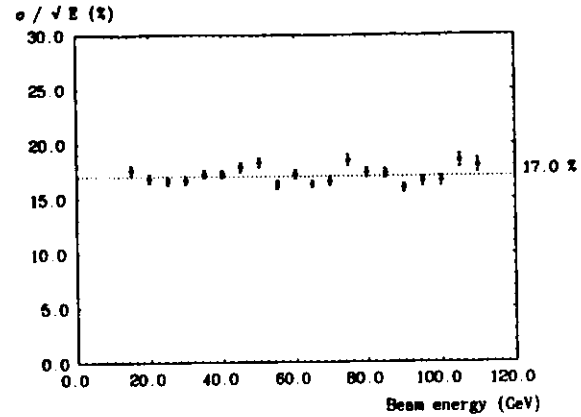


Figure 8.10: *Energy resolution as function of the energy of the electrons. The value of* $17\%/\sqrt{E}$ *is maintained over the whole energy range tested.*

8.5.1 Linearity response

One of the most important requirements of a calorimeter as an energy measurement device is that the measured signal is proportional to the deposited energy.

The different components in the readout chain have been tested for linearity over the ranges where they operate. The pipeline's non-linearity was shown in section 6.3.5 to be below 0.25% over the whole range used. In the same way the PMT's with their bases have been tested and show less than 1% deviation in the plotted range (up to 4% for the whole energy range at HERA).

The results of a linearity study with electrons are shown in figure 8.11 where a non-linearity below 0.5% can be seen. However a certain uncertainty (not show in the figure) exists in the determination of the particles momentum. For this, the MWPC's are used and a precision of 0.8% in the momentum measurement is achieved.

8.6 Minimum ionizing particles

In contrast to electrons, muons traverse the calorimeter as minimum ionizing particles and only rarely generate large showers. They deposit ionization energy in the scintillator layers that they cross. This yields a visible signal which is proportional to the number of layers of scintillator.

A few muons however might suffer Bremsstrahlung which adds to the energy loss deposition in the scintillator giving an asymmetric energy distribution which goes beyond the Landau tail as shown in figure 8.12.

In this figure we also show the results of fitting the energy spectra for 75 GeV muons

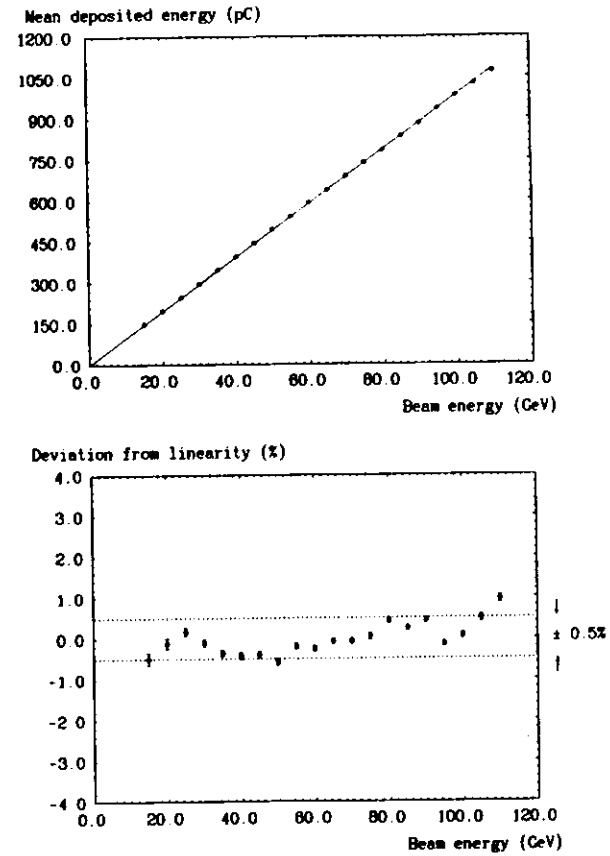


Figure 8.11: *Energy deposition for electrons of different energies (top) and deviation from a straight line (bottom).*

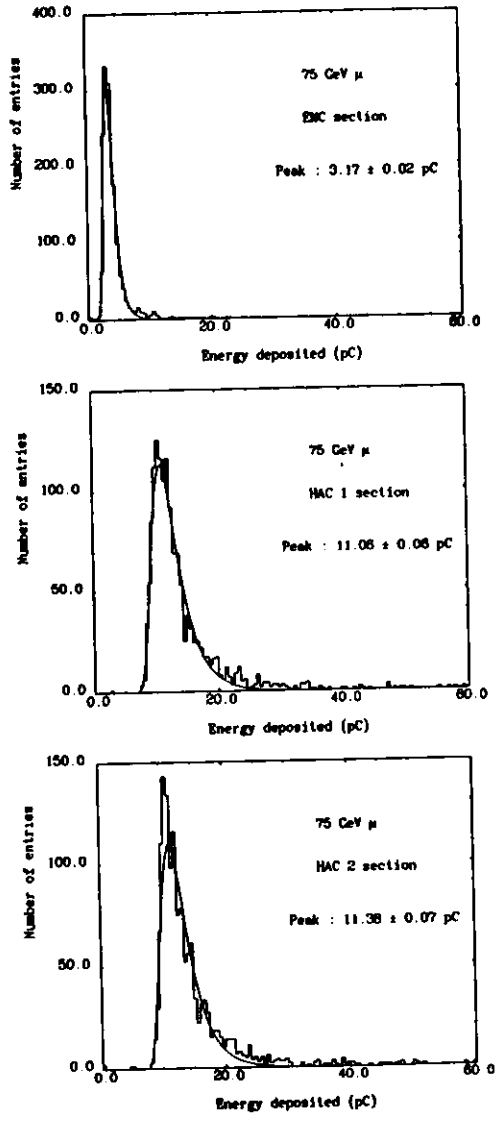


Figure 8.12: *Pulse height distributions for 75 GeV muons in different sections of the calorimeter and Landau fit results. The most probable energy is proportional to the number of layers of scintillator the muons cross (~ 25 to 80 EMC to HAC). Note that the signal in the HAC2 section is a little larger than the one in the HAC1 as we take the same normalization of the UNO signal for both HAC sections although the HAC2 signal is a little smaller due to less uranium volume.*

to an approximation of the Landau distribution [72] given by :

$$f(x) = \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}(\lambda + e^{-\lambda})}$$

being $\lambda = \frac{x - x_{mop}}{\sigma}$ This function has two free parameters, the most probable energy loss x_{mop} and a width σ. It is the fitted most probable energy loss which will be used for uniformity studies in the next section.

8.7 Calibration error and calorimeter uniformity

Finally we require from a calorimeter that it is calibrated in a way that its response is independent of the impact position of the particles.

It has been explained in section 8.2 that the procedure to tune different sections of the calorimeter among each other, is to adjust the HV of the PMTs so that the UNO current measured results equal for equal type of sections. The pulse heights from particles are normalized to these values. The aim is that this should be the only inter-calibration method used in the ZEUS calorimeter.

The alternative would be (as it is usually done in other detectors) to calibrate each section with particles of known energy and keep this number as correction constant which will be applied upon the signals given by particles of unknown energy. Only ~30% of the FCAL/RCAL channels have been tested in this way so the method would require quite some additional test beam effort.

The important result however, is to see how large the systematic error is if we apply only the UNO calibration. With the test beam measurements and collecting data for the different sections of the modules, a non-uniformity measurement can be obtained. The spread of these amounts is the systematic error we are introducing if we say that all the responses were to be equal to their mean.

This response uniformity can be checked with different particles. For the EMC sections scans with electrons of different energies are performed. Also scans with muons give a measure of the uniformity of the response. For HAC sections, both hadrons and muons have been used.

The response over the EMC strips of the module is plotted in figure 8.13 for 15 GeV electrons along with the energy resolution.

In figure 8.14 it can be seen that a similar uniformity is obtained with 75 GeV muons. The uniformity of the HAC1 and HAC2 sections is shown in figure 8.15.

The result of all the uniformity scans is that the section to section signal differences show a spread of ~1%. This is also true for inter-module calibration [20].

We conclude therefore that the constant term in the resolution amounts to 1% :

$$\frac{\sigma_E}{E} = \frac{17\%}{\sqrt{E}} \oplus 1\%$$

for electromagnetic showers.

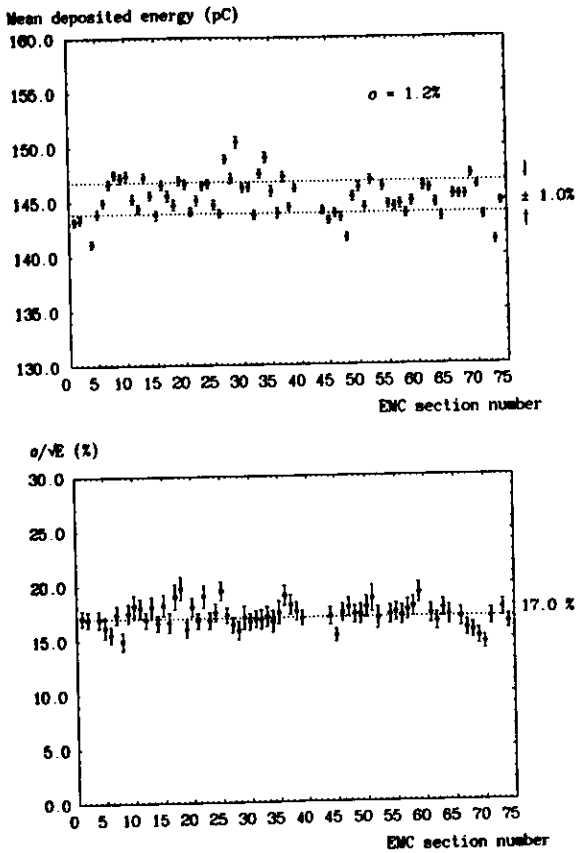


Figure 8.13: *Response of the EMC and HAC0 sections to* 15 GeV *electrons. The signal plotted is all the energy deposited in the calorimeter. The energy resolution is maintained over the whole module.*

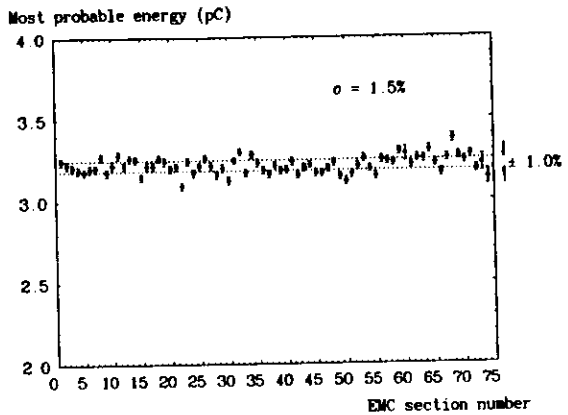


Figure 8.14: *Response of the EMC and HAC0 sections to* 75 GeV *muons. The values plotted correspond to the most probable values of the Landau peak.*

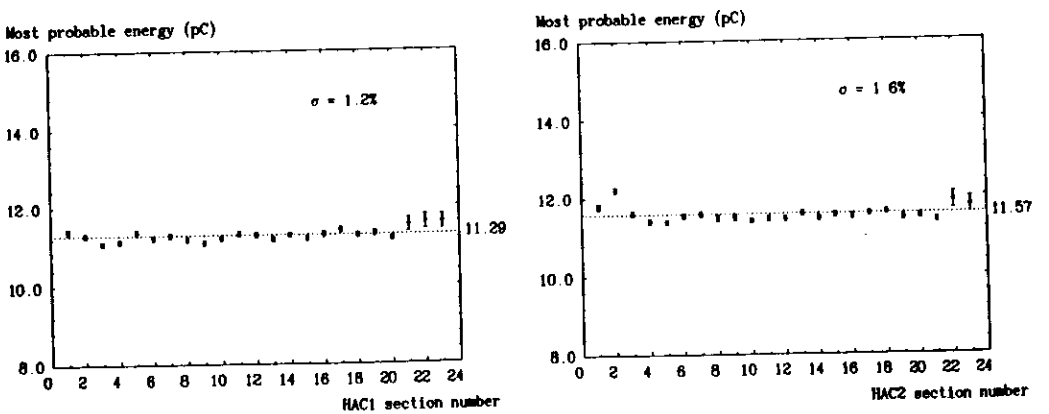


Figure 8.15: *Response of HAC1 (a) and HAC2 (b) sections to* 75 GeV *muons. Again the value plotted is the most probable value of the Landau distribution. Only the signal from the section where the particles are incident is included in the signal.*

The hadronic resolution could not be measured as only one module was tested at a time and this does not provide containment of the hadronic showers. The uniformity scans shown and measurements with a prototype calorimeter [12,73] indicate that the constant term in the resolution for hadrons is below 2% :

$$\frac{\sigma_E}{E} = \frac{35\%}{\sqrt{E}} \oplus 2\%$$

8.8 Timing resolution

As mentioned in chapter 4, one of the advantages of the shaping-sampling measuring method is that one can as well obtain a time measurement from the samples, as discussed in section 7.4.2.

Figure 8.16-(a) shows the reconstructed time for $15\,GeV$ electrons arriving asynchronously relative to the sampling clock. The correction due to the non-triangular shape of the pulse calculated in figure 7.16 is shown as measured with the TDC. In the plot (b) the time resolution achieved can be seen to be $\sim 1\,ns$.

Also shown (c) is the time resolution for muon events. As expected the time resolution degrades with decreasing energy as noise becomes relatively more important.

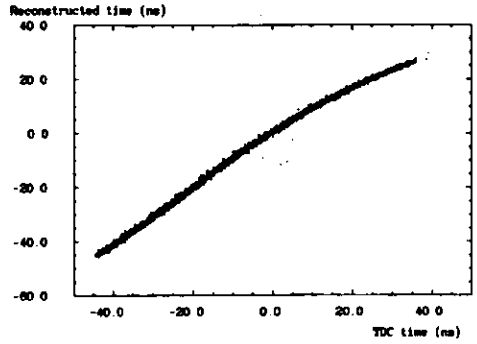
8.9 Conclusions

The analog pipelined electronics designed for the readout of the high resolution calorimeter for the ZEUS experiment has been presented in this document. The performance of its components as well as the global system is excellent and satisfies the requirements to operate at HERA.

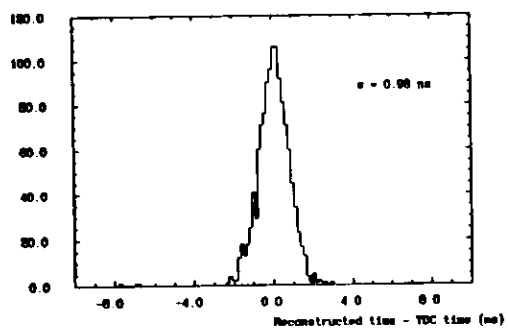
For the wide implementation of analog pipelined readout new integrated circuits have been developed. They have been tested for the characteristics which are critical for the readout of the calorimeter signals.

A highly complicated system covering all the aspects of control and operation of the readout has been described and used for data taking.

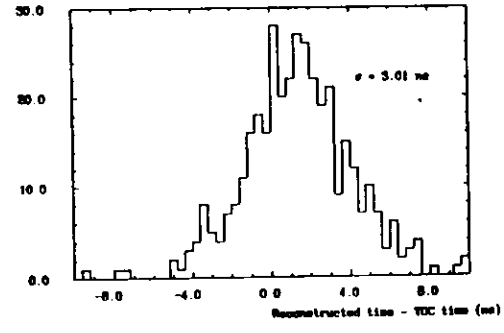
Finally the readout after installation and running was used to check the response of of single modules, part of the calorimeter in a test beam. The off-line analysis of the data taken shows excellent performance of the electronics and the calorimeter modules themselves.



(a)



(b)



(c)

Figure 8.16: *Reconstructed time for* 15 GeV *electrons shown vs. real time measured with a TDC (a). After correcting for this error,* $T_{reconstructed} - T_{measured}$ *is shown to have an rms of* $\sim$ 1 ns *(b). In plot (c) the same quantity is plotted for* 75 GeV *muons which show a time resolution* $\sim$ 3 ns..

Appendix A

Readout of future calorimeters

During the last decade, calorimetry has proven to be one of the major detector techniques. It has evolved from a rather specialized application for neutrino scattering experiments to the major tool for large collider detectors.

The ZEUS calorimeter is the state of the art for calorimeters in a collider experiment. Its readout presents new features which are being tested for the first time.

However even before the detectors for HERA are completed, discussion has already started for the construction of new collider facilities and with it, their experiments. These projects concentrate on the SSC[1] to be built in the USA, LHC[2] planned to be housed in the LEP tunnel at CERN and UNK in the Soviet Union.

All of these colliders will produce (at least initially) $p-p$ collisions at several TeV of energy in the center of mass. The extremely small cross-sections for interesting new physics forces, as in the case of HERA (though one or two orders of magnitude larger) a very high luminosity ($L \approx 10^{33} - 10^{34} cm^{-2} s^{-1}$) to be used. This leads, as in HERA, to multibunch machines with small bunch crossing times between 10 and $20\,ns$.

For accelerator construction, but mainly for detector design, this small bunch crossing time is one of the hardest factors to cope with.

Other features are also difficult for the readout electronics of the future calorimeters. Among them :

- radiation damage due to the high particle rates,
- the calorimeters have to detect energy of particles which span over 4 or 5 orders of magnitude, from minimum-ionizing particles (muons) depositing fractions of GeV up to TeV jets of hadronic events.
- calibration at the 1% level,
- timing information of the energy deposition,
- triggering decision has to be based on data from the calorimeter,

[1] Super Conducting Supercollider
[2] Large Hadron Collider

- readout of $10^4 - 10^5$ channels to obtain the necessary granularity.

The solutions depend largely on the calorimeter technique employed but many issues are common to all of them. The choice of the calorimeter and the active (and to some extent the passive) materials used determines the number of channels or the speed and magnitude of the signal obtained from the readout elements.

However the need of pipelining the signals while a trigger decision is being generated still remains. Alternative methods for pipelining in the same way as commented in the case of the ZEUS detector also appear, but once more, and for the same reasons than the ones commented in chapter 4 analog pipelining may be the only viable solution.

From the answer by ZEUS to the pipelining problem, a long way has still to be covered to reach the requirements of the next generation of colliders.

The main concepts available at present (e.g. [74,75]) adopt readout architectures similar to the one used in the ZEUS calorimeter. However all of them leave open the question of the construction of the analog pipeline which has to achieve a performance unparalleled up to now.

Many of the electronic issues must be pursued to build the different parts of a readout system however, only the pipelining problem will be addressed here.

A.1 New analog pipeline developments

All the up-to-now discussed solutions are based on the same principle as the readout for the ZEUS calorimeter, namely a switched capacitor analog storage VLSI ASIC to pipeline the high precision data while the trigger is being processed. Several research projects are underway with emphasis on various issues of which (probably) all of them are needed. They are not specific to a calorimeter or other detector type project but are being developed in the frame of general R&D for detector readout without having precise specifications as for the exact signals which have to be readout.

The solution [76,77] features many (256) storage cells per readout channel while integrating 16 channels on one chip. The sampling is performed on rising and falling edges of the clock (up to $50\,MHz$) and large sampling rates ($\leq 100\,MHz$) are achieved. However the considerable charging time constant ($16\,ns$) limits the gain of the system at high sampling rates (-0.75 at $50\,MHz$). The dynamic range (8000:1 at $10\,MHz$) is as good as in the ZEUS chip for single cell outputs, and the cell to cell non-uniformity is also comparable($4\,mV\ rms$). The non-linearity is however somewhat larger (1% in the $\pm 1\,V$ range, 3% in the $\pm 2\,V$ range). One channel of the circuit is shown in figure A.1.

The higher speed reached is due to a different design of the shift register operating the sample and hold switches. The larger integration (4096 vs. 232 sampling cells in a similar die size of $6.8 \times 4.6\,mm$) is achieved by using a common shift register for all channels and a finer technology ($2\,\mu m$ *vs.* $3\,\mu m$ CMOS processes). As a supplementary feature, the 16 channels on one chip can be readout on separate outputs or multiplexed to one common output under the control of an address set.

Another development in a similar direction is [78]. The aim of the circuit is somewhat

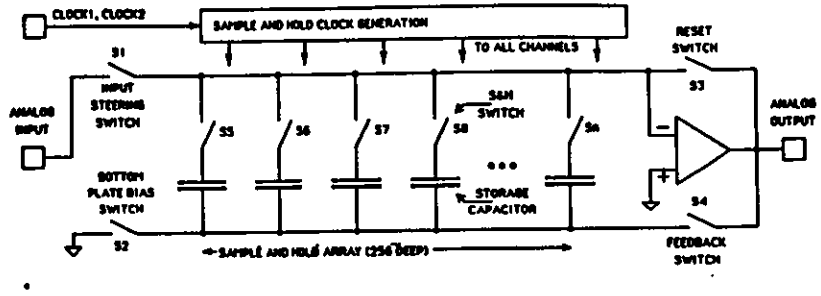


Figure A.1: *One channel 4096 cell analog pipeline circuit [76].*

different than in the ZEUS case or the above mentioned 4096 cell device. Instead of a waveform storage device, it is used as a charge sampling integrator which integrates and stores the charge arriving in a clock period. The device of a second parallel development can store one voltage sample (e.g. to sample a shaped signal like in the ZEUS case but only at the peak of the pulse) in each clock period.

The main pipeline consists of 64 cells operated at $20\,MHz$ switching rate. The device includes a second level storage of eight cells where up to eight accepted events after the first level trigger can be stored in a similar way to the ZEUS buffer-multiplexer chip. A circuit diagram for one charge integrating channel can be seen in figure A.2.

This pipeline performs simultaneous reading and writing operations opening the possibility to deadtimeless operation. In fact while cell i is being written, cell j (which represents a delay to i of the time needed for the fist level trigger to decide) is being read and stored in the first cell of the second level storage. When a trigger signal really arrives, this first cell is kept and cell j will be written onto cell 2 of the second level storage. Thus no interruption of the writing operation is necessary and no detector signal is lost : zero deadtime is achieved.

The device has been implemented in $3\,\mu m$ double-poly CMOS technology and with a size of $2 \times 8\,mm$ integrates 4 channels per dye. The pedestals ($5\,mV\ rms$) and gains non-uniformity (2%) are comparable to those of the ZEUS pipeline but the dynamic range is reduced ($\pm 2\ V$). Noise or linearity performance was not known at time of publication.

A.2 Other developments

Another R&D project [79] which is being pursued at the moment is to use the same ZEUS analog pipeline near its maximum sampling frequency. Connecting several (n) pipelines in parallel which are sampling the same input signal and which have their sampling clocks shifted by ($1/n$) clock cycles yields finally an n times faster readout system. This scheme is drawn in figure A.3

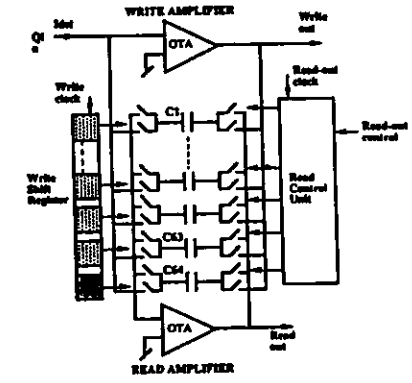


Figure A.2: *Simultaneous read and write analog pipeline [78].*

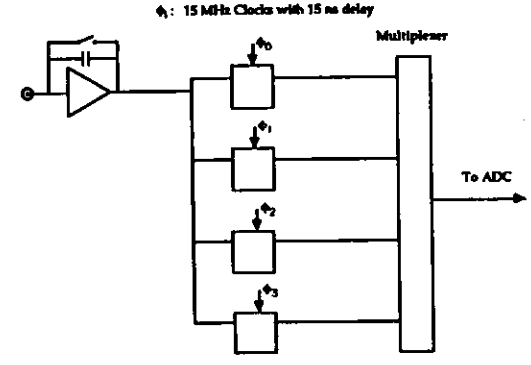


Figure A.3: *Proposal of a $60\,MHz$ pipeline system using the ZEUS analog pipeline chip [79].*

The proposal is to operate the ZEUS pipeline at $15\,MHz$ (which is quite feasible as we have seen) and use 4 pipelines in parallel thus having a full $60\,MHz$ pipelined system which could be used with the proposed bunch crossing times of 15 or $16\,ns$.

More specifically, the output from the phototubes of the calorimeter is subject to one pure integration so as to keep the signal fast. The charge pulse received is converted to an integrated voltage at the output of an operational amplifier with a feedback capacitor.

After (or during) the readout, the charge of the integrating capacitor is cleared with a reset switch. This project is still in R&D stage and does not touch problems like deadtime ...

A.3 Integrated electronics progress

All the concepts which are being handled for the readout of future calorimeters assume the existence of an analog pipeline device with enough speed, large enough integration and power consumption to cope with the requirements of the new experiments. In addition the components have to work in hostile radiation environments for several years with none or minor quality degradation.

All of these projects expect that the improvements in integrated circuit technology will provide answers to the above questions.

The two main effort directions are to develop devices which :

1. have a very high radiation resistance,
2. achieve a speed compatible with the bunch crossing time ($\sim 66\,MHz$).

The radiation hardness of CMOS devices is an unsolved problem. The ZEUS pipeline shows large power consumption after doses of very few *krad* which is a concern even for the radiation levels at HERA. The same pipeline produced at other foundries with compatible technology shows a much larger radiation tolerance (up to $50\,krad$ with similar performance). Still, the expected doses at the new detectors are orders of magnitude above the present numbers. The exact radiation dose depends of course on the localization of the electronics inside the detector.

However probably no way exists around CMOS switched capacitor technology for the implementation of the pipeline mainly due to the low power consumption and low noise readout.

The speed limit in the CMOS technology of today cannot be arbitrarily set at some level. This certainly depends on the type and design of the device.

As seen in chapter 6. the ZEUS pipeline stops functioning at frequencies over $\sim 18\,MHz$. The test chip developed previously could operate up to $\sim 25\,MHz$ (this was probably due to smaller stray capacitances because of an smaller number of capacitors). The device is however not designed for high speed operation, it should work at some secure level over the required $10.4\,MHz$. Studies [80] indicate that a optimization of the same design for speed and using the same technology could yield a maximum operating frequency of $25\,MHz$.

The devices presented in Section A.1 though with some limitations, have been shown to work up to $50\,MHz$ or $20\,MHz$.

It is clear that the design mainly of the shift register, partly limits the maximum achievable frequency in writing. Fast CMOS counters exist in $3\,\mu m$ technology where the flip-flop toggling rate is typically $60\,MHz$ with functioning devices up to $90\,MHz$.

A high switching speed can only be maintained if the storage cells load up in a fast enough way. We saw (Section 6.3.6) that the charging time constant of the ZEUS pipeline was $\sim 6\,ns$ and for the pipeline [76] it is $\sim 16\,ns$. The figure of $6\,ns$ has to maintained or even reduced so that the capacitor (almost) reaches its final voltage.

The further development of CMOS technology as an industrial application is one of the hopes to reach the higher speed these new pipelines need. Today, CMOS processes exist which use minimum feature sizes around or even under $1\,\mu m$. They are mainly used for digital applications with very low voltage swing. However it must be still proven that they can be used in analog or mixed applications because of a very limited available analog range for the signals with these small transistors (see Section 5.8).

It is also difficult to quantify the increase in speed that the size reduction of devices bring with them but it is expected that with a $1.5\,\mu m$ technology one can build a $50 - 60\,MHz$ pipeline.

A.3.1 Silicon on Insulator technology

In all of these problems the SOI CMOS[3] technology shows promising characteristics. Several processes using this technology produce digital devices mainly for military applications which tolerate $1\,Mrad$ doses.

A quick description of the SOI technology with its main advantages will be given. A review of SOI techniques can be found in [81].

SOI techniques are based on the construction of active electronic devices on a silicon region vertically isolated from the underlying substrate. How this isolation is achieved results in many different technologies which have been pursued over the last years with mixed success. Some examples of SOI techniques are the ELO (Epitaxial Lateral Overgrowth), SOS (Silicon on Sapphire) and the SIMOX (Silicon on Implanted Oxygen) technologies.

SOI techniques typically set off an insulating material and make on top of it a silicon surface where they build the devices. This layer is usually low quality silicon full of imperfections due to either a bad interface (e.g. non matching crystal net) or a rough treatment (e.g. very high temperature) of the silicon layer. As a result of this the SOI processes have typically a very low yield, a fact which has limited their use to special applications (e.g. military).

The SIMOX technology after having solved many technological problems seems to be reaching series production maturity. It uses standard monocrystalline silicon wafers as any MOS technology and buries on its upper part a silicon oxide insulator layer leaving on top a thin monocrystalline silicon volume where devices can be built onto.

[3] Silicon On Insulator CMOS.

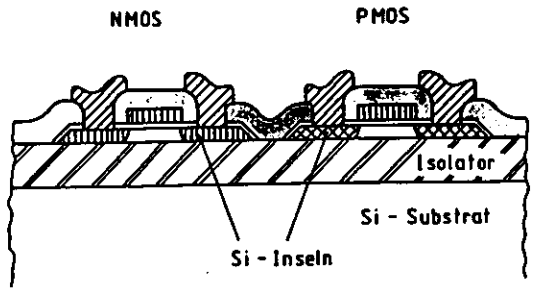


Figure A.4: *SIMOX transistors [82].*

The way to fabricate the buried insulating layer is now an industrial standard and thus SIMOX technology is starting to be commercially available. Oxygen ions are accelerated to $200\,keV$ with a linear accelerator, particles are selected with magnets and magnet lenses are used to focus the beam which is directed onto the silicon wafers. To achieve a high implantation uniformity the (up to 25) wafers are being spinned on a rotating table while the oxygen beam impacts on them.

After the implantation, an annealing process at high temperature ($\sim 1200°C$) improves the profile of the implant in the depth of the wafer so that a layer of $\sim 0.35\,\mu m$ ($\pm 10\,nm$) insulating oxide results[4], leaving a good quality $\sim 280\,nm$ thick monocrystalline silicon surface on top of it.

From here onwards a standard CMOS process is performed with the usual tools of lithographic area definition, implantations, etc. as shown in figure A.4.

The advantages of the SOI technologies in general an SIMOX in particular are :

- the devices show reduced leakage currents because no more reversed biased junctions exist with the substrate,
- many of the parasitic capacitances to the substrate disappear,
- components can be set at smaller distances to each other because no mutual disturbance will occur across the substrate,
- latchup does not occur in SOI chips as parasitic *pnpn*-paths are eliminated,
- parasitic field effect transistors which are highly radiation sensitive also disappear,

[4]This can be increased by having longer implantation times. Typically 8 hours are needed to produce 25 6 inch wafers.

- higher radiation resistance is obtained mainly because the volume where carrier generation can occur is not any more the whole bulk but only the devices thickness ($\sim 100\,nm$).

Both the lower parasitic capacitances and the smaller size as well as the smaller distance between the devices make larger speeds possible though this is incompatible with large power supply values for wide dynamic range.

A further increase in speed is possible by decreasing to a minimum ($\sim 150\,nm$) the thickness of the active silicon surface. This makes fully depleted devices and the gate channel is exclusively controlled by the gate voltage. This very thin silicon is also necessary to prevent a kink appearing in the saturation zone of the characteristic curves of transistors made with SOI techniques which destroys nice continuous properties.

Prototypes of pipelines following the ZEUS design and others will soon be produced in SIMOX technology.

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For all the errors which might have remained in this thesis I would plead the reader for patience.

Summary

The electron-proton storage ring complex HERA under construction at DESY in Hamburg is the first machine of a new generation of colliders. Not only it is the first lepton-quark collider to be built and needs two magnetic rings, one of them superconducting, to store the particles but also in order to obtain a high luminosity the beams can collide every 96 *nanoseconds*.

This has important consequences for the detector readout. No reasonable event selection can be performed in between two bunch crossings and thus all the detectors' signals have to be stored until the trigger process is finished. The readout has to be pipelined.

Since physics to be studied at HERA (covered in chapter 2) base on the precise measurement of kinematic variables over a very large range of energies, a foremost emphasis is set in calorimetry.

After long studies and an ambitious test program, the ZEUS collaboration has built a high resolution depleted uranium-scintillator calorimeter with photomultiplier readout, the state of the art in detectors of this type. In chapter 3 the principles of calorimetry are reviewed and the construction of the ZEUS calorimeter is described.

Mainly due to the large dynamic range and the short bunch crossing times a novel concept for the readout in an analog pipelined fashion had to be designed. This concept is explained in chapter 4.

The solid state implementation of the pipeline required two integrated circuits which were developed specially for the ZEUS calorimeter in collaboration with an electronics research institute and produced by industry. The design and construction of these devices and the detailed testing which has been performed for properties critical in the readout is covered in chapters 5 and 6.

The whole pipelined readout is a complicated setup with many steps and collaborating systems. Its implementation and the information to operate it are covered in chapter 7.

Finally the concepts presented and the applications discussed have been installed and tested on a test beam calibration experiment. There, the modules of the calorimeter have been calibrated. Chapter 8 presents results from these measurements which show excellent performance of the electronics as well as optimal properties of the calorimeter modules.

As a last comment, the electronics of ZEUS is the first one to cope with such a large number of channels and operate in the *nanosecond* range. However detectors being planned will have similar characteristics though with much harder requirements. An appendix shows the state of the development of analog pipelining, probably the only solution for the readout of the next generation of calorimeters.

Resumen

El sistema de anillos de acumulación HERA, actualmente en construcción en DESY, Hamburgo, es la primera máquina de una nueva generación de acceleradores de partículas. Además de ser el primer colisionador leptón-quark y usar dos anillos magneticos de almacenamineto, unos de los cuales es superconductor, para almacenar las partículas, tiene también un tiempo de cruce de los haces de 96 *nanosegundos* lo cual permite obtener una gran luminosidad.

Este hecho tiene importantes consecuencias para la lectura de los detectores. No es posible realizar una selección razonable de sucesos entre dos cruces de los haces y por lo tanto es necesario almacenar todas las señales de los detectores hasta que el proceso de trigger haya terminado. Es una lectura con almacenamiento.

Puesto que la física que se va a estudiar en HERA (descrita en el capítulo 2) se basa en la medida muy precisa de las variables cinemáticas a través de un amplio rango de energías, la experimentación pone un especial énfasis en calorimetría.

Tras largos estudios y programas experimentales, la colaboración ZEUS ha construido un calorímetro de uranio empobrecido y centelleador con lectura por phototubos que es el más moderno de este tipo de detectores. Los principios de calorimetría y la construcción del calorímetro de ZEUS están explicados en el capítuo 3.

Debido principalmente al amplio rango dinámico de energías y al breve tiempo entre collisiones, ha sido necesario desarrollar un nuevo concepto para realizar la lectura analógica con almacenamiento. El capítulo 4 describe este concepto..

La realización en estado sólido de la unidad de almacenamiento necesita dos circuitos integrados que han sido desarrollados especialmente para el calorímetro de ZEUS en colaboración con un instituto de investigación de electrónica y han sido producidos por la industria. Los capítulos 5 y 6 cubren el diseño y construcción de estos circuitos asi como las pruebas realizadas de las propiedades que pudieran ser críticas para la lectura.

El conjunto del equipo de lectura con almacenamiento es un sistema complejo con muchas partes y procesos cooperantes. El capítulo 7 explica su realización y da la información necesaria para hacerlo operativo.

Finalmente se han instalado y probado los conceptos y las aplicaciones de lectura en un experimento de calibración con haz de partículas. Este experimento ha servido para calibrar los módulos del calorímetro. Los resultados de estas medidas están en el capítulo 8 y muestran el excelente funcionamiento de la electrónica y las óptimas propiedades de los módulos.

Como comentario final, la electrónica de ZEUS es la primera que tiene que leer un tal número de canales en tiempos de *nanosegundos*. Sin embargo los nuevos detectores que ya se están planenando tendrán características similares aunque con requisitos mucho más rigurosos. Un apéndice cubre el desarrollo actual de los almacenamientos analógicos que probablemente serán la única solución para la lectura de calorimetros.