Internal Report
DESY F35D-93-02
January 1993

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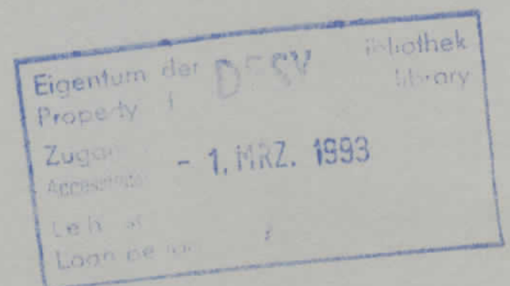

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**28 January 1993**

This doctoral dissertation is to be presented at the Faculty of Physics and Nuclear Technique, Academy of Mining and Metallurgy in Cracow.
The work described in this thesis has been carried out at the Deutsches Elektronen-Synchrotron, DESY in Hamburg in the frame of collaboration with ZEUS. Over the period of his stay at DESY the author was financially supported by DESY.

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# List of symbols

$a$ Slope of a straight line (obtained from linear regression method).
$A$ Constant in the formula for $1/f$ noise..
$A_0$ Open loop gain.
$A_i$ Ionization constant.
$a_n$ Amplitude of $n$-th term of Fourier's series ($\equiv \frac{1}{T}\int_0^T x(t)\exp(-j\omega_n t)dt$).
$A(\tau)$ Autocorrelation function of the voltage fluctuation.
$\alpha$ Sun-Plummer parameter.
$\alpha^*$ Relative Sun-Plummer parameter ($\equiv \alpha\frac{\Delta N_{it}}{\Delta V_{it}}$).
$\alpha(\mathcal{E}_h)$ Ionization rate for the weak impact ionization ($\equiv A_i\exp(-\frac{B_i}{\mathcal{E}_h})$).
$\alpha_H$ Hooge's constant.
$\alpha_{Hl}$ Hooge's constant for $1/f$ noise in lattice scattering.
$b$ $y$-intercept of straight line (obtained from linear regression method).
$b_n$ Amplitude of $n$-th term of Fourier's series.
$B_i$ Ionization constant.
$\beta$ Transconductance or gain factor ($\equiv \mu_n C_{ox}\frac{W}{L}$).
$C$ Constant.
$C_B$ Constant impurity concentration deep in the substrate.
$C_D$ Depletion region capacitance.
$C_{eff}$ Effective gate capacitance.
$C_{inv}$ Inversion layer capacitance.
$C_{it}$ Interface states capacitance.
$C_{ox}$ Gate oxide capacitance ($\equiv \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{ox}}$).
$\chi$ Electron affinity in silicon ($\equiv E_0 - E_C^{Si}$).
$D$ Radiation dose.
$D_{bt}$ Density of border states per unit area per eV.
$D_{it}$ Density of interface states per unit area per eV.
$D_{itA}$ Density of acceptor interface states.
$D_{itD}$ Density of donor interface states.
$D_{n,p}$ Diffusion constant; the index $n$ denotes the electrons in NMOSFET and $p$ - holes in PMOSFET ($\equiv \mu_n V_t$, Einstein's relation).
$D_{ot}$ Density of oxide states per unit area per eV.
$d(\tau)$ Distribution of the border traps with respect to the time constant $\tau$.
$\delta$ Inversion layer thickness.
$\delta$ Factor of the first order correction in the Taylor's expansion of the depletion region charge.
$\delta V_\mu$ Voltage fluctuation due to mobility fluctuation.
$\delta V_n$ Voltage fluctuation due to carrier number fluctuation.





$\delta X$ Fluctuation of quantity $X$ (for example $X = N_t, I_{DS}, ...$).
$\Delta X$ Change of quantity $X$ (for example $X = V_{th}, V_{ot}, N_{ot}, ...$).
$E$ Energy of the carriers in the silicon or in the oxide.
$E$ Energy of the ionizing radiation.
$E_0$ Energy of vacuum level.
$E_C^{ox}$ Oxide conduction band edge.
$E_C^{Si}$ Silicon conduction band edge.
$\overline{E}_e$ Average energy of secondary electrons created by Compton scattering of the photons.
$E_F$ Fermi energy level.
$E_{FM}$ Energy of metal Fermi level.
$E_{F_n}$ Electron quasi-Fermi level.
$E_g$ Silicon bandgap energy.
$E_g^{ox}$ Oxide bandgap energy.
$E_i$ Intrinsic energy level.
$E_V^{ox}$ Oxide valence band edge.
$E_V^{Si}$ Silicon valence band edge.
$\mathcal{E}_h$ Horizontal channel field.
$\mathcal{E}_{hd}$ Horizontal electric field in the drain space charge region.
$\mathcal{E}_{hs}$ Critical horizontal field for the velocity saturation.
$\mathcal{E}_s$ Normal electric field at the silicon surface.
$\mathcal{E}_{crit}$ Critical normal field.
$\mathcal{E}_{eff}$ Effective normal field.
$\mathcal{E}_{ox}$ Effective normal field in the oxide.
$\epsilon$ Characteristic trapping distance into the oxide.
$\varepsilon_{av}$ Average dielectric constant of $Si$ and $SiO_2$ ($\equiv \frac{1}{2}(\varepsilon_{Si} + \varepsilon_{SiO_2})$).
$\varepsilon_0$ Permittivity of free space.
$\varepsilon_{Si}$ Dielectric constant of silicon.
$\varepsilon_{SiO_2}$ Dielectric constant of silicon dioxide.
$\eta_{n,p}$ Relative mobility degradation ($\equiv \frac{\mu_{n,p\ before} - \mu_{n,p\ after}}{\mu_{n,p\ after}}$); the index $n$ denotes the electrons in NMOSFET and $p$ - holes in PMOSFET.
$\frac{dE}{dx}$ Stopping power.
$f$ Frequency.
$f$ Kink effect parameter.
$f_0$ Open loop cut-off frequency.
$F_A(\psi)$ Fermi-Dirac distribution for acceptors.
$F_D(\psi)$ Fermi-Dirac distribution for donors.
$f_h$ High limit frequency.
$f_l$ Low limit frequency.
$f_t$ Fractional occupancy.
$f_T$ Fraction of the radiation-induced holes which are trapped in the oxide.
$f(\psi_s)$ Function used for short notation the accurate equation modelling the MOS transistor characteristic in the strong inversion region.
$\phi_B$ Fermi energy level measured with respect to the midgap level deep in the substrate (under depletion region where the bands are not bended).
$\phi_G$ (similar to $\phi_B$ but for polysilicon gate electrode, ($\equiv V_t\ln\frac{N_{GATE}}{n_i}$).

$\Phi_{GB}$ Difference between the work functions of silicon substrate and gate electrode material.
$\Phi_M$ Work function of metal ($\equiv E_0 - E_{FM}$).
$\Phi_{SC}$ Work function of silicon.
$G$ Conductance.
$g(N_t)$ Function describing the generation of carriers.
$g(y) = g(V)$ Conductance per unit length of the channel at the distance $y$ from source.
$g_d$ Drain conductance.
$g_m$ Transconductance.
$\gamma$ Body effect coefficient ($\equiv \frac{\sqrt{2\varepsilon_{Si}\varepsilon_0 q N_A}}{C_{ox}}$).
$\gamma$ Frequency exponent.
$h$ Plank's constant.
$\hbar$ Plank's constant ($\equiv \frac{h}{2\pi}$).
$h(t)$ Noise extortion.
I Current.
$I_{BS}$ Current through the source-to-body diode.
$i_d$ Instantaneous value of the current noise of transistor channel.
$I_{DB}$ Current through the drain-to-body diode.
$I_{DS}$ Drain current.
$I_{DSmax}$ Maximal drain current at fixed gate voltage in the subthreshold range ($\equiv \beta C_D(\psi_s)\frac{n}{m}V_t^2\exp(\frac{V_{GS}-V_{GS}^*}{nV_t})$).
$I_{DSsat}$ Saturation drain current.
$I_{II}$ Impact ionization current.
$I_{mg}$ Midgap current ($\psi_s = \phi_B$).
$i_n$ Instantaneous value of the current input noise of amplifier.
$I_S$ Current measured in the source of the transistor.
$I_{th}$ Threshold current ($\psi_s = 2\phi_B$).
$I_{TR}$ Current through the front transistor channel.
$I_w$ Current measured in the $n$-well.
$k$ Boltzman's constant.
$K$ Constant ($\equiv V_t^2\exp(-\frac{2\phi_B}{V_t})[1-\exp(-\frac{V_{DS}}{V_t})]$).
$K$ Noise level of the drain current flicker noise.
$K_v$ Noise level normalized with respect to the drain $V_{DS}$ and threshold $V_{th}$ voltages($\equiv KR^2\left(\frac{V_{GS}-V_{th}-V_{DS}}{V_{DS}}\right)^2$).
$\kappa$ ($\equiv \frac{m}{n}\frac{V_{DS}}{V_t}$).
$L$ Nominal gate length.
$L_B$ Extrinsic Debeye length ($\equiv \sqrt{\frac{\varepsilon_{Si}\varepsilon_0 V_t}{qN_A}}$).
$L_e$ Pinch-off point distance from source.
$L_{eff}$ Effective gate length.
$L^m(p)$ Polynomial of m-degree.
$\lambda$ Characteristic length of hole trapping process.
$\lambda$ Mean separation between e-h pairs.
$\lambda$ Characteristic length for channel length modulation.
$\lambda_{eff}$ Effective mean free path.
$m$ ($\equiv \frac{C_{ox}+C_D(\frac{3}{2}\phi_B)}{C_{ox}}$).
$M$ Multiplication factor.



$m_{Si}$ Electron effective mass in the silicon.
$m_{SiO_2}$ Electron effective mass in the silicon dioxide.
$\mu$ Mobility.
$\mu_0$ Low field mobility.
$\mu_{1/f}$ Flicker noise mobility ($\equiv \frac{\mu^3}{\mu_l^2}$).
$\mu_{after}$ Mobility after irradiation.
$\mu_{before}$ Mobility before irradiation.
$\mu_{e-e}$ Mobility due to electron-electron scattering.
$\mu_{eff}$ Effective mobility.
$\mu_i$ Mobility due to impurity scattering.
$\mu_{il}$ Mobility due to phonon and impurity scattering.
$\mu_l$ Mobility due to lattice scattering.
$\mu_s$ Mobility due to surface scattering.
$\mu_{SR}$ Surface roughness mobility.
$\mu_{VS}$ Velocity saturation mobility.
$\mu_n(x,y)$ Electron mobility in the channel.
$\mu_{n,p}$ Mobility; the index $n$ denotes the electrons in NMOSFET and $p$ - holes in PMOSFET.
$n$ Oxide thickness exponent in the relationship between radiation-induced threshold voltage shift and the oxide thickness.
$n$ Inverse subthreshold slope ($\equiv 1 + \frac{C_D(\frac{3}{2}\phi_B)+C_{it}(\frac{3}{2}\phi_B)}{C_{ox}}$).
$N$ Total number of free charge carriers.
$N_0$ Initial value of $N_{e-h}$ ($t = 0$).
$N_A$ Acceptor doping concentration in the $p$-type substrate.
$n_{bt}$ Density of border states per unit volume per eV.
$N_{bt}$ Number of border traps.
$n_c$ Surface density of free carriers.
$N_{e-h}$ Number of e-h pairs which avoid recombination.
$N_{GATE}$ Doping of polysilicon gate electrode.
$n_i$ Intrinsic carrier concentration for silicon.
$N_I$ Sum of all charges in the oxide at zero band-bending ($\psi_s = 0$).
$N_{it}$ Number of interface states.
$N_{ot}$ Number of holes trapped in the oxide.
$n_s$ Electron concentration at the surface of $p$-type semiconductor.
$N_s$ Number of carriers in the interface states.
$N_{s0}$ $N_s$ in the equilibrium state.
$n_t$ Surface density of carriers captured in the border traps.
$N_t$ Number of carriers captured in the border traps.
$N_{t0}$ $N_t$ in the equilibrium state.
$N_T$ Density of hole traps.
$n(x,y)$ Density of free electrons in the channel.
$\nu$ Radiation frequency.
$\omega$ Angular frequency ($\equiv 2\pi f$).
$\omega_n$ ($\equiv \frac{2\pi n}{T}, n = 0, \pm1, \pm2, \ldots$).
$p$ Differential operator with respect to the time ($\equiv \frac{d}{dt}$).
$p_s$ Hole concentration at the surface of $p$-type semiconductor.
$\psi$ Potential at the interface measured with respect to the midgap level.

| | |
|---|---|
| $\psi_s$ | Surface potential. |
| $\psi_{s,inv}$ | Inversion surface potential ($\equiv 2\phi_B$). |
| $q$ | Electron charge. |
| $Q(E, \mathcal{E}_{ox}, D)$ | Radiation-induced charge density in the oxide. |
| $Q_{bt}$ | Border-trapped charge. |
| $Q_f$ | Fixed oxide charge. |
| $Q_D$ | Charge in the depletion region. |
| $Q_I$ | Charge in the inversion layer. |
| $Q_{it}$ | Interface-trapped charge. |
| $Q_{itFB}$ | Interface-trapped charge for flat band condition ($\psi_s = 0$). |
| $Q_m$ | Mobile ionic charge. |
| $Q_{ot}$ | Oxide-trapped charge. |
| $Q_S$ | Total charge in semiconductor ($\equiv Q_I + Q_D$). |
| $R$ | Resistance ($\equiv G^{-1}$). |
| $R$ | Resistance in the drain circuit ($\equiv \frac{R_D}{1+R_D g_d}$). |
| $R$ | Reimbold's factor. |
| $R_D$ | Load resistance. |
| $R_D$ | Drain region extrinsic resistance. |
| $R_G$ | Gate bias resistance. |
| $R_f$ | Feedback resistance. |
| $r(N_t)$ | Function describing the recombination of carriers. |
| $R_p$ | Projected range. |
| $R_S$ | Source region extrinsic resistance. |
| $S$ | Subthreshold swing. |
| $s$ | Time delay. |
| $S_{after}(I_{DS})$ | Subthreshold swing after irradiation in the function of the drain current. |
| $S_{before}(I_{DS})$ | Subthreshold swing before irradiation in the function of the drain current. |
| $S_G$ | Spectral density of the conductance fluctuations. |
| $S_g(f)$ | Spectral density of the generation function. |
| $S_{I_{DS}}$ | Spectral noise power density of the drain current. |
| $S_{N_t}$ | Power spectral density of the fluctuations of the number of trapped carriers. |
| $S_r(f)$ | Spectral density of the recombination function. |
| $S_{th}$ | Component independent of frequency representing the thermal noise of the system. |
| $S_{V_{DS}}$ | Spectral noise power density of the drain voltage. |
| $S_{v_{eq}}(f)$ | Equivalent noise power spectral density in the gate circuit. |
| $S_x(f)$ | Spectral density of the random process $X(t)$. |
| $\sigma$ | Capture cross section. |
| $\sigma$ | Cross section for the photoelectric effect. |
| $t$ | Time. |
| $T$ | Period. |
| $T$ | Temperature. |
| $t_b$ | Body thickness. |
| $t_c$ | Parameter describing inversion layer thickness ($\equiv \frac{\delta}{4}$). |
| $t_{ch}$ | Effective channel thickness ($\equiv \frac{V_t}{\mathcal{E}_s}$). |
| $t_{ox}$ | Oxide thickness. |



| | |
|---|---|
| $\tau$ | Time constant. |
| $\tau_0$ | The shortest time constant. |
| $\tau_1$ | The longest time constant belonging to traps placed in the highest distance $x_1$ from interface. |
| $\theta_c$ | Drain field reduction parameter. |
| $\theta_s$ | Gate field reduction parameter ($\equiv \frac{\varepsilon_{SiO_2}}{2\varepsilon_0 t_{ox} E_{crit}}$). |
| $\vartheta$ | Current exponent in the formula for $1/f$ noise. |
| $u$ | Parameter in the complete approximate strong inversion model. |
| $v$ | Parameter in the function describing the mobility profile in the inversion layer ($\equiv 2\lambda_{eff}$). |
| $V_{DS}$ | Drain-source voltage. |
| $V_{DSsat}$ | Saturation drain voltage. |
| $V_{DSsatI}$ | Intrinsic drain saturation voltage. |
| $V_{FB}$ | Flat-band voltage. |
| $V_{GB}$ | Gate-bulk voltage. |
| $V_{GS}$ | Gate-source voltage. |
| $V_{GS}^*$ | Gate voltage at $\psi_s = \frac{3}{2}\phi_B$. |
| $V_{it}$ | Interface charge component of the threshold voltage. |
| $V_k$ | Kink voltage. |
| $V_L$ | ($\equiv F_s L_{eff}$). |
| $V_\lambda$ | ($\equiv \mathcal{E}_{hs}\lambda$). |
| $V_{mg}$ | Midgap voltage. |
| $v_n$ | Instantaneous value of the voltage input noise of amplifier. |
| $v_o$ | Instantaneous value of the output voltage of preamplifier. |
| $V_{ot}$ | Oxide charge component of the threshold voltage. |
| $V_{SB}$ | Source-bulk voltage. |
| $V_t$ | Thermal voltage ($\equiv \frac{kT}{q}$). |
| $V_{th}$ | Threshold voltage. |
| $V_{th\mu}$ | Mobility degradation component of threshold voltage. |
| $V_w$ | $n$-well voltage. |
| $V(y)$ | Channel potential at the point at the distance $y$ from source. |
| $W$ | Nominal gate width. |
| $W_{eff}$ | Effective gate width. |
| $x$ | Coordinate perpendicular to the surface of the interface between $SiO_2$ and $Si$. |
| $x_1$ | Maximal tunneling distance into the oxide. |
| $x_{d,max}$ | Maximum depletion width. |
| $x(t)$ | Noise response at the output of system. |
| $X(t)$ | Random process. |
| $\xi$ | Emission probability from the border trap to the interface state. |
| $y$ | Coordinate along the length of transistor channel from source to drain. |
| $Y$ | Fractional yield ($\equiv \frac{N_{e-h}}{N_0}$). |
| $\upsilon$ | Constant. |
| $z$ | Coordinate along the width of transistor channel. |
| $Z$ | Atomic number. |
| $\zeta$ | Capture probability at the border trap from the interface state. |

# Chapter 1

# Introduction

The radiation hardness of electronics has recently become a very important issue not only in military and space applications, but also in large experiments of high energy physics which are carried out in order to understand the most fundamental structures of matter. It concerns the semiconductor detectors used in these experiments and the VLSI technologies used to construct readout electronics. ASIC components have proved very useful in building fast analog front-end electronics coupled to big systems of radiation detectors needed in these experiments to observe what happens in elementary particle collisions. The front-end electronics systems (preamplifiers, comparators, analog memories, buffers, pipelines, analog-to-digital converters) must be mounted very close to detectors to avoid many long cables for the transmission of analog signals. The silicon VLSI technologies are very beneficial to solving such problems. However, these systems are exposed to radiation to a significant level. Therefore the choice of more radiation tolerant silicon devices to construct such electronic systems is necessary. This study aims at providing arguments to make this choice possible.

The work presented here is the result of study carried out by the author during his work in the ZEUS detector group at DESY in Hamburg. During that time several other reports dedicated to the same goal and prepared by the author's co-workers were published at DESY [5, 6, 7, 8]. The results were also presented at the conferences [9, 10].

The main part of the ZEUS experiment is high resolution uranium sampling calorimeter surrounding the pipe of the HERA collider near the e-p interaction point. This calorimeter consists of 10 000 depleted uranium plates separated by 240 000 scintillator tiles. The uranium plates and scintillator tiles form the so-called "sandwich" structure, where alternate layers perform a stepwise process of shower development and signal generation. The light leaving the scintillator tiles is collected by sheets of a plastic wave length shifter which transports the light. Then, this optical signal is directed to the light sensitive cathodes of phototubes. In this way, the energy deposited in the calorimeter results in a current signal of the photomultipliers anodes. This analog electrical signal is directed to the analog front-end card which consists mainly of two ASIC chips: a pipeline and a buffer-multiplexer. The signal at the analog card is triggered to eliminate signals which are non-interesting for physics. After





leaving the front-end electronics the information from calorimeter has to be digitized and filtered. The total construction weights c. a. 700 tons and has 12 000 readout channels.

The pipelining and buffering is realized by means of switched-capacitor technique. The pipeline chip stores the sampled data of the preceding $5\mu s$ (for a sampling rate 10.4 $MHz$; a memory depth of 58 cells has been chosen). The second stage of the pipeline system consists of a buffer storage, which is similar to the main pipeline channels. The third stage is an analog multiplexer, which is capable of switching 12 buffered and one unbuffered (stand-by) channels to one output and a further 12 unbuffered channels to a second output [1, 2]. These two stages are integrated on one chip.

In order to fabricate these two chips the MOS technology has been chosen due to the following advantages. The fabrication process is simple, well known and cheap in comparison with bipolar and BiMOS technologies. A very high integration of devices and very low power consumption can be achieved. The switched-capacitor technique needs a lot of capacitors and switches and MOS technology is very good one for integrating capacitors and switches. MOS transistors make one of the best switch available in integrated-circuit form. They require little area, dissipate very little power, and provide reasonable values of $R_{ON}$ (range from several $k\Omega$ to 100 $\Omega$) and $R_{OFF}$ ($\approx 10^{12}\ \Omega$) [3]. Although MOS transistors exhibit very large 1/f low frequency noise, in the range of high frequency (above mentioned 10.4 $MHz$) a noise problem does not appear. The combination of analog and digital circuits on one chip does not create any additional problems.

One of the most important problems which should be solved for such applications of MOS technology is that of radiation hardness. The dose rate due to synchrotron radiation at the position of the calorimeter or its electronics should everywhere be smaller then 1 $krad/year$. Only in some places, very close to the beam pipe, the dose rate could be $\approx$ 10 $krad/year$. The dose rate due to high energy neutrons is estimated on the level of 60 $rad/year$ [4]. The neutron radiation is dangerous only for junction devices with respect to creation of atomic displacements in the crystal lattices caused by the collisions of fast neutrons with silicon atoms. For MOS transistors this kind of radiation effects is not very important because electrical current flows only in a very thin surface layer of silicon under gate oxide. The second kind of radiation damages are ionization effects which are caused mainly by photonic radiation like x-ray, $\gamma$ or synchrotron radiation. Radiation passing the insulator generates charges which influence the electrical characteristics of the transistor.

The necessity of undertaking the study presented here appeared while testing several technologies which application in the fabrication of the two analog chips described above had been planned. The main task of this study is to examine ionizing effects in MOS transistors in their physical, technological and measuring aspects. The results of the measurements carried out are related to several MOSFET parameters: threshold voltage $V_{th}$, transconductance $g_m$, subthreshold swing $S$ and spectral noise power density of drain current $S_{I_{DS}}(f)$. However, the most visible radiation effect of tested technologies is the distortion of the subthreshold characteristic due to leakage currents. A great deal of attention is focused on the radiation behaviour of the kink

effect in a SOI technology.

The test procedure used here consists in the subsequent irradiations and measurements of test structures. For irradiation the $Cs^{137}$ source of activity $A = 5Ci$ and energy of $\gamma$ quants $E_\gamma = 661 keV$ was used. A homemade system was constructed for measurements [5]. It was controlled by VME-137 computer running under program written in C language. One part of results was obtained by means of using a semiconductor parameter analyzer a HP4145B. The noise measurements were taken by a dynamic signal analyzer a HP3561A. For data acquisition a standard GPIB interface between instruments and a computer was adopted.

The dose rate used while irradiating test structures was $\approx 2.9\ krad/h$ and it allowed the achievement of a total absorbed dose at the level of 200 $krad$ during several days of irradiation. Such a dose highly exceeded the one predicted for the ZEUS detector. On the other hand, the total doses that were used were very low in comparison with modern requirements for future high energy physics experiments at the LHC or SSC: 10 $Mrad$. Such requirements for a total dose are far larger than those for space applications (100 $krad$) and defence applications ($0.1 \div 1\ Mrad$). The dose rate used in another similar study at CERN [12] reached $\approx 290\ krad/h$.

In comparison with the total dose values mentioned above, the predictions for the ZEUS detector are relatively small. Therefore, the electronic technologies dedicated for ZEUS are standard, not hardened processes developed by IMEC, ELMOS and FhG IMS. The results obtained from irradiations and measurements of these technologies are presented in this study.

The amount of the data gathered was so large that only a small part of it can be presented here. Particular attention was paid to the SOI technology because it is a newer version of a modern MOS technology which is still being developed. All graphs demonstrated here are the result of original measurements obtained by the author unless stated otherwise.

Chapter 2. describes shortly the structure and parameters of a MOS transistor. Commonly used models of a MOS transistor operating in above- and sub-threshold regions are presented in appendices. Typical process flows of MOS bulk and SOI technology are discussed in chapter 3. A great deal of attention is paid to technological details because this subject has not been consider in previous publications at DESY. Each technological step is illustrated by process parameters used at the Fraunhofer Institute in Duisburg. These parameters are: implantation energy, dose of implanted dopants, oxidation temperature, annealing temperature, oxidation time, annealing time, thickness of layers, composition of oxidation atmosphere, velocity of gas flow, concentrations of dopants, resistivity of layers and others. This review of technology gives opportunity for understanding the influence of technological parameters on radiation sensitivity. Therefore this chapter also contains a review of technological efforts undertaken to improve the radiation hardness which are presented in many articles. The next chapter deals with the physical mechanisms of creation of radiation damages in silicon dioxide. It contains also the presentation of the results obtained for electrical MOSFET parameters. The most important MOSFET parameter which was studied in the function of $\gamma$ dose is the threshold voltage. The radiation-induced change of transconductance as a parameter $\beta$ of model equation and as a maximal



value $g_{m,max}$ in the linear range of transistor operation was also observed. The methods of separation of two components of threshold voltage caused by oxide charge and interface charge are presented and illustrated by original measurement data. The results of the SOI transistors concern various transistor structures and bias conditions and the back gate parasitic transistor. The changes of the kink effect point and the parameter $f$ describing the kink effect were observed for $n$- and $p$-channel transistors. The results concerning noise properties of irradiated MOSFETs are presented in chapter 5. together with a review of flicker noise theory. The changes of noise power spectrum caused by irradiation were observed. Three parameters of noise spectrum: the noise level, the frequency exponent and the thermal noise component were fitted.

# Chapter 2

# Ideal and nonideal MOS structure

A MOS structure (Fig. 2.1) consists of three subsequent stacked layers:

- a gate electrode made of a conductor like Al or *p*- or *n*-type poly-Si;
- an insulator separating the upper conducting layer from the semiconductor below made of silicon dioxide $SiO_2$, silicon nitride $SiN_3$ or a nitride/oxide double-layer;
- a semiconductor substrate made of *p*- or *n*-type crystalline silicon $Si$.

This means that the two most important materials are $Si$ and $SiO_2$. The table below (Tab. 2.1) summarizes the electrical and physical parameters of these two materials.

Idealized MOS n-channel transistor structures for bulk and SOI version are shown on Fig. 2.1. The band diagram for such structures near the source area where $V(y) = 0$ is shown on Fig. 2.2. The radiation effects are related to nonidealities present in the oxide layers. We can distinguish three types of oxide layers:

**gate-oxide** - a thin ($40 \div 15$ $nm$) $SiO_2$ layer between the gate electrode and the transistor channel, covering the area $W \times L$, fabricated by the thermal oxidation of the silicon layer;

**field-oxide** - a thick ($500 \div 1000$ $nm$) $SiO_2$ layer covering the whole silicon area not occupied by active devices; fabricated by thermal oxidation (LOCOS) or chemical vapour deposition; the task of such a layer is the lateral separation of adjacent devices;

**buried-oxide** - a thick ($150 \div 500$ $nm$) $SiO_2$ layer separating a device body from the substrate in a vertical direction, fabricated by oxygen ion implantation into the silicon wafer (SIMOX); used only in SOI technologies.

The nonidealities are charges and electronic states which exist in the oxide and at the $Si - SiO_2$ interface. The standard classification and terminology for them proposed in 1980 by Deal committee [17] and supplemented recently by Fleetwood [18] is presented in Fig. 2.3. In general, these charges can be split in two groups. The charges of the first type ($Q_{ot}, Q_f$) cannot interact with free carriers existing in the underlying silicon, but the charges of the second type ($Q_{it}, Q_{bt}$) are in an electrical communication with the silicon and can be charged or discharged, depending on the surface potential. Such electron states show acceptor or donor properties. Donor states are positively charged when empty (above Fermi level), and neutral when filled





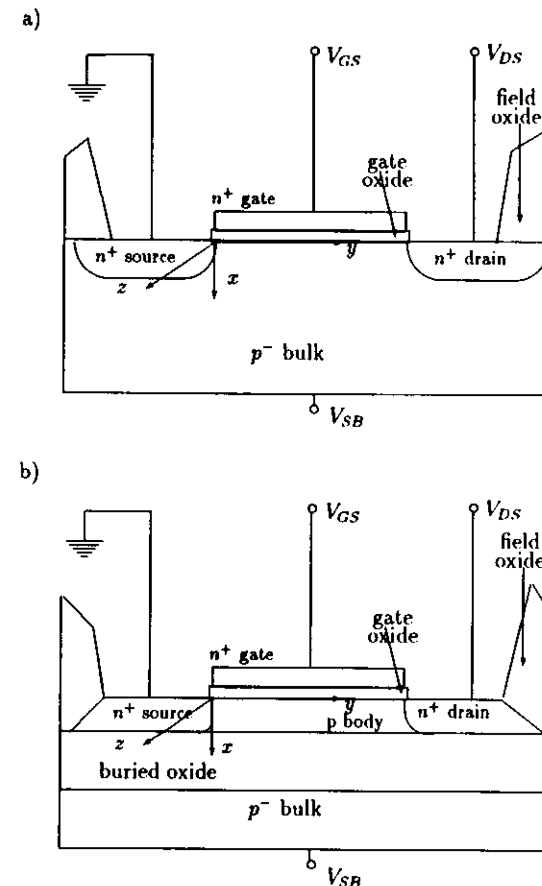


Figure 2.1: The ideal MOS n-channel transistor structure: a) bulk technology, b) SOI technology.

Table 2.1: Properties of intrinsic silicon $Si$ and silicon dioxide $SiO_2$.
All other values without references are given according to [13].
If in the table below only one value is given, it means that this value was measured at a temperature of 300°K.
If a range is given, it indicates that the quantity is temperature and field dependent in the specified range.

| Material | $Si$ | $SiO_2$ |
|---|---|---|
| Type | Semiconductor | Insulator |
| Crystal structure | Diamond<br>8 atoms<br>per unit cell | Random tetrahedra<br>1 $Si$ and 4 $O$ atoms<br>per unit cell [14] |
| Atomic/molecular weight | 28.09 | 60.08 |
| Atomic/molecular density ($10^{22} cm^{-3}$) | 5.0 | 2.3 |
| Lattice constant (A) | 5.43 | 5.03 |
| Spacing to the nearest neighbour (A) | 2.35 (Si-Si) | 1.62 (Si-O)<br>2.62 (O-O)<br>3.12 (Si-Si) [14] |
| Density ($gcm^{-3}$) | 2.33 | 2.27 |
| Work function $\Phi$ (eV) | 4.1-5.2 | — |
| Electron affinity $\chi$ (eV) | 4.1 | 0.9 |
| Band gap energy $E_g$ (eV) | 1.11 | 8.5 |
| Hole-electron pair generation energy $E_i$ ($eV$) | 3.6 | 17.0±1 |
| Effective density of ($10^{19} cm^{-3}$)<br>- states in conduction band $N_c$<br>- states in valence band $N_v$ | <br>2.80<br>1.04 | <br>—<br>— |
| Intrinsic carrier concentration $n_i$ ($10^{10} cm^{-3}$) | 1.483 | — |
| Diffusion coefficient of ($cm^2 s^{-1}$)<br>- electrons $D_n$<br>- holes $D_p$ | <br>35.0<br>12.5 | |
| Mobility of<br>- electrons $\mu_n$ ($cm^2 V^{-1} s^{-1}$)<br>- holes $\mu_p$ ($cm^2 V^{-1} s^{-1}$) | <br>1350<br>480 | <br>20÷40 [15]<br>$10^{-4} \div 10^{-11}$ [15] |
| Dielectric constant $\varepsilon$ | 11.7 | 3.9 |
| Dielectric permittivity $\varepsilon\varepsilon_0$ ($10^{11} Fcm^{-1}$) | 0.104 | 0.0345 |
| Breakdown field ($V/\mu m$) | 30 | 600 |
| Melting point (°$C$) | 1415 | 1650 |
| Vapour pressure (torr), at temp. (°$C$) | $10^{-7}$, 1050<br>$10^{-5}$, 1250 | $10^{-3}$, 1450<br>$10^{-1}$, 1750 |
| Specific heat $C_h$ ($J/g°C$) | 0.70 | 1.0 |
| Thermal conductivity $K_{th}$ ($W/cm°C$) | 1.5 | 0.014 |



(Continuation of table 2.1.)

| Material | $Si$ | $SiO_2$ |
|---|---|---|
| Thermal diffusivity $\kappa$ ($cm^2/s$) | 0.9 | 0.006 |
| Linear coefficient of thermal expansion $\Delta L/L\Delta T$ ($10^{-6}/°C$) | 2.5 | 0.5 |
| Effective mass $m^*/m_0$ for<br>- electrons<br>- holes | <br>$m_l^*$=0.97; $m_t^*$=0.19 [16]<br>$m_{lh}^*$=0.16; $m_{hh}^*$=0.5 [16] | <br>—<br>— |
| Stopping power for 1-MeV electrons $dE/dx$ ($MeVg^{-1}cm^2$; $pairs/cm$) | | 1.6; $2\times10^5$ [15] |

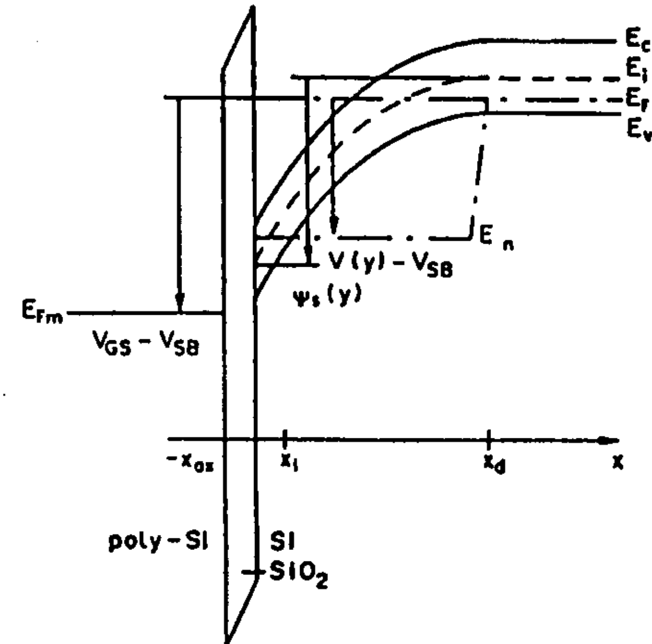


Figure 2.2: The band diagram of an ideal MOS n-channel transistor.

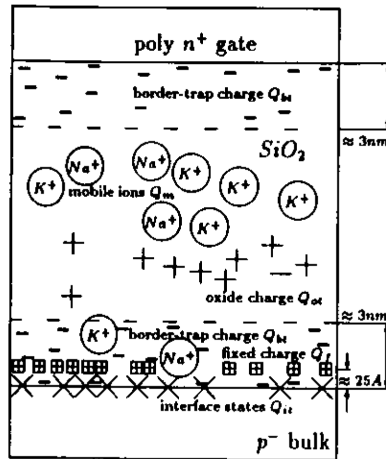


Figure 2.3: The classification of localized electronic state and charges in a MOS transistor structure.

with an electron (below Fermi level). On the contrary, acceptor states are neutral when empty, and negatively charged after having been filled with an electron.

The following charges are distinguished:

$Q_{ot}$ - oxide-trapped charges caused by holes and electrons trapped in the bulk of the oxide; this kind of the charge is mainly positive because of great difference between hole and electron mobilities in $SiO_2$ (see Tab. 2.1). The holes are almost immobile whereas the electrons are swept out of the oxide very rapidly (in a few ps). Then, the trapping of electrons is negligible;

$Q_m$ - mobile ionic charges caused by those ionic impurities such as $Li^+, Na^+, K^+$ and possibly $K^+$ present in the bulk of the oxide and which can move under thermal and electrical stresses. Negative ions and heavy metals are not mobile at low temperature;

$Q_f$ - fixed oxide charges which are structural defects in the oxide layer, located within ≈25 A of the $Si - Si0_2$ interface. The density of this charge, whose origin is related to the oxidation process, depends on the oxidation ambient, temperature, cooling conditions, and on the silicon orientation. After the oxidation process, some ionic silicon is left near the interface. Such an excess silicon should give rise to fixed oxide charges (Deal's model). Typical density of $Q_f$ for $< 100 >$-oriented silicon is $10^{10} cm^{-2}$ and for $< 111 >$ surface, $Q_f$ is about $5 \times 10^{11} cm^{-2}$. Commonly, this kind of charge has been always considered as a positive charge. Recently, the negative fixed interface charge $N_{fit}$ has been found in MOS capacitors processed without postoxidation annealing [19];

$Q_{it}$ - interface-trapped charges caused by holes and electrons captured by trapping centres located on the oxide-semiconductor interface. Typical density of $Q_{it}$ for



$< 100 >$-oriented silicon is $10^{10} cm^{-2}$ (about one interface trap per $10^5$ surface atoms) and for $< 111 >$-oriented silicon, $Q_{it}$ is about $10^{11} cm^{-2}$.

$Q_{bt}$ - border-trapped charges caused by holes and electrons trapped by near-interfacial traps in oxide. These border traps are in electrical communication with the silicon substrate but they lie not directly at the interface but within a distance of $\approx 3\ nm$ from the $SiO_2$ interface. They provide also donor and acceptor levels for free carriers from the transistor channel but with time constant longer than that for interface states (up to 1 min). The communication mechanism between border traps and free carriers in the silicon is tunneling. The necessity of distinguishing of such a kind of traps is especially acute in the $1/f$ noise literature (see chapter 5). A very interesting consequence of the concept of border traps is that there are no oxide traps $Q_{ot}$ in the oxides thiner than 6 $nm$ and all traps can act as border traps.

The annealing properties of two kinds of charges $Q_{ot}$, $Q_{it}$ are very important from the radiation hardness point of view. The radiation-generated interface traps do not anneal causing so called rebound effect [24]. The rebound is the recovery of an $n$-channel device past its preirradiation threshold voltage and results when radiation-induced trapped holes in the oxide bulk are annealed (at late times or at low dose rates) leaving only uncompensated interface traps. Because the rebound occurs in a positive voltage direction increasing the threshold voltage over its preirradiation value, the interface traps must contribute a net negative charge and therefore are postulated to be acceptors. It is evident that the annealing behaviour can be used for distinguishing two kinds of charges and for determining the acceptor or donor type interface states.

The physical nature and origin of these charges have been intensely studied for many years. A lot of information concerning this subject can be found in related reviews (see [20, 21]) and in many other articles. In general, the interface traps are associated with $P_b$ centres, $[Si_3 \equiv Si\cdot]$, which are trivalent Si defects at the $Si - SiO_2$ interface. The oxide traps are associated with $E'$ centres, $[(Si - O_3) \equiv Si\cdot]$, which are trivalent $Si$ defects in $SiO_2$. These kinds of traps were detected by the electron paramagnetic resonance (ESR) [22].

The measurements performed by the ESR method permit the recognition of the typically observed "U-shaped" energy distribution [23] of interface traps. In this context the "U-shaped" profile is a simple consequence of amphoteric nature of $P_{b0}$ centre [25]. Such a centre has one- and two-electron transitions energies centred around the midgap. As the Fermi level moves from the valence band toward the midgap, the positively charged $P_{b0}$ centre accepts an electron and becomes paramagnetic and neutral (a donor-like trap). When the Fermi level moves from the midgap toward the conduction band edge, the neutral $P_{b0}$ centre picks up an additional electron and becomes diamagnetic and negatively charged (a acceptor-like trap). It is clear that this explanation supports also a well-known and usually used model postulating that the interface traps are acceptors in the upper part of the bandgap and donors in the lower part of the bandgap.

An other type of traps has been recently proposed by Sah [21]. They are called proton or protonic traps, and they are centres which can capture one or more protons

or hydrogen atoms. The protonic centre can also have an electronic state to capture an electron or a hole. It means that electronic traps can be annealed or eliminated by hydrogenation.

The next problem is the significance of the upper interface, that is, gate-oxide interfacial layer. The presence of defects in this region is commonly neglected. The Sah's [21] argument against such neglecting is as follows: the gate-oxide interfacial layer can have an extremely high density of traps about $10^{14} traps/cm^2$; even if it is reduced by a thickness ratio gate-oxide interfacial layer/oxide layer $\approx 1A/100A$ , it can induce $10^{12} q/cm^2$ charges in the Si surface layer (when all the $10^{14}$ traps are charged in a 100A gate oxide); this would cause a 500mV threshold voltage shift.

We will not deal with mobile ions charges $Q_m$ because their influence on electrical MOS structures characteristics is related to a thermal and/or electrical stress but not to $\gamma$ irradiation.

Our interest will be focused on four remaining charges and their changes after irradiation as the reasons of changes of electrical parameters of MOS transistors.

## 2.1 Definitions of MOS transistor parameters

In this section the fundamental information about the physical sense of the MOSFET parameters are presented. The definitions of electrical parameters are explained in terms of physical quantities and phenomena such as carrier concentration, energy band bending, carrier mobility, interface states density and various mechanisms of carriers scattering, impact ionization. When the noise spectrum is discussed, the mathematical concept of the spectral density as a notion of the Fourier analysis is shortly described. Some parameters are illustrated by original measurements.

### 2.1.1 A theoretical definition of threshold voltage

The threshold (the onset of strong inversion) condition in MOS structure is achieved when the concentration of the minority carriers at the semiconductor surface equals to the doping concentration in the semiconductor bulk.

For the $n$-channel transistor structure we can write this condition in the following way:

$$n_s = N_A, \tag{2.1}$$

where $n_s$ - the electron concentration at the surface of $p$-type semiconductor substrate, $N_A$ - the acceptor doping concentration in the $p$-type bulk. Both these values can be expressed as a function of the potential $\psi$:

$$n_s = n_i \exp\frac{\psi_s - \phi_B}{V_t}, \tag{2.2}$$

$$N_A = p_p(\psi = 0) = n_i \exp\frac{\phi_B}{V_t}, \tag{2.3}$$

where $n_i$ is the intrinsic carrier concentration for silicon (see Tab. 2.1), $p_p$ is the majority carrier (holes) concentration, $\psi_s$ is the surface potential, and $\phi_B = \frac{E_i - E_F}{q}$



where $E_i$ is the intrinsic energy level at a midgap at a point of substrate deeper than the edge of depletion region, and $E_F$ is the Fermi energy level, $V_t = \frac{kT}{q}$ is the thermal voltage. In the equation (2.3) the fact that the doping and the majority carrier concentrations are equal deeply in the semiconductor substrate where the band is flat ($\psi = 0$), has been used .

After substitution of the expressions (2.2) (2.3) to (2.1), the following equation is obtained:

$$n_i \exp\frac{\psi_{s,inv} - \phi_B}{V_t} = n_i \exp\frac{\phi_B}{V_t}. \tag{2.4}$$

It means that in order to reach strong inversion condition the surface potential $\psi_s$ must be:

$$\psi_{s,inv} = 2\phi_B = 2V_t \ln\frac{N_A}{n_i}, \tag{2.5}$$

where the equation (2.3) has been used to calculate $\phi_B$.

The threshold voltage is defined as the gate voltage $V_{GS}$ required for surface potential equal to $\psi_s = 2\phi_B + V_{SB}$ (where the substrate bias is also taken into account):

$$V_{th} = V_{GS}(\psi_s = 2\phi_B + V_{SB}). \tag{2.6}$$

For a smaller surface potential the inversion layer also exists and the concentration of the minority carriers in it depends on the surface potential as follows [26]:

$$n_s = N_A \exp\frac{\psi_s - 2\phi_B}{V_t}. \tag{2.7}$$

Equation (2.7) is a simple consequence of (2.2), (2.3) and it is plotted in Fig. 2.4. The beginning point of this plot, $\psi_s = 0$, is the flat-band condition and the respective gate voltage is called the flat-band voltage $V_{FB}$. At $\psi_s = \phi_B$, the surface concentration $n_s$ becomes equal to the intrinsic concentration. It is a natural consequence of (2.2) and of the mass action law that $n_s = p_s = n_i$. This is defined as the limit point between the depletion and the inversion regions. This point is also called midgap point because the intrinsic energy level at the surface is equal to the Fermi level. The respective gate voltage is called the midgap voltage $V_{mg}$. Of course, even in depletion the surface concentration $n_s$ is non zero but much smaller than the intrinsic concentration $n_i$. With the increasing $\psi_s$ above $\phi_B$, $n_s$ increases drastically, and at $\psi_s = 2\phi_B$, the strong inversion condition is obtained. The model of a MOS transistor operated in the strong inversion region is presented in App. A.

The facts mentioned above suggest that below the threshold voltage a MOS transistor also conducts current. The region between the midgap voltage $V_{mg}$ and the threshold voltage $V_{th}$ is called the subthreshold or weak inversion region. In this region the dominant conduction mechanism is diffusion and therefore the drain current depends exponentially on the gate voltage. The channel region of a MOS transistor is equivalent of the base region of a bipolar transistor (see App. B.).

Many publications distinguish a third region of the MOS transistor operation called the moderate inversion [26, 27] or the transition region [31]. This region exists

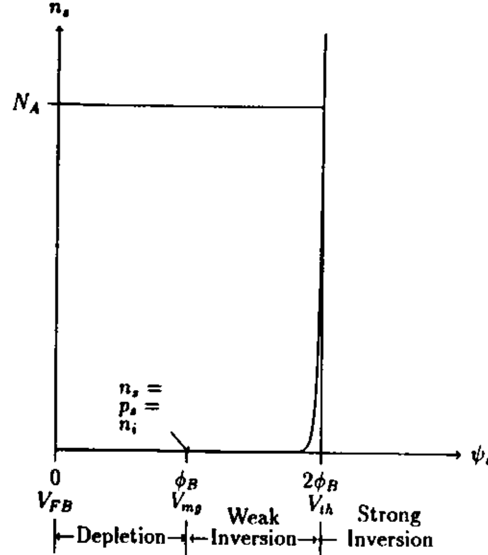


Figure 2.4: The electron concentration at the surface vs. the surface potential (linear axes).

when the value of gate voltage is around threshold voltage, where both strong and weak inversion approximations do not apply. The drift current is comparable in magnitude to the diffusion current.

In order to generalize, two more fundamental definitions of the onset of the strong inversion in MOS devices will be rewritten. These definitions are valid for a nonhomogeneously doped substrate. The nonuniformity can be caused by an expedient ion implantation step during a technological process as well as by the redistribution of dopants which cannot be avoided during the thermal oxidation process.

The first definition [32] says that the strong surface inversion occurs when the surface minority carrier concentration equals or exceeds the majority carrier concentration at the boundary of the depletion region $n_s \geq N_A(x_{d,max})$. It means that the surface potential at the onset of the strong inversion is:

$$\psi_{s,inv} = V_t \ln \left[ \frac{N_A(x_{d,max}) C_B}{n_i^2} \right], \tag{2.8}$$

where $x_{d,max}$ is the maximum depletion width (see equation (3.1)), $C_B$ the constant impurity concentration deep in the substrate.

The second definition [33] describes the onset of the strong inversion condition by means of equality:

$$\frac{dQ_I}{d\psi_s} = \frac{dQ_D}{d\psi_s}, \tag{2.9}$$



where $Q_I$ is the charge in the inversion layer and $Q_D$ is the charge in the depletion region.

### 2.1.2 Transconductance

The definition of the transconductance is:

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}, V_{SB}=const}, \tag{2.10}$$

where $I_{DS}$ is the drain current, $V_{DS}, V_{SB}$ are the drain and bulk voltage measured in respect to the source terminal.

If the double integrated Pao-Sah [34] formula is taken into account :

$$I_{DS} = q\frac{W}{L} \int_0^{V_{DS}} dV \int_0^{\delta} \mu_n(x,y) n(x,y) dx, \tag{2.11}$$

where $\delta$ is the inversion layer thickness, $\mu_n(x,y)$ is the electron surface channel mobility, $n(x,y)$ is the density of free electrons in the channel, $V(y)$ is the channel potential, it is clear that the most important physical quantity which influences the transconductance $g_m$ is mobility. Channel mobility is obtained by Mathiessen's rule:

$$\mu_n = \frac{\mu_0}{1 + \frac{\mu_0}{\mu_{SR}} + \frac{\mu_0}{\mu_{VS}}}, \tag{2.12}$$

where $\mu_0$ is the low field mobility caused by phonon and point charge scattering from both oxide and bulk centres, $\mu_{SR}$ is the surface roughness mobility due to surface asperity, $\mu_{VS}$ is the velocity saturation mobility.

The surface roughness mobility $\mu_{SR}$ depends on the effective normal electric field $\mathcal{E}_{eff}$ at the interface and describes mobility degradation with the increasing gate bias $V_{GS}$ [35, 37, 38]. The three other components of mobility associated with quantum mechanical effects [36] can be neglected. In the classical approach it is assumed that at room temperature all free carriers lie in the lowest conduction subband. Then:

$$\mu_{SR} = \mu_0 \frac{\mathcal{E}_{crit}}{\mathcal{E}_{eff}} = \mu_0 \mathcal{E}_{crit} \frac{\varepsilon_{Si}\varepsilon_0}{Q_D + \frac{Q_I}{2}}, \tag{2.13}$$

where $\mathcal{E}_{crit}$ is the critical normal field whereas the effective normal field $\mathcal{E}_{eff}$ has been expressed by the charges $Q_D$ and $Q_I$ of the depletion and inversion layers charges respectively. Using a very simple expression for these charges (see App. A., equations (A.3), (A.4), (A.5), (A.6), (A.18)):

$$\begin{aligned} Q_I &= -C_{ox}(V_{GS} - V_{th} - V(y)), \\ Q_D &= C_{ox}\gamma\sqrt{V_{SB} + 2\phi_B + V(y)}, \end{aligned} \tag{2.14}$$

where $\gamma = \frac{\sqrt{2\varepsilon_{Si}\varepsilon_0 q N_A}}{C_{ox}}$ is the body effect coefficient (A.13), $C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{ox}}$ is the gate oxide capacitance,

and then, introducing a parameter $\theta_s$:

$$\frac{\mu_0}{\mu_{SR}} = \frac{Q_I + 2Q_D}{2\varepsilon_{Si}\varepsilon_0 E_{crit}} = \frac{\theta_s}{C_{ox}}(Q_I + 2Q_D)$$

$$= \theta_s(V_{GS} - V_{th} - V(y) + 2\gamma\sqrt{V_{SB} + 2\phi_B + V(y)}), \quad (2.15)$$

where

$$\theta_s = \frac{\varepsilon_{SiO_2}}{2\varepsilon_0 t_{ox} \mathcal{E}_{crit}} \quad (2.16)$$

is the gate field reduction parameter.

The velocity saturation mobility $\mu_{VS}$ depends on the longitudinal electric field along the channel and describes the mobility degradation with the increasing drain bias $V_{DS}$ [35]. This phenomenon may be approximated as:

$$\frac{\mu_0}{\mu_{VS}} = \theta_c L \frac{dV}{dy}. \quad (2.17)$$

where $\theta_c$ is the drain field reduction parameter.

Taking both effects into account, one obtains:

$$\mu_n(y) = \frac{\mu_0}{1 + \theta_s(V_{GS} - V_{th} - V + 2\gamma\sqrt{V_{SB} + 2\phi_B + V}) + \theta_c L \frac{dV}{dy}}. \quad (2.18)$$

The effective mobility is defined as a value averaged along the channel thickness:

$$\mu_{eff} = \frac{\int_0^\delta \mu(x) n(x) dx}{\int_0^\delta n(x) dx}. \quad (2.19)$$

The gain factor (called also transconductance) $\beta$ is defined as:

$$\beta = \mu_n C_{ox} \frac{W}{L}. \quad (2.20)$$

The product of $\beta$ and drain voltage $V_{DS}$ is an ideal limit of the transconductance for a low normal field (absence of surface roughness scattering), infinite inversion layer capacitance $C_{inv}$ and without interface states:

$$g_{m,limit} = \beta V_{DS}. \quad (2.21)$$

A similar simple equation for the saturation region $V_{DS} \ll V_{DSsat}$ is:

$$g_{m,sat} = \beta(V_{GS} - V_{th}). \quad (2.22)$$

When the capacitance of the inversion layer $C_{inv}$ is finite, it can be taken into account replacing $C_{ox}$ in equation 2.20 by effective capacitance $C_{eff}$ of the serial connection of the gate oxide capacitance $C_{ox}$ and the inversion layer capacitance $C_{inv}$ [39]:

$$C_{EFF} = \frac{C_{ox} C_{inv}}{C_{ox} + C_{inv}}. \quad (2.23)$$

The approximation of $C_{inv}$ is a separate problem not discussed here.



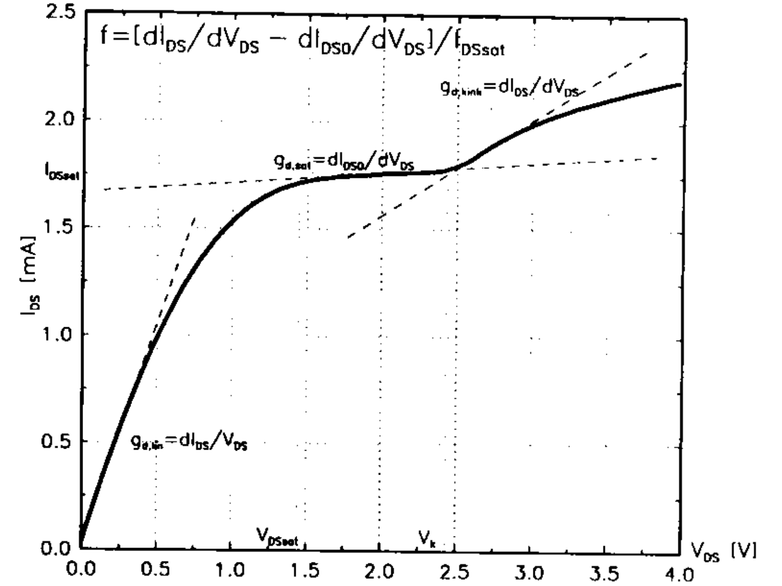


Figure 2.5: The definition of the drain conductance $g_d$ in the linear, saturation and kink modes of operation and the kink effect parameter $f$ shown on the output characteristic of a SOI MOS transistor. $f = 0.225V^{-1}$, $V_k = 2.43V$, $g_{d,sat} = 47.76\mu S$, $g_{d,kink} = 445.2\mu S$, $V_{Dsat} = 1.45V$, $I_{Dsat} = 1.76mA$

### 2.1.3 Drain conductance

The drain (or channel) conductance is defined as:

$$g_d = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}, V_{BS}=const}. \quad (2.24)$$

At a very low drain bias ($V_{DS} = (1\ldots4)V_t$), the channel conductance is large:

$$g_{d,lin} = \beta(V_{GS} - V_{th}), \quad (2.25)$$

but in the saturation $g_d$ is almost zero:

$$g_{d,sat} = 0. \quad (2.26)$$

This definition is illustrated in Fig. 2.5.

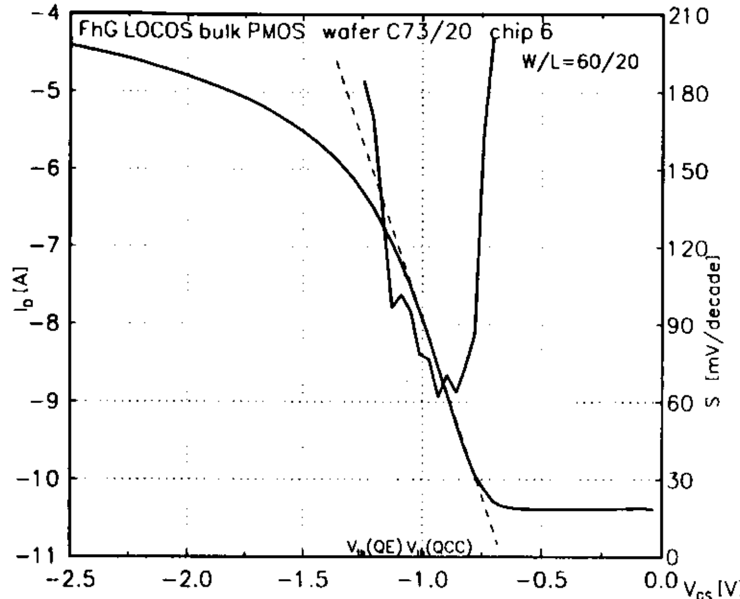


Figure 2.6: The subthreshold characteristics and the subthreshold swing $S$ dependence on gate voltage $V_{GS}$ for PMOS bulk transistor. $S = 108.8 mV/decade$

### 2.1.4 Subthreshold swing

The subthreshold swing is defined as the change of the gate voltage $V_{GS}$ needed to reduce the subthreshold current by one order of magnitude:

$$S = \ln 10 \, \frac{\partial V_{GS}}{\partial \ln I_D}. \tag{2.27}$$

This parameter is also called the inverse subthreshold slope factor.

The subthreshold curves and the subthreshold swing $S$ dependence on gate voltage $V_{GS}$ are presented in Fig 2.6. The method to extract the average value of subthreshold swing $S$ by using linear regression method is also shown in this figure.

The most popular theoretical expression for subthreshold swing is (see App. B.):

$$S = V_t \ln 10 \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right). \tag{2.28}$$

where $C_D$ is the depletion region capacitance (see equation (B.16)), $C_{it} = qD_{it}$ is the interface states capacitance, $D_{it}$ is the density of interface states. This expression is valid for the bulk and the SOI with body contact transistors. Theoretical lower limit for $(C_D + C_{it}) \ll C_{ox}$ is:

$$S \to V_t \ln 10 = 60 mV/dec \tag{2.29}$$

(at room temperature).



Table 2.2: Values of the ionization constants for electrons and holes in silicon. Reported values are given according to [43, 44]. More detailed review of impact ionization constants can be found in [45, 46].

| | Electrons | | Holes | |
|---|---|---|---|---|
| | $A_i$ $10^6 cm^{-1}$ | $B_i$ $10^6 V/cm$ | $A_i$ $10^6 cm^{-1}$ | $B_i$ $10^6 V/cm$ |
| Surface | 2.45 | 1.92 | — | — |
| Bulk | 0.703[1] | 1.23[1] | 1.582[2] 0.671[3] | 2.036[2] 1.693[3] |

The electric field $E$ in the drain space charge region:
[1] for $1.75 \times 10^5 \le E \le 6.4 \times 10^5 \; Vcm^{-1}$
[2] for $1.75 \times 10^5 \le E \le 4 \times 10^5 \; Vcm^{-1}$
[3] for $4 \times 10^5 \le E \le 6.4 \times 10^5 \; Vcm^{-1}$

### 2.1.5 Kink effect

The anomalous output characteristic is observed for SOI $n$-channel transistor or bulk $n$-channel transistor built on high-resistivity silicon substrate [40, 41] or with floating substrate [42]. This behaviour of a transistor is called the kink effect (Fig. 2.5). It results from the fact that the body of the transistor is floating and its potential depends on the majority carrier (hole) current. This current is always generated in the high field region near the drain of the transistor operating in saturation. The mechanism of its generation is the weak impact ionization by electrons injected from the transistor channel to the drain space charge region. The electrons generated in this way flow together with the channel electrons to the drain electrode, but the holes, as always in the case of a bulk transistor, are collected by the substrate electrode resulting in a well-known $I_{sub}(V_{GS})$ curve [43] presented in Fig. 2.7. When the substrate is floating and the body volume is finite as in SOI transistors, the holes are accumulated in the body region raising the potential of the transistor body. The change of the body potential in relation to the source electrode yields a change of the threshold voltage hereby increasing the drain current and resulting in a bend in $I_{DS}(V_{DS})$ curves (Fig. 2.5). When the drain voltage $V_{DS}$ increases the hole substrate current $I_{sub}$ also increases, and it can be expressed [48] as:

$$I_{sub} = (M - 1) I_{DSsat}, \tag{2.30}$$

where $(M-1) = \int_{L_e}^{L} \alpha(\mathcal{E}_{hd}) dy$ (the integral of the field-dependent ionization rate over the high-field region from the pinch-off point $L_e$ to the drain $L$), $\alpha(\mathcal{E}_{hd}) = A_i \exp(-\frac{B_i}{\mathcal{E}_h})$ is the ionization rate expressed by Chynoweth's law [47], $A_i, B_i$ are the ionization constants presented in Tab. 2.2, $\mathcal{E}_{hd}$ is the electric field in the drain space charge region.

The increase of the impact ionization hole current $I_{sub}$ results in an increasing of the source-substrate diode bias and then causes lowering of the threshold voltage $V_{th}$

due to the body effect. Therefore the kink effect depends strongly on the substrate doping. For lower threshold voltage, the drain current $I_{DS}$ is higher. The change of the threshold voltage from $V_{th1}$ to $V_{th2} < V_{th1}$ results in the effect that within one curve of the output characteristic ($V_{GS}$ =const) a considerable bend or kink occurs, as there is a continuous transition from the curve ($V_{GS} - V_{th1}$) to curve ($V_{GS} - V_{th2}$).When the drain current $I_{DS}$ is increased again, it enhances further the multiplication of carriers because of impact ionization and positive feedback occurs.

Such an undesirable increase of the current in the saturation region is observed only in NMOS transistors. In p-channel transistors, no kink is observed because the impact ionization cross-section for a hole is far smaller than for an electron.

The methods to avoid the kink effect are:

- eliminating the presence of the neutral body region by applying a positive backside voltage or fabricating enough thin and slightly doped transistor islands [49, 50] (fully depleted devices are described in section 3.2). The holes injected into the body can recombine in the source region without modifying the body potential.
- design additional contacts to maintain the body potential (similar to a substrate electrode in the bulk transistor). Such contacts are commonly prepared in the source area and therefore cause a drain current reduction. The source region must be distributed in a mosaic $\cdots -p-n-p-n- \cdots$ configuration with sufficient number of body contacts to suppress both the kink effect and the reduction

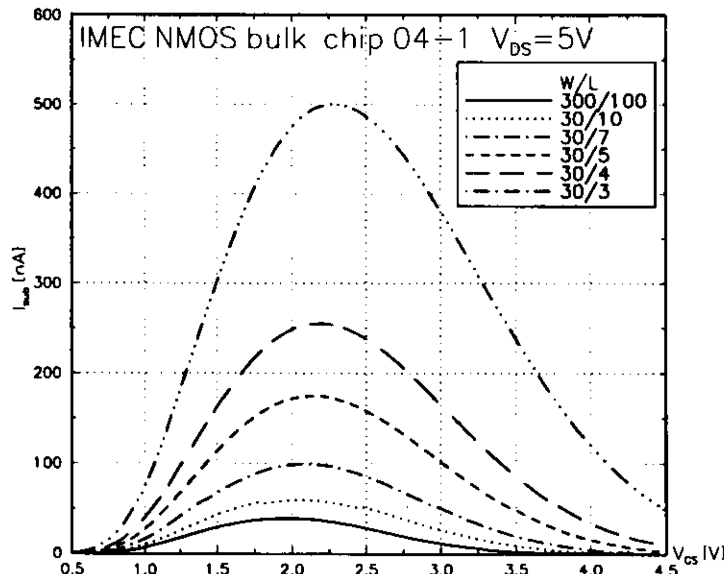


Figure 2.7: The substrate current $I_{sub}$ vs. the gate voltage $V_{GS}$ measured for several bulk NMOS transistors with different dimensions.



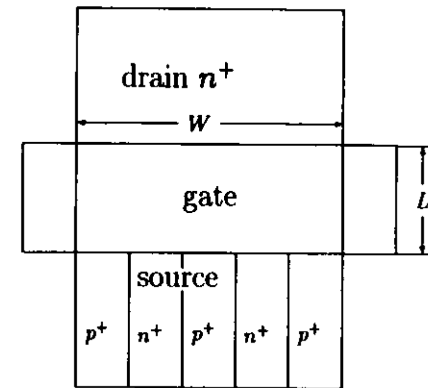


Figure 2.8: The design of the source region of SOI NMOSFET to suppress kink effect. The split source technique.

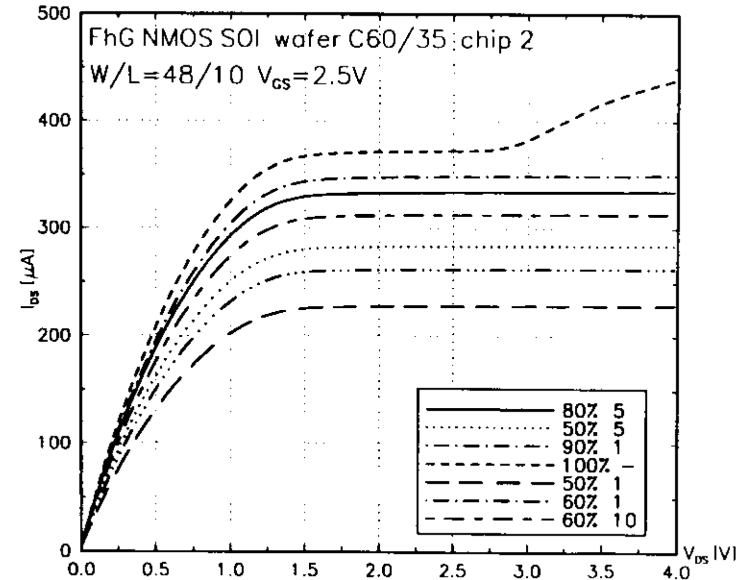


Figure 2.9: The output characteristics of split-source SOI NMOS transistors. The first digit in the legend gives the percentage of the whole source area which is $n$ doped. The second digit is a number of $p$-type contacts made in the source region. The transistor with full $n$-type source exhibits the kink effect. The kink effect disappears for six remaining transistors with the body short-circuited to the source. The reduction of drain current depends on the configuration of $\cdots - p - n - p - n - \cdots$ regions in the source.

of drain current [51]. It is called a split-source structure and is presented in Fig. 2.8. The disappearance of kink effect is shown in Fig. 2.9. The value of the drain current strongly depends on the body contact configuration. The second disadvantage of this solution is that the area consumed by the device with such a complicated source region increases considerably;

- dividing the NMOS transistor island by a reachthrough $n^+$ region into two separate bodies, the upper body (close to the drain) and the lower body (close to the source). It is a so called twin-MOSFET structure [53]. This additional $n^+$ region confines the holes generated by impact ionization in the upper body. Although the n-channel is also divided into two sub-channels, the device operates as a classical MOSFET with one channel consisting of two pieces connected by $n^+$ region. When the device operates in the saturation, the generated holes cannot flow to the body but they recombine with electrons of $n^+$ region. Therefore, the lower body is protected against hole injection, the $V_{th}$ of the lower channel is kept unchanged. The kink effect can take place only in the upper body. It means that the $n^+$ region should be made as close to the drain as possible. If the ratio of lengths of lower and upper channels is larger, a bigger reduction of the kink effect is observed. Similarly, the parasitic bipolar effect is suppressed by dividing the base of BJT into two pieces.

The mechanism described above is not the only reason responsible for existence of the kink effect. There is the second kink effect arising from bipolar action of parasitic BJT (see section 3.2) presence in a SOI transistor structure. Such bipolar effects are observed also in a fully depleted submicrometer SOI MOSFETs [41, 52].

In order to describe kink effect the parameter $f$ is used. It is defined as the difference between the drain conductance above and below the kink point $V_k$, divided by the saturation current $I_{DSsat}$ [121]:

$$f = \frac{\frac{\partial I_{DS}}{\partial V_{DS}} - \frac{\partial I_{DS0}}{\partial V_{DS}}}{I_{DSsat}}. \tag{2.31}$$

The meaning of each symbol is shown in Fig. 2.5. From the point of view of the application of the SOI transistors the value $f < 0.1V^{-1}$ is accepted.

Another important parameter describing kink effect can be the length of a plateau of the output characteristic in saturation region of transistor. It will be expressed as difference $V_k - V_{DSsat}$ (see Fig. 2.5).

### 2.1.6 Spectral noise power density

Spectral density is a function defined in the general Fourier analysis. This notion will be applied to a random process [139] and then to the noise of a drain current of a MOS transistor.

A random process $X(t)$ expanded by Fourier's series for the interval $0 \leq t \leq T$ is:

$$X(t) = \sum_{n=-\infty}^{\infty} a_n \exp(j\omega_n t), \tag{2.32}$$



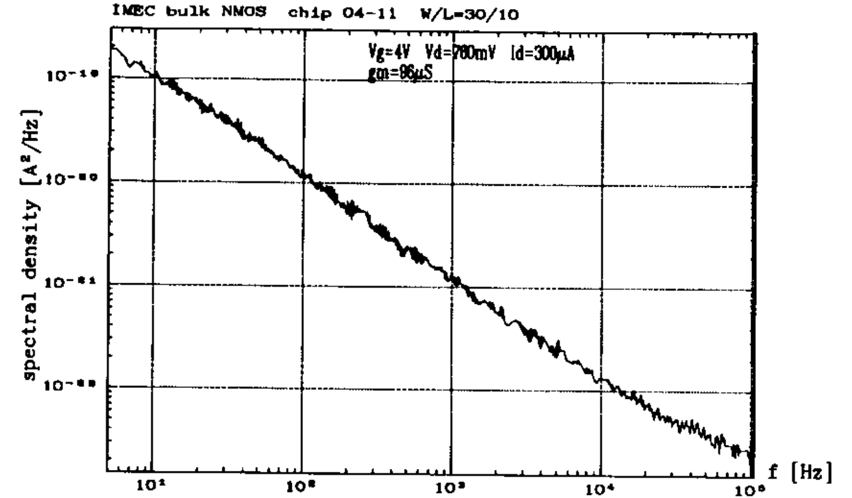


Figure 2.10: Typical noise power spectrum of drain current of the MOS transistor.

where $\omega_n = \frac{2\pi n}{T}, n = 0, \pm 1, \pm 2, \ldots$, and

$$a_n = \frac{1}{T}\int_0^T X(t)\exp(-j\omega_n t)dt \tag{2.33}$$

is the amplitude of $n$-th term of Fourier's series. The spectral density $S_x(f)$ of $X(t)$ is defined [136] as:

$$S_x(f) = \lim_{T\to\infty} 2T\overline{a_n a_n^*}, \tag{2.34}$$

where the asterisk denotes the complex conjugate of the quantity involved. One of the most useful theoretical result concerning the spectral density is its relationship to the autocorrelation function $\overline{X(t)X(t+s)}$, called the Wiener-Khintchine theorem:

$$S_x(f) = 2\int_{-\infty}^{\infty} \overline{X(t)X(t+s)}\exp(j\omega s)ds. \tag{2.35}$$

The example of the measured noise power spectra of MOSFET drain current $S_{I_{DS}}(f)$ is presented in Fig.2.10. The measurement was done by measurement system described in section 5.2.

The measured noise power spectra of MOSFET drain current are commonly presented as the equivalent noise power spectral density in the gate circuit (at the input):

$$S_{v_{eq}}(f) = \frac{S_{I_{DS}}(f)}{g_m^2}, \tag{2.36}$$

where $g_m = \mu C_{ox}\frac{W}{L}V_{DS}$ is the transconductance of device, which should be known as a function of frequency.

The theory presented in chapter 5. mainly concerns the power spectral density of the fluctuations of the number of trapped carriers $S_{N_t}$ occupying the border traps in the gate oxide. The measurable quantities are the spectral density of the fluctuations in the drain current $S_{I_{DS}}$ or drain voltage $S_{V_{DS}}$. The relation between these two quantities is:

$$S_{V_{DS}}(f) = R^2 S_{I_{DS}}(f), \tag{2.37}$$

where $R$ is the resistance in the drain circuit (usually the parallel connection of drain conductance $g_d$ and the load resistance $R_D$). Most frequently the measurement is carried out under constant gate voltage $V_{GS}$ and drain current $I_{DS}$ bias. In the strong inversion and in the linear range of operation, the simple formula (2.42) for recalculation of the spectral density of the fluctuations in the drain voltage $S_{V_{DS}}$ to the spectral density of the fluctuations in the number of trapped carriers $S_{N_t}$ was derived [150]. The fluctuation in the gate voltage is:

$$\delta V_{GS} = -\frac{q}{C_{ox} W L}\delta N_t, \tag{2.38}$$

where $\delta N_t$ is the fluctuation in the number of trapped carriers in the border traps. The fluctuation in the drain voltage is:

$$\delta V_{DS} = \frac{\partial V_{DS}}{\partial V_{GS}}\delta V_{GS}. \tag{2.39}$$

The derivative in this equation can be calculated using equation (A.17):

$$V_{DS} = \frac{1}{\beta}\left(\beta(V_{GS} - V_{th}) - \sqrt{\beta^2(V_{GS} - V_{th})^2 - 2\beta I_{DS}}\right), \tag{2.40}$$

and the equations (2.38), (2.39) give:

$$\delta V_{DS} = -\frac{q}{C_{ox} W L}\frac{V_{DS}}{V_{GS} - V_{th} - V_{DS}}\delta N_t. \tag{2.41}$$

For spectral density it is:

$$S_{V_{DS}}(f) = \left[\frac{q V_{DS}}{C_{ox} W L (V_{GS} - V_{th} - V_{DS})}\right]^2 S_{N_t}(f), \tag{2.42}$$

It means that if the measurement is carried out under constant gate voltage $V_{GS}$ and drain current $I_{DS}$ bias, and the drain voltage $V_{DS}$ is comparable with effective gate voltage $V_{GS} - V_{th}$, the obtained spectrum should be divided by factor $\left[\frac{V_{DS}}{(V_{GS} - V_{th} - V_{DS})}\right]^2$ to normalize result with respect to drain $V_{DS}$ and threshold $V_{th}$ voltages.

Such normalization is very important when the noise power spectrum is measured after subsequent irradiations because of the threshold voltage and work point radiation shift (see sec: 5.3.).

# Chapter 3

# Technologies

The principle of the surface field-effect transistor was first proposed in the early 1930s by Lilienfeld (U.S. patent) and Heil (British Patent), but the first MOSFET was fabricated by Kahng and Atalla no sooner than in 1960 [54]. On the other hand, the first integrated circuit (IC) was manufactured by Kilby in 1958 [55]. These were phase-shift oscillators and flip-flops, fabricated in germanium substrate. From these early primitive forms, ICs technology has been developed to very complicated and sophisticated processes. Today ICs contain hundreds of thousands of individual components on a single chip of silicon and technological processes consist of over 300 distinct steps and each of them comprises a large number of individual activities. Such remarkable advances in this field during the last three decades are the results of multidisciplinary research and development works including devices physics, material science and chemistry.

The ICs technology from the first laboratory attempts was developed to very complicated processes flows available not only in the form of completed products but also as a special service for IC designers. Today any electronic engineer can be a designer of IC for his own specific applications. A process flow is a set of fabrication steps, which must be carried out in a specific sequence. It comprises many steps such as ion implantation, diffusion, oxidation, film depositions, lithography and etching. These steps provide precisely controlled impurity layers in silicon which form the individual circuit components (i.e. transistors, diodes, capacitors, resistors) as well as the dielectric and metal layers used for interconnecting the individual components into an IC. All the steps in the process are strongly interrelated so no step can be changed arbitrarily [56]. A typical process flow is illustrated by the diagram presented in Fig. 3.1.

There are several, general kinds of VLSI technology depending on the type of the active devices which is the most important component of IC. From this point of view the following technologies can be distinguished: standard bipolar (BJ), integrated injection logic ($I^2L$), n-channel MOS (NMOS), complementary MOS (CMOS), mixed bipolar-MOS (BiMOS). The greatest interest is focused on MOS technology because of its low cost and simplicity. Although both devices, bipolar and MOS use lateral oxide isolation, there is no need for vertical isolation in the MOSFET, while a buried layer $n^+ - p$ junction is required in the bipolar transistor. The doping profile in a





MOSFET is not as complicated as in a BJT, and the control of the dopant distribution is also less critical [57].

In the field of MOS technology which is our main interest here, great progress has been made in last 20 years. That is why it has been possible to create new directions in computer science, signal processing and in many others fields of electronics. For example the functional density of ICs has increased almost 200-fold, and speed has increased 20-fold. MOSFET with good characteristic can be fabricated with effective channel lengths of between 0.1 and 0.2 $\mu m$. In addition, a recent detailed analytical study has predicted that CMOS inverters with $L_{eff} = 0.14\mu m$ could have a gate delay of less than 20 $ps$, which is more than seven times faster than present-day VLSI CMOS circuits with $L_{eff}$ of about $= 1\mu m$ [58].

The list below summarizes some of the contemporary processing trends being investigated and used to overcome the limitations. The problems are listed without detailed explanations [58]:

- continued shrinking (below $L_{eff} = 1\mu m$ up to $0.14\mu m$);
- new isolation techniques (SOI, deep-trench well and epitaxial layer);
- new materials for gate electrodes (Mo, W, silicides - with higher work function and smaller resistance);
- prevention of hot electron instabilities (lightly doped drain LDD);
- lower parasitic resistances and capacitances (new metallurgical methods for forming contacts);
- multilevel metallizations;
- lower defect density;
- bipolar/CMOS (higher transconductance, smaller area for power stages);
- 3-D circuits (many subsequent stacked layers of oxide and silicon).

The study which has been carried out in here has been based on several technologies. Test structures were provided by the IMEC (Louvain, Belgium), the ELMOS (Dortmund, Germany), the Fraunhofer Institute FhG IMS (Duisburg, Germany). The fundamental parameters concerning these technologies are presented in Tab. 3.1.

In this chapter some fundamental information about MOS technology will be presented following several textbooks and articles [26, 57, 56, 60]. At first, the technological process flow for bulk transistors fabrication will be discussed. The details of the LOCOS (local oxidation of silicon) and SOI (silicon on insulator) technologies developed by Fraunhofer Institute will be described. The last section of this chapter will deal with special technological and layout design procedures which increase the radiation hardness of MOS transistors.

## 3.1 Bulk technology

The Fig. 3.1. presents a specific sequence of performing the steps in a typical MOS technology process flow. The text below describes the most important steps contained in this diagram.

There are several kinds of MOS bulk technologies depending on the techniques of forming of substrates for two types of MOSFETs, $n$- and $p$-channel:

Table 3.1: The values of the most important technological parameters: the thickness of gate oxide $t_{ox}$ and the doping of substrate $N_{sub}$ of transistors fabricated by using tested technologies.
The values marked by † were measured and extracted by the author.
Other presented values were delivered by the producers.

| | | IMEC | ELMOS | FhG bulk | FhG SOI |
|---|---|---|---|---|---|
| PMOS | $t_{ox}[nm]$ | 39.2 | 40 | 40 | 25 |
| | $N_{sub}[cm^{-3}]$ | $9.94 \times 10^{15}$ | $1.248 \times 10^{16}$† | $2 \times 10^{16}$ | $5 \times 10^{16}$ |
| NMOS | $t_{ox}$ [nm] | 38.7 | 40 | 40 | 25 |
| | $N_{sub}[cm^{-3}]$ | $1.186 \times 10^{15}$ | $1.343 \times 10^{15}$† | $2 \times 10^{14}$ | $5 \times 10^{16}$ |

- $n$-type substrate with $p$-well which is formed in it for NMOS transistor fabrication;
- $p$-type substrate with $n$-well which is formed in it for PMOS transistor fabrication;
- $\nu$-type (lightly doped $n$-type) substrate with two wells $n$- and $p$-type;
- $\pi$-type (lightly doped $p$-type) substrate with two wells $n$- and $p$-type.

The input material is a monocrystalline silicon wafer fabricated by slicing an ingot prepared by the Czochralski process or with additional epitaxial layers. Crystal orientation < 100 > is preferred over < 111 > because it has an interface trap density one order of magnitude lower. The $p(n)$ well is implanted or diffused into $n(p)$ substrate at an impurity concentration five to ten times higher then that in the substrate to overcompensate the substrate doping. It increases the influence of body effect upon the transistor made in the well and also increases the source/drain-to-well capacitance. The "twin-well" approach allows to avoid these disadvantages and adjust the doping profiles in each well independently. In such approach, the starting material is lightly doped $n$ epitaxial layer over a heavily doped $n^+$ substrate. The wells are made in similar method like in LOCOS process described below. The $n$-well is form by phosphorus implantation when the remaining area is covered by a composite layer of $SiO_2$ and $Si_3N_4$. After selective field oxidation over $n$-well regions and removing the nitride layer, $p$-well is created by boron implantation.

The processes developed by the ELMOS company and the Fraunhofer Institute are of the $n$-well type. All values of process parameters usually given in parentheses refer to FhG IMS LOCOS technology [119]. The two CMOS processes mentioned above employ different isolation techniques. This results in a fundamental technological difference between the ELMOS and FhG IMS processes. At the beginning, the ELMOS-process, uses the growing thick field oxide everywhere on the silicon wafer



and then defines the active area of transistors by cutting windows in it. The thin gate oxide is later grown in these windows and then the polysilicon is deposited.

The starting material used by IMS FhG is $\pi$-type wafer (boron doped, < 100 > oriented, $100mm$ diameter). The epitaxial $p$-type layer (thickness $\approx 10\mu m$) of such a wafer has a resistivity of 30 to 50 $\Omega cm$ ($\approx 3 \times 10^{14} cm^{-3}$). The rest of the substrate is highly doped. In $n$-well technology the well oxide ($80nm$, without nitride layer) is formed on the $p$-substrate and after lithographical definition of $n$-well the implantation of phosphorus ($150keV, 4 \times 10^{12} cm_{-2}$) is made to overcompensate $p$ doping in the $n$-well area. The long term, high-temperature oxidation and diffusion step ($1170°C, 7h, N_2$ ambient) is performed next resulting in a depth of the well of about $4 - 6\mu m$.

The LOCOS technique used by FhG IMS begins with covering the whole surface with a composite silicon-nitride/pad oxide layer. At first a thin (28nm) oxide-pad layer is grown by means of thermal oxidation (900°C) and next $Si_3N_4$ is deposited. After the delimiting of active areas by means of a resist mask, the remaining surface is etched by plasma (dry) etching. The silicon-nitride oxidation mask is retained over the active device area to prevent it from being oxidized later. The next step is the field implantation by boron ($100keV, 4 \times 10^{13} cm^{-2}$) to the non-prevented regions to form a $p^+$ layer separated adjacent devices. This is called a chan-stop. The field oxide is grown ($45min$, 1025°C) over this layer. The silicon-nitride is stripped using wet etching ($H_3PO_4$, 150°C). Thin ($28nm$) sacrificial oxide is grown (900°C) and then removed to ensure a high-quality gate insulator. At this moment a critical step - gate oxide growing ($25nm$, 960°C) takes place. The ambient during thermal growing of the gate oxide can be either dry oxygen, steam, or a combination of the two. The atmosphere in a oxidation furnace at IMS FhG consists of 0.7 $l/min$ $H_2$ and 7 $l/min$ $O_2$. Other contaminations of the atmosphere (fluorine or chlorine) is not used. The postoxidation treatment is performed in a nitrogen ambient at 960°C during $10min$.

The LOCOS technique has the advantage of recessing about half of the field oxide below the silicon surface which makes the surface more planar. Another advantage is that such a technique allows chan-stop layers to be formed self-aligned to the active transistor area. The depth of the chan-stop implantation is adjusted to allow sufficient boron to remain in the underlying silicon after oxidation. A too heavy a chan-stop doping increases the source/drain-to-substrate capacitance and reduces junction breakdown voltage. The shortcoming of LOCOS process is the encroachment of field oxide into the active region, is the so-called "bird's beak" effect.

When the gate oxide and windows in it for buried contacts are completed, the next step of the process flow is an implantation for threshold voltage adjustment. This is done by two subsequent steps, each with a different mask. The first one is for NMOS transistors - boron implantation ($50keV, 3 \times 10^{12} cm^{-2}$) and the second one is for PMOS - arsenic implantation ($50keV, 3 \times 10^{12} cm^{-2}$). Sometimes in the case of submicrometer devices two kinds of channel doping implantation are used to provide the desired threshold and subthreshold characteristics. The implantation for threshold voltage adjustment should be shallow to avoid an increase in body effect sensitivity and source/drain-to-substrate capacitance as well. When the device

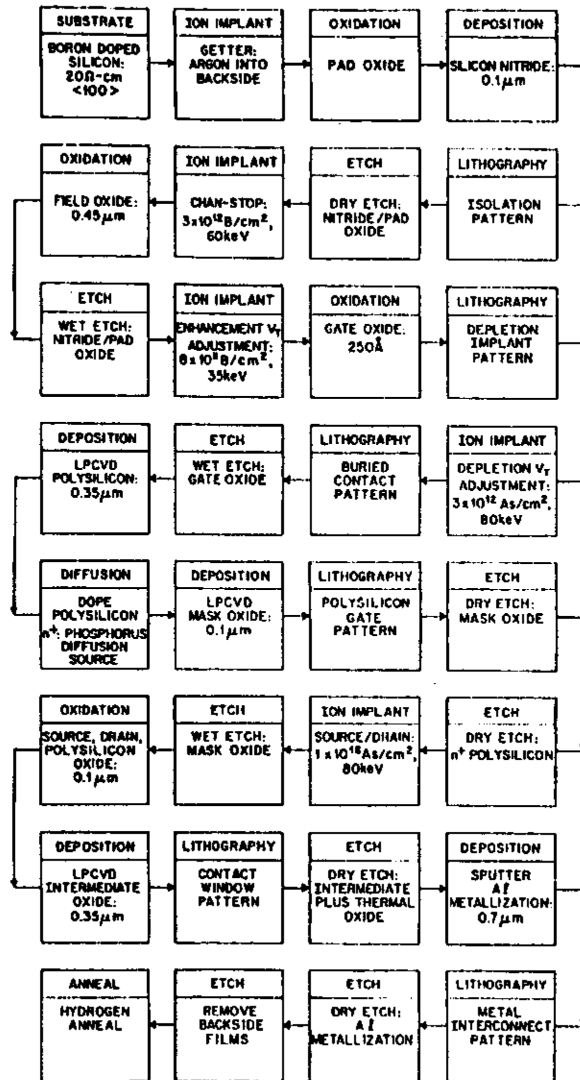


Figure 3.1: The diagram describing the main steps in an example of typical $n$-channel, polysilicon-gate, MOS, IC process flow [56].



is shorter a necessity of a deep implant (at longer projected range $R_p > 0.5\mu m$) can appear to prevent punchthrough by drain electric field . The deep implant also decreases subthreshold swing and increases carrier mobility because the channel is deeper and therefore the flowing current depends on surface roughness and interface states to a lesser degree. However, the capacitance of the channel is smaller and transconductance can be exacerbated.

When the adjustment implants through the gate oxide are completed, a high-temperature anneal is performed to minimize the post process density of charge in the oxide (800°C - dry ambient, 500°C - wet ambient).

Then the polysilicon for gate electrode and interconnections is deposited by the LPCVD (low-pressure chemical vapour deposition) method ($520nm, 630°C$). The $n^+$ doping of polysilicon is achieved by diffusion ($POCl^3, 975°C$). It can also be done by implantation or during deposition by adding phosphatine but the diffusive method offers the lowest value of resistivity of 20 to 30 $\Omega/\square$ [59]. For short devices, refractory metals or polysilicides should be used to achieve a resistance of about 1 $\Omega/\square$ [58]. After the PSG is deposited, polysilicon is patterned and dry etching of the PSG mask and polysilicon is carried out.

During the next step of the process the drain/source regions are implanted. This can be done by two subsequent steps using two different masks. The first mask relates to PMOS transistors - boron implantation ($30keV, 1 \times 10^{15}cm^{-2}$) and the second one to NMOS - arsenic implantation ($100keV, 3 \times 10^{15}cm^{-2}$). The energy of this implant should be high enough for the impurities to enter the silicon through the exposed gate oxide, but low enough to prevent their penetration through the polysilicon or field oxide. The sources and drains are thus self-aligned with respect to the gates. The self-alignment minimizes the overlap of the gate and the lateral source/drain diffusions, so that coupling capacitances are lowered there. To simplify the process flow only one mask can be used to form sources and drain regions. In this case the $p^+$ source/drain implant is nonselective. Thereafter phosphorus (or arsenic) is selectively implanted into the n-channel source/drain regions at a higher dose so that it overcompensates the existing boron.

If it is necessary to apply the technique to enhance both breakdown voltage and tolerance for hot electrons called LDD (lightly doped drain) the additional masking step before drain/source implant of NMOS transistors should be used. It consists of phosphorus implantation ($100keV, 8 \times 10^{12}cm^{-2}$) which forms special lightly doped $n^-$ region near drain (or source too) in the high lateral electric field space. The field is spread at the drain pinchoff region as in a lightly doped p-n diode, so the energy of the channel electrons decreases. Thus, the probability of the creation of hot carriers by impact ionization also decreases. This allows either an increase in power supply voltage or a reduction in channel length at a given voltage. The oxide is deposited by means of using the CVD method and spacer (thickness $0.3\mu m$, length $0.15\mu m$ - wafer C60/35) is formed between the gate electrode and the drain. The resulting gate-to-source/drain overlap is strongly related to the hot electron sensitivity of the device [61].

Phosphorus-doped silicon dioxide (called P-glass or PSG) is used as an insulator between two layers of polysilicon or metals or between polysilicon and metal, or

as a final passivation over the entire device. P-glass is deposited by means of the CVD method (100 $nm$-undoped, 650 $nm$-doped with 8%P). A concave shape in oxide going over the polysilicon gate can cause an opening in the metal film, resulting in device failure. The poor step coverage of the phosphorus-doped silicon dioxide can be corrected by heating the samples until the oxide softens and flows (960°C, $O_2$ ambient). This process is called P-glass flow. To ensure a good viscous of oxide during this process the phosphorus doping (8%) and sufficiently long time are necessary . Then, the windows for the contacts to the source/drain and the polysilicon are etched in the PSG. Aluminium (with 1% Si) deposited by sputtering is used for a metallization. The contacts are later sintered (440°C, wet ambient) to form a good ohmic connection to the silicon.

Finally, a protective oxide layer is deposited (700 $nm$, 2%P) on the wafer to seal it from contaminations and to serve as a mechanical scratch protection. The last step is masking and etching the P-glass for opening the pads for wire bonding.

At the end of bulk technique discussion, one of the most important problem associated with CMOS technology must be mentioned. It is an undesirable conduction mechanism known as latchup which is a condition where currents are conducted between two power supply nodes $V_{DD}$ and $V_{SS}$ of IC. The typical CMOS structure consists of $n$- and $p$-channel transistors (one of them is made in well) and contains also undesirable parasitic bipolar transistors. For example, for $p$-well approach, $n-p-n$ vertical transistor exists between source/drain of NMOSFET, $p$-well and substrate silicon regions respectively. The lateral $p-n-p$ parasitic structure is formed by source/drain of PMOSFET, substrate and p-well respectively. The collectors of each of these bipolar transistors feed each others' bases and together make up a thyristor $p-n-p-n$ device [57]. Normally, such a thyristor structure is in a blocking state but some random triggering event can switch it to a latched state. In this latched condition, currents of big magnitude can flow, causing a rapid and uncontrolled increase of power consumption, corruption of circuit operation or even functional destruction. Generally, triggering occurs when minority carriers are injected into the silicon region which plays the role of parasitic BJT base. It can be caused by input/output node overshoot, photocurrent, punchthrough, action of FOXFET or other occurrences. A full classification of triggering modes and operational p-n-p-n configurations is given in [62]. There are several methods to prevent latchup and they are shortly discussed in sec. 3.3.

## 3.2 SOI technology

Because of the disadvantages of conventional bulk CMOS technology, like non-sufficient lateral isolation between devices and difficulties with achieving greater packing density, a new tendency in MOS technology development appears. This new direction of investigations relies on the use of an additional isolation layer in depth of substrate. All such techniques are called silicon-on-insulator (SOI). In such a new approach each transistor is like a separate silicon island surrounded by dielectric material both in horizontal and also in vertical direction. To achieve isolation of the device at its



bottom, a special type of substrate material with buried isolation layer is necessary. There are several methods for such substrate preparation:

1. epitaxial silicon-on-sapphire (SOS),
2. recrystallized polycrystalline silicon,
3. oxidized porous silicon,
4. buried dielectric formation by using ion implantation

and others. The most popular method called separation-by-implanted-oxygen (SIMOX) belongs to the group number four listed above.

Formation of buried $SiO_2$ layer by oxygen-ion implantation into silicon was first reported by Watanabe and Tooi [115]. The first fabrication of CMOS devices using such input material were presented by Izumi et al. [116].

One of the newest SIMOX preparation procedure developed by the Fraunhofer Institute in Duisburg will be presented below [117], [118], [119]. The SIMOX wafers are fabricated by means of the implantation of oxygen atoms deeply into a standard $p$-type (100) $30-65$ $\Omega cm$ silicon wafer. A high current implanter is used. The energy of oxygen-ions is $200keV$, and used oxygen dose is in the range $1.6-2.0\times10^{18}cm^{-2}$. The wafer temperature is kept under constant control only by the ion beam current. The implantation temperature is chosen in the range of $550-700$°C, and the ion current is about $35-60mA$. A special silicon coating is used within the implanter. It prevents metal atoms from contaminating the ion beam as well as the SIMOX wafer. Annealing is the next step. The conditions of this step have crucial influence on the quality of the SIMOX wafer. These conditions should be adjusted in optimal manner for minimizing the density of dislocations in the silicon layer. The annealing is carried out at the temperature of $1250-1300$°C in an $Ar/O_2$ ambient for about $8h$. The SIMOX wafer obtained in this way consists of a monocrystalline layer of about 200 $nm$ thickness on top of a 380 $nm$ thick $SiO_2$ insulator. The density of dislocations in the monocrystalline layer is achieved at the level of $10^5cm^{-2}$ (observed in the TEM cross-section). In most cases reported in literature this parameter is on the order of $10^9cm^{-2}$ [120]. Then, the crystalline layer is thinned to about 130 $nm$ by means of an additional oxidation-etching step. The cross-section of the SIMOX wafer obtained by means of this technological procedure is presented in Fig. 3.2.

The transistors are fabricated in this silicon film existing after oxygen implantation and annealing over the buried oxide layer by the LOCOS process. The cross section of such devices is shown in Fig. 3.3.

The SOI transistor can be divided into three classes, with respect to body thickness $t_b$ and doping $N_A$. At first the value of the maximal depth of the depletion region $x_{d,max}$ must be calculated. Using the equation (B.16), remembering that $C_D=\frac{\epsilon_{Si}\epsilon_0}{x_d}$, and knowing that maximal depletion depth is achieved at the onset of the strong inversion ($\psi_s=2\phi_B$), it is obtained:

$$x_{d,max}=\sqrt{\frac{2\epsilon_{Si}\epsilon_0(2\phi_B)}{qN_A}} \tag{3.1}$$

The following classes of SOI transistors are distinguished:

**fully depleted** - the silicon layer is thinner than the maximal depth of the depletion region: $t_b < x_{d,max}$. A fully depleted transistor may operate with its back

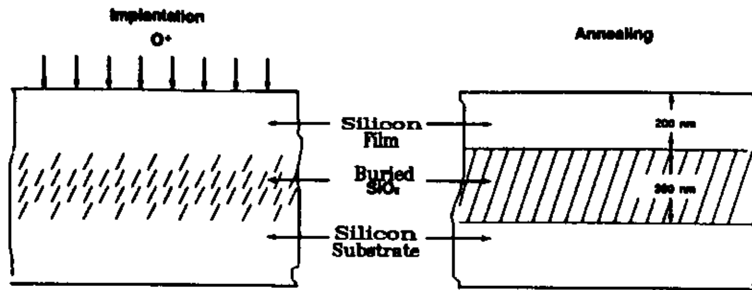


Figure 3.2: The Separation-by- IMplanted-OXygen input material for fabricating SOI MOS structures.
(Folder of Fraunhofer-Gesellschaft)

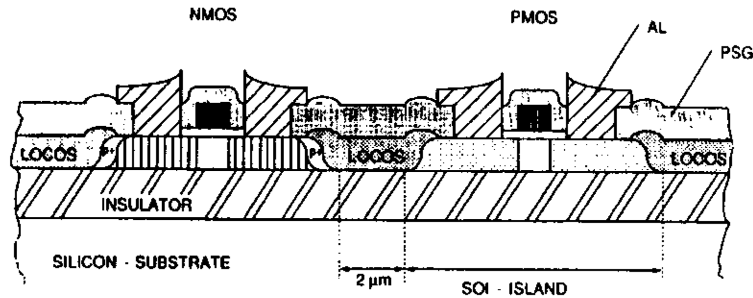


Figure 3.3: The CMOS structure fabricated by LOCOS technique on SIMOX material by FhG IMS.
(Folder of Fraunhofer-Gesellschaft)

interface in accumulation, depletion, weak or strong inversion by adjusting the voltage on the substrate $V_{BG}$. For doping $N_A = 5 \times 10^{16}$ $cm^{-3}$, the transistor body should be thinner than 100 $nm$.

**partially depleted** - the silicon layer is thicker than double the maximal depth of the depletion region: $t_b > 2x_{d,max}$. The behaviour of the partially depleted transistor is similar to bulk transistors with floating substrate.

**intermediate thickness** - the silicon layer thickness satisfies the condition: $x_{d,max} > t_b > 2x_{d,max}$. These transistors can operate in the fully depleted mode when substrate bias is appropriate to merge front and back depletion regions. In other bias conditions these transistors behave like partially depleted ones. The transistors used in this study belong to this group.

Fig. 3.4.(a) shows the cross section of an $n$-channel SOI MOSFET. The corresponding equivalent circuit diagram which includes various current components is shown in Fig. 3.4.(b). In addition to the main MOS channel that is controlled by the polysilicon gate, two additional parasitic transistors exist. The parasitic bipolar transistor has a floating base (MOSFET body) and, therefore, can amplify the im-



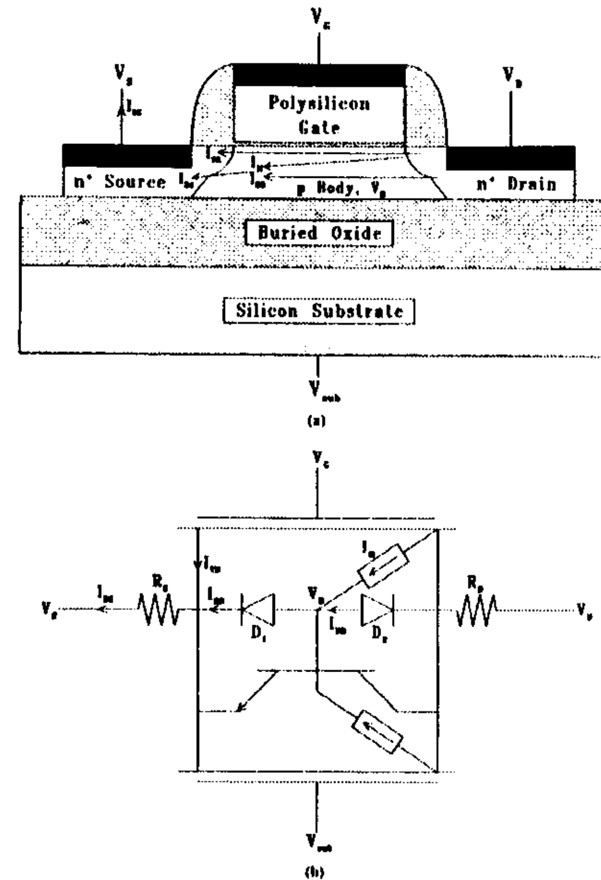


Figure 3.4: (a) The cross-section of $n$-channel SOI MOSFET, (b) The equivalent circuit showing parasitic components for $n$-channel SOI MOSFET [122]. The explanation of symbols: $I_{TR}$ is the current through the front transistor channel (main component of $I_{DS}$ terminal current), $I_{II}$ is the impact ionization current caused by front channel electrons, $I_{DB}$ is the current through the drain-to-body diode $D_2$, $I_{BS}$ is the current through the source-to-body diode $D_1$, $R_S$ is the source region extrinsic resistance, $R_D$ is the drain region extrinsic resistance.

pact ionization current. The gain of the bipolar transistor is very low (about 1-3). The back-gate transistor is a MOSFET controlled by substrate voltage through the buried oxide. Impact ionization current can also originate due to current flow at this back interface and therefore the second current source is drawn. The diodes $D_1$ and $D_2$ are the source and drain-to-body junctions respectively. The diode $D_2$ is always reverse-biased but the diode $D_1$ may be biased in forward direction by impact ionization current. The parasitic sidewall MOSFET transistors (see sec. 3.3) are not included in this picture.

Some advantages and problems related to SOI technologies are listed and shortly discussed:

- **simpler fabrication sequence in comparison with bulk CMOS.** For example [124], the bulk process requires sixteen major fabrication steps. Among them there are nine masking stages. If the SOI technique is employed the same goal can be achieved using ten major technological steps with seven masking stages. When the device shrinks, additional process complications are not required. The structures of the devices are simple and there are no epi and trench layers. Different types of devices (BJT, JFET, MOSFET, diode) can be integrated on one chip much easier too, which is due to the existence of a buried isolation layer.
- **high packing density.** This is due to the simplicity of shrinking devices, lowering nonused areas between devices and not needed wells. For CMOS technology with a minimum size of $1.5\mu m$ the typical isolation width between devices is about $3-4\mu m$, but SOI technique can easily exploit the minimum dimension as an interdevice separation. LETI has fabricated a processor which integrates 10000 transistors [125]. What is more, the SOI approach offers the possibility to construct 3-D circuits [126] using many subsequent stacked layers of oxide and silicon.
- **high operating speed.** This is caused by higher mobility and lower capacitances. The mobility increases due to the reduction of the vertical field in the channel in comparison with bulk devices. In fully depleted devices part of the gate voltage is dropped across the buried oxide and across the depletion region, rather than all across the channel as in the bulk case. The gate to the substrate and to the source/drain overlap capacitances are similar to those of equivalent bulk structures but diffusion and interconnection capacitances are significantly lower. This is due to three reasons:
  - the junction volume is smaller because the film thickness is much smaller than the typical depth of an ion implanted junction and there is no possibility to diffuse the dopants under field oxide;
  - the bottom and three sides of the junction are bounded by dielectric layers;
  - the dielectric constant for silicon dioxide is almost three times smaller than for silicon (see Tab. 2.1.).

  The critical parameters determining the value of capacitances are the thicknesses of buried and field oxides which should be greater than $0.1-0.2\mu m$ [124]. It means that the buried oxide thickness should be optimized to achieve reasonable compromise between circuit speed and radiation hardness (see sec. 3.3.).



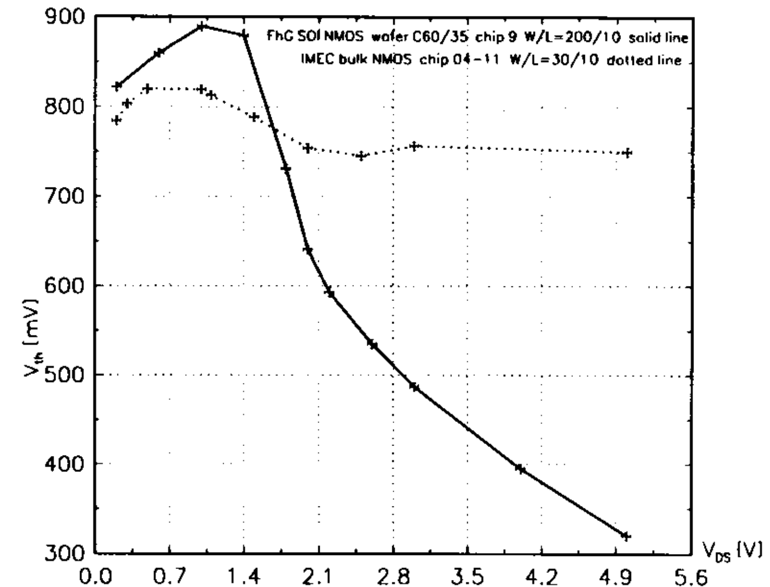


Figure 3.5: Threshold voltage $V_{th}$ vs. drain voltage $V_{DS}$. The big reduction of $V_{th}$ due to floating body effect is visible in comparison with bulk transistor.

- **totally immune to conventional latch-up phenomena.** This is due to the total isolation of each transistor and nonexisting parasitic p-n-p-n structure. However, the parasitic BJT exists in each transistor island (see Fig. 3.4.) and it can cause single-transistor latch phenomenon [127, 128].

There are several other advantages of SOI transistors: low leakage currents, faster turn-on, higher hot-carrier and radiation tolerance, and higher drive current.

The main disadvantage of SOI MOSFETs is floating body effect. It causes trouble with kink effect (see subsec. 2.1.5.) on the output characteristic. The floating body condition causes also significant (nonexisting in bulk devices) dependence of threshold voltage on drain bias. For higher drain voltage the reduction of the threshold voltage is observed and it is presented in Fig 3.5. The noise characteristic is exacerbated for SOI transistors (see sec. 5.4.), too. On the other hand, the subthreshold characteristic is improved by floating body effect [129, 130] but reduction in subthreshold swing can be so considerable, that at higher drain voltage, an almost vertical rise of drain current is observed (see Fig 3.6). This causes hysteresis in the subthreshold characteristic and single-transistor latch [127].

A detailed discussion of all shortcomings and advantages of SOI transistors is a very attractive topic in modern silicon technology but it is beyond the scope of this study.

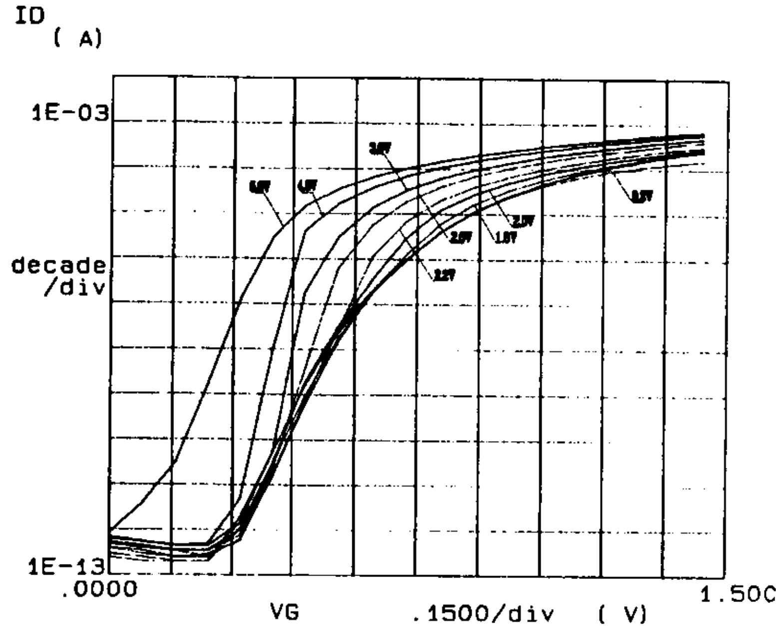


Figure 3.6: Subthreshold characteristics at several drain voltages $V_{DS}$. The reduction of subthreshold swing $S$ due to floating body effect is visible.

## 3.3 Radiation hardened technology

In this section the technological aspects of radiation hardening will be discussed. The major attention will be directed to the thermal oxidation process for growing the gate oxide which has the fundamental impact on the radiation sensitivity of ICs fabricated by given technology. Generally, the technological details are regarded as a trade secret by companies. However, some fundamental guidelines are available in literature concerning that topic. The text below will discuss the topic according to the reviews [65, 66, 67]. The second subsection of this section deals with layout consideration which can enhance the radiation hardness of designed ICs. The advices given there are directed to IC designers, and they can give a knowledge to designers how to achieve higher radiation tolerance of designed ICs for a chosen technology without changing any process parameters.

### 3.3.1 Technological considerations

The most frequently used criterion for optimization of the technological process for radiation hardness is minimizing the threshold voltage shift $\Delta V_{th}$. However, for a $n$-channel transistor such a criterion is not sufficient because of the possible compen-



sation of two radiation-induced charges: $Q_{ot}$ - oxide charge, $Q_{it}$ - interface charge, which occurs for NMOSFETs. The well-known chart (Fig. 3.7.) shows that effect. What is more, the relative ratio of these two components considerably depends on the dose rate. Next plot (Fig. 3.8.) proves that for a low dose rate, the total threshold voltage shift can have opposite sign even during all irradiation time. It means that the interface trapping dominates at low dose rates ($10^{-6} - 10^{0} rad/s$) over the trapping in the volume of the gate oxide. Therefore, the better criterion is minimizing both components: $\Delta V_{ot}$ (caused by oxide charge) and $\Delta V_{it}$ (caused by interface charge) individually, i.e. the radiation hardness testing must take into account not only $\Delta V_{th}$ but also subthreshold swing change $\Delta S$ (see section 4.5).

The first problem which should be discussed is the influence of the gate oxide thickness on the radiation hardness. The number $\Delta N_{ot}$ of holes generated by radiation in the oxide which are then trapped depends linearly on the oxide thickness $t_{ox}$:

$$\Delta N_{ot} = f_T Q(E, \mathcal{E}_{ox}, D) t_{ox}, \tag{3.2}$$

where $f_T$ is the fraction of the radiation-induced holes which are trapped in the oxide, $Q(E, \mathcal{E}_{ox}, D)$ is the radiation-induced charge density in the oxide depending on the energy of the ionizing radiation $E$, the effective field in the oxide $\mathcal{E}_{ox}$, and the dose $D$. On the other hand, the threshold voltage shift, due to the oxide charge $\Delta V_{ot}$, is the quotient of the oxide charge $\Delta Q_{ot} = q\Delta N_{ot}$ and the gate oxide capacitance $C_{ox}$:

$$\Delta V_{ot} = -q\Delta N_{ot} \frac{t_{ox}}{\epsilon_0 \epsilon_{SiO_2}}. \tag{3.3}$$

It means that the radiation-induced shifts of the threshold voltage for a MOS device would be expected to depend on the oxide thickness squared [15]. There are many simplifying assumptions which must be taken into consideration for deriving such a simple formula as (3.3),(3.2).

The square low, described above, changes to a cubic one for oxides thinner than the characteristic length $\lambda$ of hole trapping process: $\lambda \gg t_{ox}$. The quantity $\lambda$ is inversely proportional to the capture cross section $\sigma$, and to a higher one of two quantities: the density of hole traps $N_T$ and the density of radiation generated holes immediately after creation $N_0$ [68]. Additionally, the contribution of surface states depends on the gate oxide thickness $t_{ox}$ in a cubic manner because of square dependence of the average surface state density $N_{it}$ on oxide thickness $t_{ox}$: $\overline{N_{it}} \propto t_{ox}^2$ [68]. The next complication is dependence of the fraction $f_T$ of the radiation-induced holes, which are trapped in the oxide, on the oxide thickness $t_{ox}$. All these facts result in a power low:

$$\Delta V_{th} \propto t_{ox}^n, \tag{3.4}$$

where the exponent $n$ is observed in a range from between 1 and 3. Generally, for the flatband voltage shift $\Delta V_{FB}$, the value of $n$ is between 1 and 2 for dry-oxygen-grown and steam-oxygen oxides, and between 2 and 3 for oxides grown in a dilute dry-oxygen ambient. For oxides thinner than 20 $nm$, the radiation-induced threshold voltage shift decreases much faster than it could be predicted by the power law.

The influence of the substrate preparation before gate oxide growing on the radiation sensitivity can be recapitulated as below:

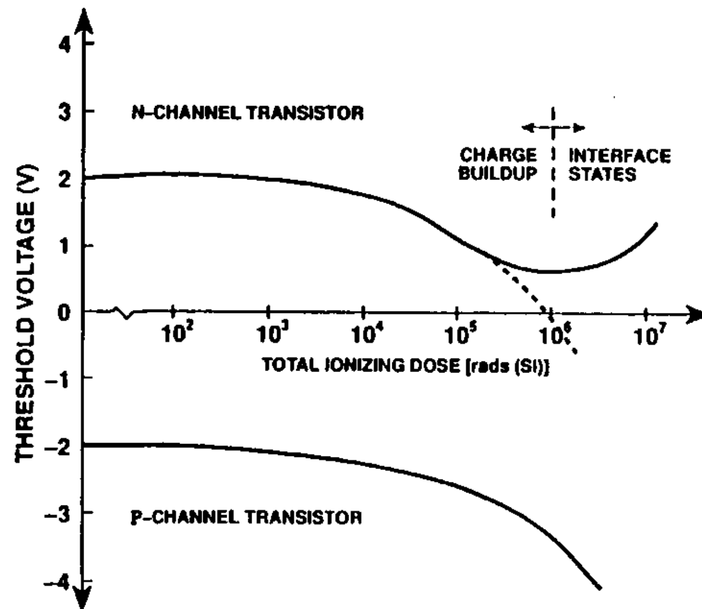


Figure 3.7: Typical curves of threshold voltage shift $\Delta V_{th}$ vs. total $\gamma$ dose $D$ for $p$- and $n$-channel MOSFETs. The curve for NMOS transistors shows minimum and subsequent changing back, related to compensation between oxide trapping and interface trapping.

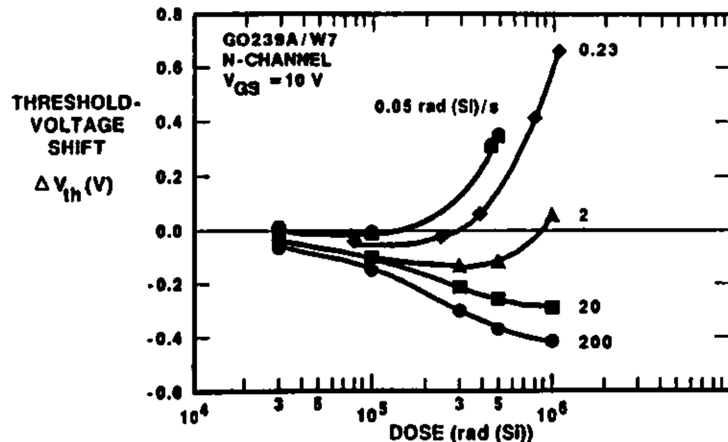


Figure 3.8: Threshold voltage shift $\Delta V_{th}$ versus $\gamma$ dose rate $\dot{D}$ for n-channel MOSFET for several values of dose rate. For dose rate below 1 $rad/s$, negative charge of interfaces traps dominates [63, 64].
(Presented by P.S. Winokur at MUG meeting at CERN)



- the oxidation performed on < 111 > substrate orientation shows a higher growth rate under identical conditions than on < 100 >, and therefore leads to a bigger threshold voltage $V_{th}$ before irradiation which results in the increase of the radiation-induced threshold voltage shift $\Delta V_{th}$ by a factor of 1.5 to about 2. This phenomenon causes a great trouble for the SOI technology, where oxides are grown simultaneously on different orientations: on the top of the silicon island and on its edges. This is a so-called sidewall effect (see Fig. 3.11, 3.10.). There is no other radiation tolerance problem with substrate orientation despite the fact that the orientation < 111 > has higher interface state density;
- the lightly doped epitaxial grown layer on heavily doped substrate ($\nu$, $\pi$-type) is effective in preventing radiation-induced latchup;
- the density of silicon surface defects, such as stacking faults, edge dislocations and contaminations (especially by iron) are associated with increased radiation damages. The radiation tolerance can be improved when the final step of the cleaning procedure is a dilute fluorine HF rinse rather than a deionized water rinse. The variability in radiation-induced threshold voltage shift $\Delta V_{th}$ is greatly increased by a field oxide growing on the active area and stripping it before gate oxide fabrication [69].

The crucial point in the fabrication of the radiation hardened devices is choosing the optimal conditions of the thermal growing of the gate oxide. These conditions are the temperature during oxide growth subsequent annealing, and the composition of the atmosphere in the oxidation furnace. Generally, two kinds of atmosphere in the furnace are used: dry oxygen and steam. It was shown that there is an optimal temperature but different for different growth ambients. The optimum means that the radiation-induced threshold voltage shift $\Delta V_{th}$ has a minimal value in function of oxide growth temperature. For oxides grown in dry oxygen, the optimum temperature is about 1000°C [69], but for steam oxides it is lower, in the range of 850 – 925°C. The existence of such an optimal temperature can be understood with help of the viscous shear flow model [70, 71]. Below the optimum temperature, the viscosity of the oxide is high enough that it cannot flow to provide stress relief during the growth process. When the oxide grows, stress at the interface increases and causes strained bonds and disorder at the interface. The presence of water lowers the viscosity of the oxide at any given temperature. As a consequence, the optimum growth temperature is lower in a steam ambient than in a dry-oxygen ambient. Despite this, it is possible to develop both the steam-grown and dry-oxygen-grown processes in such an optimized way, that they show comparable radiation hardness.

It was found that the hardness is degraded drastically when the growth rate is reduced by means of decreasing oxygen partial pressure if nitrogen is the carrier gas, but it is relatively unaffected if argon is used [69].

For commercial devices, a commonly used method is the incorporation of 1.1.1.-trichloroethane (TCA) into the oxidation ambient. It improves the oxide breakdown strength, enhances the minority-carrier lifetime, increases the oxide growth rate and reduces the size and the density of oxidation-induced stacking faults. Simultaneously, TCA contamination affects the radiation hardness considerably. It can act profitably for steam oxides, but in dry-oxygen its influence depends strongly on time. The mini-

mum interface state density is observed at TCA purge time $\approx 2min$. The degradation for shorter and longer times increases and this increase is faster for bigger gate sizes, but the optimal purge time is nearly the same for all sizes [72, 73]. Similar effect was observed for fluorine $NF_3$ which shows optimal purge time $\approx 10s$.

It could seem that high temperature annealing of the gate oxide should profitably affect the radiation hardness due to the reduction of the post process density of the charge in the oxide. However, it was found that a temperature greater than about 925°C even for short time ($> 20\ min$) significantly degrades the hardness. The annealing in nitrogen is not sufficiently different from annealing in argon. The decrease of the hardness above temperature $\approx$ 925°C appears to be a threshold effect; hence, a longer annealing below 925°C should reduce the flatband voltages acceptably without seriously degrading the radiation hardness. The 90-min annealing at 850°C in $N_2$ seems to be satisfactory [69].

The maintaining of the oxidation environment as clean as possible is always very important for achieving a good hardness of the technological process. The cleaning of the oxidation tube with HCl before oxidation has a beneficial effect on hardness. The concentration of mobile alkali impurities must be minimized.

On the other hand the intentional contaminations incorporated into the gate oxide have shown an improvement in the hardness. The chromium doping into gate oxide made by diffusion has a good influence on decrease of radiation-induced interface buildup. Similarly, ion implantation of aluminium, chromium, nitrogen, oxygen, neon, sodium, argon, xenon and cerium improve the radiation hardness. The improvement achieved in this way is observed only under positive gate bias during irradiation, whereas under negative bias degradation occurs. Such an implantation creates electron traps by displacement damage in the oxide (not by the chemical nature of the implanted species). Therefore electron trapping compensates the normal hole buildup.

There are several other gate materials which are sometimes used in MOS structures:

- dual-layer silicon nitride/oxide (MNOS structures);
- oxynitride;
- nitrided thermal grown silicon dioxide;
- aluminium oxide.

However, the best results for radiation hardening are achieved using a pure, undoped silicon dioxide layer for the gate insulator. Other materials are used very seldom, only for specialized applications.

Despite the fact that metal (aluminium) gate electrode devices are commonly considered as more hardened, there are no reasons for the difference in hardness for polysilicon vs. metal gate technologies which originate directly from the type of material itself. Modern ICs are fabricated using the self-aligned method to form source/drain areas (see sec. 3.1.). It requires polysilicon or other refractory materials as a gate electrode. In a metal gate technology, the gate dielectric is grown very near the end of the process, so that very little additional processing and no high-temperature steps are required after its formation. In a polysilicon technology, a large number of steps must be performed after the gate oxide growth. One key factor in maintaining the hardness of the gate oxide, is the minimization of both the



temperature and time of high-temperature processing steps after the gate oxide is grown. For example the P-glass flow at the temperature in the range 1000 – 1100°C is necessary (see sec. 3.1.) and it is a problem to achieve sufficient smoothness of topography below 900°C. One method is using $SiO_2$ doped with both phosphorus and boron as an intermediate dielectric. In other cases, it is necessary to develop patterning capabilities for rough topography.

Also the implants for threshold voltage adjustment and source/drain regions formation which are made after gate oxidation cause the damages of the gate oxide. Generally, such damages affect the degradation of hardness. As was mentioned above, the improvement of hardness by means of dopant implantation into gate oxide is restricted only to a particular bias regime. Processes that in themselves cause radiation damage, such as implantation through the gate oxide, electron-beam metallization, or electron-beam lithography, should be avoided whenever possible.

The sintering of the final metallization reduces the surface state density. The improvement of radiation hardness is observed when the sintering temperature increases in the range of 300 – 550°C and pure nitrogen should be used as a forming gas (the inclusion of hydrogen is detrimental).

Among other triggering mechanisms (see sec. 3.1.), the latchup in CMOS ICs can be caused by radiation-generated photocurrents. The conventional technological techniques for latchup prevention are shortly listed below:

- the current gains $h_{FE}$ of two parasitic BJTs can be reduced by lowering of the minority-carrier lifetimes. Such a reduction is achieved by deep centres introducing into substrate or well. It can be made by means of gold doping or neutron irradiation. The deleterious effect of such method is excess leakage. Another method for reducing the gain of vertical transistor is using a high-doped buried-layer under well;
- the shunt resistors, existing in the substrate or well between emitter and base of parasitic BJTs, can be reduced by use of an $n$ ($p$) epitaxy over $n^+$ ($p^+$) substrate. A more conductive substrate reduces the lateral resistance under the $p^+$ ($n^+$) source/drain.

The existing latchup screen techniques can be invalidated to a certain degree due to an additional phenomenon called latchup window [74]. This phenomenon appears in an IC when more than one latchup current path exist. In the different range of dose rate different paths can be activated and several subsequent latch and no latch regions appear along the dose rate axis.

Several other technological problems are related to the SOI technology which is commonly considered as more radiation hardened than the bulk one due to the better devices isolation. It was found that SOI MOSFETs tested for transient ionizing radiation effects and SEU (single event upset) phenomena show extremely encouraging improvement in comparison to SOS and surpass bulk CMOS. These devices are also free from classical latch-up action . However, the measured transient radiation-induced photocurrent is larger than expected due to the parasitic bipolar action (see Fig. 3.4. and sec. 3.2.). This problem is bigger for scaled down devices [75]. For total dose hardening, the SOI structure gives also additional problems related to back- and side-interfaces. After irradiation these interfaces open additional leakage paths.

It is clear that the sensitivity to the ionizing radiation of the back-channel leakage path depends on the quality of the back silicon/buried oxide interface and on the initial threshold voltage $V_{bth}$ of the parasitic back-gate MOS transistor between source and drain. The formation of the back interface is significantly altered and the properties of it are also completely different. At the first, the oxide thickness at the back gate is significantly bigger ($\approx 380\ nm$ in comparison to $\approx 25\ nm$). It results in a big initial threshold voltage $V_{bth}$ ($\approx 12V$) and a very big radiation-induced threshold voltage shift $\Delta V_{bth}$ (see equations (3.2),(3.3)). It means that a reduction in the thickness of buried oxide is beneficial. The quality of the back interface and the whole top silicon layer depends very strongly on the postimplant annealing condition. The differences in the TEM pictures of the top layer of the SIMOX wafer after various annealing temperature are very significant and easily visible [119]. It means that the post implant annealing temperature is a crucial process parameter for the radiation sensitivity of the back gate parasitic MOS transistor, and a higher temperature ($\approx$ 1300°C) is better. The radiation characteristics of the back channel can be improved by means of a lower oxygen dose for the buried oxide implant, or by adding a low-dose nitrogen implant. This improvement is attributed to the decrease of the buried layer thickness or to the formation the interfacial oxynitride layer [77]. A very beneficial solution is using a highly oxygen-doped polysilicon layer under the silicon island at the top of the buried oxide (see Fig. 3.9.). Such a layer is formed using dose level of $1 \times 10^{18} cm^{-2}$ at $80keV$ and annealing at 1150°C for $2\ h$ in $N_2$. It provides a large number of deep traps for electrons to compensate the positive charge buildup from irradiation in the buried oxide [78, 79, 80]. However, such a low annealing temperature results in a very bad quality of the silicon film and therefore the transistors must be formed in epitaxial Si layer.

For fully depleted SOI transistors, the radiation sensitivity may be greater than in those made in thick SOI films where the top surface is shielded by the neutral region of the transistor body from changes in the back interface charge. When the device substrate voltage is chosen to accumulate the back interface (for fully depleted), the threshold voltage shift $\Delta V_{th}$ is seen to be lessened. However, in this mode of operation the subthreshold swing and the transconductance degradation are worse than when the back interface is depleted [123]. In another study [76], it was found that the radiation sensitivity of the front channel device does not depend on the back gate bias. However, a negative substrate bias reduces the back channel radiation-induced threshold voltage shift $\Delta V_{bth}$ due to sweeping the radiation-generated holes away from the back interface. Therefore this has a significant impact on the leakage current in the subthreshold range of the front channel device characteristic. A negative bias of the IC substrate is not appropriate for an IC containing both types of transistors NMOS and PMOS. The second complication is an additional power supply voltage for the IC. Another solution for back gate parasitic transistor hardening is a deep boron implantation [82] which increases the threshold voltage $V_{bth}$ and keeps this transistor closed longer during irradiation.

Another leakage path in a SOI NMOS transistor is the sidewall parasitic transistor. The influence of the radiation-induced action of such a transistor on the subthreshold curve is shown in Fig. 3.10. The sidewall transistor has a bigger threshold voltage shift



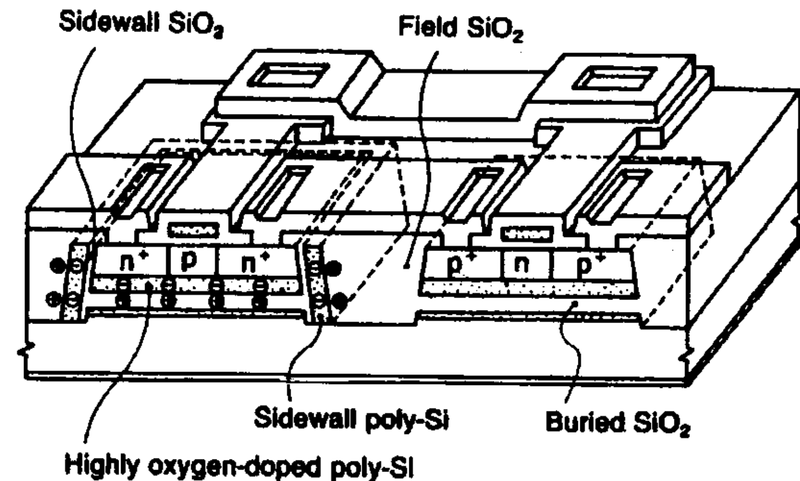


Figure 3.9: The method for improving radiation hardness of SOI CMOS/SIMOX devices by means of the formation of a poly-Si layer under and at the edges (SGP) of the silicon island [80].

and therefore causes a characteristic bend on the subthreshold curve. The threshold voltage shift is bigger because the gate oxide in the sidewall region is thicker (see Fig. 3.11.(a).) than at the top of island. This is caused by another silicon crystal orientation on the island wall than at its top. If the LOCOS technique is used to form a transistor on the SIMOX wafer (see Fig. 3.3.) the field oxide is present at the edges of the island and a big radiation-induced charge buildup in it causes a similar effect. The method to prevent the sidewall effect is a selective boron implant performed at the edges of the silicon island along the whole length of the transistor from the source to the drain. This implant increases the doping in these more radiation sensitive regions and in this way increases the initial threshold voltage $V_{th}$ of the sidewall parasitic transistor. Another method to kill the sidewall transistor is related to a special design of the source region (see subsec. 3.3.2.). The results of another process technique for sidewall hardening, called passivation of edges, were reported in [81], but details concerning the process were not given. An interesting and effective method was introduced by Izumi et. al. [78, 79, 80]. The special vertical polysilicon layer was used (see Fig. 3.9.). The sidewall polysilicon is connected to the substrate and is constructed so as to surround the sidewall of the n-channel MOSFET. This lateral isolation technique is called screening with grounded polysilicon (SGP). When the NMOSFET is irradiated, electrons induced by positive charges, which are generated and trapped in the field $SiO_2$ layer, appear only in the sidewall polysilicon layer and

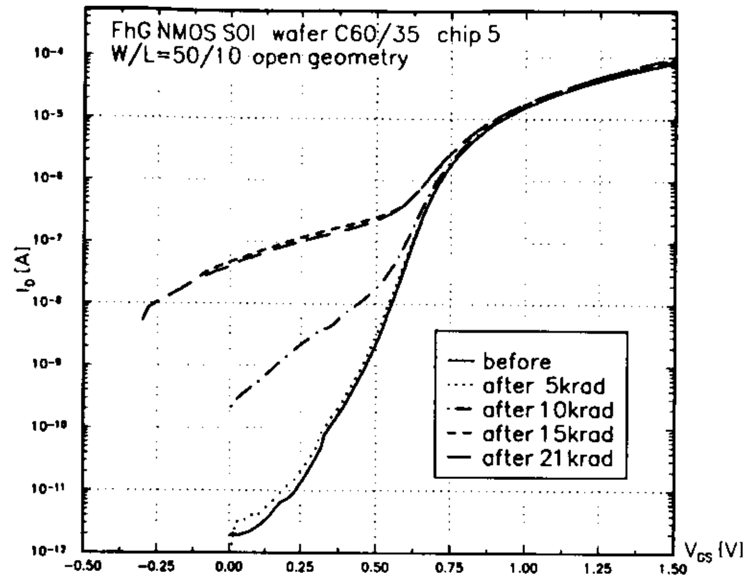


Figure 3.10: The sidewall effect on the subthreshold characteristics of open geometry SOI MOSFET appearing after irradiation up to 20 *krad*.

the substrate near the $Si/SiO_2$ interface. This indicates that the sidewall polysilicon layer acts to shield the body region from the positive charges in the field $SiO_2$. On the other hand, positive charges trapped in the thin sidewall $SiO_2$ layer can induce electrons into the sidewall surface of the body region. However, the number of these positive charges can be sufficiently decreased by reducing the thickness of the sidewall $SiO_2$ layer. In this way, such transistors can work perfectly at a 2 *Mrad* total dose.

A very interesting behaviour of the sidewall leakage at high total dose level was observed [63]. The action of a sidewall transistor, easily visible at lower doses disappears when the total dose achieves 10 *Mrad* value. It is caused by a big negative interface charge buildup, which shifts the threshold voltage of the sidewall transistor in the positive direction and turns off the sidewall leakage.

There are several other reasons which can degrade the radiation hardness:

- process-induced radiation damages may result from plasma etching steps, x-ray lithography, x-ray generated during thermal evaporation of metals and UV generated during sputtering;
- passivation layers, which are the final processing steps;
- high-temperature die bonding;
- packaging;
- package sealing (using a forming gas instead of nitrogen during sealing, the hardness can be improved four times).



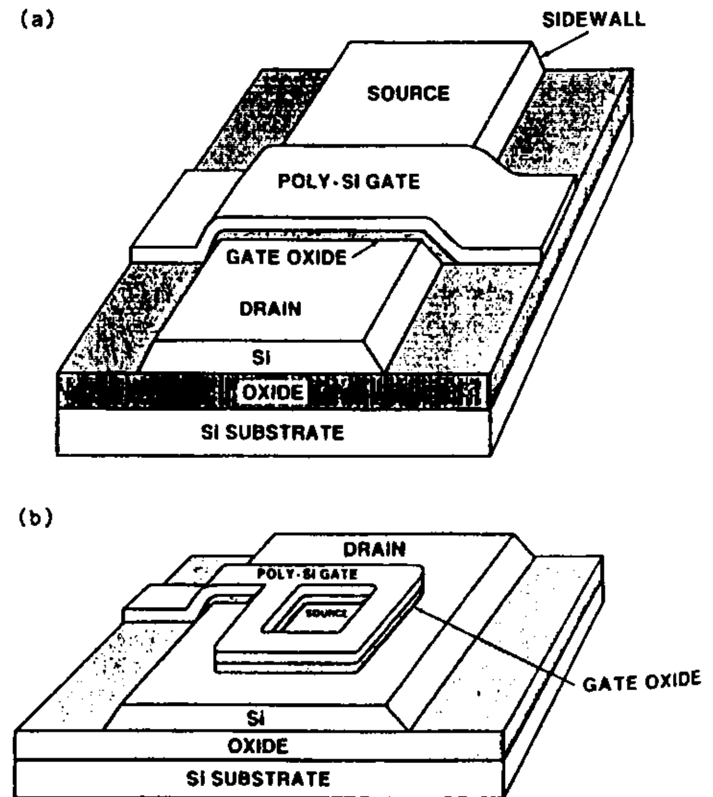


Figure 3.11: The explanation of the origin of the sidewall effect in open geometry SOI MOSFET (a), and its prevention by designing an edgeless SOI transistor (b).

### 3.3.2 Layout considerations

In modern technologies the dominant total dose radiation effect is field oxide leakage. This is due to the existence of parasitic field oxide transistors (called FOXFETs) which are very sensitive to the radiation-induced charge buildup because of the thick unhardened oxide. The number of such potentially existing parasitic structures can be minimized by a careful layout design and an appropriate doping of more sensitive places in the devices and between them (see subsec 3.3.1.) or by using hardened field oxides.

The designing of edgeless (i. e. in close geometry) (see Fig. 3.11.(b).) transistors is the most effective method to maintain good subthreshold characteristics, down to the level of a picoampere of the drain current, for both bulk and SOI NMOSFETs. In such a layout geometry there is no possible leakage path between the source and

the drain. However, that solution takes a large amount of IC surface and therefore is inefficient particularly for multiple-input gates. Another method for suppressing detrimental radiation-induced leakage paths will be also discussed below.

For bulk transistors, the close geometry layout prevents a radiation-induced widening of the transistor due to electron accumulation near the edges of the active area by the positive charge buildup in the field oxide. This effect is shown on the subthreshold characteristics of four irradiated NMOS transistors in Fig. 3.12. The bend in the subthreshold curve and the drastic change in the subthreshold swing is caused by the edge field oxide transistors. The field oxide transistor has a huge radiation-induced threshold voltage shift $\Delta V_{th}$ due to the large thickness of the field oxide. Even if the potential of the polysilicon gate connection over the field oxide is strongly negative (-9V), the drain current through such a field transistor is several orders of magnitude higher than other leakages. The high value of the subthreshold swing is attributed to the high interface state density under the field oxide. The method to suppress radiation-induced transistor widening in the open geometry transistor is achieved by using a chan-stop layer under field oxide (see sec. 3.1.) or by implanting a highly doped $p^+$ guardring around the active area of device and making an extension of the gate oxide over the guardring (see Fig. 3.13.).

Another leakage path for bulk transistor can be opened after irradiation between

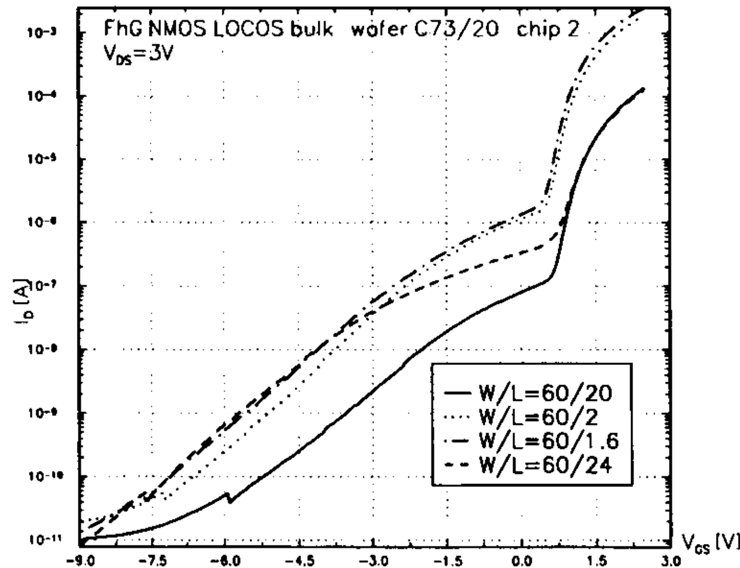


Figure 3.12: The radiation-induced leakage current under field oxide visible on the subthreshold characteristics of the open geometry bulk NMOSFET appearing after irradiation up to 20 *krad*.



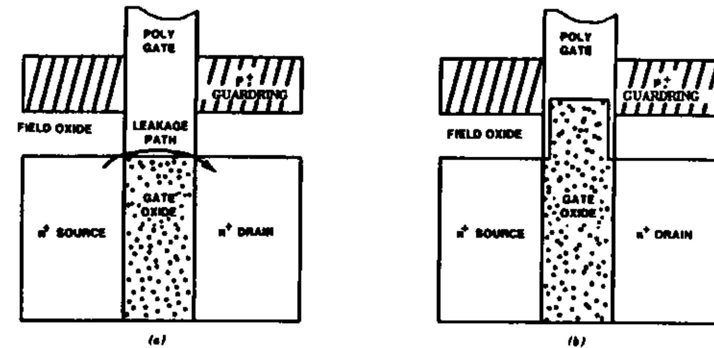


Figure 3.13: The illustration of a possible radiation-induced leakage path between the n-channel source and drain regions (a), and the method of its prevention by means of an extension of the gate oxide over the guardring (b) [65].

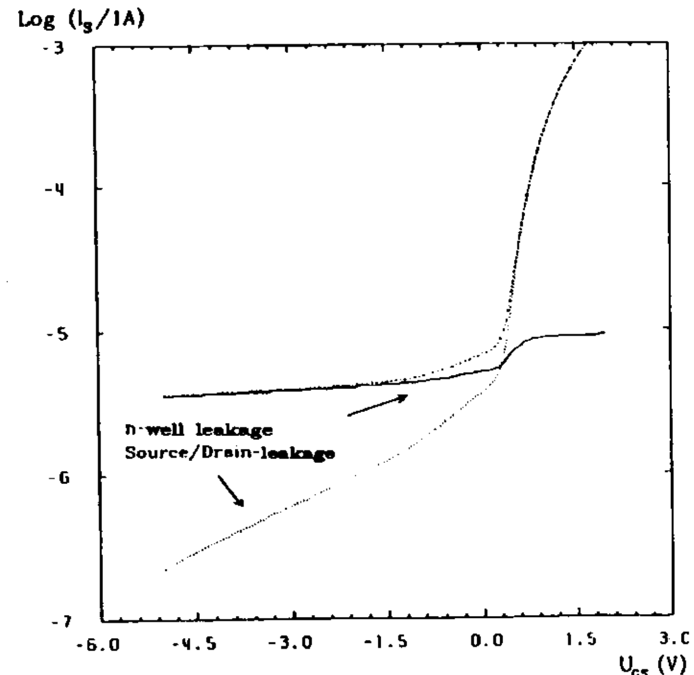


Figure 3.14: The subthreshold characteristics of the NMOSFET (ELMOS W/L=60/3) after irradiation of $\gamma$ dose 35 *krad*. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured at: dotted line - $V_{DS} = 5V, V_w = 0V, V_{DS} = 0V$ (current through the NMOSFET), full line - $V_{DS} = 0V, V_w = 5V, V_{DS} = 0V$ (current through the FOXFET), dashed-dotted line - $V_{DS} = 5V, V_w = 5V, V_{DS} = 0V$ (sum of the currents through the NMOS and FOX transistors).
(Presented earlier in [6].)

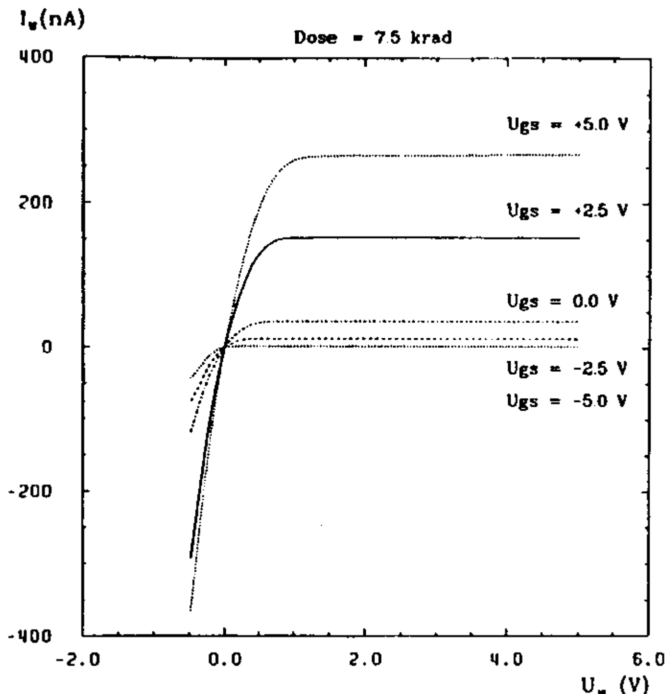


Figure 3.15: The output characteristics of radiation activated FOXFET. The $n$-well acts as a FOXFET drain. The source is grounding. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$.
(Presented earlier in [6].)

the $n$-well region and the source of NMOS transistor. This component of source current is presented in Fig. 3.14. and in Fig. 3.15. as a current through the $n$-well region. The FOXFET structure was activated by radiation (7.5 *krad*) where the $n$-well acts as a drain and the polysilicon gate connection acts as a gate (see Fig. 3.16.). The output characteristics of this FOXFET were measured and this measurement proves that the leakage to the $n$-well under the field oxide is a big part of the radiation-induced leakage current.

For SOI transistors, a close geometry transistor layout eliminates the sidewall effect. Fig. 3.18.(a) shows a very good radiation behaviour of the subthreshold characteristic for a transistor with the gate electrode of the octagonal polygon ring with the width of 10 $\mu m$. Only a small (5 $\mu m$) gap made in such a "ring" transistor results in a pronounced exacerbation of its subthreshold behaviour Fig. 3.18.(b). It is possible to suppress the sidewall leakage by a special design of the source region. Two similar methods are shown in Fig. 2.8 and Fig. 3.17. One can use a special



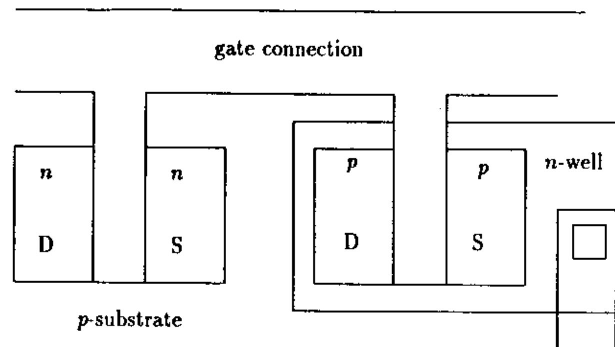


Figure 3.16: The fragment of test structure layout (ELMOS). The channel of FOXFET (leakage path) is opened under the field oxide covering by the gate connection.

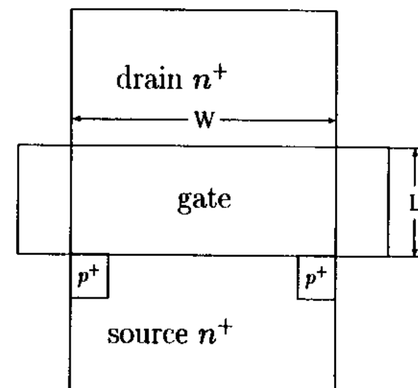


Figure 3.17: The design of the source region of SOI NMOSFET to suppress radiation-induced sidewall leakage current. The channel-stop technique.

selective $p^+$ implant (called a channel stop) in the source region of NMOSFET, close to the gate at the edges of the island (see Fig. 3.17.). This implant causes that there is no source region for the sidewall transistor [83]. A similar effect can be obtained using the split-source technique (see subsec. 2.1.5.) with $p^+$ contact at the edges of the source region (see Fig. 2.8.). These methods lead to a reduction of the transistor width $W$, and the effective width $W_{eff}$ must be measured and taken into account in the circuit design.

Generally, for PMOS transistors there are no sidewall and channel widening effects because the characteristic of the parasitic transistor shifts deeper under the characte-

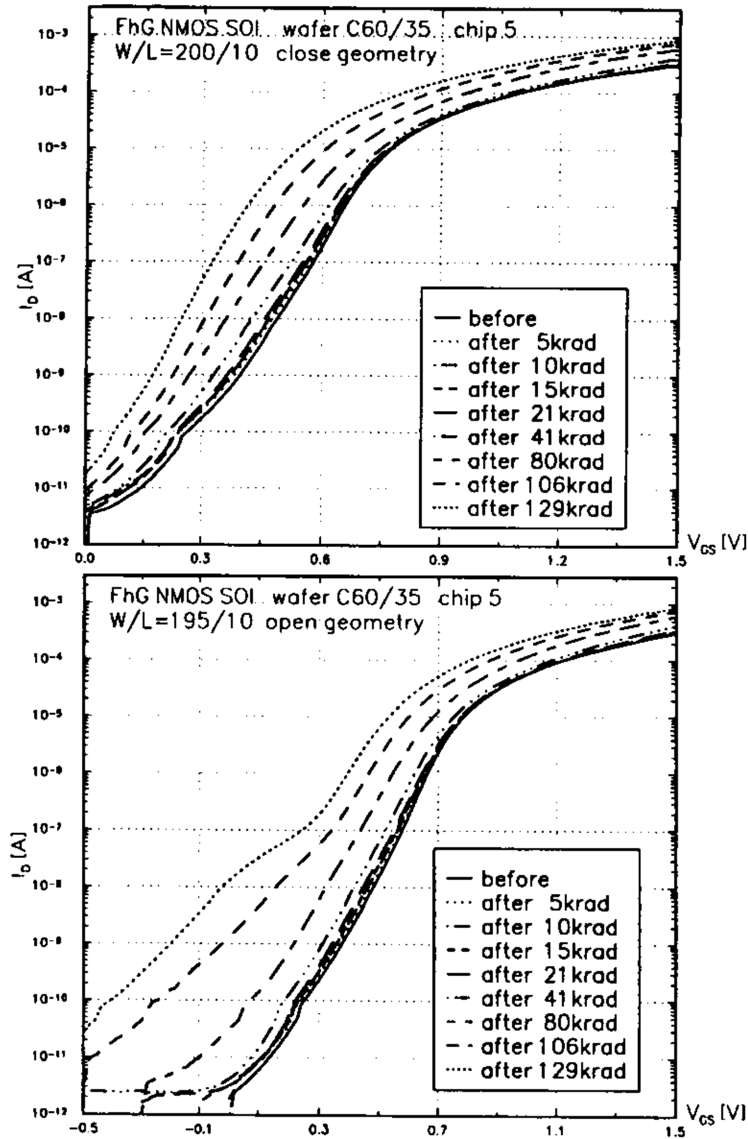


Figure 3.18: The subthreshold transfer characteristics of SOI NMOSFETs: close geometry (a), and similar one with small gap (b), before and after subsequent irradiations up to 128 *krad*.



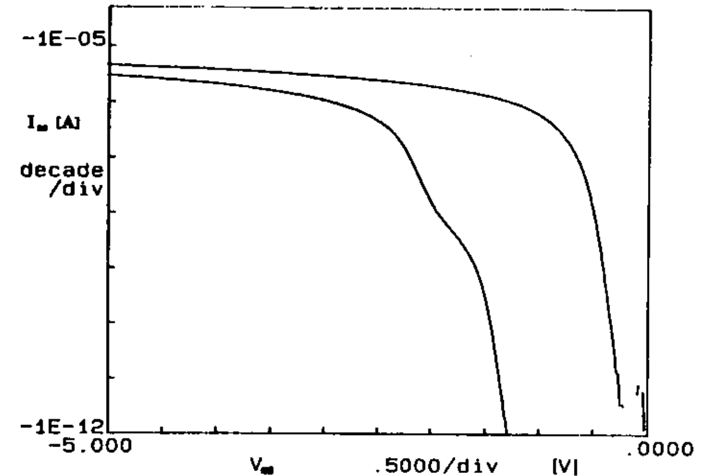


Figure 3.19: The subthreshold characteristics of SOI PMOSFET (FhG wafer C75/47 chip W/L=50/50) before irradiation and after $\gamma$ dose 125 *krad*. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$. Measured at $V_{DS} = -50mV, V_{BS} = 0V$.

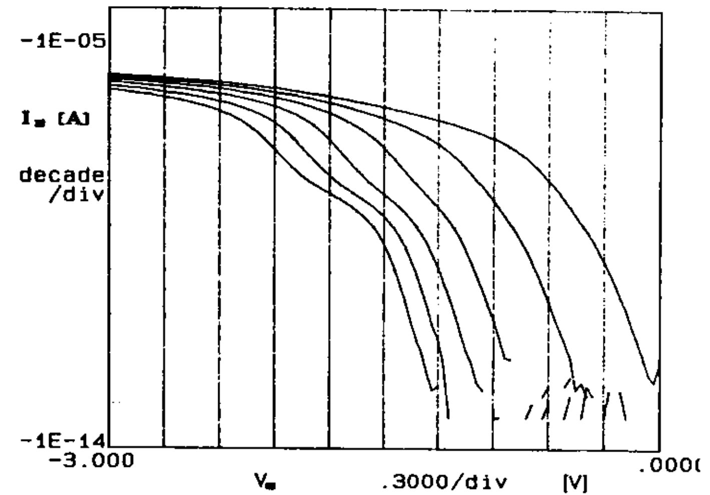


Figure 3.20: The changes of the subthreshold characteristic of SOI PMOSFET (FhG wafer C75/47 chip W/L=50/50) irradiated up to the dose of 125 *krad* when the back gate voltage increases from $0V$ to $12.5V$ with the step $2.5V$. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$. Measured at $V_{DS} = -50mV, V_{BS} = 0 - 12.5V$, step $2.5V$.

ristic of the main transistor. Therefore, the characteristic of the parasitic transistor cannot protrude from the main transistor characteristic. However, for the PMOS SOI transistor, an effect similar to the sidewall effect was observed when the transistor was irradiated with a grounding back gate. Fig. 3.19. presents such a situation when the threshold voltage shift of the front gate is bigger than the shift of the sidewall transistors. The distortion of this characteristic can be corrected by a positive bias applied to the back gate (see Fig. 3.20.).

# Chapter 4

# Threshold voltage shift and transconductance degradation

The damages in MOS transistors caused by $\gamma$ radiation are related to ionizing effects in the $SiO_2$ layer. The charge is generated while a quant is passing through $SiO_2$. This charge is frozen in $SiO_2$ because of the low mobility of charge carriers in insulators. The displacement damages caused by neutron radiation, commonly discussed in the case of bipolar electronics, are negligible in devices like MOSFETs where the surface conduction mechanism is dominant.

The subsequent processes occurring in $SiO_2$ during irradiation are listed below together with a short discussion of their physical mechanisms and models. The two next sections deal with the influence of radiation-generated charges on the two most important parameters of MOSFETs: threshold voltage $V_{th}$ and transconductance $g_m$. Then the separation of bulk and interface radiation effects are described. The most important part of this chapter presents the results obtained while testing the radiation sensitivity of transistors fabricated by the factories mentioned already: IMEC, EL-MOS and FhG. A great deal of attention is paid to the SOI transistors because such a technological solution is a new tendency in VLSI silicon MOS technology and radiation hardening of electronics. The discussion concerns the devices with and without the lightly doped region (LDD) near the drain. A separate section is dedicated to the radiation influence on the kink effect which is the most difficult problem limiting the application of SOI MOSFETs.

The tests were carried out by means of using the radiation source $Cs^{137}$ of activity 5 $Ci$. The value of dose rate in the place of test structure irradiation was measured by means of using the liyhium fluoride $LiF$ thermoluminescent dosimeters TLD-100 produced by the Harshow company. Small dosimeters were irradiated for a short time about 15 $min$. The results indicates that the dose rate was at the level of $\approx 2.9\ krad/h$.

All data presented in this chapter are original data obtained by the author by means of using the homemade equipment for static characteristic measurement or the HP4145B semiconductor parameter analyzer .





## 4.1 Mechanisms and processes leading to degradation

The degradation of MOS structures during irradiation by $\gamma$-ray is related to the ionizing effects in the silicon dioxide layer. The whole ionizing-radiation-induced process taking place in MOS a structure consists of several subsequent steps:

- **energy deposition in $SiO_2$.** High energy photons interact with matter primarily by Compton scattering, therefore most of its energy is carried away and deposited in $SiO_2$ by secondary electrons. The average energy of secondary electrons for $Co^{60}$ source ($1.17MeV$ and $1.33MeV$) is $\overline{E}_e \approx 0.66MeV$ and for $Cs^{137}$ ($661keV$) $\overline{E}_e \approx 0.32MeV$. The contribution from the photoelectric effect is larger for a caesium than for a cobalt radiation source because the cross-section for this process increases with decreasing photon energy as follows $\sigma \propto Z^4(h\nu)^{-3}$. It implies that there is some amount of secondary electrons with energy nearly the same as photon energy.
- **charge generation in $SiO_2$.** On the average each 17 $eV$ (see Tab. 2.1.) of energy deposited in the oxide results in the formation of one electron/hole pair.
- **recombination** of created e-h pairs occurs only during a few picoseconds when electrons have not been swept out of the oxide, yet. After this short period of time the survived holes stay almost where they were created. When the oxide is irradiated by 1-MeV electrons, the stopping power is $\frac{dE}{dx} = 1.6\ MeVg^{-1}cm^2$, $N_0 = 2.13 \times 10^5\ pairs/cm$ and the mean separation between e-h pairs is $\lambda = \frac{1}{N_0} = 46.8nm$. In $SiO_2$ the initial distance $r_t$ between the hole and its corresponding electron after they reach thermal energy is on the order of 5 or 10nm. When $\lambda > r_t$ the geminate recombination model is appropriate. The most important parameter is fractional yield $Y = \frac{N_{e-h}}{N_0}$ where $N_{e-h}$ is the number of e-h pairs which avoid recombination in the limit as $t \rightarrow \infty$. For $Co^{60}$ (and for 12-MeV electrons) radiation at a field 1 $MV/cm$ almost 80% of charge does not recombine [84]. The remaining holes must be trapped in the oxide and increases the positive charge buildup.
- **electron and hole transport in $SiO_2$.** These two kinds of charge transport are strongly different due to the huge difference in mobility for holes and electrons (see Tab. 2.1.). The electrons and holes which have avoided initial recombination are free to undergo transport in the $SiO_2$ layer in response to any electric field present in the oxide. The electrons are relatively highly mobile, and they are rapidly swept out of the oxide and collected at the positive electrode in times of the order of picoseconds. The hole transport is rather anomalous in nature, being highly dispersive in time (typically, it takes several seconds at room temperature) due to a wide distribution of transit times of the holes through the oxide film. The best model to describe dispersive transport in amorphous semiconductors and insulators is the generalized CTRW (continuous-time random walk) model. This stochastic model can be attributed to different microscopic charge transfer mechanisms. The two most important of them are the trap-mediated valence band hole conduction and the hopping transport via localized

trap sites within the $SiO_2$ bandgap. The second of them are more suitable to silicon dioxide because of its independence of temperature. It relies on carriers moving directly between localized trap sites via phonon-assisted tunneling processes. The small polaron hopping theory is the best mechanism explaining the observed characteristics of hole transport in $SiO_2$.

- **hole trapping in the bulk of $SiO_2$** is the long-term radiation effect in MOS structure, which causes negative threshold and flat band voltage shift. The $E'$ centres which were observed by the ESR method [22] are the dominant type of hole traps in the bulk of $SiO_2$. They are trivalent silicon defects associated with an oxygen vacancy in the $SiO_2$ and they are described as $[(Si-O_3) \equiv Si\cdot]$. The negative electron trapping is not observed in thermal $SiO_2$ under irradiation. Although surface trap densities for holes and electrons have similar values at the level of $10^{12}cm^{-2}$, the capture cross-section is three orders of magnitude higher for the hole than for the electron. The electron trapping cross-section can be enhanced by implantation (see sec. 3.3.).
- **generation of interface states at the $Si/SiO_2$ interface.** During irradiation the typical "U-shaped" energy distribution of interface traps (see chap.2.) is distorted by appearance of peaks which are superimposed on this spectrum. The measurements [94] have reported a larger number of interface traps in the upper half of the $Si$ bandgap than in the lower half (a peak about 0.25eV above midgap). The explanation of such a spectrum takes into consideration two amphoteric traps $P_{b0}$, $P_{b1}$ identified by ESR method [85]. If $P_{b0}$ (the same like $P_b$ which has the structure $[(Si_3) \equiv Si\cdot]$) and $P_{b1}$ (which has probably the structure $[(SiO_2) \equiv Si\cdot]$) both increases during irradiation, the tending of $P_{b1}$ toward the upper part of the bandgap should lead to a radiation-induced interface trap distribution with more traps in the upper half of the bandgap. However, other measurements [86] show that the interface state buildup consists entirely of $P_{b0}$ centres and $P_{b1}$ centres have no buildup.

For describing the formation of interface traps many models were developed [25, 87]. They can be divided into three classes. These three fundamental mechanisms give their own contributions to the total interface state buildup. The main process for radiation-induced interface generation is the two-stage model proposed by McLean [88]. In the first stage, holes transported through the oxide interact with the oxide lattice to free positive $H^+$ ions existing in it. The energy for the ion release is obtained from the energy exchange between the transported holes and the lattice via the polaron-hopping process. The hole is annihilated by an electron initially involved in bonding the ion to a $Si$ atom $Si-H$, and the positive charge is then carried out by the ion. The defect site remains in a natural charge state. At the second stage, the released ion is transported by a field-assisted hopping mechanism similar to the hole transport. When it reaches the interface the reaction forming interface trap occurs. The positive bias during this stage is necessary to move a positive ion to the interface. The second type of model is related to the transport of holes and the trapping of them at the $Si/SiO_2$ interface followed by the injection of electrons from the silicon. It explains an existence of a rapid buildup component which dominates



in field oxides. This component cannot be explained by the slow two-stage $H^+$ hopping transport process. The third class of models assigns a key role to the diffusion of neutral hydrogen. The chemical reaction which occurs when the hydrogen reaches the interface requires an electron supplied from silicon substrate to account for the polarity dependence in the data.

A more detailed description of today's knowledge about physics related to the processes listed above and their models is beyond the scope of this work. This topic is handled in a more exhaustive manner in [15, 25, 87].

## 4.2 Threshold voltage and transconductance extraction methods

There are several methods for threshold voltage extraction [108, 38]. The extraction methods most frequently used are linear (LE) or quadratic (QE) extrapolation of the channel current to zero. The two other methods measure the gate voltage at the chosen value of the drain current. These are the constant-current (CC) and quasi-constant-current (QCC) methods depended on the method for determining the threshold current. There are two other methods which are based on the transconductance curve $g_m(V_{GS})$. This curve is obtained by the numerical differentiation of the transfer characteristic or by the small signal transconductance measurement. The transconductance-change (TC) method determines the threshold voltage as a gate voltage at which the rate of transconductance change $\frac{\partial g_m}{\partial V_{GS}}$ is a maximum. The Fowler-Hartstein (FH) method determines the threshold by a stright line extrapolation of the transconductance from the point of maximum slope to zero. The last two methods are not used in this study.

The linear extrapolation (LE) method uses that part of transfer characteristic for which $V_{GS} \geq V_{DS} + V_{th}$. It means that transistor is biased in the linear region and the channel exists along the entire length of the device. The transfer characteristic in this condition is modelled by the simple equation (A.17) with $\delta = 0$:

$$I_{DS} = \beta(V_{GS} - V_{th} - \frac{1}{2}V_{DS})V_{DS} \tag{4.1}$$

If the plot $\frac{I_{DS}}{V_{DS}}$ versus $V_{GS}$ is drawn, the gate voltage range where the characteristic is very well linear should be found. It is the range above saturation region ($V_{GS} \leq V_{DS} + V_{th}$) and below the region where high normal electric field degradation has a visible influence on mobility. Using a simple linear regression procedure to this part of the transfer characteristic, the gain factor $\beta$ and the threshold voltage $V_{th}$ can be determined respectively:

$$\begin{aligned} \beta &= a \\ V_{th} &= -\frac{b}{a} - \frac{1}{2}V_{DS} \end{aligned} \tag{4.2}$$

The indicator of the proper choice of gate voltage range is a correlation coefficient $r$ which should be greater than 0.999.

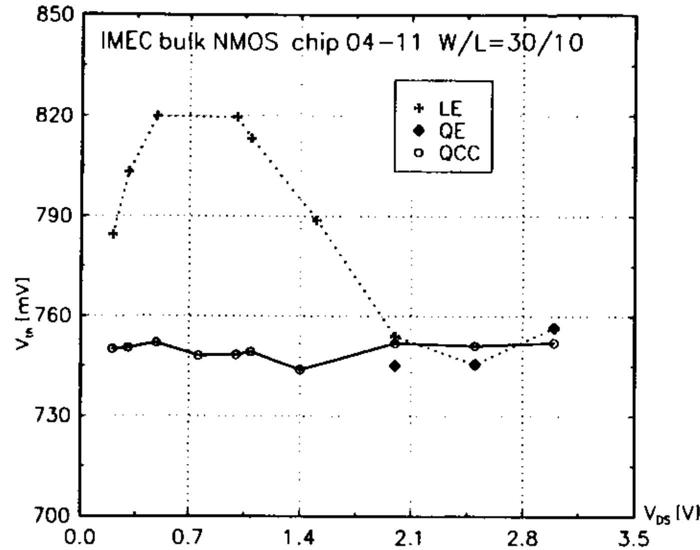


Figure 4.1: The comparison between the linear extrapolation LE method and quasi-constant-current QCC method.

Another version of this method starts from the numerical differentiation of the measured curve $I_{DS}(V_{GS})$ to obtain the transconductance $g_m(V_{GS})$ in the function of the gate voltage. Drawing a tangent line to the curve $I_{DS}(V_{GS})$ at the point where transconductance is maximal $g_{m,max}(V_{GS,max})$, the threshold voltage $V_{th}$ is obtained as the $V_{GS}$-intercept lowered by $\frac{1}{2}V_{DS}$.

The quadratic extrapolation (QE) method is very similar but it is based on the part of the transfer characteristic related to the saturation region $V_{GS} \leq V_{DS} + V_{th}$. In this range the following relationship (A.20) with $\delta = 0$ is applied:

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_{th})^2 \tag{4.3}$$

The plot $\sqrt{I_{DS}}$ versus $V_{GS}$ is drawn, and the calculation of the linear regression coefficients $a$ and $b$ should be done for the properly chosen linear part of this curve. Then:

$$\begin{aligned} \beta &= a^2 \\ V_{th} &= -\frac{b}{a} \end{aligned} \tag{4.4}$$

The other kind of extraction method is based on the subthreshold range of the transfer characteristic. The simplest way is to choose arbitrarily the drain current value ($10pA \div 1\mu A$) as a threshold current. The determining of the threshold voltage $V_{th}$ is done by finding the gate voltage corresponding to this current value on measured



subthreshold characteristic. This method is called the constant-current (CC) method. When the extraction of $V_{th}$ is made for different transistor geometries, the threshold current value should be normalized by the width-to-length ratio $W/L$.

A fault of this method is the lack of physical meaning of the arbitrarily chosen threshold current. To improve this method [108] the threshold current $I_{th}$ must be determined from the weak inversion conduction model (App. B), introducing $\psi_s = 2\phi_B$ to the equation (B.17):

$$I_{th} = \beta V_t^2 \frac{C_D}{C_{ox}} \left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right] \tag{4.5}$$

where $C_D$ can be calculated using the substrate doping $N_A$ (equation (B.16)) or from the subthreshold slope (equation (B.25)). This method is called the Quasi-Constant-Current (QCC) method. The advantage of this method is visible in Fig. 4.1.

## 4.3 The influence of radiation generated charges on transconductance

The radiation influence of transconductance can be related to mobility variation or to the change of the extrinsic resistance of the source/drain regions.

The low field mobility (see subsec. 2.1.2.) $\mu_0$ is related to phonon scattering and Coulomb scattering by oxide charges $Q_{ot}$, fixed charges $Q_f$, interface charges $Q_{it}$ and lattice ions. It can be expressed as [38]:

$$\mu_0 = \frac{\mu_{il}}{1 + \alpha\left(N_I + \int_0^{\psi_s(y)} D_{it}(\psi)d\psi\right)}, \tag{4.6}$$

where $\mu_{il}$ is the mobility due to phonon and impurity scattering in the silicon, $N_I$ is the sum of all charges in the plane of $Si/SiO_2$ interface at zero band-bending ($\psi_s = 0$) and is independent of surface potential $\psi_s$, $D_{it}$ is the density of interface states per unit area per eV, $\alpha$ is the parameter.

The parameter $\alpha$ is usually considered as an empirical factor known from additional measurements but a quantum mechanical theory for this parameter exists, too. Using a simplified two-dimensional electron gas model, Ning and Sah [90] derived a simple analytical expression for $\alpha$:

$$\alpha = \mu_{il}\frac{m_{Si}q^3}{32\varepsilon_{av}^2\hbar kT}, \tag{4.7}$$

where $\varepsilon_{av} = \frac{1}{2}(\varepsilon_{Si} + \varepsilon_{SiO_2})$ is the average dielectric constant of $Si$ and $SiO_2$, $m_{Si} = 0.259m_0$ is the electron effective mass in the silicon. In this theory a delta-function was assumed as the distribution of total charge at the interface. The measured $\alpha$ is about 20 times larger than the value predicted by the theory. Equation (4.7) predicts a value $2.7 \times 10^{-15}Vs$ for $\frac{\alpha}{\mu_{il}}$ at the room temperature after correction by a factor 20 [145].

The relation (4.6) presented above is usually employed for studying the radiation effects [92], [95] in the form proposed by Sun-Plummer [91]:

$$\mu_{\text{after}} = \frac{\mu_{\text{before}}}{1 + \alpha \Delta N_{it}}, \tag{4.8}$$

where $\Delta N_{it}$ is the radiation-induced increase in the number of interface states.

## 4.4 The influence of radiation generated charges on threshold voltage

Let us examine the relation between the surface potential $\psi_s$ and the gate voltage $V_{GS}$. From Kirchoff's voltage law:

$$V_{GB} = V_{GS} + V_{SB} = \psi_s + \Phi_{GB} - \frac{Q_S}{C_{ox}} - \frac{Q_m + Q_{ot} + Q_f}{C_{ox}} - \frac{Q_{it}}{C_{ox}}, \tag{4.9}$$

where $C_{ox}$ is the gate oxide capacitance per unit area, $\Phi_{GB}$ is the difference between the work function of silicon substrate and gate electrode material, $Q_S = Q_I + Q_D$ is the total charge in silicon. The small polarization effect in $SiO_2$ has been neglected.

The small voltage drop across the conducting channel is negligible and the total charge in silicon can be simply calculated in the depletion approximation:

$$\begin{aligned} Q_D \approx Q_S = -\varepsilon_{Si}\varepsilon_0 \mathcal{E}_s &= -\sqrt{2\varepsilon_{Si}\varepsilon_0 q N_A}\sqrt{\psi_s} \\ &= -C_{ox}\gamma\sqrt{\psi_s}, \end{aligned} \tag{4.10}$$

where $\mathcal{E}_s$ is the electric field at the silicon surface (B.9), $\gamma$ is the body effect coefficient (A.12).

The term related to work functions is:

$$\Phi_{GB} = \phi_G - \phi_B, \tag{4.11}$$

where $\phi_B$ is defined by the equation (2.3), $\phi_G = V_t \ln \frac{N_{GATE}}{n_i}$, $N_{GATE}$ is the doping of the polysilicon gate electrode. The terms in equation (4.11) are measured with respect to the midgap level because it is parallel to the vacuum level. When the gate electrode is made of metal the corresponding expression must be written:

$$\Phi_{GB} = \frac{\Phi_M - \Phi_{SC}}{q} = \frac{1}{q}[\Phi_M - (\chi + \frac{E_g}{2} + kT \ln \frac{N_A}{n_i})], \tag{4.12}$$

where $\Phi_M = E_0 - E_{FM}$ is the work function of metal ($4.1eV$ for aluminium), $E_0$ is the energy of vacuum level, $E_{FM}$ is the energy of metal Fermi level, $\Phi_{SC}$ is the work function of silicon which varies with doping and temperature, $\chi = E_0 - E_C^{ox}$ is the electron affinity in silicon ($4.1eV$).



From equation (4.9) the gate voltage can be calculated:

$$\begin{aligned} V_{GS} = V_{GB} - V_{SB} &= \psi_s - V_{SB} + \Phi_{GB} + \gamma\sqrt{\psi_s} \\ &- \frac{Q_m + Q_{ot} + Q_f}{C_{ox}} - \frac{Q_{it}}{C_{ox}}. \end{aligned} \tag{4.13}$$

When the surface potential is $\psi_s = 2\phi_B + V_{SB}$, the threshold voltage $V_{th}$ can be written according to definition (2.6):

$$V_{th} = 2\phi_B + \Phi_{GB} + \gamma\sqrt{2\phi_B + V_{SB}} - \frac{Q_m + Q_{ot} + Q_f}{C_{ox}} - \frac{Q_{it}}{C_{ox}}. \tag{4.14}$$

In this way a complete equation for the threshold voltage has been obtained.

The well-known equation (4.14) contains four types of charges discussed in chapter2. The oxide charge $Q_{ot}$ and the interface charge $Q_{it}$ depends on radiation. Therefore the radiation-induced threshold voltage shift can be expressed:

$$\Delta V_{th} = -\frac{\Delta Q_{ot} + \Delta Q_{it}}{C_{ox}}. \tag{4.15}$$

The first component of total threshold voltage shift $-\frac{\Delta Q_{ot}}{C_{ox}}$ does not depend on the bias condition on the device terminals. However, the second component $-\frac{\Delta Q_{it}}{C_{ox}}$ depends on the device bias. The interface traps exchange charge carriers with silicon surface and the amount of charge trapped at them, depends on the band bending $\psi_s$ at the surface.

Because the interface charge originates from two kinds of traps according to their donor- or acceptor-like properties (see chap. 2.) the total charge in interface states is [89]:

$$Q_{it} = q\int_{-\frac{E_g}{2}}^{\frac{E_g}{2}} [F_D(\psi)D_{itD}(\psi) - F_A(\psi)D_{itA}(\psi)]d\psi. \tag{4.16}$$

The variable $\psi$ is measured with respect to the midgap level. The quantities $D_{itD}$, $D_{itA}$ are the donor and acceptor states density at the interface . The Fermi-Dirac distribution function for donors can be approximated as:

$$\begin{aligned} F_D(\psi) &= 0, \quad \psi < \phi_B, \\ &= 1, \quad \psi \geq \phi_B, \end{aligned} \tag{4.17}$$

and for acceptors as:

$$\begin{aligned} F_A(\psi) &= 1, \quad \psi < \phi_B, \\ &= 0, \quad \psi \geq \phi_B. \end{aligned} \tag{4.18}$$

Therefore for flat band condition ($\psi_s = 0$):

$$Q_{itFB} = q\int_{\phi_B}^{\frac{E_g}{2}} D_{itD}(\psi)d\psi - q\int_{-\frac{E_g}{2}}^{\phi_B} D_{itA}(\psi)]d\psi. \tag{4.19}$$

For a given bias condition when the surface band bending is $\psi_s$:

$$Q_{it}(\psi_s) = Q_{itFB} + q \int_{\phi_B+\psi_s}^{\phi_B} D_{it}(\psi) d\psi, \tag{4.20}$$

where $D_{it}(\psi) = D_{itD}(\psi) + D_{itA}(\psi)$.

After the irradiation both components in equation (4.20) are changed. Therefore the threshold voltage shift due to interface traps should be considered as:

$$-\frac{\Delta Q_{it}(\psi_s)}{C_{ox}} = -\frac{\Delta Q_{itFB}}{C_{ox}} + \frac{q}{C_{ox}} \int_0^{\psi_s} \Delta D_{it}(\psi) d\psi, \tag{4.21}$$

where the variable $\psi$ is measured with respect to the Fermi level.

When the threshold voltage is determined by the constant-current (CC) method one more component of radiation-induced threshold voltage shift should be taken into account. This component is attributed to the mobility degradation [92]. The radiation-induced change of the transfer characteristic slope results also in a change of the linearly extrapolated x-intercept. The mobility degradation is described by the Sun-Plummer equation (4.8). Therefore the drain currents before and after irradiation can be expressed as follows:

$$\begin{aligned} I_{DS\ \text{before}} &= \tfrac{W}{L}\mu_{\text{before}} C_{ox}(V_{GS} - V_{th\ \text{before}} - \tfrac{V_{DS}}{2})V_{DS}, \\ I_{DS\ \text{after}} &= \tfrac{1}{1+\alpha \Delta N_{it}} \tfrac{W}{L}\mu_{\text{before}} C_{ox}(V_{GS} - V_{th\ \text{before}} \\ &\quad -\Delta V_{th\mu} - \tfrac{q\Delta N_{ot}}{C_{ox}} - \tfrac{q\Delta N_{it}}{C_{ox}} - \tfrac{V_{DS}}{2})V_{DS}, \end{aligned} \tag{4.22}$$

where $\Delta V_{th\mu}$ is the mobility degradation component of the threshold voltage shift. When the threshold voltages are measured by the constant-current (CC) method (see section 4.2) $I_{DS\ \text{before}} = I_{DS\ \text{after}} = I_{th}$, this additional component is:

$$\Delta V_{th\mu} = \frac{\alpha I_{th} L}{\mu_{\text{before}} W C_{ox} V_{ds}}. \tag{4.23}$$

## 4.5 The methods for separating the effects of interface traps and oxide charges

The total radiation-induced threshold voltage shift $\Delta V_{th}$ consists of two components:

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}. \tag{4.24}$$

These components are related to the two different radiation effects in the $SiO_2$ layer: oxide charge $\Delta V_{ot}$ and interface charge $\Delta V_{it}$. Several methods for extracting these two components of radiation-induced threshold voltage shift $\Delta V_{th}$ which use only measurements of the static characteristics of transistors have been invented. There are:

- **midgap method** [93],



- **subthreshold swing degradation method** [94],
- **transconductance degradation method** [92],
- **dual-transistor method** [95],
- **subthreshold output characteristic method** [112].

There is also a more complicated method requiring the fitting algorithm and using the charge-sheet model (developed by Brews) [96].

All methods listed above employ only static characteristic measurements to extract the desired parameters. There are also many other methods which are based on high-frequency capacitance-voltage (HFCV) [97], high-low frequency capacitance C-V, conductance, charge pumping, low temperature capacitance [98], and thermally stimulated current (TSC) [99] measurements. They determine the interface state density $D_{it}$ or oxide trapped charge $N_{ot}$ which can be used for separating the two effects. However, only the methods which are based on static characteristic measurements were used in this study .

All methods which are presented below are based on several assumptions. At the beginning they should be highlighted:

1. the interface traps are acceptor-like in the upper half of the silicon bandgap and donor-like in the lower. The problem related to these properties of interface states was discussed in section 4.4. More detailed measurements and discussions show that this assumption is not always true [100, 101].
2. the assumption 1. implies that for NMOSFETs the interface charge is negative (acceptors above midgap) and produce a positive shift, while for PMOSFETs the interface charge is positive (donors below midgap) and produce a negative shift.
3. the mobility degradation is predominantly due to a scattering from the interface charge, but charge in the bulk of the oxide have little effect on mobility.
4. the mobility degradation is described by the Sun-Plummer equation (4.8) taking the same value of parameter $\alpha$ for $n$- and $p$-channel transistors.
5. the oxide charge contribution $V_{ot}$ is approximately equal for the n- and p-channel transistors irradiated at the same oxide electric field.

The midgap method is based on the fact, that when the Fermi level at the silicon surface coincides with the midgap energy level the interface states are neutral. This occurs when the gate voltage is equal to the midgap voltage $V_{mg}$ and the energy band bending is $\psi_s = \phi_B$ (see sec. 2.1.1. and Fig. 2.4.). Since the interface states are neutral the radiation-induced midgap voltage shift $\Delta V_{mg}$ is only due to oxide traps:

$$\Delta V_{ot} = \Delta V_{mg}. \tag{4.25}$$

Because the midgap point usually lies below the leakage current in the range of $0.01 - 0.1\ pA$ the subthreshold curve must be linearly extrapolated down to this drain current level. The midgap current $I_{mg}$ must be calculated using the equation (B.17) for $\psi_s = \phi_B$:

$$I_{mg} = \beta \frac{C_D(\phi_B)}{C_{ox}} V_t^2 \exp(\frac{-\phi_B}{V_t})[1 - \exp(-\frac{V_{DS}}{V_t})]. \tag{4.26}$$

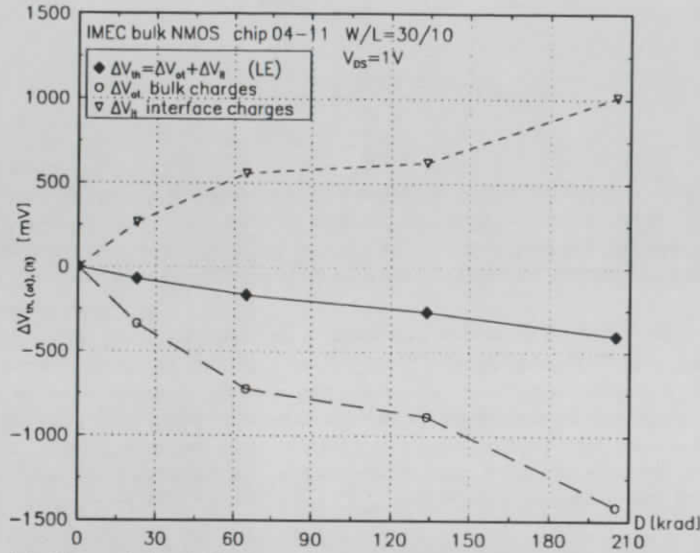


Figure 4.2: The total threshold voltage shift $\Delta V_{th}$ and contributions due to oxide traps $\Delta V_{ot}$ and interface traps $\Delta V_{it}$ vs. the total $\gamma$ dose for NMOS transistor extracted by the midgap method. Irradiation condition: $V_{DS}=0V$, $V_{BS}=0V$, $V_{GS}=5V$.

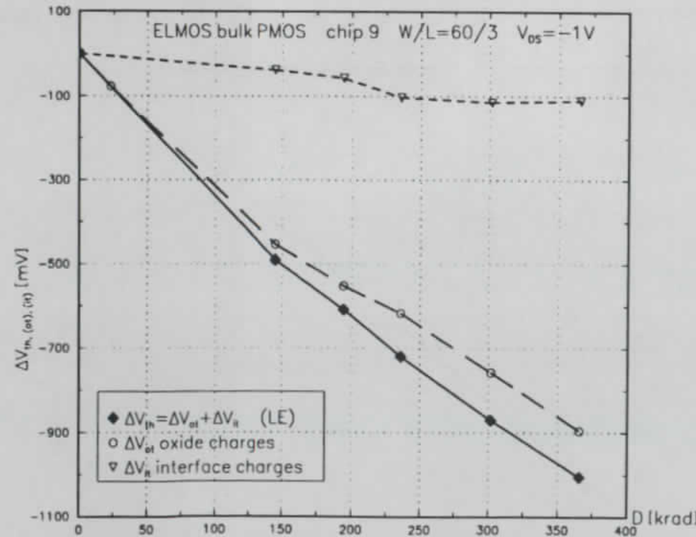


Figure 4.3: The total threshold voltage shift $\Delta V_{th}$ and contributions due to oxide traps $\Delta V_{ot}$ and interface traps $\Delta V_{it}$ vs. the total $\gamma$ dose for PMOS transistor extracted by the midgap method. Irradiation condition: $V_{DS}=0V$, $V_{BS}=0V$, $V_{GS}=-5V$.



The depletion capacitance at midgap condition can be calculated knowing the inversion surface potential $C_D(\phi_B)=\sqrt{\frac{q n_i \epsilon_{Si}\epsilon_0}{2\phi_B}}\exp(\frac{\phi_B}{2V_t})$ (see equation (B.16)) or using the equation (B.25) and the measured values of inverse subthreshold slope $n$. The gain factor $\beta$ must be determined either by means of method LE or QE. When the value of the midgap current $I_{mg}$ is known, the midgap voltage $V_{mg}$ is determined from extrapolation of the subthreshold curve (using the subthreshold slope $\frac{1}{n}$).
The voltage shift caused by the occupation of interface states in the silicon bandgap when gate voltage changes from midgap to inversion condition results in a widening of the subthreshold curve. The stretchout voltage $V_{so}$ is defined as voltage difference between the midgap and inversion points:

$$V_{so}=V_{th}-V_{mg}. \tag{4.27}$$

The increase in the stretchout of the current curve along the gate voltage axis yields:

$$\Delta V_{it}=\Delta V_{so}=V_{so\ \mathrm{after}}-V_{so\ \mathrm{before}}. \tag{4.28}$$

In this way both components are determined. This method can be applied only when the subthreshold curve is measured precisely and is made for a transistor with a very small leakage current. The results are presented in Fig. 4.2. for NMOSFET and Fig. 4.3. for PMOSFET.

The method described above can be modified using the subthreshold swing $S$ (see equation 2.27) instead of the stretchout voltage $V_{so}$:

$$\Delta D_{it}(\psi_s)=\frac{C_{ox}}{V_t q\ln 10}\Delta S(\psi_s). \tag{4.29}$$

where $\Delta D_{it}$ is the increase in density of interface states after irradiation.
The comparison of this approach with that described above is presented in Fig. 4.4. The values $\Delta V_{it}=\frac{q\Delta N_{it}}{C_{ox}}$ are obtained by the midgap method and are plotted as a function of:

$$\frac{\Delta C_{it}}{C_{ox}}=\frac{\Delta S}{V_t\ln 10}, \tag{4.30}$$

where $\Delta C_{it}=q\Delta D_{it}$ is the increase of interface state capacitance. The value of the subthreshold swing $S$ is a global value describing the slope of subthreshold curve in the whole range of drain current. The obtained linear regression parameter $a$ is related to the integral of density of the radiation-induced interface states along the surface potential (see equation (4.21)). The Fig. 4.4. shows that the relationship between the interface component of threshold voltage shift and the increase of interface state capacitance is linear. The equation (4.29) can also be used to determine surface potential distribution of radiation-induced interface states. At the beginning the subthreshold swing before $S_{\mathrm{before}}(I_{DS})$ and after irradiation $S_{\mathrm{after}}(I_{DS})$ must be determined for each point of the two subthreshold curves. Both curves should be measured with current extortion to obtain values $S_{\mathrm{before}}$ and $S_{\mathrm{after}}$ for the same values of drain current $I_{DS}$ (measurement of gate voltage $V_{GS}$ for extorted $I_{DS}$). Then the surface potential for each point of the two curves must be calculated using equations (B.17), (B.25):

$$\psi_s=V_t\ln\left(\frac{I_{DS}}{\beta K\left(\frac{S_{\mathrm{before}}(I_{DS})}{V_t\ln 10}-1\right)}\right), \tag{4.31}$$

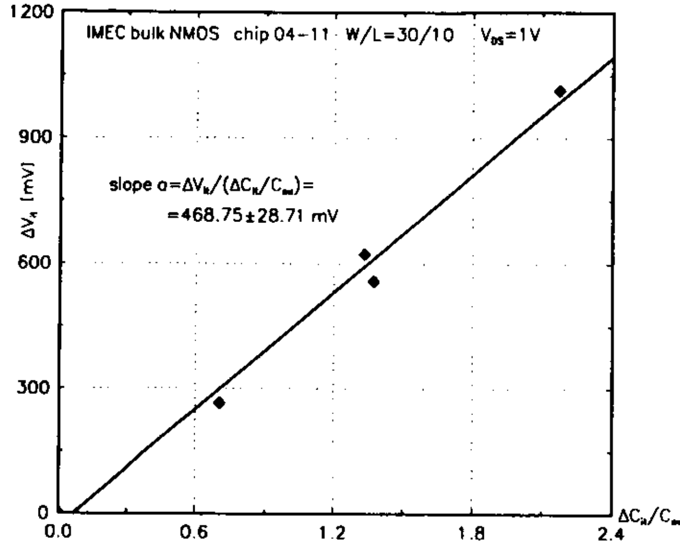


Figure 4.4: The correlation between the interface state component of the threshold voltage shift $\Delta V_{it}$ and the increase of the interface state capacitance $\frac{\Delta C_{it}}{C_{ox}}$ for NMOS-FET. Irradiation condition: $V_{DS} = 0V$, $V_{BS} = 0V$, $V_{GS} = -5V$.

where $K = V_t^2 \exp(-\frac{2\phi_B}{V_t})[1 - \exp(-\frac{V_{DS}}{V_t})]$.
The function $S_{\text{before}}(I_{DS}(\psi_s)) = V_t \ln 10 \left(\frac{C_D(\psi_s)}{C_{ox}} + 1\right)$ is used for determining the depletion capacitance dependence on the surface inversion potential, necessary in the equation (B.17). The surface interface capacitance before irradiation is assumed to be negligible and the depletion capacitance remains unchanged during irradiation. The surface inversion potential $2\phi_B$ must be known from other measurements. Then, if the increase of density of interface state $\Delta D_{it}(\psi_s)$, calculated using equation (4.29), is plotted versus the surface potential $\psi_s$ calculated from equation (4.31), the distribution is obtained.

The transconductance degradation method uses only the above-threshold transfer characteristic. The subthreshold part need not be measured. However, the additional parameter $\alpha$ defined by equation (4.6) must be known. When the threshold voltage is measured by the constant-current (CC) method the following system of equations can be written:

$$\begin{aligned} \Delta V_{th} &= -\frac{\Delta Q_{ot}}{C_{ox}} + \left(\frac{\alpha I_{th}}{\beta_{\text{before}} V_{DS}} - \frac{q}{C_{ox}}\right)\Delta N_{it}, \\ \Delta\beta &= \frac{\alpha \Delta N_{it}}{1 + \alpha \Delta N_{it}} \beta_{\text{before}}. \end{aligned} \tag{4.32}$$



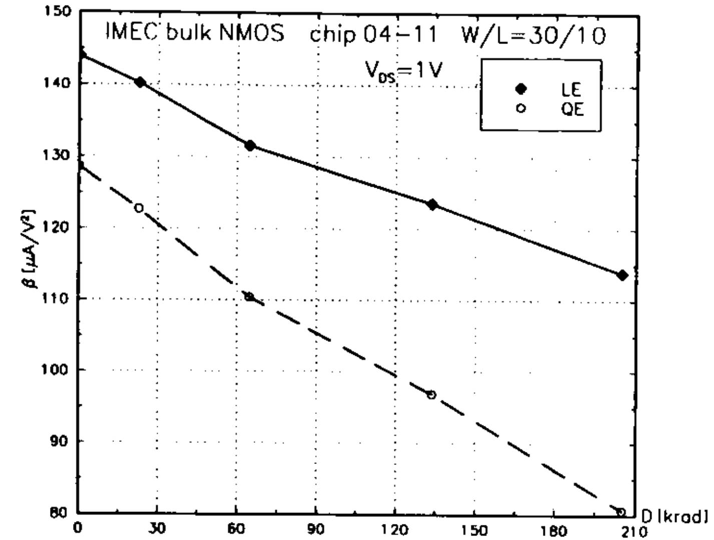


Figure 4.5: The transconductance $\beta$ vs. the total $\gamma$ dose for the NMOS bulk transistor.

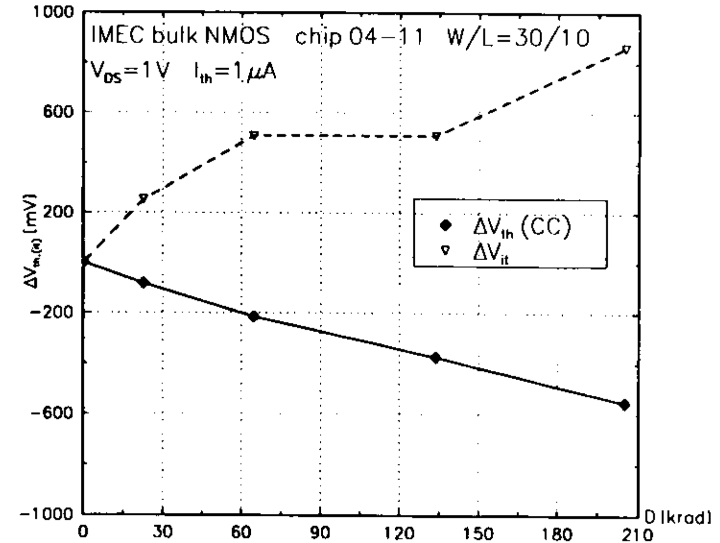


Figure 4.6: The total radiation threshold voltage shift $V_{th}$ determined by constant-current (CC) and the threshold voltage shift induced by radiation-generated interface state $\Delta V_{it}$ determined by transconductance degradation method vs. the total $\gamma$ dose for the NMOS bulk transistor.

The first equation is the result of two equations (4.23), (4.15) presented above. The second one is a simple consequence of the Sun-Plummer equation (4.8). The solution of system of equations is not possible because three quantities $\alpha, \Delta N_{ot}, \Delta N_{it}$ are not known. One of them must be determined by additional measurement because the theoretical predictions are very inaccurate (4.7). For presentation of this method the values of oxide traps density $N_{ot}$ determined by means of using the midgap method can be used (see Fig. 4.2.). The transconductance degradation for the same transistor is presented in Fig. 4.5. The threshold voltage shift measured by the CC method and interface traps component of it extracted by the solution system of equations (4.32) is shown in Fig. 4.6. Although the obtained curve is very similar to that calculated by midgap method the values of parameter $\alpha$ vary strongly after irradiation in the range of $6 - 18 \times 10^{-15} cm^2$. It means that the analysis is not self-consistent. One or more of the assumptions 3, 4 are broken down in that application.

The dual-transistor method does not require good quality of subthreshold curve. It can be applied for devices with large parasitic leakage under field oxide or due to the back-gate or sidewall effect or when the subthreshold curve is distorted by floating body effect. According to assumptions 5, 2 and equation (4.24), for two transistors of opposite types with identically processed oxides and irradiated in the same conditions:

$$\Delta V_{thn} = |\Delta V_{ot}| + |\Delta V_{itn}|, \tag{4.33}$$

$$\Delta V_{thp} = |\Delta V_{ot}| + |\Delta V_{itp}|, \tag{4.34}$$

where the indices $n$ and $p$ denote the type of transistor channel. Using assumption 4 two new variables $\eta_{n,p}$ and $\alpha^*$ are defined :

$$\eta_n = \alpha^* |\Delta V_{itn}|, \tag{4.35}$$

$$\eta_p = \alpha^* |\Delta V_{itp}|, \tag{4.36}$$

where $\eta_{n,p} = \frac{\mu_{n,p\ before} - \mu_{n,p\ after}}{\mu_{n,p\ after}}$ is the relative mobility degradation, $\alpha^* = \alpha \frac{\Delta N_{it}}{\Delta V_{it}}$ is the relative Sun-Plummer parameter (4.8). The solution of the four equation system (4.33), (4.34), (4.35), (4.36) gives:

$$\alpha^* = \frac{\eta_n + \eta_p}{\Delta V_{itn} - \Delta V_{itp}}, \tag{4.37}$$

$$\Delta V_{itn} = \frac{\Delta V_{itn} - \Delta V_{itp}}{\eta_n + \eta_p} \eta_n, \tag{4.38}$$

$$\Delta V_{itp} = -\frac{\Delta V_{itn} - \Delta V_{itp}}{\eta_n + \eta_p} \eta_p, \tag{4.39}$$

$$\Delta V_{ot} = \frac{\eta_p \Delta V_{itn} + \eta_n \Delta V_{itp}}{\eta_n + \eta_p}, \tag{4.40}$$

The relative Sun-Plummer parameter should be constant all the time through a sequence of irradiations. It is the indicator of self-consistence of the dual-transistor



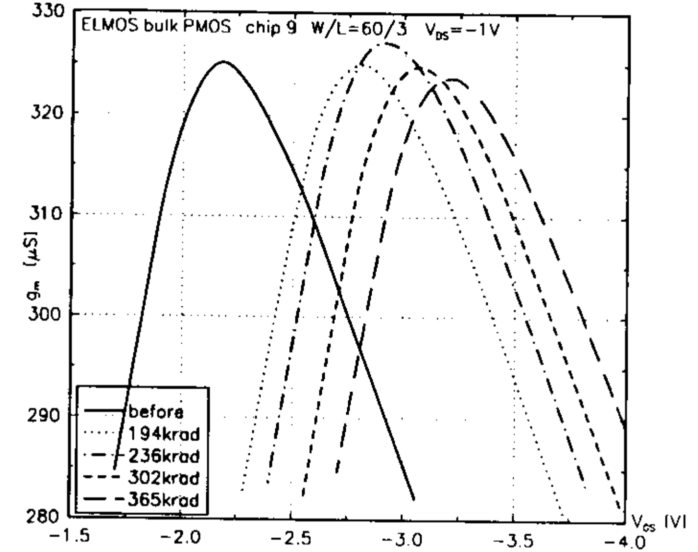


Figure 4.7: The transconductance $g_m$ vs. gate voltage $V_{GS}$ after several subsequent irradiations of the PMOS transistor. Irradiation conditions: $V_{DS} = 0V$, $V_{BS} = 0V$, $V_{GS} = -5V$.

method. If $\alpha^*$ changes, this is due to an error in the measurement or one of the assumptions is not valid. The variables $\eta_{n,p}$ must be determined from gain factor $\beta$:

$$\eta_{n,p} = \frac{\mu_{n,p\ before}}{\mu_{n,p\ after}} - 1 = \frac{\beta_{n,p\ before}}{\beta_{n,p\ after}} - 1, \tag{4.41}$$

what results from (2.20). The influence of extrinsic resistances on transconductance is neglected here.

Both of the methods discussed above, i.e.: transconductance degradation and dual-transistor are suitable for technologies which exhibit considerable decrease of transconductance. In general the tested technologies show a very small radiation-induced change of transconductance and the Sun-Plummer equation cannot be used for analysis. An example of such behaviour is shown in Fig. 4.7. This figure presents several curves $g_m(V_{GS})$ in the range around their maximal values after subsequent irradiations of the PMOS transistor. The irregular change and the very stable maximum of the transconductance $g_m$ is visible in this figure. Especially for the SOI NMOS transistors the increase of transconductance is observed and therefore the Sun-Plummer equation is useless (see Fig. 4.10. 4.11. 4.12.).

One more method for separating the two components of the threshold voltage shift should be described although it was not employed in this work. The method of subthreshold output characteristic is based on the equation describing the subthres-

hold characteristic derived in [112]. It can be written in a simple form:

$$I_{DS} = I_{DSmax}\left[1 - \exp\left(-\frac{m}{n}\frac{V_{DS}}{V_t}\right)\right] \tag{4.42}$$

where $I_{DSmax}$ is the maximal drain current for an applied gate voltage, and is found by putting $V_{DS} = \infty$ in equation (B.26). Introducing a designation:

$$\kappa = \frac{m}{n}\frac{V_{DS}}{V_t} = \ln(1 - \frac{I_{DS}}{I_{DSmax}}), \tag{4.43}$$

and using equations (B.21), (B.27) as functions of $\psi_s$, an expression for density of interface states is obtained:

$$D_{it} = \frac{C_{ox} + C_D(\psi_s)}{q}(-\frac{V_{DS}}{\kappa V_t} - 1). \tag{4.44}$$

For simplicity, the parameter $\kappa$ can be chosen as $-1$, which results in $I_{DS} = 0.632 \times I_{DS\,max}$. Therefore the equation below can be used for calculating interface density:

$$D_{it} = \frac{C_{ox} + C_D(\psi_s)}{q}(\frac{|V_{DS}|}{V_t} - 1). \tag{4.45}$$

The output characteristic at gate voltage $V_{GS}$ below threshold voltage $V_{th}$ must be measured and then, the value of drain voltage $V_{DS}$ at drain current equal to $I_{DS} = 0.632 \times I_{DS\,max}$ is determined. The equation (4.45) gives the desired value of interface states density $D_{it}$. To obtain the whole interface states spectrum $D_{it}(\psi_s)$ in the range between midgap and inversion point, several output characteristics at different gate voltage values $V_{GS}$ should be measured. The surface potential $\psi_s$ is determined by means of using equation (4.31), considering also the drain voltage value. This method is a better one than those which use the subthreshold range of the transfer MOSFET characteristic. The surface potential fluctuations caused by lateral charge nonuniformities (LNUs) influence on $I_{DS} - V_{GS}$ curve similarly to interface traps [113]. It was demonstrated [112] that LNUs do not affect the slope of $I_{DS} - V_{DS}$ curve. It means that the output characteristic method is a good method to avoid the influence of LNUs and it can be used for separating the interface states and LNUs effects.

## 4.6 The results for SOI transistors and discussion

The results presented below concern the SOI technology developed by IMS FhG in Duisburg. The test structures from three different wafers were studied. The main difference between these wafers is that the NMOS transistors on the wafer C60/35 are LDD (lightly doped drain) transistors whereas the NMOS transistors on the C75/47 and C75/34 are "conventional" devices. Another technological difference concerns the condition of the annealing after oxygen implantation. The wafers C60/35 and C75/34 were annealed in an ambient of $Ar/O_2$ at $1250°C$ for 8 $h$ whereas the C75/47 was annealed in an ambient of $N_2/O_2$ at $1250°C$ for 8 $h$. The implantation parameters for



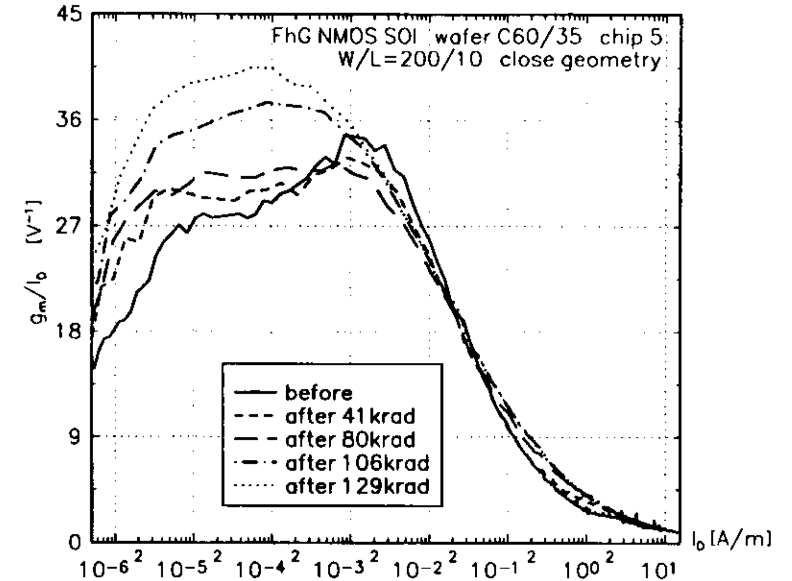


Figure 4.8: The transconductance scaled by the drain current $\frac{g_m}{I_{DS}}$ vs. current density $\frac{I_{DS}}{W}$ for the SOI NMOS LDD transistor after subsequent irradiation by $\gamma$ radiation source. Irradiation condition: $V_{GS} = 5V, V_{DS} = V_{BS} = 0V$. Measured at $V_{DS} = 2V$.

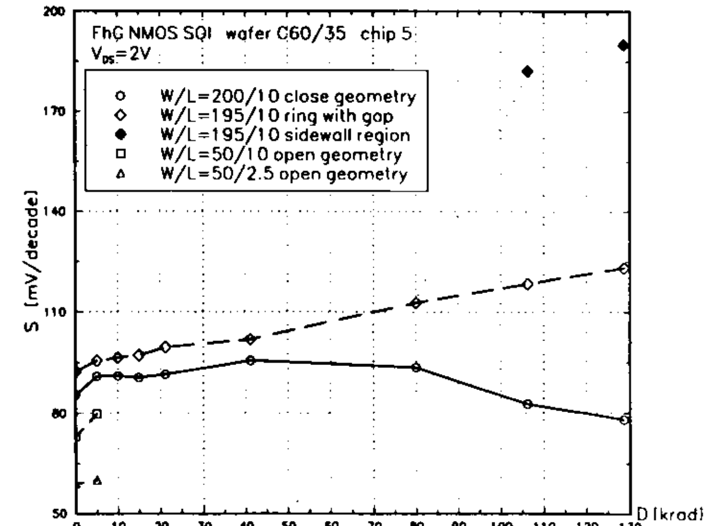


Figure 4.9: The variation of the subthreshold swing $S$ with the total $\gamma$ dose for the SOI NMOS LDD transistor. Irradiation condition: $V_{DS} = 0V = V_{BS} = 0V, V_{GS} = 5V$. Measured in saturation at $V_{DS} = 2V$.

p-channel threshold voltage adjustment are slightly different for these wafers. Also the drain/source implantations have different parameters.

The radiation behaviour of a NMOS SOI LDD edgeless transistor is summed up in Fig. 4.8. The method of results presentation proposed by Dąbrowski et al. [102] and used also in another study at CERN [103] is applied. The transconductance values are scaled with the value of the drain current and plotted as a function of current per unit gate width of transistor (logarithmic scale). Such a method makes the comparison between different $W/L$ factors easier and supplies a very good method to distinguish week from strong inversion regions. A simple model of transistor operation in the weak inversion region (App. B, equation (B.24)) predicts an exponential dependence for the relation $I_{DS}(V_{GS})$. It means that the ratio $g_m$ to $I_{DS}$ is independent of the drain current $I_{DS}$ (and also on gate voltage $V_{GS}$) in this region of operation. Therefore the curve $\frac{g_m}{I_{DS}}$ vs. $I_{DS}$ should be flat in the subthreshold region, and the drop from this constant value indicates the onset of the strong inversion. However, the peak at the beginning of the weak inversion region is observed (Fig. 4.8.). It is probably caused by the floating body effect [130]. This peak disappears after irradiation which is consistent with the observed amelioration in the kink effect (see sec: 4.7.). After the initial degradation of transconductance $g_m$ in the weak inversion, a significant increase is observed. Because of the inverse proportionality between the ratio $\frac{g_m}{I_{DS}}$ and the subthreshold swing $S$, similar changes are visible in Fig. 4.9. At smaller doses, the average subthreshold swing (extracted by linear regression) slightly increases. It can be caused by an increase in the interface state capacitance $C_{it}$, but in the case of SOI transistors also a decrease in the influence of the floating body effect must be taken into account. At bigger doses (above 40 *krad*), the close geometry transistor exhibits a decrease of the subthreshold swing. This effect is also visible in Fig. 4.8. as an increase of $\frac{g_m}{I_{DS}}$ after irradiation. When the influence of the floating body region is smaller, the creation of an oxide charge in the buried oxide layer causes the widening of the depletion region and decreases the depletion capacitance $C_D$. Such an effect was also observed at CERN [103] after 1 *Mrad* dose, but at a higher total dose (10 *Mrad*) and after annealing the decrease of $\frac{g_m}{I_{DS}}$ was reported. It can be explained by the negative interface state charge generation at back interface between transistor body and buried oxide layer [123] which does not undergo annealing. For transistors with

Table 4.1: The gain factor $\beta$ and the threshold voltage $V_{th}$ for two SOI NMOS LDD transistors (FhG wafer C60/35 chip 5, round shape) before and after irradiation by $\gamma$ radiation up to dose 129 *krad*. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured in linear range at: $V_{DS} = 0.2V$.

| W/L | $\beta$(LE) $[\frac{mA}{V^2}]$ | | $V_{th}(LE)$ $[mV]$ | |
|---|---|---|---|---|
| | 0 krad | 129 krad | 0 krad | 129 krad |
| 200/10 | 1.549 | 1.667 | 812.9 | 470.1 |
| 195/10 | 1.453 | 1.568 | 808.7 | 460.1 |



edges (round shape) (Fig. 3.18.b)) the increase of the subthreshold swing is observed in the whole range of the total dose but the subthreshold characteristic is distorted by the sidewall effect. Therefore the subthreshold swing was extracted in the range for higher and smaller currents than when the sidewall hump occurs. For two open geometry transistors the leakages at 10 *krad* dose were so big that the subthreshold swing parameter did not make sense.

Another abnormal behaviour of SOI NMOS transistors was observed with respect to transconductance in the strong inversion range of operation. In Fig. 4.10. it is shown that the gain factor $\beta$ in saturation increases almost twice after total dose about 80 *krad*. The increase of the gain factor is observed also in the linear range (Tab. 4.1.) but significantly smaller on the level of +8%. Such radiation behaviour of transconductance was also observed by other investigators [104, 12] (+20% after 1 Mrad dose). Other plots presented in Fig. 4.11. show irregular behaviour of the transconductance maximum in the linear range for the SOI NMOSFETs irradiated at negative bias of the back gate. This figure also indicates the increase of the transconductance (+6 − +10%) especially in the range of low doses. A similar increase of the transconductance is also observed (Fig. 4.12.) for the back gate transistors (+7 − +12%). The irregularity on a level of several percent in the behaviour of transconductance can be explained by a very simple method of differentiation of

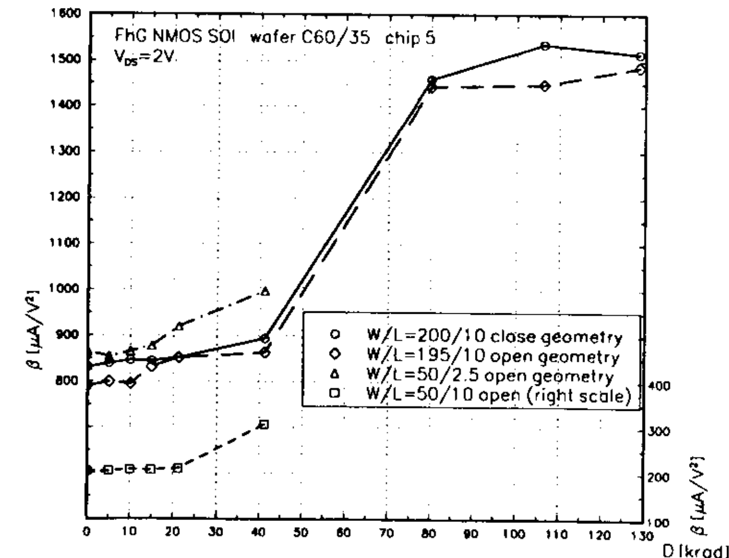


Figure 4.10: The variation of gain factor $\beta$ with the total $\gamma$ dose for the SOI NMOS LDD transistors. The value of mobility for the close geometry transistor after irradiation is $550\frac{cm^2}{V_s}$. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured in saturation at: $V_{DS} = 2V$.

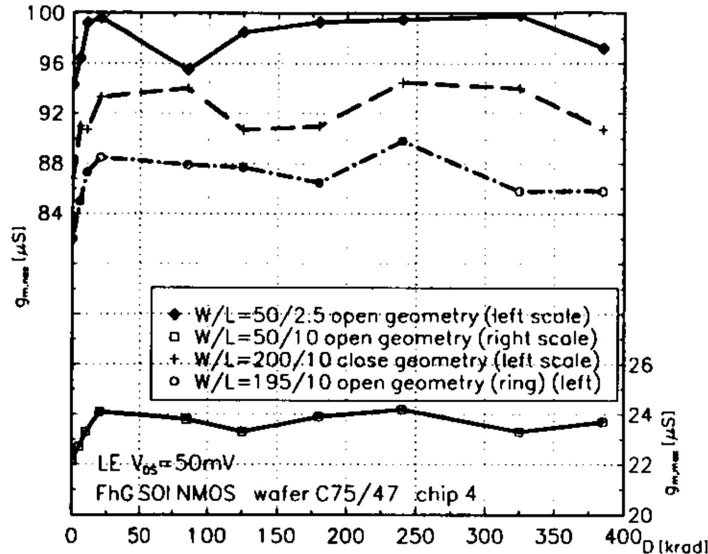


Figure 4.11: The variation of the maximum transconductance $g_{m\ max}$ with the total $\gamma$ dose for the SOI NMOS transistors. The value of mobility for the close geometry transistor after irradiation is $657\frac{cm^2}{V_s}$. Irradiation condition: $V_{DS} = 0V, V_{BS} = -5V, V_{GS} = 5V$. Measured in the linear range at: $V_{DS} = 50mV$.

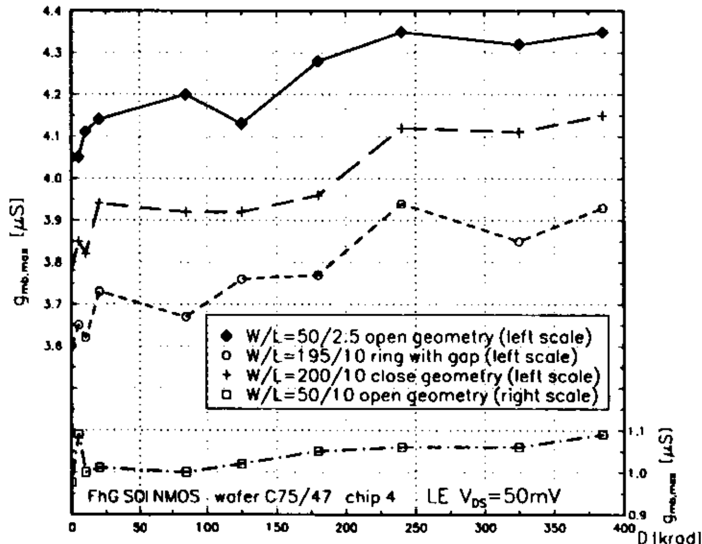


Figure 4.12: The variation of the maximum transconductance $g_{mb\ max}$ of back gate transistors with the total $\gamma$ dose for the SOI NMOS transistors. The value of mobility for the close geometry transistor after irradiation is $457\frac{cm^2}{V_s}$. Irradiation condition: $V_{DS} = 0V, V_{BS} = -5V, V_{GS} = 5V$. Measured in linear range at: $V_{DS} = 50mV$.



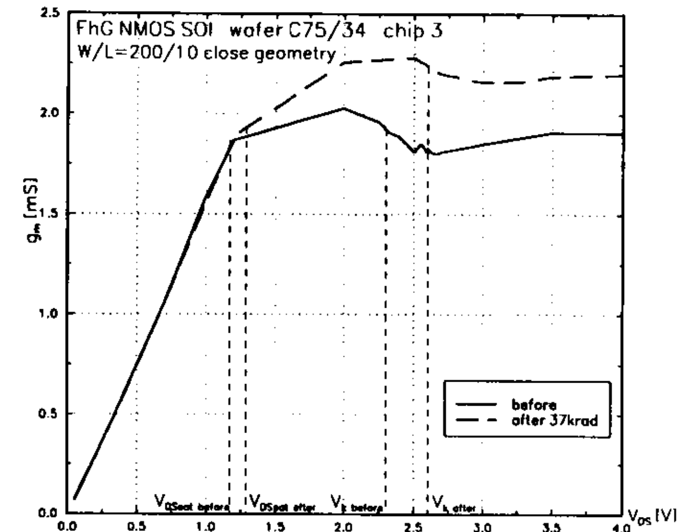


Figure 4.13: The transconductance $g_m$ versus the drain voltage $V_{DS}$ before and after irradiation by $\gamma$ irradiation for SOI NMOS transistor. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured at $V_{DS} = 2V, V_{BS} = 0V$.

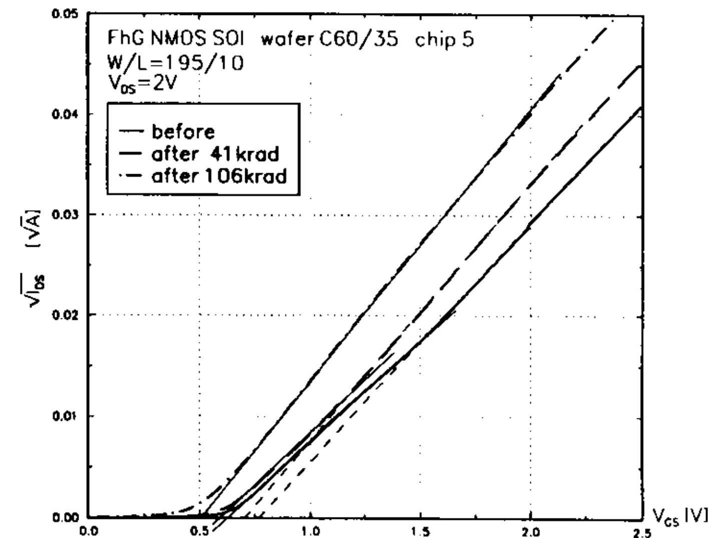


Figure 4.14: The transfer $I_{DS} - V_{GS}$ curves for the NMOS SOI transistor after subsequent irradiation by $\gamma$ radiation. Irradiation condition: $V_{GS} = 5V, V_{DS} = V_{BS} = 0V$. Measured in saturation at $V_{DS} = 2V$. The linear scale for drain current was used to present radiation behaviour above threshold voltage.

measurement data supplied by the HP4145B instrument. However, the tendency for transconductance to increase especially at the beginning of irradiation is evident. The Fig. 4.13. shows that the increase of transconductance occurs mainly in saturation. In the linear region a decrease at the level of −7% is observed; in the saturation below the kink point the transconductance increase amounts to +11.3% and above this point +16.8% (these values are measured at fixed gate voltage $V_{GS} = 2V$). The larger increase visible in Fig. 4.10. is related to the fact that it concerns the LDD structures. Therefore the radiation effect on the characteristic of SOI transistors is disturbed by the hot electron effect in a lesser degree.

The curves of the transfer characteristic in saturation i. e. the square root of drain current $\sqrt{I_{DS}}$ vs. gate voltage $V_{GS}$ for the SOI NMOS transistors exhibit two linear regions (see Fig. 4.14.): the first for smaller currents near the threshold voltage $V_{th}$, and the second for higher currents. The existence of the two characteristic parts is probably caused by the impact ionization current (see equation (2.30)). The electrons generated in this process are added to the channel current and increase observed drain current. This increase is especially visible in the neighbourhood of the threshold voltage when channel current is comparable with the impact ionization current. Such a phenomenon does not occur in the linear range of operation. In the second region of the transfer characteristic, the gain factor $\beta$ is bigger than in the first one. It is visible in Fig. 4.14. that the threshold voltage $V_{th}(QE)$ extracted from the second part of the curve is higher and does not adequately describe the behaviour of the transistor. Therefore the first part of the curve was chosen to extract the threshold voltage $V_{th}$ and the gain factor $\beta$. After irradiation, such an increase of the transconductance for rising gate voltage $V_{GS}$ disappears and the transfer characteristic becomes smooth. This is the first reason for the observed increase of the gain factor presented in Fig. 4.10. The second reason, which should be taken into account, is the interaction of back interface. The electrical field of positive oxide charge buildup induced by radiation in the buried oxide layer can affect electrons in the inversion layer (if there is no screening by floating body region). It results in the fact that the channel is thicker and the surface roughness scattering of electrons is smaller. In this way the mobility can increase in the SOI structure, especially for fully depleted devices [123]. On the other hand, the inversion layer capacitance is smaller in case of a thicker channel and therefore the effective capacitance (see equation (2.23)) lowers. It means that such a mechanism causes also a decrease of the gain factor but this effect is assumed negligible when $|V_{GS} - V_{th}| \geq 2V$ and the gate oxide thickness $t_{ox} \geq 15nm$. Another hypothesis, which could explain that effect, is a irradiation-induced increase of the extrinsic resistance $R_{EX}$. It was also studied in the range of smaller doses. However, the results indicate that such a hypothesis (which was mentioned in sec. 4.3.) cannot be confirmed.

The radiation behaviour of the threshold voltage $V_{th}(QE)$ of the front interface is presented in Fig. 4.15. The round transistors (200/10, 195/10) show very similar radiation induced changes. For the lower doses the radiation sensitivity of the threshold voltage $V_{th}$ is small and at the level of $-0.365\frac{mV}{krad}$ but above 80 $krad$ the radiation-induced threshold voltage shift $\Delta V_{th}$ increases and it is about $-3.09\frac{mV}{krad}$. The range of saturation in the threshold voltage shift was not observed. Two open geometry



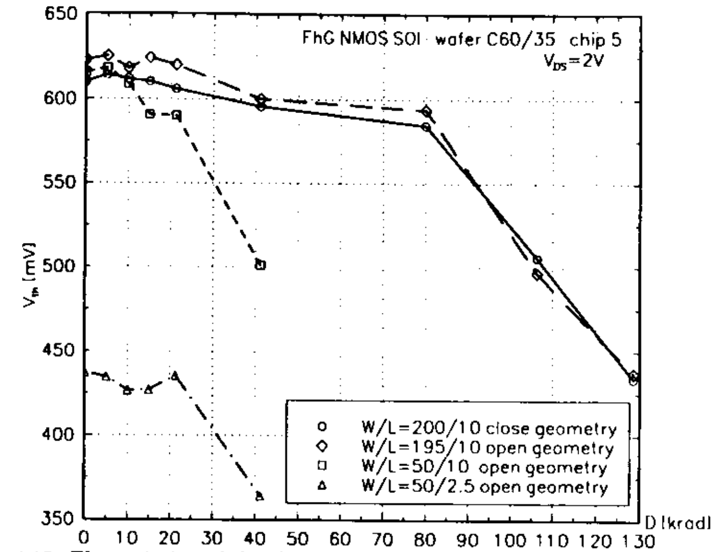


Figure 4.15: The variation of the threshold voltage $V_{th}$ with the total $\gamma$ dose for the SOI NMOS LDD transistors. Irradiated conditions: $V_{DS} = V_{BS} = 0V$, $V_{GS} = 5V$. Measured in saturation at: $V_{DS} = 2V$.

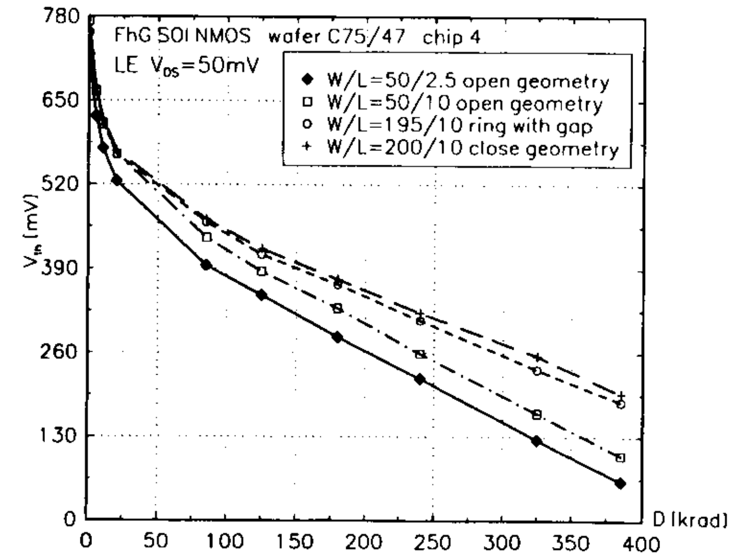


Figure 4.16: The variation of the threshold voltage $V_{th}$ with the total $\gamma$ dose for the SOI NMOS transistor. Irradiated conditions: $V_{DS} = 0, V_{BS} = -5V$, $V_{GS} = 5V$. Measured in linear range at: $V_{DS} = 50mV$.

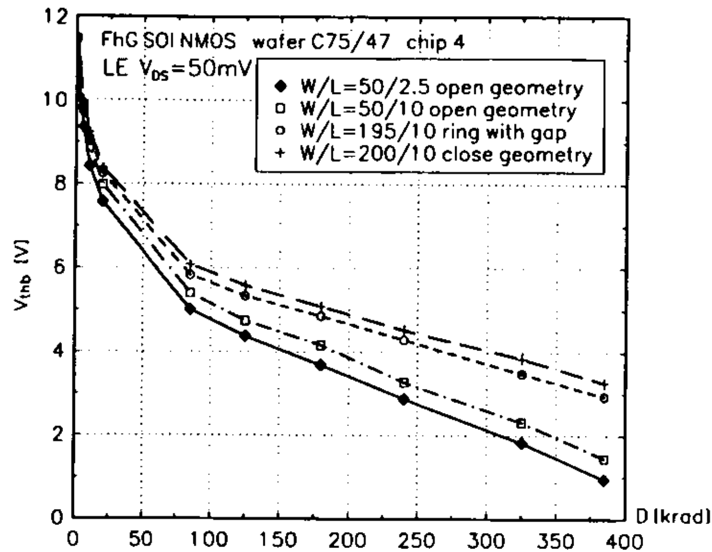


Figure 4.17: The variation of the threshold voltage of back interface $V_{thb}$ with the total $\gamma$ dose for the SOI NMOS transistor. Irradiated conditions: $V_{DS} = 0V$, $V_{BS} = -5V$, $V_{GS} = 5V$. Measured in linear range at: $V_{DS} = 50mV$.

transistors have also good stability of the threshold voltage, but at the dose of 40 $krad$ the leakage currents are so big that the notion of threshold voltage does not make sense. Therefore, a drastic crisis in the extracted value $V_{th}(QE)$ is visible. Another radiation behaviour is observed for transistors fabricated by another technological run and irradiated with a negative bias of the back gate $V_{BS} = -5V$ (Fig. 4.16.). For a low dose the threshold voltage shifts quickly $-13.9\frac{mV}{krad}$ and for the higher doses (above 125 krad) the radiation sensitivity is smaller on the level of about $-0.85\frac{mV}{krad}$. Simultaneously, in the same irradiation and measurement conditions, the shift of the back gate threshold voltage (Fig. 4.17.) exhibits radiation sensitivity $-235\frac{mV}{krad}$ at the beginning of irradiation (below 10 $krad$) and $-8.9\frac{mV}{krad}$ for the higher doses above 125 krad. The initial threshold voltage of back interface is about $11V$ due to the buried oxide thickness about $380nm$. In the Fig. 4.17. and Fig. 4.16. it is visible that linear geometry transistors (50/2.5 and 50/10) have lower threshold voltage values. It is caused by high leakages of activation of the sidewall transistors which achieve $1\mu A$ at 80 $krad$ for a short transistor and at 325 $krad$ for a long transistor (measured at $V_{GS} = V_{BS} = 0V$ neglecting the threshold voltage shift). A similar difference is also visible between the fully closed ring transistor and the ring transistor which has small gap.

The NMOS SOI transistors without the LDD spacers are very sensitive to a breakdown when they are irradiated with a grounded back gate. Breakdowns usually occur



during the first step of irradiation. Only several NMOS transistors worked properly after the dose at the level of 20 – 30 $krad$ achieved in four steps of irradiation. The biggest dose without breakdown was 125 $krad$. This was observed in the case of biggest transistor ($W/L = 50/50$) and its variation of threshold voltage is presented in Fig. 4.18. This figures contains the comparison between two similar transistor irradiated in different conditions: with a grounded and negatively biased back gate electrode. When the back gate is grounded the threshold voltage decreases linearly and the slope of the curve is about $\approx -3.5\frac{mV}{krad}$. When the back gate is negatively biased the radiation sensitivity for a low dose below 10 $krad$ is considerably higher $\approx -13.9\frac{mV}{krad}$ but for higher doses it is at the level of about $\approx -1\frac{mV}{krad}$. It means that in the range of lower doses the radiation sensitivity of the threshold voltage is smaller when the device is irradiated with grounded back gate but in the range of higher doses the devices with a negatively biased back gate exhibit smaller radiation sensitivity of the threshold voltage. However, the breakdown sensitivity during irradiation shows the necessity of negative bias at the back gate.

The device with split-source structure suppressing the kink effect and (in the case of $p$-type source edges) the radiation-induced sidewall leakage are very sensitive to the breakdowns. For transistors with $p$-type contacts made at the edges of the

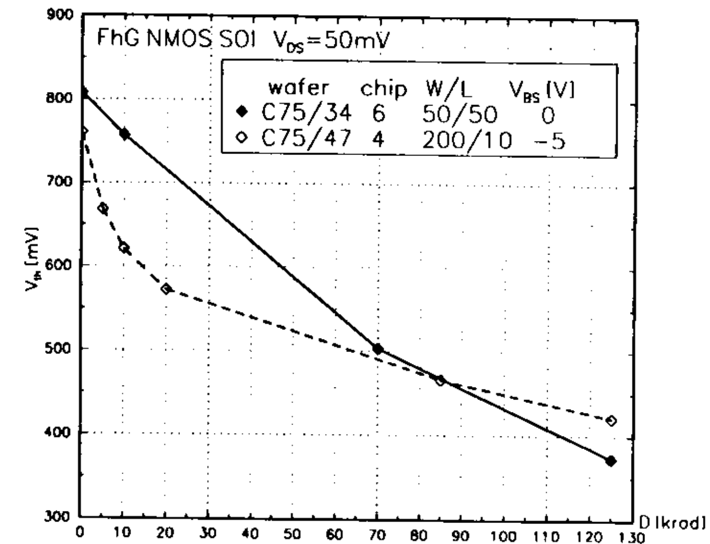


Figure 4.18: The comparison of the radiation-induced threshold voltage changes for two SOI NMOSFETs without the LDD spacer irradiated with $0V$ and $-5V$ at the back gate. Irradiated conditions: $V_{DS} = 0V$, $V_{GS} = 5V$, $V_{BS} = 0V$ for the transistor from wafer C75/34 and $V_{BS} = -5V$ for the transistor from wafer C75/47. Measured in linear range at: $V_{DS} = -50mV$.

source region (see Fig. 2.8.) the proper operation after the first step of irradiation ($\approx$ 5 *krad*) was only observed onece. The transistors with *n*-type contacts fabricated at the source edges work properly to a high doses without breakdown but the sidewall effect is considerably.

For the PMOS SOI transistor the radiation-induced changes of the subthreshold swing are shown on Fig. 4.19. At the beginning of irradiation a decrease of the subthreshold swing is observed. Then, in the range of a dose above 40 *krad* a considerable increase occurs. In comparison with Fig. 4.9 (the curve for close geometry transistor) the changes up and down occur in a reverse sequence. When the subthreshold swing for the NMOSFET increases the same parameter for the PMOSFET decreases and inversely. Probably, this is a result of the competition of two mechanisms. When for PMOSFET the decrease of depletion capacitance predominates, for NMOSFET the increase of interface state capacitance prevails. In the range of the bigger doses the effect of depletion capacitance reduction predominates for NMOSFET, but the interface state increase predominates for PMOSFET.

The transconductance reduction for PMOSFETs are presented in figures: Fig.4.20 for structures (wafer C60/35) irradiated with the back gate bias $V_{BS} = 0V$, Fig.4.21 for structures (wafer C75/47) irradiated with the back gate bias $V_{BS} = -5V$, Fig.4.22 irradiated with back gate bias $V_{BS} = 0V$. These reductions are about $-12\%$, $-13\%$, $-18\%$ respectively for the cases listed above at the level of 125 *krad*.

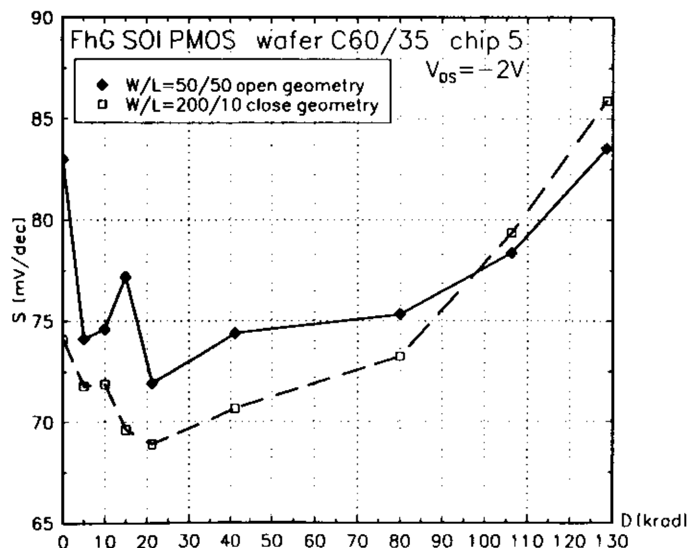


Figure 4.19: The variation of the subthreshold swing $S$ with the total $\gamma$ dose for the SOI PMOS transistor. Irradiation condition: $V_{DS} = 0V = V_{BS} = 0V, V_{GS} = 5V$. Measured in saturation at $V_{DS} = -2V$.



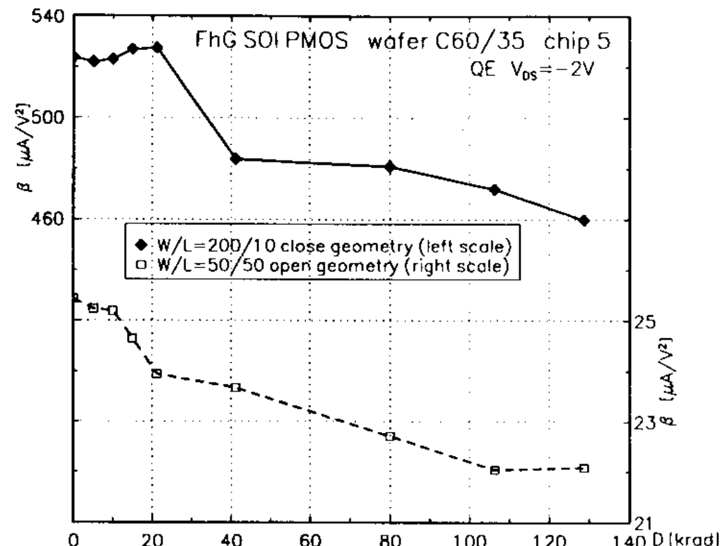


Figure 4.20: The variation of the gain factor $\beta$ with the total $\gamma$ dose for the SOI PMOS transistors. Irradiation condition: $V_{DS} = 0V, V_{BS} = 0V, V_{GS} = 5V$. Measured in linear range at: $V_{DS} = -2V$.

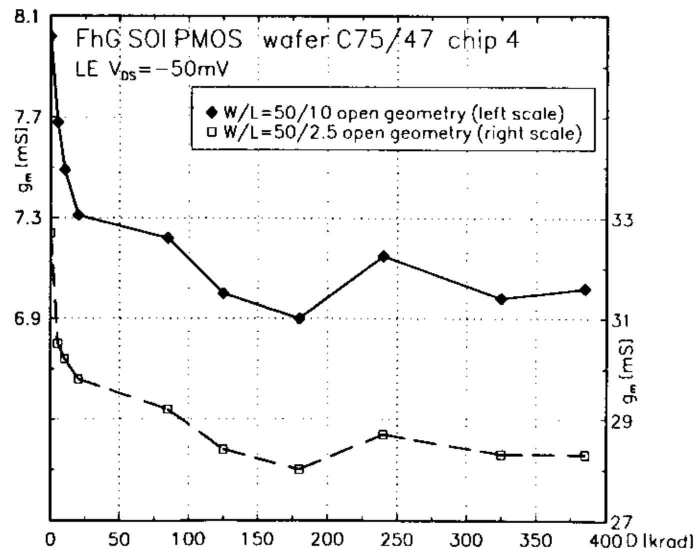


Figure 4.21: The variation of the maximum transconductance $g_{m,max}$ with the total $\gamma$ dose for the SOI PMOS transistors. Irradiation condition: $V_{DS} = 0V, V_{BS} = -5V, V_{GS} = -5V$. Measured in linear range at: $V_{DS} = -50mV$.

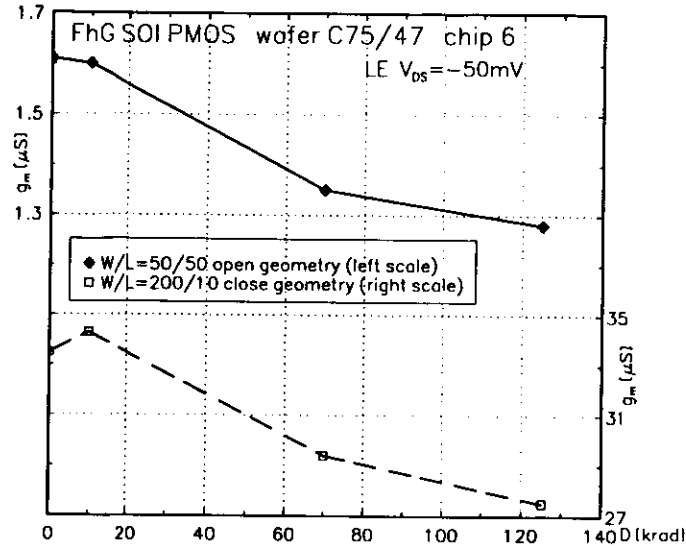


Figure 4.22: The variation of the maximum transconductance $g_{m,max}$ with the total $\gamma$ dose for the SOI PMOS transistors. Irradiation condition: $V_{DS} = 0V, V_{BS} = 0V, V_{GS} = -5V$. Measured in linear range at: $V_{DS} = -50mV$.

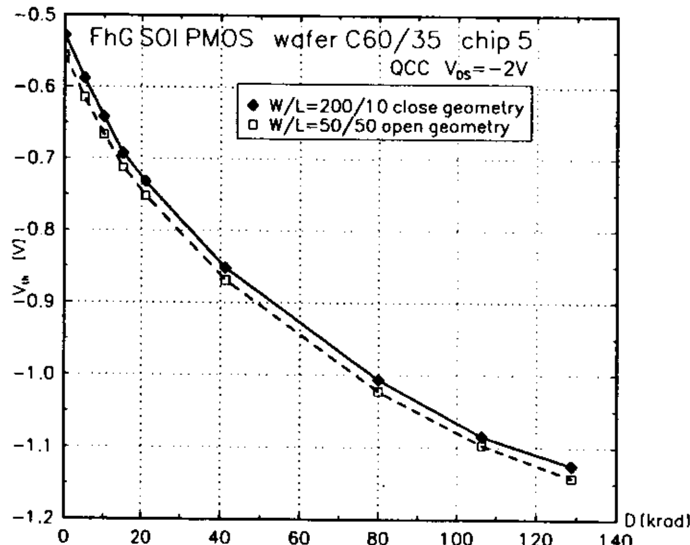


Figure 4.23: The variation of the threshold voltage $V_{th}$ with the total $\gamma$ dose for the SOI PMOS transistors. Irradiated conditions: $V_{DS} = V_{BS} = 0V$, $V_{GS} = 5V$. Measured in saturation at: $V_{DS} = -2V$.



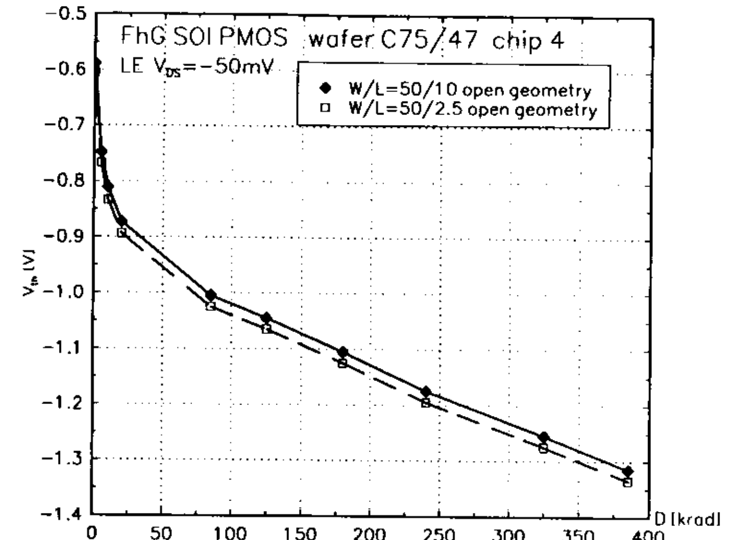


Figure 4.24: The variation of the threshold voltage $V_{th}$ with the total $\gamma$ dose for the SOI PMOS transistors. Irradiated conditions: $V_{DS} = 0$, $V_{BS} = -5V$, $V_{GS} = -5V$. Measured in linear range at: $V_{DS} = -50mV$.

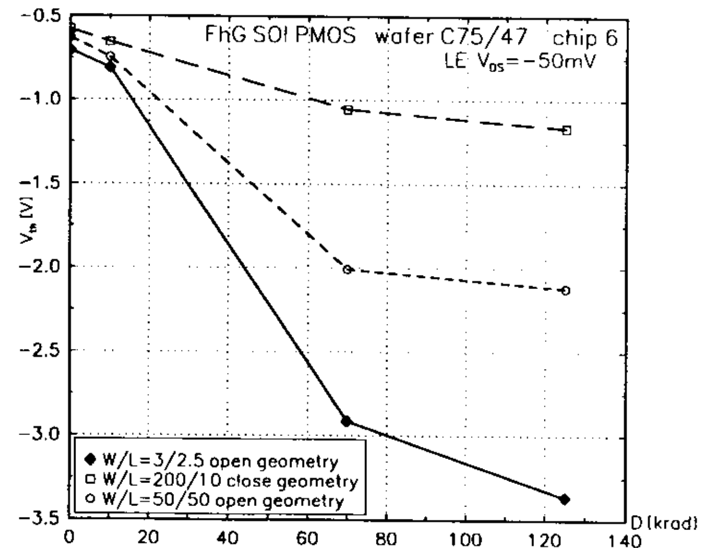


Figure 4.25: The variation of the threshold voltage $V_{th}$ with the total $\gamma$ dose for the SOI PMOS transistors. Irradiated conditions: $V_{DS} = V_{BS} = 0V$, $V_{GS} = -5V$. Measured in linear range at: $V_{DS} = -50mV$.

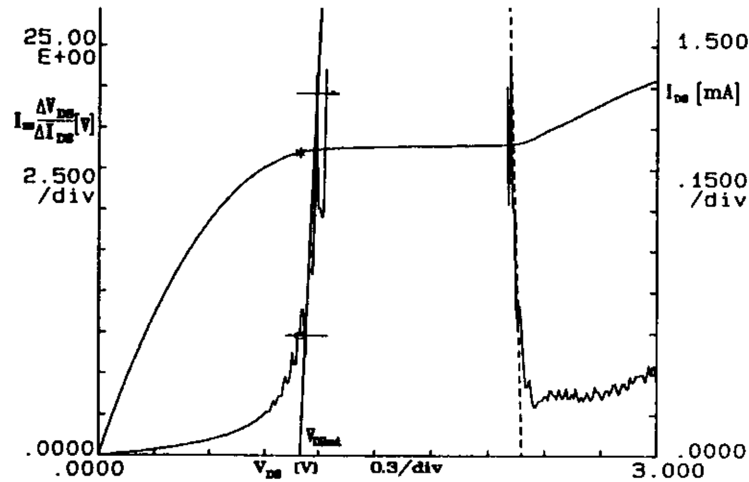


Figure 4.26: The extraction method for the drain saturation voltage $V_{DSsat}$ and the kink effect voltage $V_k$ by using the HP4145 instrument.

The radiation sensitivity of threshold voltage of PMOS SOI transistors is demonstrated in Fig. 4.23 for structures irradiated with back gate bias $V_{BS} = 0V$ and in Fig. 4.24 for structures (another wafer) irradiated with back gate bias $V_{BS} = -5V$. For low doses (up to $10 - 15$ *krad*) the threshold voltage shift for one krad is bigger: $\approx 10\frac{mV}{krad}$ (wafer C60/35) and $\approx 23\frac{mV}{krad}$ (wafer C75/47). In the range of bigger doses respective values are considerably smaller $\approx 3.5\frac{mV}{krad}$, $\approx 1\frac{mV}{krad}$.

A general conclusion is that SOI transistors work better in the presence of a negative bias on the back gate. Although the radiation-induced changes especially at the beginning of irradiation are bigger when negative potential is applied to the back gate electrode, the NMOS transistors work properly up to the radiation level of several hundred krad. When the back gate potential is zero (and also $V_{DS} = 0V$) during irradiation the NMOS transistors exhibit a breakdown phenomena already at the level of $20-40$ *krad*. The radiation behaviour of PMOSFETs is also very irregular and very varying from one to the other device even within the same chip. Sometimes the threshold voltage shift of the front gate transistor is bigger than for the sidewall transistors (see Fig. 3.19. and Fig. 4.25.).

## 4.7 The influence of radiation on the kink effect

The well-known kink effect (see sec. 2.1.5) is restricting the use of SOI MOS transistors in analog circuit applications. The radiation behaviour of the kink effect is also very important for systems operating in radiation environment.

While testing the radiation hardness of SOI MOS transistors fabricated by the



FhG IMS an amelioration of the output characteristic of NMOSFETs and an exacerbation of PMOSFETs were observed.

The results presented below employed drain saturation voltage $V_{DSsat}$ and current $I_{Dsat}$ values extracted by the method proposed by Moon et al. in [105]. The model presented in this work is based on more accurate velocity-field relationship in the linear region and finite drain conductance due to the channel length modulation effect in the saturation region. This model supplies the following asymptotic relationship for drain-to-source current in the deep saturation regime:

$$I_{DSsat}\frac{\partial V_{DS}}{\partial I_{DS}} = \frac{V_{DSsatl}^2 + V_L^2}{V_L V_\lambda}(V_{DS} - V_{DSsat}) \qquad (4.46)$$

where $V_{DSsatl}$ is the intrinsic drain saturation voltage (excluding influence of the source and the drain parasitic resistances), $V_L = \mathcal{E}_{hs}L_{eff}$, $\mathcal{E}_{hs}$ is the critical field for velocity saturation, $L_{eff}$ is the effective gate length, $V_\lambda = \mathcal{E}_{hs}\lambda$, $\lambda$ is the characteristic length for channel length modulation. The equation (4.46) shows that the $V_{DSsat}$ can be determined from the plot $I_{DS}\frac{\Delta V_{DS}}{\Delta I_{DS}}$ versus $V_{DS}$ as a x-intercept of the straight line tangential to this plot. This method is easy to implement using HP4145B instrument as it is presented in Fig. 4.26. For extraction of the kink voltage $V_k$ a similar method can be used, despite the lack of an analytical model describing this region of the output characteristic.

The Fig. 4.27. and Fig. 4.28. present radiation-induced changes in the output characteristic of the SOI NMOS transistor. Three facts are visible:

- both the saturation value of the drain current $I_{Dsat}$ and the kink effect voltage $V_k$ increase in a similar manner (see Fig. 4.29.). It means that the power consumption increases after irradiation (from $3mW$ before irradiation to $8.5mW$ after 385 *krad* at the kink point);
- the kink effect voltage $V_k$ increases faster than the saturation drain voltage $V_{Dsat}$ (see Fig. 4.30.), so the length of the output characteristic plateau ($g_{dsat} \approx 12\mu S$) in the saturation region increases. It means that the device properties in a saturation ameliorate after irradiation;
- the parameter $f$ rapidly decreases in the range of lower doses (up to 30 *krad*) from a very high initial value (see Fig. 4.31.), crosses the border line ($f = 0.1V^{-1}$, see sec. 2.1.5.) just after 10 *krad* and then saturates above 200 *krad* ($f = 0.03V^{-1}$). This behaviour is due to a decrease in drain conductance in the range above kink point $g_{dkink}$ which is visible in Fig. 4.28. It means that an irradiated device is better in the aspect of kink effect.

The second kink is not shifted after irradiation and the sublinear region between two kinks shortens, so for a big dose the output characteristic is superlinear in the whole kink region and only the second kink can be observed. However, the drain conductance decreases in the region above the second kink point, too.

The Fig. 4.32. and Fig. 4.33. present radiation-induced changes in the output characteristic of the SOI PMOS transistor. Three facts are visible:

- both the saturation value of drain current $I_{Dsat}$ and the kink effect voltage $V_k$ decrease in similar manner (see Fig. 4.34.). It means that the power consumption decreases after irradiation (from $880\mu W$ before irradiation to $100\mu W$ after 385 *krad* at the kink point);

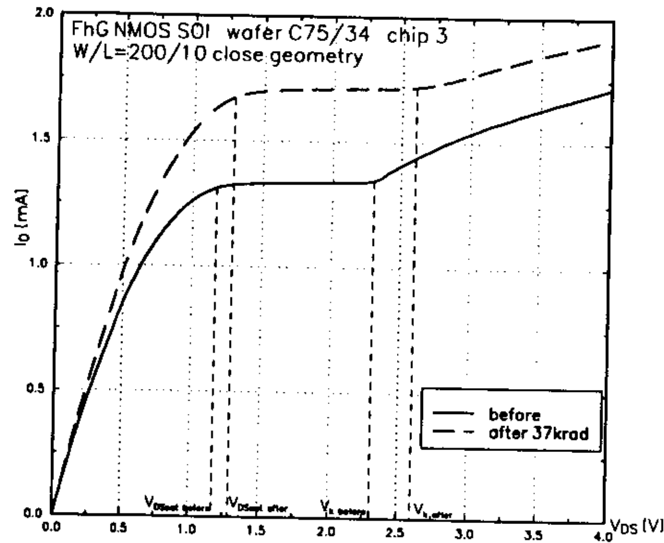


Figure 4.27: The output characteristics of the SOI NMOSFET before and after irradiation by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured at $V_{DS} = 2V, V_{BS} = 0V$.

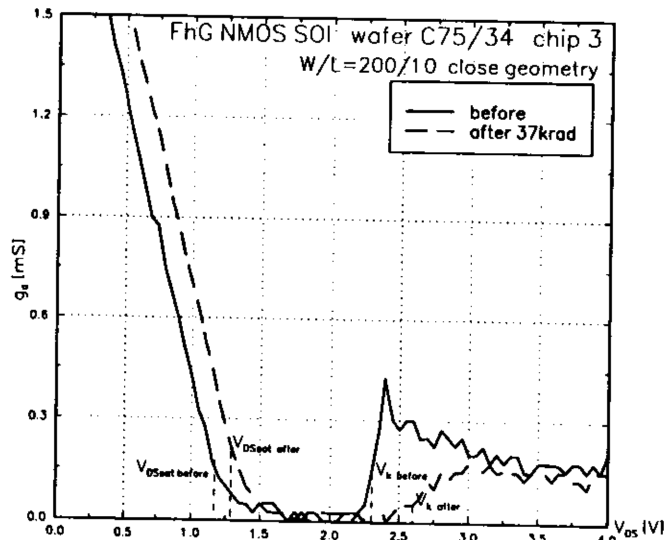


Figure 4.28: The drain conductance $g_d$ versus the drain voltage $V_{DS}$ before and after irradiation by $\gamma$ irradiation for the SOI NMOSFET. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured at $V_{DS} = 2V, V_{BS} = 0V$.



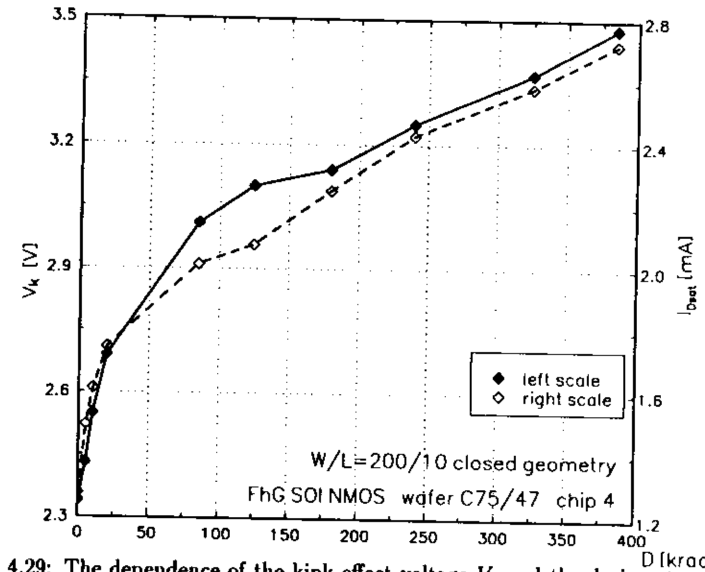


Figure 4.29: The dependence of the kink effect voltage $V_k$ and the drain saturation current $I_{Dsat}$ on total $\gamma$ dose for the SOI NMOSFET. Irradiation condition: $V_{DS} = 0V, V_{GS} = 5V, V_{BS} = -5V$. Measured at $V_{GS} = 2V, V_{BS} = 0V$.

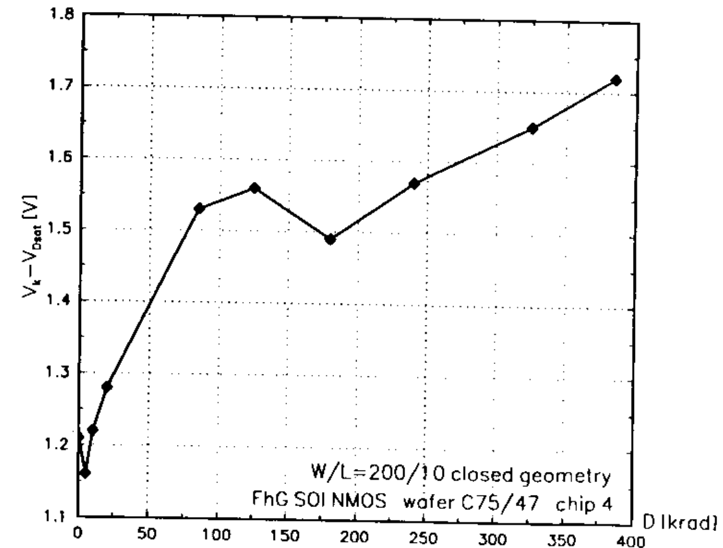


Figure 4.30: The difference between the kink effect voltage and the drain saturation voltage $V_k - V_{Dsat}$ for the SOI NMOSFET versus total $\gamma$ dose. Irradiation condition: $V_{DS} = 0V, V_{GS} = 5V, V_{BS} = -5V$. Measured at $V_{GS} = 2V, V_{BS} = 0V$.

- the kink effect voltage $V_k$ decreases faster than the saturation drain voltage $V_{DS\ sat}$ (see Fig. 4.35.), so the length of the output characteristic plateau ($g_{dsat} \approx 0.5\mu S$) in the saturation region decreases. It means that the device properties in saturation deteriorate after irradiation;
- the kink effect appears after irradiation. The parameter $f$ increases in the manner presented in Fig. 4.36. and its value exceeds the limit of $0.1V^{-1}$ at total dose 350 $krad$. This behaviour is due to the increase in the drain conductance in the range above kink point $g_{dkink}$ (see Fig 4.33. It means that the device after irradiation is worse in the aspect of the kink effect.

A general conclusion is that the radiation-induced changes in the charge buildup in the buried oxide and at the back $Si - SiO_2$ interface cause the change of electric field near the drain of the transistor. In the case of a NMOSFET the field decreases but simultaneously for a PMOSFET it increases. For the PMOS SOI transistors such an explanation of radiation-induced kink effect was confirmed by 2D simulation reported in [106].

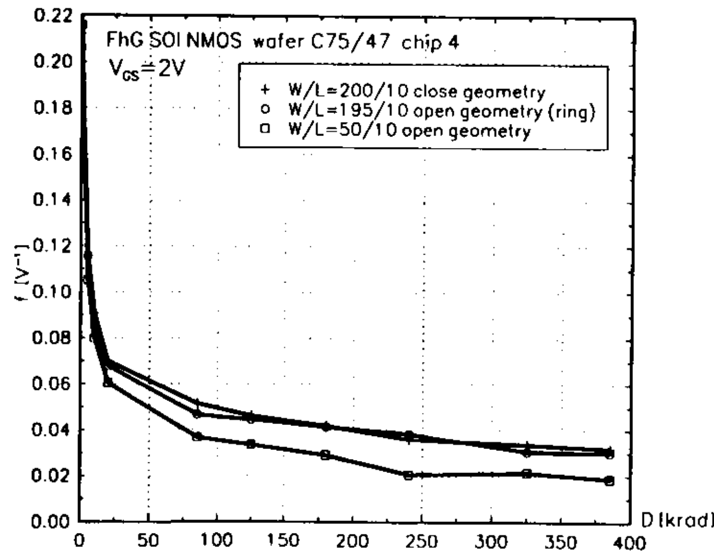


Figure 4.31: The dependence of the parameter $f$ describing the kink effect on the total $\gamma$ dose for the SOI NMOSFET. Irradiation condition: $V_{DS} = 0V, V_{GS} = 5V, V_{BS} = -5V$. Measured at $V_{GS} = 2V, V_{BS} = 0V$.



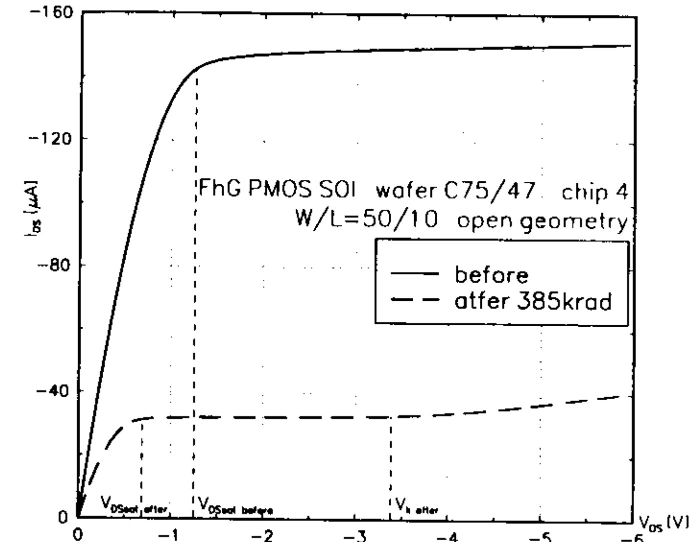


Figure 4.32: The output characteristics of the SOI PMOSFET before and after irradiation by $\gamma$ radiation. Irradiation condition: $V_{DS} = 0V, V_{BS} = -5V, V_{GS} = -5V$. Measured at $V_{DS} = -2V, V_{BS} = 0V$.

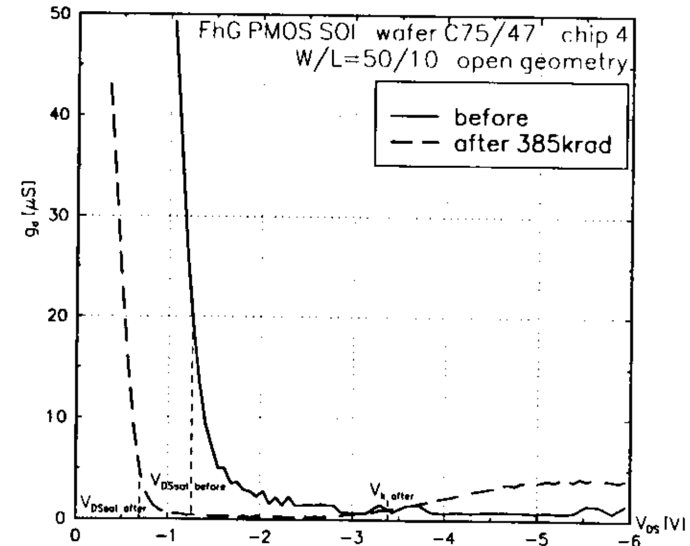


Figure 4.33: The drain conductance $g_d$ versus the drain voltage $V_{DS}$ before and after irradiation by $\gamma$ irradiation. Irradiation condition: $V_{DS} = 0V, V_{BS} = -5V, V_{GS} = -5V$. Measured at $V_{DS} = -2V, V_{BS} = 0V$.

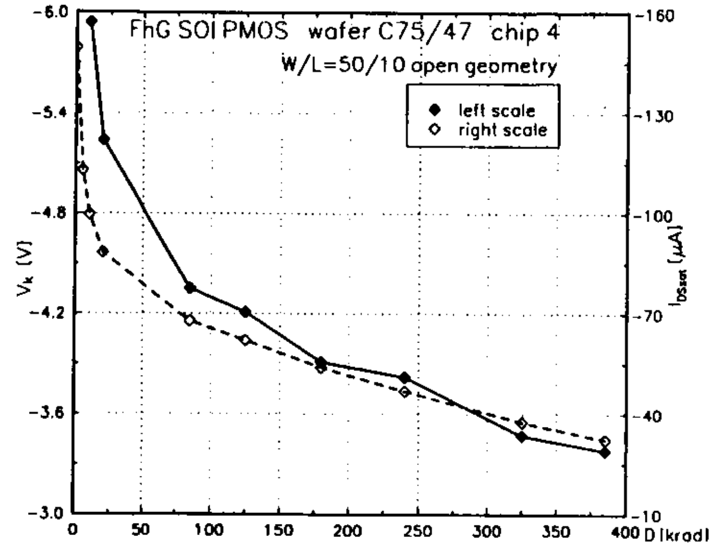


Figure 4.34: The dependence of the kink effect voltage $V_k$ and the drain saturation current $I_{Dsat}$ on total $\gamma$ dose for the SOI PMOSFET. Irradiation condition: $V_{DS} = 0V, V_{GS} = -5V, V_{BS} = -5V$. Measured at $V_{GS} = -2V, V_{BS} = 0V$.

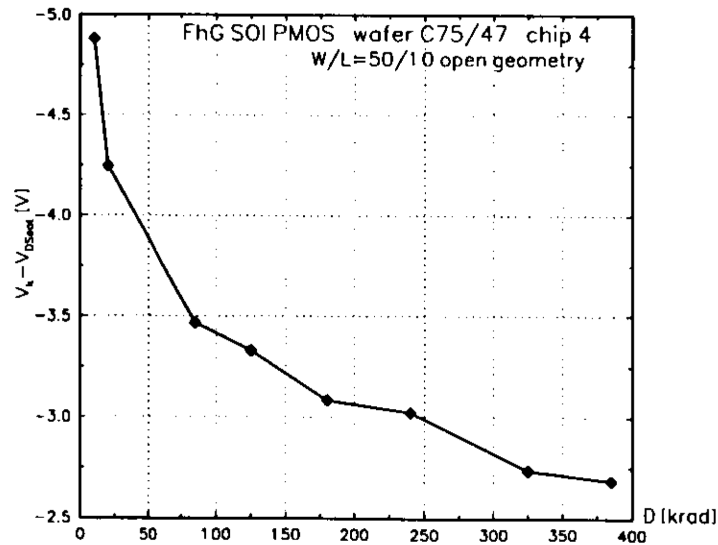


Figure 4.35: The difference between the kink effect voltage and the drain saturation voltage $V_k - V_{Dsat}$ for the SOI NMOSFET versus total $\gamma$ dose. Irradiation condition: $V_{DS} = 0V, V_{GS} = -5V, V_{BS} = -5V$. Measured at $V_{GS} = -2V, V_{BS} = 0V$.



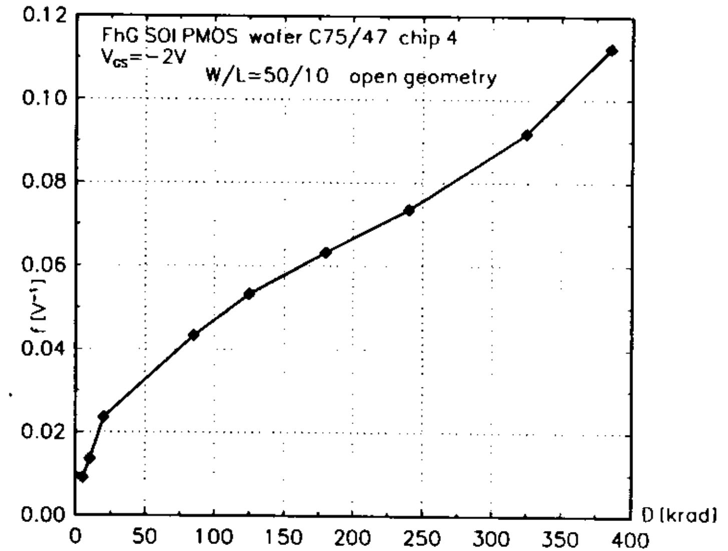


Figure 4.36: The dependence of the parameter $f$ describing the kink effect on total $\gamma$ dose for the SOI PMOSFET. Irradiation condition: $V_{DS} = 0V, V_{GS} = -5V, V_{BS} = -5V$. Measured at $V_{GS} = -2V, V_{BS} = 0V$.

# Chapter 5

# Flicker noise

When we say "flicker noise" we have in mind the noise phenomena with the following spectrum [134]:

$$S(f) = \frac{AI^{\vartheta}}{f^{\gamma}}, \tag{5.1}$$

where $A$, $\vartheta$, $\gamma$ are constants, $I$ is the current, $f$ is the frequency. Although the exponent $\gamma$ is not always strictly equal to 1, the name "$1/f$ noise" is also commonly used.

In spite of nearly fifty years of investigations on $1/f$ noise, this phenomenon is still not well-understood. This kind of noise is observed not only in the domain of electricity but also in geological, physiological and musical phenomena. The theory of flicker noise is developed on the basis of the very abstract fields of thermodynamics, statistical and quantum mechanics and also of the chaos theory. There are also more speculative investigations of the common origin of all $1/f$ fluctuation phenomena.

However, it is impossible to answer the question whether the $1/f$ noise can be reduced (like generation-recombination noise) or whether it is a fundamental low which governs this phenomenon (like thermal noise). In the field of semiconductor devices physics, this dilemma can be expressed more precisely. Is the $1/f$ noise caused by generation-recombination processes between free carriers and surface traps or by some other fluctuations in the lattice scattering in the bulk? These two opinions are well-formulated in two competitive theories. The first theory is called the number-fluctuation model and it was proposed by McWhorter and later developed mainly by Sah and van der Ziel. The second theory is the mobility-fluctuation model proposed by Hooge and it is based on many experimental facts but today there are quantum theories supporting this point of view.

The MOS transistors fabricated by different technologies show the behaviour which supports one of the two competitive theories. Recently, a new approach which comprises elements of both models has appeared.

In this chapter, an attempt to review of $1/f$ noise theories in the MOS structure will be given and then the observations of this phenomenon in the function of total $\gamma$ dose will be presented. A separate section will be dedicated to the noise kink effect in the SOI MOS transistor and its dependence on radiation.





## 5.1 Models for flicker noise in MOSFETs

A general mathematical concept [140] for explaining $1/f$ spectrum consists in summation of a large number of so called Lorentzian spectra. This type of spectrum (commonly related to generation-recombination phenomena) is caused by fluctuations $\delta X$ which satisfies the following simple differential equation:

$$\frac{d\delta X}{dt} + \frac{\delta X}{\tau} = 0. \tag{5.2}$$

This equation leads to the exponential autocorrelation function $\overline{\delta X(t_0)\delta X(t_0+t)}$ and after using Wiener-Khintchine theorem we obtain a Lorentzian spectrum:

$$S_X(f) = \overline{(\delta X)^2}\frac{4\tau}{1+(2\pi f\tau)^2}. \tag{5.3}$$

The summation of these spectra, each for a different time constant $\tau$, produces $1/f$ spectrum when the statistical weights used, are proportional to $\tau^{-1}$. Below, this mathematical principle will be applied in the case of McWhorter's [131] model. It will be reported following van der Ziel [134].

The mobility fluctuation school of ideas is based on the empirical relation proposed by Hooge [140] for homogeneous samples:

$$\frac{S_G}{G^2} = \frac{\alpha_H}{N}\frac{1}{f}, \tag{5.4}$$

where $G$ is the sample conductance, $S_G$ is the spectral density of the conductance fluctuations, $N$ is the total number of charge carriers, $\alpha_H$ is a dimensionless constant with a value of about $2\times10^{-3}$ usually called Hooge's constant. It was experimentally proved that $\alpha_H$ depends mainly on the lattice scattering. Other scattering mechanisms like impurity, surface or electron-electron scattering do not take part in fluctuations responsible for $1/f$ noise. The presence of other scattering mechanisms in mobility decreases $\alpha_H$ value according to equation:

$$\alpha_H = (\frac{\mu}{\mu_l})^2\alpha_{Hl}, \tag{5.5}$$

where $\alpha_{Hl} = 2\times10^{-3}$ is the Hooge's constant for $1/f$ noise in lattice scattering, $\mu$ is the mobility which consists of several kinds of mobility: $\mu_l$, $\mu_i$, $\mu_s$, $\mu_{e-e}$ each caused by respective scattering mechanisms: lattice, impurity, surface, electron-electron. Mathiessen's rule combines these mobilities as follows:

$$\frac{1}{\mu} = \frac{1}{\mu_l} + \frac{1}{\mu_i} + \frac{1}{\mu_s} + \frac{1}{\mu_{e-e}}. \tag{5.6}$$

The relation (5.4) concerns the volume of homogeneous sample and therefore cannot be directly used to the inversion layer of a MOS structure. To describe the MOSFET noise by using the equation (5.4), the finite thickness of the inversion layer and the carrier density and mobility profiles in it must be taken into account. Below, this theory developed by Vandamme [141], [142] will be discussed shortly.

### 5.1.1 The number-fluctuation model

The number-fluctuation model assumes that flicker noise in MOSFETs is caused by carriers density fluctuations, brought about by interactions of free carriers to border traps via interface states. The classical works in this topic use term "oxide traps" but here the newer terminology (see chap: 2) introduced recently by Fleetwood [18] will be used. The name "border traps" seems to be more suitable for $1/f$ noise considerations.

The interactions of free carriers to border traps occur by tunneling [132] at constant energy $E$, but not directly to the border traps. Neither the Auger-impact mechanism, nor the photon mechanism, nor even the multiphoton process are plausible. Interface states must act like intermediate states [133]. The tunneling barrier is assumed as a rectangular barrier of a height $\psi_B$:

$$\psi_B = \frac{E_C^{ox} - E_C^{Si}}{q}, \tag{5.7}$$

where $E_C^{ox}$ is the oxide conduction band edge, $E_C^{Si}$ is the silicon conduction band edge. We neglect band bending in the oxide and barrier lowering caused by the image force.

Let us consider the number of border traps in the volume $\Delta x \Delta y \Delta z$ of oxide

$$N_{bt} = n_{bt}(E)\Delta E \Delta x \Delta y \Delta z, \tag{5.8}$$

and the number of interface states in the surface $\Delta y \Delta z$

$$N_{it} = D_{it}(E)\Delta E \Delta y \Delta z, \tag{5.9}$$

both with an energy between $E$ and $E + \Delta E$. The differential equation describing the trapping process on the border and surface states is:

$$\frac{dN_t}{dt} = g(N_t) - r(N_t), \tag{5.10}$$

$$\begin{aligned} g(N_t) &= \zeta N_s(N_{bt} - N_t), \\ r(N_t) &= \xi N_t(N_{it} - N_s), \end{aligned} \tag{5.11}$$

where $N_t$, $N_s$ are the numbers of carriers in the border traps and in the interface states respectively, $g(N_t)$, $r(N_t)$ are the functions describing the generation and the recombination of carriers, $\zeta, \xi$ are constants. The interactions between the channel carriers and the surface states can be neglected because they are considerably faster than interactions between channel carriers and the border traps.

In an equilibrium:

$$g(N_t) = r(N_t), \tag{5.12}$$

$$\begin{aligned} N_s &= N_{s0} = N_{it}f_t, \\ N_t &= N_{t0} = N_{bt}f_t, \end{aligned} \tag{5.13}$$

where $f_t$ is the fractional occupancy which is expressed by the Fermi-Dirac statistics:

$$f_T = \{1 + \exp(\frac{E - E_F}{kT})\}^{-1}, \tag{5.14}$$



and $E_F$ is the quasi-Fermi level. Substituting (5.13) to (5.12), we obtain the following condition for the equilibrium state:

$$\zeta = \xi. \tag{5.15}$$

Let us consider slow fluctuations:

$$\begin{aligned} N_s &= N_{s0} + \delta N_s, \\ N_t &= N_{t0} + \delta N_t. \end{aligned} \tag{5.16}$$

Expanding functions (5.11) around equilibrium state $N_{t0}$, $N_{s0}$, the differential equation for fluctuations in the number of carriers trapped in the border traps $\delta N_t$ is obtained:

$$\frac{d\delta N_t}{dt} = \zeta N_{bt}\delta N_s - \zeta N_{it}\delta N_t + g(t) - r(t). \tag{5.17}$$

Let us now substitute $\delta N_s = -v\delta N_t$ and bear in mind that $N_{bt}$ is proportional to $\Delta x \Delta y \Delta z$ and $N_{it}$ to $\Delta y \Delta z$. In subsequent integration process with respect to $x$, we let $\Delta x$ go to zero, so that the first term in (5.17) becomes negligible. Therefore it can be assumed:

$$\tau = \frac{1}{\zeta N_{it}}, \tag{5.18}$$

as the dominant lifetime.

The general differential equation for our noise system is:

$$\frac{d\delta N_t}{dt} + \frac{\delta N_t}{\tau} = g(t) - r(t). \tag{5.19}$$

Using the Langevin method the power spectral density of the fluctuations in the number of trapped electrons (App. C) is obtained:

$$S_{N_t}(f) = \frac{\tau^2}{1 + \omega^2\tau^2}(S_g(f) + S_r(f)). \tag{5.20}$$

Functions $S_g(f)$, $S_r(f)$ represent shot-noise sources and therefore:

$$S_g(f) = S_r(f) = 2g(N_{t0}) = 2r(N_{t0}). \tag{5.21}$$

Using (5.21), (5.20), (5.11), (5.13), (5.8), one obtains:

$$g(N_{t0})\tau = n_{bt}(E)\Delta E \Delta x \Delta y \Delta z f_T(1 - f_T). \tag{5.22}$$

Hence:

$$S_{N_t}(f) = 4n_{bt}(E)\Delta E \Delta x \Delta y \Delta z f_T(1 - f_T)\frac{\tau}{1 + \omega^2\tau^2}. \tag{5.23}$$

This formula contains the well-known generation-recombination term called Lorentzian spectrum. The following step is to integrate this formula over volume $\Delta x \Delta y \Delta z$ and energy $E$.

For integrating along distance $x$ into oxide depth the distribution of the border traps versus the time constant $\tau$ must be known:

$$d(\tau) = \frac{dN_{bt}}{d\tau} = \frac{dN_{bt}}{dx}\frac{1}{\frac{d\tau}{dx}}. \quad (5.24)$$

The time constant $\tau$ associated with a trapping event depends exponentially on the distance into the oxide, because the electron wave function decays exponentially into a rectangular barrier:

$$\tau = \tau_0 \exp(\epsilon x), \quad (5.25)$$

and:

$$\epsilon = \sqrt{\frac{8m_{SiO_2}\psi_B}{\hbar^2}}, \quad (5.26)$$

where $m_{SiO_2}$ is the effective electron mass in the oxide, $\hbar$ is Plank's constant divided by $2\pi$. If an uniform trap distribution in space $\frac{dN_{bt}}{dx} = C$ is assumed for $0 < x < x_1$ and the lack of traps for $x > x_1$:

$$d(\tau) = \frac{C}{\epsilon\tau} \quad (5.27)$$

If the exponent at $\tau$ deviates from 1, the exponent $\gamma$ in the spectrum (5.1) will be also different than 1. Normalizing:

$$\int_{\tau_0}^{\tau_1} d(\tau)d\tau = 1, \quad \text{one obtains} \quad C = \frac{1}{x_1} = \frac{\epsilon}{\ln(\frac{\tau_1}{\tau_0})}, \quad (5.28)$$

where $\tau_1$ is the longest time constant belonging to traps placed in the highest distance $x_1$ from interface. Expressing $dN_{bt}$ in two ways: in $\tau$ domain:

$$dN_{bt} = d(\tau)d\tau = \frac{d\tau}{\tau\ln(\frac{\tau_1}{\tau_0})}, \quad (5.29)$$

and in $x$ domain:

$$dN_{bt} = C dx = \frac{dx}{x_1}. \quad (5.30)$$

Hence:

$$dx = x_1\frac{d\tau}{\tau\ln(\frac{\tau_1}{\tau_0})}. \quad (5.31)$$

It means that $\Delta x$ in (5.23) can be substituted by $x_1 d(\tau)d\tau$. Integrating (5.23) with respect to $\tau$:

$$S_{N_t}(f) = 4n_{bt}(E)\Delta E\Delta y\Delta z x_1 f_T(1-f_T)\frac{1}{\ln\frac{\tau_1}{\tau_0}}\int_{\tau_0}^{\tau_1}\frac{d\tau}{1+\omega^2\tau^2}$$

$$= \frac{n_{bt}(E)\Delta E\Delta y\Delta z x_1 f_T(1-f_T)}{f\ln\frac{\tau_1}{\tau_0}}\frac{2}{\pi}(\arctan(\omega\tau_1) - \arctan(\omega\tau_0)). \quad (5.32)$$



In the frequency range $\frac{1}{\tau_1} < \omega < \frac{1}{\tau_0}$, this yields:

$$S_{N_t}(f) = \frac{n_{bt}(E)\Delta E\Delta y\Delta z x_1 f_T(1-f_T)}{f\ln\frac{\tau_1}{\tau_0}}. \quad (5.33)$$

Below the frequency $\frac{1}{\tau_1}$ equation (5.32) predicts flattened spectrum and above frequency $\frac{1}{\tau_0}$ the spectrum should be steeper, it means $1/f^2$. These two facts have not been experimentally observed.

Integration of (5.33) in energy domain is simple because the function $f_T(1-f_T)$ has a very sharp peak at the Fermi energy level $E_F$. A new parameter $n_{bt}(E_F)_{eff}$ called the effective trap density at the Fermi level must be introduced:

$$n_{bt}(E_F)_{eff} = \int_{-\infty}^{+\infty} n_{bt}(E)f_T(1-f_T)dE = n_{bt}(E_F)kT \quad (5.34)$$

where in last step it was assumed that $n_{bt}(E) \approx n_{bt}(E_F)$ for $E$ not far from $E_F$. After integration (5.33) with respect to $z$ along the entire device width $W$:

$$S_{N_t}(f) = \frac{n_{bt}(E_F)_{eff}x_1}{f\ln\frac{\tau_1}{\tau_0}}W\Delta y = \frac{x_1 n_{bt}(E_F)kT}{f\ln\frac{\tau_1}{\tau_0}}W\Delta y = \frac{kTD_{bt}(E_F)}{f\ln\frac{\tau_1}{\tau_0}}W\Delta y, \quad (5.35)$$

where $D_{bt}(E) = \int_0^{x_1} n_{bt}(E)dx = x_1 n_{bt}(E)$ is the border trap density per unit energy per unit area. Spectral density of fluctuations in the number of trapped electrons $S_{n_t}(f)$ defined for a unit area is equal to:

$$S_{n_t}(f) = \frac{kTD_{bt}(E_F)}{f\ln\frac{\tau_1}{\tau_0}}. \quad (5.36)$$

Now, the formula (5.35), (5.36) for power spectral density of fluctuations in the number of trapped electrons is derived. Next, the influence of this quantity upon the measurable characteristics of a device at certain bias should be considered.

In a very strong inversion the fluctuation in the number of free carriers $\delta N$ is equal to fluctuation in the number of trapped carriers $-\delta N_t$. When the gate voltage $V_{GS}$ changes toward the threshold voltage $V_{th}$ and below it, the ratio:

$$R = \left|\frac{\delta N}{\delta N_t}\right|, \quad (5.37)$$

defined by Reimbold [138], decreases from value 1 to very small value $10^{-4}$ in weak inversion. It means:

$$\delta N = -R\delta N_t, \quad S_N(f) = R^2 S_{N_t}(f), \quad S_n(f) = R^2 S_{n_t}(f). \quad (5.38)$$

This ratio can be expressed as:

$$R = \left|\frac{\delta Q_I}{\delta Q_{bt}}\right| = \frac{\frac{Q_I}{V_t}}{C_D + C_{ox} + C_{it} - \frac{Q_I}{V_t}} \quad (5.39)$$

where $\delta Q_I = -C_{inv}\delta\phi_s$ is the channel charge fluctuation, $\delta\phi_s$ is the surface potential fluctuation, $\delta Q_{bt} = (C_{ox} + C_{it} + C_D + C_{inv})\delta\phi_s$ is the charge of carriers trapped in the oxide calculated from charge conservation law applied to MOS structure, $C_{ox}$, $C_{it}$, $C_D$, $C_{inv} = -\frac{Q_I}{V_t}$ are the gate oxide, interface states, depletion layer and channel capacitances respectively. The channel capacitance is expressed using the same idea like in equation (B.5).

Spectral density of drain voltage fluctuation (in linear range of operation) can be expressed using equation (2.42):

$$S_{V_{DS}}(f) = \frac{q^2}{C_{ox}^2 WL}\left[\frac{V_{DS}}{(V_{GS} - V_{th} - V_{DS})}\right]^2 \frac{kTD_{bt}(E_F)}{\ln\frac{\tau_1}{\tau_0}}\frac{1}{f}. \tag{5.40}$$

### 5.1.2 The mobility-fluctuation model

The mobility-fluctuation model is developed by means of Hooge's relations (5.4), (5.5) and therefore sometimes is also called "$\alpha$-noise". When the MOS transistor is considered as a sample with resistance $R = \frac{1}{G}$, the spectral density of conductance fluctuation is [141]:

$$\frac{S_G}{G^2} = \frac{\alpha_H}{Nf} = \alpha_{Hl}\left(\frac{\mu_n}{\mu_l}\right)^2 \frac{q\mu_n R}{L^2}\frac{1}{f} = \frac{\alpha_{Hl} q\mu_{1/f} R}{L^2 f}, \tag{5.41}$$

where $\mu_{1/f} = \frac{\mu_n^3}{\mu_l^2}$ is the noise mobility introduced to take into account the reduction in $\alpha_H$ in comparison with $\alpha_{Hl}$, $N = \frac{L^2}{q\mu_n R}$ is the number of free carriers in the transistor inversion layer which is obtained by integrating the following equation:

$$\begin{aligned} g(V) &= \frac{I_{DS}dy}{dV} = \frac{Q_I dy}{dV dt} \\ &= \frac{q\Delta N\mu_n dV}{dV dy} = \frac{q\mu_n \Delta N}{\Delta y}, \end{aligned} \tag{5.42}$$

where $I_{DS} = g(V)\frac{dV}{dy}$ is the drain current, $g(y) = g(V)$ is the conductance per unit length of the channel at the distance $y$ from source, $V(y)$ is the channel potential at the same point, $Q_I$ is the charge in the inversion layer.

To make the result (5.41) more realistic the channel must be considered as built of sub-layers parallel to the interface. Each sub-layer has its own mobility, carrier concentration and parameter $\alpha_H$. A good approximation of electron distribution along the depth of channel is:

$$n(x) = n_s \exp\left(-\frac{x}{t_c}\right), \tag{5.43}$$

where $n_s$ is the carrier concentration at the interface, $t_c = \frac{\delta}{4}$ where $\delta$ is the inversion layer thickness. To estimate surface scattering effects the following equation for mobility profile was proposed:

$$\mu_n(x) = \mu_l\left(1 - \exp\left(-\frac{x}{v}\right)\right), \tag{5.44}$$



where $v = 2\lambda_{eff}$, $\lambda_{eff}$ is the effective mean free path. For one sub-layer with thickness $dx$ the equation (5.41) can be written:

$$dS_G = \frac{\alpha_H}{Nf} = \frac{\alpha_{Hl} q}{\mu_l^2 L^2 f}\mu_n^3(x) dG, \tag{5.45}$$

where $dG = q\mu_n(x)n(x)\frac{W dx}{L}$ is the conductance of one sub-layer. Assuming no correlation between noise in each sub-layer, the integration of (5.45) along channel depth $\delta$ gives:

$$\frac{S_G}{G^2} = \frac{\alpha_{Hl} q}{L^2 f}\left[\mu_l \frac{\int_0^\delta (\mu_n(x)/\mu_l)^4 n(x)dx}{\int_0^\delta (\mu_n(x)/\mu_l) n(x)dx}\right] R, \tag{5.46}$$

where $R^{-1} = G = \frac{qW}{L}\int_0^\delta \mu_n(x)n(x)dx$ is the total channel conductance obtained by adding the conductance of each sub-layer. From comparison with (5.41), we see that the expression in rectangular parenthesis defines the effective noise mobility $\mu_{1/f}$ for this case. Using equations (5.43), (5.44), we find:

$$\mu_{1/f} = \frac{\mu_l}{(1 + v/2t_c)(1 + v/3t_c)(1 + v/4t_c)}. \tag{5.47}$$

It means that in the linear region the equation (5.41) is valid with the effective noise mobility calculated by equation (5.47). For drain current fluctuations, using simple expression for conductance $G = \mu_{eff} C_{ox}(V_{GS} - V_{th})\frac{W}{L}$, it leads to:

$$S_{I_{DS}} = \frac{\alpha_{Hl} q(\mu_{1/f}/\mu_{eff}) I_{DS}^2}{WLC_{ox}(V_{GS} - V_{th})f}, \tag{5.48}$$

where $\mu_{eff}$ is the effective mobility and it is defined by equation (2.19).

Up to that point it has been assumed that the drain voltage $V_{DS}$ is small in comparison with $V_{GS} - V_{th}$ and therefore we have been able to use functions $n$ and $\mu_n$ which do not depend on distance $y$ along the channel. This is not true in the non-ohmic region where gradient of the free carrier concentration along the channel can be very large. Therefore for non-ohmic region, the second component of noise besides the mobility fluctuations must be taken into account. The mobility fluctuation at point $y$ induces fluctuation in resistance of an elemental section of channel and then it causes change also in the effective gate voltage at this point of channel. The next consequence is a change in number of carriers in the channel part beyond $y$. Such a positive feedback mechanism leads to a correlation between the fluctuation of the resistance of an elemental section at $y$ due to the mobility fluctuations and the resistance fluctuation in the channel beyond $y$ which is due to the number fluctuations. Taking both components into account and using well-known expression for saturation current, the equation for the drain current spectral density at the saturation point ($V_{DS} = V_{DSsat} = V_{GS} - V_{th}$) is obtained [142]:

$$S_{I_{DS}} = \frac{\alpha_{Hl} q\mu_{1/f}\mu_{eff} WC_{ox}(V_{GS} - V_{th})^3}{2L^3 f}. \tag{5.49}$$

Generally, it can be said that at the saturation point the relative noise in the current is just twice the relative noise in the ohmic region. Therefore in this mode of operation the expression (5.48) for drain current spectral density containing additional factor 2 in the numerator can be used. In this way the equation (5.49) was obtained.

### 5.1.3 The unified model

There are several attempts of unification of two presented above models. Because the fluctuation of trapping process results in mobility and in number of carriers fluctuations, two components of fluctuating voltages are correlated. The autocorrelation function $A(\tau)$ of the voltage fluctuation can be expressed [143]:

$$\begin{aligned} A(\tau) &= \overline{[\delta V_n(t) + \delta V_\mu(t)][\delta V_n(t+\tau) + \delta V_\mu(t+\tau)]} \\ &= \overline{\delta V_\mu(t)\delta V_\mu(t+\tau)} + \overline{\delta V_n(t)\delta V_n(t+\tau)} \\ &+ \overline{\delta V_n(t)\delta V_\mu(t+\tau)} + \overline{\delta V_\mu(t)\delta V_n(t+\tau)}, \end{aligned} \tag{5.50}$$

where $\delta V_\mu, \delta V_n$ are voltage fluctuation due to mobility and carrier number fluctuation, respectively. The last two terms in above equation represent cross-correlation terms. When the variance of $\delta V_n$ is significantly larger than $\delta V_\mu$, or vice versa, they can be neglected. The correlated manner of combination was presented by two slightly different methods in articles [144], [145] and it was applied to circuit simulation [146].

When the drain current in a small section $\Delta y$ of transistor channel is expressed in the following way:

$$I_{DS} = Wq\mu n_c \mathcal{E}_h, \tag{5.51}$$

where $\mathcal{E}_h$ is the horizontal channel field, $n_c$ is the surface density of free carriers in the channel, the fractional change of local drain current is:

$$\frac{\delta I_{DS}}{I_{DS}} = \left[\frac{R}{N} \pm \frac{1}{\mu}\frac{\delta\mu}{\delta N_t}\right]\delta N_t, \tag{5.52}$$

where $N = n_c W\Delta y$, $N_t = n_t W\Delta y$, $n_t$ is the surface density of carriers captured in the border traps. It means that the fluctuation in the occupancy in the number of border traps $\delta N_t$ induces correlated fluctuations in the carrier number (the first term) and mobility (the second term). The Reimbold's parameter $R$ was defined by equation (5.37). To evaluate the second term, the Sun-Plummer relation (see equations (4.6), (4.7)) is used in the form:

$$\frac{1}{\mu} = \frac{1}{\mu_{il}} + \frac{\alpha}{\mu_{il}} n_t \tag{5.53}$$

where $(\frac{\alpha n_t}{\mu_{il}})^{-1}$ represents the mobility limited by the border charge scattering and $\mu_{il}$ is the mobility limited by the other scattering mechanisms (see equations (5.6), (2.12)). The equation (5.53) results in:

$$\frac{\delta\mu}{\delta N_t} = -\frac{\alpha}{\mu_{il}}\frac{\mu^2}{W\Delta y}, \tag{5.54}$$

and (5.52) becomes:

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{R}{n_c} \pm \frac{\alpha}{\mu_{il}}\mu\right)\frac{\delta N_t}{W\Delta y}, \tag{5.55}$$



The Langevin method (App. C) gives the local current fluctuations [145] [144]:

$$S_{I_{DS}}(f) = -\left[\frac{I_{DS}}{N}(R \pm \frac{\alpha}{\mu_{il}}\mu n_c)\right]^2 S_{N_t}(f), \tag{5.56}$$

where $S_{N_t}(f)$ is the power spectral density of the fluctuations in the number of trapped electrons over the area $W\Delta y$ , supplied by the conventional theory of number fluctuations (see equation (5.35)).

The equation (5.56) provides several complicated formulas describing flicker noise of MOSFET for each region of operation. Three fitted parameters are required [146]. These formulas despite of their complication are suitable for circuit simulation and give very good results.

## 5.2 Noise measurement

The measurement system for noise shown on Fig. 5.1 consists of the shielded probe station and FFT spectrum analyzer. The probe station contains the investigated transistor called DUT (Device Under Test), the batteries biasing the transistor, the potentiometers for adjusting work points of the transistor and the preamplifier. The preamplifier works in the current mode and converts the current noise signal to the voltage signal $v_o$ which is fed to the input of the signal analyzer. The noise signal consists not only of the drain current fluctuations but also of the thermal noise of load $R_D$ and feedback $R_f$ resistors, as well as of the current $i_n$ and the voltage $v_n$ input noise of the operational amplifier. When the gate is not hf short-circuited to the ground the thermal noise of the gate bias resistor $R_G$ must be also taken into account. The thermal noise of the drain conductance $g_d$ is included in the quantity $i_d^2$. All noise sources present in the measurement system are shown on Fig. 5.1 b). The noise at the output of the current preamplifier is expressed by the relation:

$$\begin{aligned} \frac{d<v_0^2>}{df} &= R_f^2[\frac{d<i_d^2>}{df} + \frac{d<i_n^2>}{df} + \frac{d<v_n^2>}{df}(\frac{1}{R_f} + \frac{1}{R_D} + g_d) \\ &+ 4k_BT(\frac{1}{R_f} + \frac{1}{R_D} + R_G g_m^2)] \end{aligned} \tag{5.57}$$

Shielding of the probe station is effective in eliminating the influence of fluorescent lights, interferences with power supplies and other equipment working in the laboratory. The power supply of the operational amplifier is connected through a simple two-pole passive filter in both plus and minus terminals. The precautionary measures were used to avoid the presence of a 50-Hz peak and its multiples in the observed spectrum.

The frequency range in which the noise spectrum is observed depends on the $R_D$, $R_f$ resistances . The low limit frequency can be expressed as:

$$f_l = \frac{1}{2\Pi}\frac{1}{C(\frac{R_f}{1+|A_0|} + \frac{R_D}{1+g_d R_D})}. \tag{5.58}$$

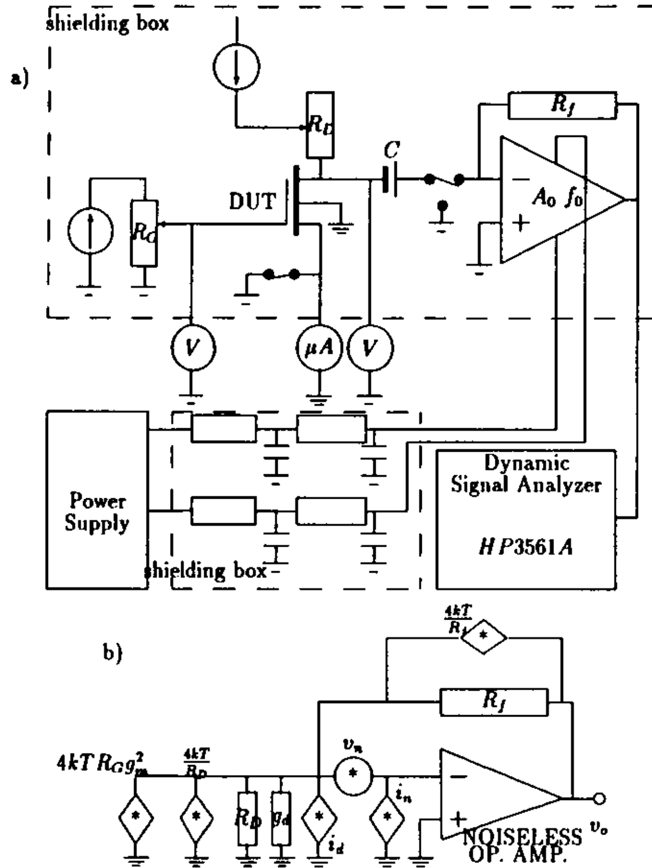


Figure 5.1: The noise measurement system: a) the schematic diagram, b) the equivalent circuit of noise preamplifier.

Respectively the high frequency limit is:

$$f_h = f_0 \left( 1 + |A_0| \frac{\frac{R_D}{1+g_dR_D}}{R_f + \frac{R_D}{1+g_dR_D}} \right), \tag{5.59}$$

where $A_0$ is the open loop gain, $f_0$ is the open loop cut-off frequency. All other symbols are shown in Fig. 5.1.

The main part of the measurement system is a HP3561A dynamic signal analyzer [147].



Table 5.1: The flicker noise parameters $K_v, \gamma, S_{th}$ for bulk NMOS transistor (IMEC, chip 04-11, W/L=30/10) after subsequent irradiations by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured in linear range at: $V_{GS} = 4V, I_{DS} = 300\mu A$.

| D [krad] | $K[\frac{A^2}{Hz^{1-\gamma}}]$ | $\frac{K}{g_m^2}[\frac{V^2}{Hz^{1-\gamma}}]$ | $K_v\,[\frac{V^2}{Hz^{1-\gamma}}]$ | $\gamma$ | $S_{th}[\frac{A^2}{Hz}]$ |
|---|---|---|---|---|---|
| 0 | $1.096 \times 10^{-18}$ | $1.165 \times 10^{-10}$ | $7.7915 \times 10^{-11}$ | 0.990 | $1.267 \times 10^{-23}$ |
| 23 | $1.174 \times 10^{-18}$ | $1.315 \times 10^{-10}$ | $8.7757 \times 10^{-11}$ | 1.005 | $1.407 \times 10^{-23}$ |
| 65 | $1.065 \times 10^{-18}$ | $1.231 \times 10^{-10}$ | $8.7460 \times 10^{-11}$ | 0.995 | $1.380 \times 10^{-23}$ |
| 134 | $1.113 \times 10^{-18}$ | $1.287 \times 10^{-10}$ | $9.7444 \times 10^{-11}$ | 1.007 | $1.440 \times 10^{-23}$ |
| 205 | $1.175 \times 10^{-18}$ | $1.373 \times 10^{-10}$ | $1.0616 \times 10^{-10}$ | 1.007 | $1.230 \times 10^{-23}$ |

**The presented parameters are:**
$\frac{K}{g_m^2}$ **is the noise level transformed to an equivalent gate voltage,**
$K_v = K R^2 \left(\frac{V_{GS}-V_{th}-V_{DS}}{V_{DS}}\right)^2$ **is the noise level normalized with respect to drain** $V_{DS}$ **and threshold** $V_{th}$ **voltages,**
$R = \frac{R_D}{1+R_D g_d}$ **is the resistance in the drain circuit,**
$\gamma$ **is the frequency exponent,**
$S_{th}$ **is the component independent of frequency.**

## 5.3 Radiation influence on flicker noise

The noise power spectrum of the drain current was fitted to a simple formula similar to (5.1):

$$S_{I_{DS}}(f) = \frac{K}{f^\gamma} + S_{th} \tag{5.60}$$

where $K$ is the noise level of the drain current flicker noise, $\gamma$ is the frequency exponent, $S_{th}$ is the component independent of frequency representing the thermal noise of the system. These three parameters were chosen to fit the data.

The bulk NMOS transistor was irradiated with the gate voltage $V_{GS} = 5V$ and the grounded drain, source and bulk terminals . The noise power spectra were recorded by the presented system (see Fig. 5.1.) during five pauses in the irradiation. The spectrum before irradiation is presented in Fig. 2.10. The bias condition during the measurement was chosen at the fixed gate voltage $V_{GS} = 4V$ and at the fixed drain current $I_{DS} = 300\mu A$. Changes in the position of the work point after subsequent irradiations together with values of the drain conductance and the transconductance at these work points are presented in Fig. 5.2. and Fig. 5.3. The inaccuracies in the adjustment of work points are visible. The fitting results are presented in Tab. 5.1. The noise level was transformed by means of equations (2.36), (2.42). The increase of the noise level is presented in Fig. 5.4.

The noise level $K$ is five orders of magnitude higher then the component independent of frequency $S_{th}$. Only 60% of last one can be explained by three thermal noise sources present in the measurement system (see Fig. 5.1.): channel noise $4kTg_d$,

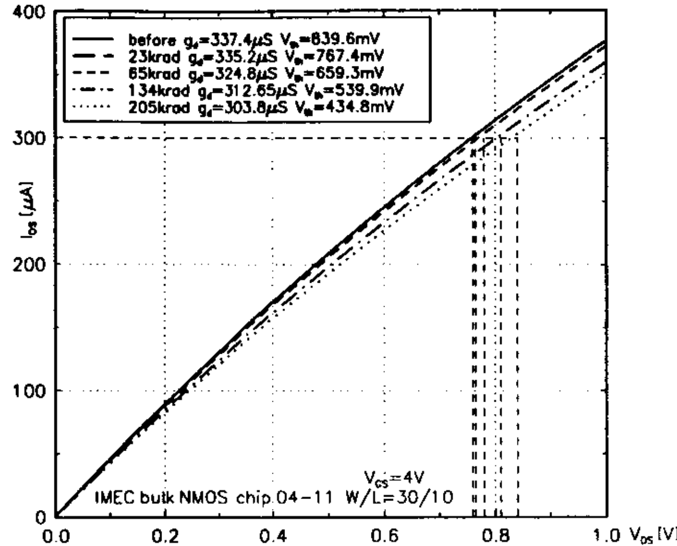


**Figure 5.2:** The work points during the noise spectra measurements after subsequent irradiations of the bulk NMOS transistor by $\gamma$ radiation marked on the output characteristics. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$.

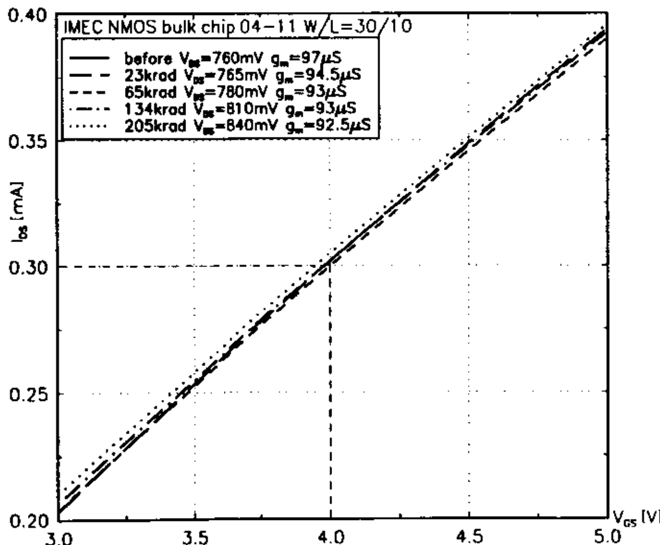


**Figure 5.3:** The work points during noise spectra measurements after subsequent irradiations of the bulk NMOS transistor by $\gamma$ radiation marked on the transfer characteristics. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$.



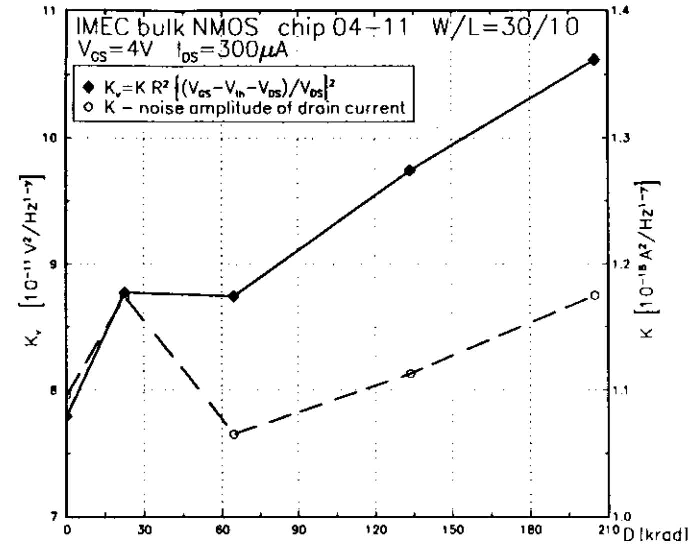


**Figure 5.4:** The noise level as the function of the total $\gamma$ dose for the NMOS bulk transistor. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$.

load resistance noise $4kTR_D$, and gate biasing circuit noise $4kTR_G g_m^2$. The remaining 40% cannot also be explained by noise of the amplifier input and the feedback resistor which do not excess the level of $10^{-22}\frac{A^2}{Hz}$ at the frequency 1Hz and rapidly decrease achieving the constant level of $10^{-24}\frac{A^2}{Hz}$ at 100Hz. This fact was recognized by the background noise measurement in two configurations: with open preamplifier input and with a known resistance connected to the input. It means that the white noise component on the level of about $5 \times 10^{-24}\frac{A^2}{Hz}$ origins from transistor and it does not depend on radiation.

The bulk PMOS transistor was irradiated up to the dose of 365 *krad*. During irradiation the drain, source and bulk terminals were short-circuited to the ground and the gate voltage was $V_{GS} = -5V$. The work point for the noise power spectra recording was chosen before irradiation in the linear range. After the dose of 85 *krad* this work point shifted so much that it was in the saturation range. The choosing of a new work point was necessary. Therefore only results concerning the range 85 − 365 *krad* are presented. The measurements for smaller doses are not comporable with these results. This second bias condition during the measurement was chosen at the fixed gate voltage $V_{GS} = -3.5V$ and at the fixed drain current $I_{DS} = -240\mu A$. Changes in the position of the work point and values of the drain conductance and the transconductance are presented in Fig. 5.5. and Fig. 5.6. The transfer characteristic intersect at this work point and the transconductance increases. Despite this fact the equivalent noise at the gate increases. The increase of the noise level is presented in Fig. 5.7. and other results from fitting are listed in the Tab. 5.2.

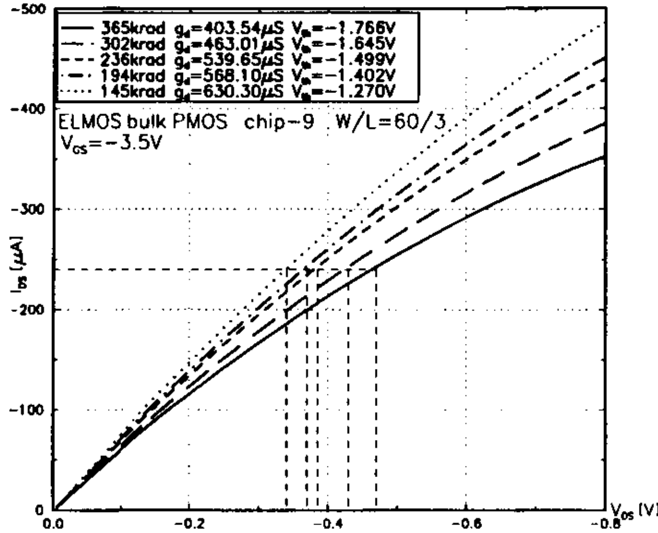


Figure 5.5: The work points during the noise spectra measurements after subsequent irradiations of the bulk PMOS transistor by $\gamma$ radiation marked on the output characteristics. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$.

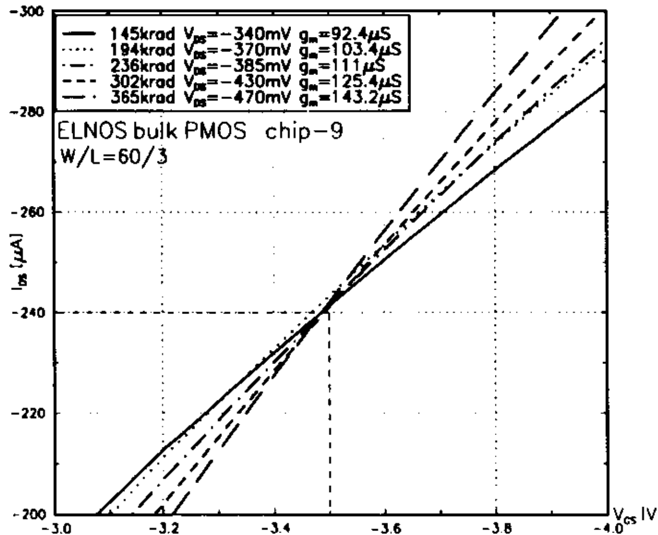


Figure 5.6: The work points during the noise spectra measurements after subsequent irradiations of the PMOS transistor by $\gamma$ radiation marked on the transfer characteristics. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$.



Table 5.2: The flicker noise parameters $K_v, \gamma, S_{th}$ for bulk PMOS transistor (ELMOS, chip 9, W/L=60/20) after subsequent irradiations by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$. Measured in linear range at: $V_{GS} = -3.5V, I_{DS} = -240\mu A$.

| D [krad] | $K[\frac{A^2}{Hz^{1-\gamma}}]$ | $\frac{K}{g_m^2}[\frac{V^2}{Hz^{1-\gamma}}]$ | $K_v\ [\frac{V^2}{Hz^{1-\gamma}}]$ | $\gamma$ | $S_{th}[\frac{A^2}{Hz}]$ |
|---|---|---|---|---|---|
| 85.4 | $2.719 \times 10^{-19}$ | — | — | 1.123 | $1.926 \times 10^{-23}$ |
| 145 | $2.645 \times 10^{-19}$ | $3.098 \times 10^{-11}$ | $1.532 \times 10^{-11}$ | 1.055 | $1.275 \times 10^{-23}$ |
| 194 | $7.288 \times 10^{-19}$ | $6.816 \times 10^{-11}$ | $3.561 \times 10^{-11}$ | 1.114 | $1.760 \times 10^{-23}$ |
| 236 | $6.333 \times 10^{-19}$ | $5.140 \times 10^{-11}$ | $2.727 \times 10^{-11}$ | 1.123 | $1.951 \times 10^{-23}$ |
| 302 | $4.189 \times 10^{-18}$ | $2.664 \times 10^{-10}$ | $1.451 \times 10^{-10}$ | 1.204 | $1.568 \times 10^{-23}$ |
| 365 | $5.275 \times 10^{-18}$ | $2.572 \times 10^{-10}$ | $1.505 \times 10^{-10}$ | 1.193 | $1.910 \times 10^{-23}$ |

Table 5.3: The flicker noise parameters $K, \gamma, S_{th}$ for bulk PMOS transistor (ELMOS, chip 9, W/L=60/20) during annealing after irradiations up to total dose of 365 *krad* by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$. Measured in linear range at: $V_{GS} = 3.5V, I_{DS} = 240\mu A$.

| Time [h] | $K[\frac{A^2}{Hz^{1-\gamma}}]$ | $\gamma$ | $S_{th}[\frac{A^2}{Hz}]$ |
|---|---|---|---|
| 0.5 | $5.275 \times 10^{-18}$ | 1.193 | $1.910 \times 10^{-23}$ |
| 1.72 | $1.968 \times 10^{-18}$ | 1.074 | $1.950 \times 10^{-23}$ |
| 2.82 | $3.383 \times 10^{-18}$ | 1.150 | $2.092 \times 10^{-23}$ |
| 3.93 | $1.980 \times 10^{-18}$ | 1.100 | $2.210 \times 10^{-23}$ |
| 5.08 | $2.400 \times 10^{-18}$ | 1.145 | $2.751 \times 10^{-23}$ |
| 23.93 | $1.048 \times 10^{-18}$ | 1.075 | $2.300 \times 10^{-23}$ |

Immediately after the last irradiation the five subsequent noise power spectra measurements were carried out at the same work point. The last measurement was performed one day after finishing the irradiation. The obtained results are presented in Fig. 5.8. and Tab. 5.3. They show the annealing of radiation-induced flicker noise. The noise level decreases rapidly during a 5-hour period but after 24 hours the noise level remained more than three times higher than after 85 *krad*. It means that there are two different kinds of border traps taking part in the flicker noise phenomena. The first kind decays in short time but the second kind is annealed slower. On the other hand, the component independent of frequency remains constant during the irradiation but increases during the annealing.

The nondestructive method of radiation hardness testing proposed by Scofield and Fleetwood [148, 150] is based on the assumption that both oxide component of the radiation-induced threshold voltage shift $\Delta V_{ot}$ and the flicker noise level $K_v$ are caused by the same type of traps. Therefore both phenomena can be described by a

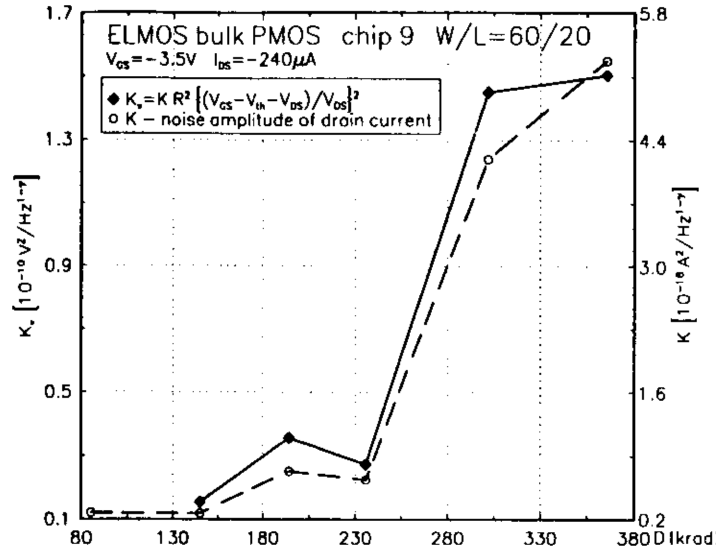


**Figure 5.7:** The noise level as the function of total $\gamma$ dose for PMOS bulk transistor. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$.

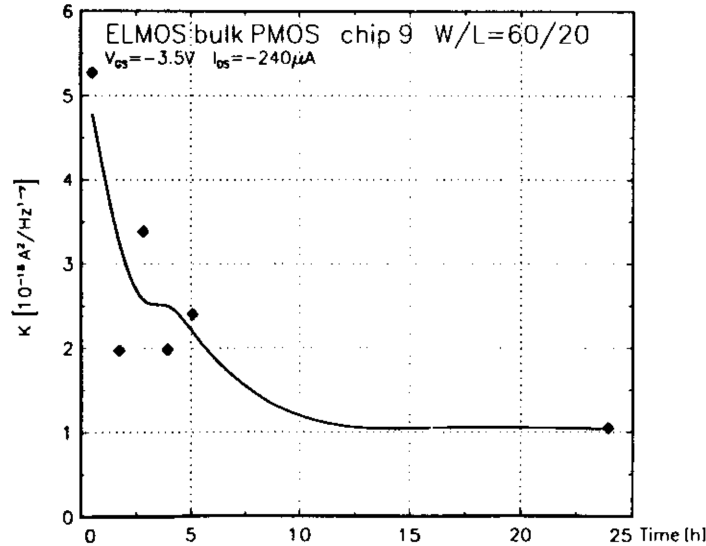


**Figure 5.8:** The noise level of bulk PMOS transistor as the function of annealing time after irradiation up to total dose of 365 *krad* by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = -5V$.



single trap density:

$$D_{ot}(E) = D_{bt}(E), \tag{5.61}$$

where $D_{ot}$ is the oxide trap density per unit energy per unit area, $D_{bt}(E)$ is defined by equation (5.35). This assumption leads to a linear relationship between preirradiation $1/f$ noise level $K_v$ and the oxide component of the radiation-induced threshold voltage shift $\Delta V_{ot}$:

$$K_v \approx \frac{qt_{ox}}{\varepsilon_0 \varepsilon_{SiO_2} W L} \frac{kT}{\lambda E_g^{ox} \ln \frac{\tau_1}{\tau_0}} |\Delta V_{ot}|, \tag{5.62}$$

where $|\Delta V_{ot}| = \frac{q\Delta N_{ot}}{C_{ox}}$, $\lambda = \frac{\Delta N_{ot}}{N_{ot}}$ is the relative increase of the total number of oxide traps increasing with radiation total dose, $N_{ot} = \int_{E_V^{ox}}^{E_C^{ox}} D_{ot}(E)dE = E_g^{ox} D_{ot}$ is the preirradiation total number of oxide traps obtained by integration along entire oxide bandgap energy $E_g^{ox} = E_C^{ox} - E_V^{ox}$. The oxide traps are assumed to be uniformly distributed in energy.

In the similar way the linear relationship between the radiation-induced increase of noise level $\Delta K_v$ and the oxide component of radiation-induced threshold voltage shift $\Delta V_{ot}$ can be expected [149]:

$$\Delta K_v \approx \frac{qt_{ox}}{\varepsilon_0 \varepsilon_{SiO_2} W L} \frac{kT}{E_{gox} \ln \frac{\tau_1}{\tau_0}} |\Delta V_{ot}|, , \tag{5.63}$$

where $|\Delta V_{ot}| = \frac{q\Delta D_{ot} E_{gox}}{C_{ox}}$. Therefore the correlations between the radiation-induced increase of the noise level $\Delta K_v$ and both the oxide and interface components of the radiation-induced threshold voltage shift $\Delta V_{ot}$, $\Delta V_{it}$ respectively were studied (see Fig. 5.9. and Fig. 5.10.).

The results from separation of two components of radiation-induced threshold voltage shift (see Fig. 4.2. and Fig. 4.3.) are plotted versus noise level $K_v$ obtained from measurements carried out during the same breaks in the irradiation (see Tab. 5.1. and Tab. 5.2.). For the NMOS transistor the value of correlation coefficient between $K_v$ and $\Delta V_{ot}$ is similar to the value of correlation coefficient between $K_v$ and $\Delta V_{it}$ and it is on the level of 0.95 (see Fig. 5.10.). A small difference between these two correlation coefficients cannot confirm hypothesis that flicker noise is caused by the same type of defects in oxide like oxide component of radiation threshold voltage shift. For the PMOS transistor the result is different. The correlation of noise level change to oxide traps component is considerably higher than to interface traps component of radiation threshold voltage shift but its value is low $r = 0.926$ (see Fig. 5.9.).

## 5.4 Kink effect in noise and its dependence on radiation

The trouble concerning undesired kink phenomenon in SOI NMOSFETs (discussed earlier in sections 2.1.5. and 4.7.) is also observed in noise dependence on drain voltage (see Fig. 5.11.). The low frequency noise overshoot at the drain current kink was observed for the first time by Chen et al. [42]. This effect indicates the usefulness of SOI device in precision analog circuits.

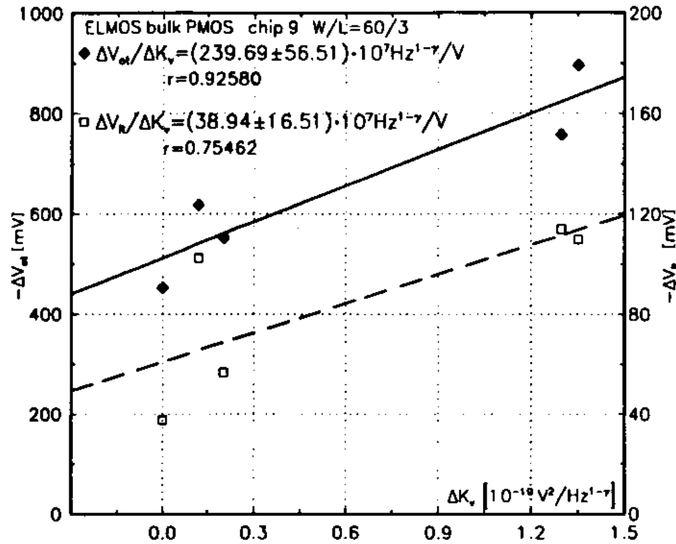


Figure 5.9: The correlation between preirradiation $1/f$ noise level $K_v$ and oxide $\Delta V_{ot}$ and $\Delta V_{it}$ traps component of radiation-induced threshold voltage shift for PMOS transistor.

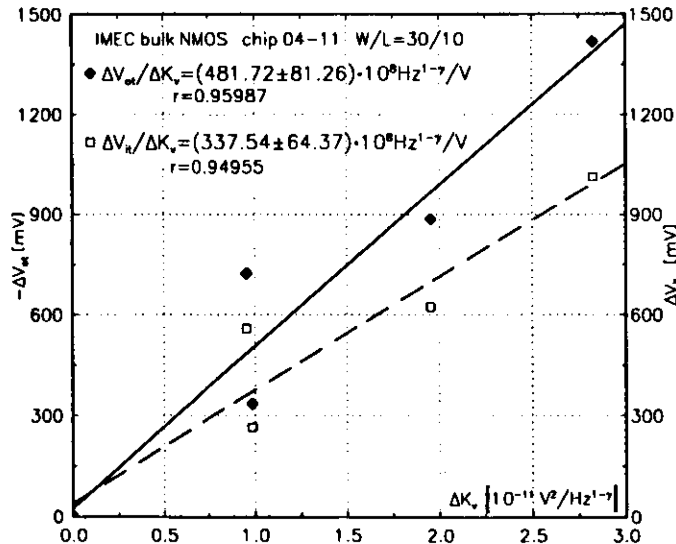


Figure 5.10: The correlation between preirradiation $1/f$ noise level $K_v$ and oxide $\Delta V_{ot}$ and $\Delta V_{it}$ traps component of radiation-induced threshold voltage shift for NMOS transistor.



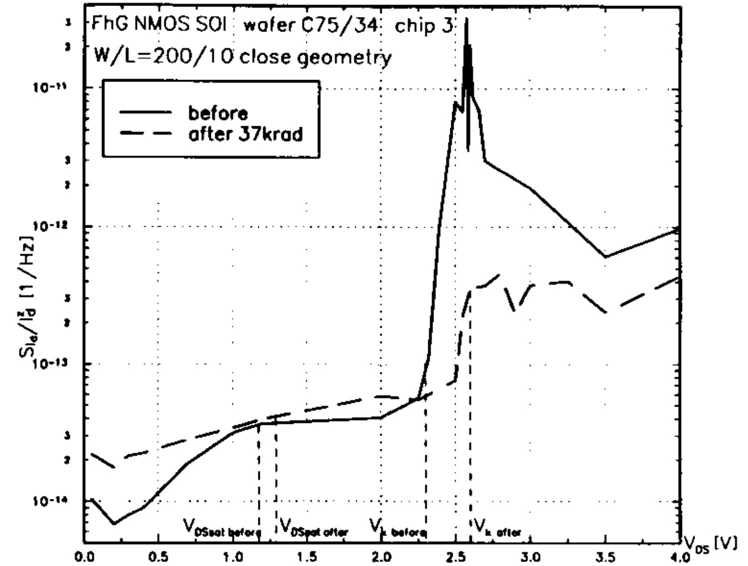


Figure 5.11: The normalized drain current noise spectrum intensity $\frac{S_{I_{DS}}}{I_{DS}^2}$ versus the drain voltage $V_{DS}$ before and after irradiation by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$. Measured at $V_{DS} = 2V, V_{BS} = 0V, f = 100Hz$.

Two presented figures 5.12 and 5.13 show the noise spectra before and after irradiation measured at the three different drain voltages: in transition region between the linear and saturation regions ($V_{DS} = 1V$), in the saturation very close to the kink point ($V_{DS} = 2.55V$), and above the kink point ($V_{DS} = 4V$). These work points can be found on the output characteristics presented in Fig. 4.27.

The occurrence of the noise overshoot (Fig. 5.12.) and noise peak (Fig. 5.11.) can be explained by the body potential fluctuations [42]. The holes generated due to the impact ionization at high electric field near the drain junction are trapped and detrapped at the bottom $Si - SiO_2$ interface. The fluctuations of the hole number causes the fluctuations of the body potential and as a consequence the drain current fluctuations. It can be described as:

$$\delta I_{DS} = \frac{\partial I_{DS}}{\partial V_{BS}} \frac{\partial V_{BS}}{\partial I_{BS}} \delta I_{BS}, \tag{5.64}$$

where $V_{BS}$ is the body to source voltage, $I_{BS}$ is the current flowing through the source-to-body junction. Therefore the drain current noise peak can be attributed to the resistance $\frac{\partial V_{BS}}{\partial I_{BS}}$ peak. It means that both the kink $\frac{\partial I_{DS}}{\partial V_{BS}}$ and noise in body

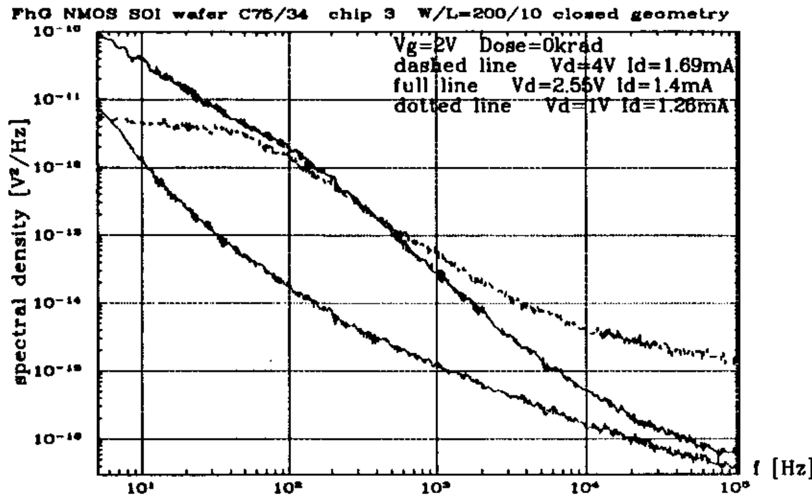


Figure 5.12: The equivalent gate voltage spectral noise power density $S_{V_{geq}}$ before irradiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$.

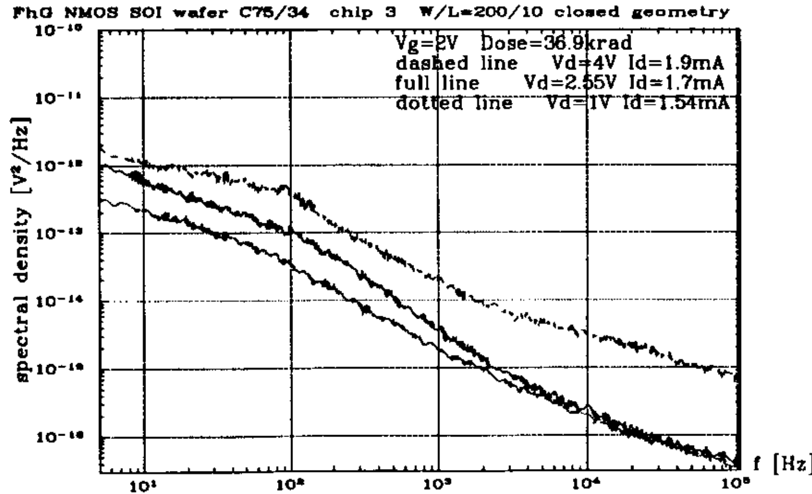


Figure 5.13: The equivalent gate voltage spectral noise power density $S_{V_{geq}}$ after irradiation by $\gamma$ radiation. Irradiation condition: $V_{DS} = V_{BS} = 0V, V_{GS} = 5V$.



potential $\frac{\partial V_{BS}}{\partial I_{BS}} \delta I_{BS}$ are required to produce the noise overshoot. Such a phenomenon is not observed for bulk transistors with floating body which exhibit the kink effect because the bottom interface does not exist.

Another unexpected phenomenon is the decrease of the noise almost in the entire frequency range. Small increase is observed only at the drain voltge $V_{DS} = 1V$ in the frequency range of $0.1 - 20$ $kHz$ (see Fig. 5.13.). The normalized noise measured at the frequency 100 $Hz$ exhibits the same radiation behaviour (see Fig. 5.11.). In the linear range, the noise increases about twice. In the saturation range belowe the kink point, the increase is small. However, at the kink point and above it the noise decreases significantly. After irradiation the bottom interface influences on the drain current noise in a lesser degree. This result is consistent with those presented in section 4.7.

# Chapter 6

# Conclusion

The conclusions presented below concern the NMOS transistors when the type of transistors is not explicitly stated. It is so because the p-channel transistors do not cause such additional problems as leakages under the field oxide and through the parasitic transistors. However, the radiation induced changes of the electrical parameters of the PMOSFETs are generally bigger due to the lack of compensation effect between the oxide and the interface charges. For example the total threshold voltage shift at 385 $krad$ for the SOI NMOS transistor is about $-560mV$ but for the SOI PMOSFET it is about $-730mV$ (irradiated with $V_{BS} = -5V$, $V_{GS} = \pm 5V$).

Among MOS VLSI technologies tested at DESY the technology provided by IMEC company exhibits the best radiation hardness. It shows relatively small leakage current below the subthreshold characteristic which is on the level of several $nA$ after the dose of 200 $krad$. The radiation-induced threshold voltage shift does not show a rapid drop at the beginning of irradiation. The technologies of the ELMOS and FhG IMS factories exhibit very large leakage current under the field oxide after a small total dose on the level of $20 - 40$ $krad$. Despite the considerable difference between the methods of forming the transistor active area for this two technologies the leakage current is on the level of several $\mu A$ or even more. It means that the charge buildup in the field oxide is so big that the transistors cannot be closed even when the big negative voltage is supplied to the gate electrode. On the other hand the radiation sensitivity of transconductance is smaller for the ELMOS and FhG IMS technologies. The IMEC transistors show the biggest transconductance reduction.

The work just presented is largely devoted to the SOI technology developed at FhG IMS. These transistors needs a negative bias of the back gate electrode for operating properly in the radiation environment. When they are irradiated with grounded back gate they are subjected to breakdown which usually occurs during the first step of irradiation. The application of split source approach with $p$-type edges of the source region enhances the sensitivity of breakdown. The breakdown resistance is improved by the LDD solution.

The radiation hardness of the SOI transistors is the best one for the LDD structures (in the range of the lower doses) even when they are irradiated with the drain terminal grounding. For structures without the LDD spacer the application of negative bias at the back gate accelerates the shift of the threshold voltage at the beginning





of irradiation. The transconductance exhibits a radiation-induced increase which is very difficult to explain. The biggest increase is observed in the case of the LDD structures. For a particular transistor the transconductance increase is bigger in the saturation than in the linear region of operation. In the linear region the maximum of the transconductance increases in the range of the low doses. When irradiation is continued its value remains on the same level. The subthreshold swing does not always increase as it would be expected. All these facts indicate that the influence of the back $Si - SiO_2$ interface is considerable. The charge buildup in the buried oxide is very big and it significantly changes the electrical condition of the transistor body and the electric field in the front channel. The threshold voltage shift of the back gate transistor is very big and the transconductance also increases.

A similar conclusion can be formulated as far as the kink effect is concerned. After irradiation the elongation of flat portion of output characteristic is observed and the drain conductance above the kink point decreases. The kink effect is not observed for the PMOSFETs because of a smaller cross-section for e-h pairs creation by the impact ionization. However, after irradiation the kink on the output characteristic appears. Both changes mentioned above occur in an opposite direction for the PMOSFETs than for the NMOSFETs.

The kink effect was also observed in the noise spectrum. The peak of the normalized drain current noise spectrum intensity occurs when the drain voltage is equal to the kink voltage. After irradiation this peak disappears. Simultaneously an unexpected decrease of the low frequency noise was observed.

The noise power spectrum of the drain current was recognized as a less sensitive to radiation than the threshold voltage. A significant effect was only observed in the case of the PMOS device for the radiation dose on the level of $200 - 300$ $krad$. Such a spectrum was measured at the fixed gate voltage and drain current. The increase of the noise level is better visible after normalization with respect to the threshold voltage shift and the drain voltage change.

To recapitulate the discussion of radiation-hardening technology it should be emphasized that the most important step in producing a radiation-hardened device is the gate oxidation. There is an optimum growth temperature for hardness, being around 1000°C for dry-oxygen-grown oxides and in the range of 850 – 925°C for steam oxides. The postoxidation anneals at high temperatures (> 925°C) tend to degrade the hardness of the gate oxide. The process temperatures after gate oxide growth should be minimized as much as possible. All these processes should be performed at 900°C or below. To minimize the buildup of radiation-induced interface traps, the amount of hydrogen should be minimized.

The comparison of these technological instructions given in many articles with process parameters used at FhG IMS leads to several conclusions. The conditions of gate oxidation (960°C, dry ambient - $O_2, H_2$) are very close to optimal parameters. They should result in a good radiation sensitivity of the gate oxide. This sensitivity is degraded by other high-temperature processes performed after the fabrication of the gate oxide. The diffusion of phosphorus dopant into the polysilicon of the gate electrode and interconnections is made at a temperature of 975°C. The P-glass reflow is performed at 960°C. These temperatures are too high and should be lowered in

order to maintain the quality of the gate oxide. However, an arbitrary change of such parameters in a well established process is very dangerous because of strong interrelations among various steps.

On the other hand the dominant problem in achieving the desired radiation hardness is the elimination of the radiation-induced leakage currents. Even if the gate oxide is of very good quality but the leakages between source and $n$-well and between source and drain through the radiation-activated FOXFET structures exist, the technology is not hardened. It means that the guardrings and gate extensions are necessary to achieve good results in the hardening. The application of these geometrical methods considerably improves the radiation tolerance of unhardened technology. This conclusion has been confirmed at DESY recently by using test structures from the ORBIT company and new generation structures from the FhG IMS [11]. The elimination of the sidewall transistor in SOI structures is more difficult and it has not been done successfully, yet.

# Appendix A

# The approximate model for the strong inversion region

The drain current of the NMOS transistor consists of two components [34]:

$$I_{DS} = -\mu_n W Q_I \nabla V(y) + \mu W V_t \nabla Q_I = \mu_n W Q_I V_t \nabla E_{F_n}. \quad (A.1)$$

where: $W$ is the width of the transistor, $\mu_n$ is the electron mobility (constant along the channel), $V_t$ is the thermal voltage, $Q_I$ is the charge in the inversion layer, $V(y)$ is the voltage drop from the source to a point $y$ along the channel in the inversion layer, $E_{F_n}$ is the electron quasi-Fermi level. The first component is drift and the second diffusion current. The drain current has, of course, the same value along whole distance from source to drain according to continuity equation, but its contributions change. In the case of a strong inversion, the current near the source is almost only of the drift nature, but in the space charge region near the drain, the diffusive component dominates. The distribution of drift to diffusive components ratio along $y$ axis (see Fig. 2.1.) depends on the drain voltage. When drain voltage increases, the transistor region, where the diffusion current dominates, lengthens. This ratio depends also on gate biasing. When the gate bias is below the threshold (weak inversion), the drain current is almost only diffusive (see app. B.). In the transition mode of operation between a weak and strong inversion (moderate inversion), both components must be taken into account to achieve good modelling for the drain current. The compact equation for the drain current can be obtained by means of using the electron quasi-Fermi level notion (see the second equal in equation (A.1)).

For strong inversion approximation, only the first term in equation (A.1) should be considered:

$$I_{DS} = -\mu_n W Q_I \frac{dV(y)}{dy}. \quad (A.2)$$

This model is presented according to the several textbooks [26, 28, 57].

The charge in the inversion layer is simply:

$$Q_I = Q_S - Q_D, \quad (A.3)$$

where:

$$Q_S = [-V_{GS} + \psi_s(y)]C_{ox} \quad (A.4)$$





is the total charge induced in the semiconductor,

$$Q_D = -\sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A \psi_s(y)} \quad (A.5)$$

is the depletion charge in the bulk (for full explanation see app. B. equations (B.9), (B.15)). In nonequilibrium, the surface potential in the inversion layer at a point $y$ may be approximated as the sum of the inversion charge potential $2\phi_B$ and the voltage drop from the source to the point $y$:

$$\psi_s(y) = 2\phi_B + V(y). \quad (A.6)$$

Substituting (A.4), (A.5, (A.6) into (A.3):

$$Q_I = -[V_{GS} - V(y) - 2\phi_B]C_{ox} + \sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A (V(y) - 2\phi_B)}. \quad (A.7)$$

Integrating (A.2) along the channel:

$$I_{DS} = -\frac{\mu_n W}{L} \int_0^{V_{DS}} Q_I dV, \quad (A.8)$$

and using (A.7), the static output equation is obtained:

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}\{[(V_{GS} - 2\phi_B - \frac{V_{DS}}{2})V_{DS}] \quad (A.9)$$

$$- \frac{2}{3}\frac{\sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A}}{C_{ox}}[(V_{DS} + 2\phi_B)^{3/2} - (2\phi_B)^{3/2}]\}. \quad (A.10)$$

For illustration the symmetry of source and drain of a MOS transistor, the equation (A.10) may be rewritten as [29, 30]:

$$I_{DS} = \frac{W}{L}[f(2\phi_B + V_{DS}) - f(2\phi_B)], \quad (A.11)$$

where $2\phi_B$ is the surface potential near source, $2\phi_B + V_{DS}$ is the surface potential near drain, and function $f$ is:

$$f(\psi_s) = \mu_n C_{ox}[V_{GS}\psi_s - \frac{1}{2}\psi_s^2 - \frac{2}{3}\gamma\psi_s^{3/2}], \quad (A.12)$$

where

$$\gamma = \frac{\sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A}}{C_{ox}} \quad (A.13)$$

is the body effect coefficient.

The model (A.10) well simulates the MOSFET characteristic in the linear region up to the saturation point $V_{DSsat}$. The most problematic complication in this equation is the presence of terms with $\frac{3}{2}$ powers. It is very useful to develop a simpler,

approximated model without this complication. It is clear that the exponent $\frac{3}{2}$ originates from square root in the equation (A.5). The approximation $-\frac{Q_D}{C_{ox}}$ by the first to terms of its Taylor's expansion around the convenient point $\psi_s = 2\phi_B$:

$$-\frac{Q_D}{C_{ox}} \approx \gamma\sqrt{2\phi_B} + \delta V(y). \tag{A.14}$$

The straight line with slope $\frac{\partial(-Q_D/C_{ox})}{\partial V}|_{V=0}$ overestimates the values predicted by the accurate model (A.5). Therefore, some value:

$$\delta < \left.\frac{\partial(-Q_D/C_{ox})}{\partial V}\right|_{V=0} \tag{A.15}$$

should be taken into account. Now, the inversion layer charge at point $y$ is:

$$Q_I = -C_{ox}[V_{GS} - 2\phi_B - \gamma\sqrt{2\phi_B} - (1+\delta)V(y)], \tag{A.16}$$

and after integration (A.8):

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{th} - \frac{1+\delta}{2}V_{DS})V_{DS}, \tag{A.17}$$

where:

$$V_{th} = 2\phi_B + \gamma\sqrt{2\phi_B} \tag{A.18}$$

is the threshold voltage neglecting the flat band voltage and the charges in the gate oxide.

The expression at the right hand side of the equation (A.17) is a quadratic function with respect to the variable $V_{DS}$ which has a maximum called the saturation point:

$$I_{DSsat} = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_{th})^2}{2(1+\delta)}, \quad \text{at} \quad V_{DSsat} = \frac{V_{GS} - V_{th}}{1+\delta}. \tag{A.19}$$

The equation (A.17) can be used only up to this point $V_{DS} \leq V_{DSsat}$. For a higher drain voltage value the drain current remains almost constant. Therefore the transistor operation in this region is described by the equation:

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS} - V_{th})^2}{2(1+\delta)}, \tag{A.20}$$

which is independent of the drain voltage.

The complete model consists of two equations (A.17), (A.20). It can be rewritten in a very compact form:

$$I_{DS} = I_{DSsat}(1 - u^2), \tag{A.21}$$

where

$$u = \begin{cases} 1 - \frac{V_{DS}}{V_{DSsat}}, & V_{DS} \leq V_{DSsat}, \quad \text{linear region}, \\ 0, & V_{DS} > V_{DSsat}, \quad \text{saturation region}, \end{cases} \tag{A.22}$$

is a parameter.

# Appendix B

# The model for the weak inversion region

Let us consider the uniform doped n-channel MOS transistor structure (according to several articles [31, 109, 114] and textbooks [26, 28, 57]. For a surface potential $\psi_s$ smaller than the inversion surface potential $2\phi_B$, the charge in the inversion layer is so small that it can be neglected. Therefore, the flowing current is of almost only diffusive nature:

$$I_{DS} = W t_{ch} q D_n \frac{dn}{dy}, \tag{B.1}$$

where: $W$ - the width of the transistor, $t_{ch}$ - the effective channel thickness, $D_n = \mu_n V_t$ - the diffusion constant of electrons, expressed by Einstein's relation, $n(y)$ - electron concentration along the channel. The change of electron concentration in $y$ direction along the channel from the source $y = 0$ to the drain $y = L$ (Fig. 2.1.), can be calculated:

$$\frac{dn}{dy} = \frac{n(0) - n(L)}{L}, \tag{B.2}$$

where:

$$n(0) = n_i \exp\frac{\psi_s - \phi_B}{V_t}, \tag{B.3}$$

$$n(L) = n_i \exp\frac{\psi_s - V_{DS} - \phi_B}{V_t}. \tag{B.4}$$

It is assumed that the source is short circuit to bulk $V_{BS} = 0$. If it were not true, $\psi_s$ should be replaced by $\psi_s - V_{SB}$.

The distance from the interface to the point at which the potential decreases by one thermal voltage $V_t$ will be called the effective channel thickness :

$$t_{ch} = \frac{V_t}{\mathcal{E}_s}. \tag{B.5}$$

The normal electric field is assumed to be constant over the distance $t_{ch}$ and the same as on the surface. The surface normal electric field $\mathcal{E}_s$ can be calculated by integration





of Poisson's equation. In the weak inversion condition, the depletion approximation neglecting the charge of electrons can be used:

$$\frac{d^2\psi}{dx^2} = \frac{qN_A}{\varepsilon_{Si}\varepsilon_0}, \tag{B.6}$$

where $x$ is vertical coordinate directed into the depth of silicon substrate (Fig. 2.1). The term on the right hand side of the equation (B.6) determines the charge density of ionized acceptor ions. Multiplying the equation (B.6) by $\frac{d\psi}{dx}$ and using the identity:

$$\frac{1}{2}\frac{d}{dx}\left(\frac{d\psi}{dx}\right)^2 = \frac{d\psi}{dx}\left(\frac{d^2\psi}{dx^2}\right), \tag{B.7}$$

the integration along $x$ variable can be avoided:

$$d\left(\frac{d\psi}{dx}\right)^2 = 2\frac{qN_A}{\varepsilon_{Si}\varepsilon_0}d\psi. \tag{B.8}$$

Integrating from the interface $x = 0$ ($\psi = \psi_s, \frac{d\psi}{dx} = \mathcal{E}_s$), to the depletion edge $x = d$ ($\psi = 0, \frac{d\psi}{dx} = 0$) the electric field at the surface $\mathcal{E}_s$ is obtained:

$$\mathcal{E}_s = -\left(\frac{d\psi}{dx}\right)_{x=0} = \sqrt{\frac{2qN_A}{\varepsilon_{Si}\varepsilon_0}\psi_s}. \tag{B.9}$$

It means:

$$t_{ch} = V_t\sqrt{\frac{\varepsilon_{Si}\varepsilon_0}{2qN_A\psi_s}}. \tag{B.10}$$

Using well known relation:

$$N_A = n_i \exp\left(\frac{\phi_B}{V_t}\right), \tag{B.11}$$

the channel thickness is:

$$t_{ch} = V_t\sqrt{\frac{\varepsilon_{Si}\varepsilon_0}{2qn_i\psi_s}}\exp\left(-\frac{\phi_B}{2V_t}\right). \tag{B.12}$$

Substituting (B.2) (B.3) (B.4) to (B.1) and using relation (B.11):

$$I_{DS} = \mu_n \frac{W}{L} V_t^2 \sqrt{\frac{qn_i\varepsilon_{Si}\varepsilon_0}{2\psi_s}} \exp\left(\frac{\psi_s - 1,5\phi_B}{V_t}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right]. \tag{B.13}$$

A simpler form of this equation can be obtained by considering the capacitance of MOS structure in the depletion approximation:

$$C_D = -\frac{dQ_D}{d\psi_s}, \tag{B.14}$$

where: $C_D$ - the capacitance of the depletion layer. The total silicon charge $Q_S$ is approximately equal to the depletion charge $Q_D$ due to very small free carrier density. Using Gauss's law:

$$Q_D \approx Q_S = -\varepsilon_{Si}\varepsilon_0\mathcal{E}_s. \tag{B.15}$$

Using equation (B.9):

$$C_D = \sqrt{\frac{qN_A\varepsilon_{Si}\varepsilon_0}{2\psi_s}} = \sqrt{\frac{qn_i\varepsilon_{Si}\varepsilon_0}{2\psi_s}}\exp(\frac{\phi_B}{2V_t}). \tag{B.16}$$

Using this result and (2.20) in equation (B.13):

$$I_{DS} = \beta\frac{C_D(\psi_s)}{C_{ox}}V_t^2\exp(\frac{\psi_s - 2\phi_B}{V_t})[1 - \exp(-\frac{V_{DS}}{V_t})]. \tag{B.17}$$

Equation (B.13) can also be written in another entirely equivalent form:

$$I_{DS} = \frac{W}{L}\mu_n q N_A V_t L_B(\frac{n_i}{N_A})^2\exp(\frac{\psi_s}{V_t})[1 - \exp(-\frac{V_{DS}}{V_t})](\frac{2\psi_s}{V_t})^{-\frac{1}{2}}, \tag{B.18}$$

where equation (B.11) has been used and new symbol $L_B = \sqrt{\frac{\varepsilon_{Si}\varepsilon_0 V_t}{qN_A}}$, which is called the extrinsic Debeye length, has been introduced. The physical meaning of this parameter is the thickness of the surface semiconductor layer where the space charge and the electric field exist and the bands are bent when the semiconductor is located in the external electric field. The derivation of equation (B.18) has been based on the charge sheet model developed by Brews [110, 111].

It remains a problem how to determine a relation between the surface potential $\psi_s$ and gate voltage $V_{GS}$ (see equation (4.9) with $V_{SB} = 0$):

$$V_{GS} = \psi_s + \frac{Q_D + Q_{it}}{C_{ox}} + \frac{Q_m + Q_{ot} + Q_f}{C_{ox}} + \Phi_{GB}. \tag{B.19}$$

The solution of this equation is not explicit because the charges $Q_{it}$, $Q_D$ depend on the surface potential $\psi_s$. The method proposed by [112] is to do a Taylor's series expansion around the central voltage point of the weak inversion i. e. $\psi_s = 1.5\phi_B$ (see Fig. 2.4):

$$V_{GS} = V_{GS}(1.5\phi_B) + \left(\frac{\partial V_{GS}}{\partial\psi_s}\right)_{1.5\phi_B}(\psi_s - 1.5\phi_B), \tag{B.20}$$

where:

$$\left(\frac{\partial V_{GS}}{\partial\psi_s}\right)_{1.5\phi_B} = n = \left(1 + \frac{C_D(\psi_s) + C_{it}(\psi_s)}{C_{ox}}\right)_{1.5\phi_B}, \tag{B.21}$$

where $n$ is the inverse subthreshold slope, $C_{it} = qD_{it}$ is the interface state capacitance. Substituting $\psi_s = 2\phi_B$ in (B.20), the threshold voltage is calculated:

$$\frac{1}{n}V_{th} = \frac{1}{n}V_{GS}(1.5\phi_B) + 0.5\phi_B. \tag{B.22}$$

Recalculating (B.20):

$$(\psi_s - 2\phi_B) = \frac{1}{n}(V_{GS} - V_{GS}(1.5\phi_B)) - 0.5\phi_B = \frac{1}{n}(V_{GS} - V_{th}), \tag{B.23}$$



and substituting (B.23) to (B.17):

$$I_{DS} = \beta(n-1)V_t^2\exp(\frac{V_{GS} - V_{th}}{nV_t})[1 - \exp(-\frac{V_{DS}}{V_t})], \tag{B.24}$$

where the equation (B.21) with the assumption that $C_{it} \ll C_D$ is used in the following manner:

$$C_D(1.5\phi_B) = (n-1)C_{ox}. \tag{B.25}$$

Slightly another derivation of the analytical expression for the subthreshold characteristic is presented by van Overstraeten [112]. It leads to:

$$I_{DS} = \beta C_D(\psi_s)\frac{n}{m}V_t^2\exp(\frac{V_{GS} - V_{GS}^*}{nV_t})[1 - \exp(\frac{-V_{DS}}{V_t}\frac{m}{n})], \tag{B.26}$$

where

$$m = \frac{C_{ox} + C_D(\frac{3}{2}\phi_B)}{C_{ox}}, \tag{B.27}$$

$V_{GS}^*$ is the gate voltage at $\psi_s = \frac{3}{2}\phi_B$. The depletion capacitance $C_D$ is calculated by means of a slightly different equation than (B.16) discussed above:

$$C_D(\psi_s) = \sqrt{\frac{qN_A\varepsilon_{Si}\varepsilon_0}{2(\psi_s + V_t)}}. \tag{B.28}$$

The most important parameter describing device quality in the weak inversion region is the subthreshold swing $S$ defined by the equation (2.27):

$$S = \ln 10\left[\frac{\partial \ln I_{DS}}{\partial V_{GS}}\right]^{-1} = \ln 10\left[\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial\psi_s}\frac{\partial\psi_s}{\partial V_{GS}}\right]^{-1}, \tag{B.29}$$

where:

$$\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial\psi_s} = \frac{1}{V_t} - \frac{1}{2\psi_s} \tag{B.30}$$

(using equations (B.17), (B.16)),

$$\frac{\partial\psi_s}{\partial V_{GS}} = \frac{C_{ox}}{C_{ox} + C_D + C_{it}} \tag{B.31}$$

(using equation (B.21)).
As a result [114]:

$$S = \ln 10\left(\frac{1}{V_t} - \frac{1}{2\psi_s}\right)^{-1}\frac{C_{ox} + C_D + C_{it}}{C_{ox}}. \tag{B.32}$$

The second term in the parentheses is negligible because the surface potential $\psi_s$ at the center of weak inversion is:

$$\psi_s = \frac{3}{2}V_t\ln\frac{N_A}{n_i} = 0.525V, \tag{B.33}$$

(for $N_A = 2\times10^{16}cm^{-3}$) but thermal voltage at room temperature is:

$$V_t = 0.025V. \tag{B.34}$$

# Appendix C

# The Langevin method of $S_x(f)$ evaluation

The physical system which produces the noise can be described by a differential equation. The white random-source function $h(t)$ will be taken as a noise extortion. If the noise response at the output of system is signed $x(t)$, the result is [139]:

$$L^m(p)x(t) = h(t), \tag{C.1}$$

where $L^m(p)$ is the polynomial of m-degree, p is the differential operator with respect to the time. Making a Fourier expansion for $0 \leq t \leq T$ by putting [135]:

$$h(t) = \sum_{n=-\infty}^{+\infty} b_n exp(j\omega_n t), \tag{C.2}$$

$$x(t) = \sum_{n=-\infty}^{+\infty} a_n exp(j\omega_n t), \tag{C.3}$$

where factors $a_n$ and $b_n$ are the amplitudes of $n$-th term of Fourier's series (2.33), one obtains:

$$a_n = \frac{b_n}{L(j\omega_n)}. \tag{C.4}$$

Because the following relation is satisfied (2.34):

$$2\overline{a_n a_n^*} = S_x(f)\Delta f, \tag{C.5}$$

where $\Delta f = \frac{1}{T}$, the power spectral density of signal $x(t)$ is:

$$S_x(f) = \frac{S_h(f)}{L(j\omega)^2}. \tag{C.6}$$

For example, if the differential equation of system is:

$$(\frac{1}{\tau} + \frac{d}{dt})x(t) = h(t), \tag{C.7}$$





then:

$$L^1(p) = \frac{1}{\tau} + p, \tag{C.8}$$

and:

$$(\frac{1}{\tau} + j\omega_n)a_n = b_n. \tag{C.9}$$

The power spectral density of $x(t)$ is:

$$S_x(f) = \frac{\tau^2}{1 + \omega^2\tau^2} S_h(f). \tag{C.10}$$

# Bibliography


[1] L. Hervas *"The Pipelined Readout for the ZEUS Calorimeter"* DESY, Hamburg 1991, DESY F35D-91-01

[2] J. Moeschen at al. *"High-Speed Analog CMOS Pipeline System"* Nucl. Instr. & Meth., vol. A(288), pp. 180-186 (1990)

[3] P.E. Allen, E. Sanchez-Sinencio *"Switched Capacitor Circuits"* Van Nostrand Reinhold, New York 1984

[4] ZEUS Collaboration *"The ZEUS Detector. Status Report 1989."* DESY, Hamburg 1989

[5] P. Malecki *"Wpływ promieniowania jonizującego na tranzystory CMOS"* Raport INT 225/E, Kraków 1989

[6] C. Coldewey *"Untersuchungen von Strahlenshaeden an Feldeffekttransistoren und an CMOS-Speicherbausteinen"* Interner Bericht DESY F35-91-02, Hamburg 1991

[7] S. Boettcher *"Untersuchungen analoger CMOS-Pufferspeicher mit einem rechnergesteuerten Messplatz"* DESY, Hamburg 1991

[8] D. Zer-Zion, A. Seidman, U. Koetz *"Degradation of CMOS-Integrated Electronics under Ionizing Irradiation"* Hamburg 1990

[9] S. Boettcher, C. Coldewey, U. Koetz, A. Skoczeń *"Radiation Induced Degradation of ZEUS CMOS - Analog Buffer/Multiplexer Chip"* Sixth European Symposium on Semiconductor Detectors, 24-26 February 1992, Milan

[10] A. Skoczeń *"Work at DESY and IMS(FhG) Duisburg on Radhard Circuits"* Microelectronic User Group meeting - Radhard Electronics, CERN, 28 January 1992, Geneva

[11] S. Boettcher, C. Coldewey *private communication*

[12] P. Jarron *"HSOI3HD of Thomson TMS. A preliminary status report."* Microelectronic User Group meeting - Radhard Electronics, CERN, 28 January 1992, Geneva

[13] G.C. Messenger, M.S. Ash *"The Effects of Radiation on Electronic Systems"* Van Nostrand Reinhold Company, 1986

[14] S. Rigo *"Silica Films on Silicon"* in: ed. G. Barbotin, A. Vapaille *"Instabilities in Silicon Devices"* Elsevier Science Publishers, 1986







[15] F.B. McLean, H.E. Boesch, Jr., and T.R. Oldham *"Electron-Hole Generation, Transport, and Trapping in $SiO_2$"* in: ed. T.P. Ma, P.V. Dressendorfer *"Ionizing Radiation Effects in MOS Devices and Circuits"* John Wiley & Sons, 1989

[16] V.A.J. van Lint, T.M. Flanagen, R.E. Leadon, J.A. Naber, V.C. Roger *"Mechanism of Radiation Effects in Electronic Materials"* John Wiley & Sons, 1980

[17] B.E. Deal *"Standardized Terminology for Oxide Charge Associated with Thermally Oxidized Silicon"* IEEE Trans. Electron Devices, vol. ED-27, pp. 606-608 (1980)

[18] D.M. Fleetwood *"'Border Traps' in MOS Devices"* IEEE Trans. Nucl. Sci., vol. NS-39, pp. 269-271 (1992)

[19] Z. Shanfield, G.A. Brown, A.G. Revesz, H.L. Hughes *"A New MOS Radiation-Induced Charge: Negative Fixed Interface Charge"* IEEE Trans. Nucl. Sci., vol. NS-39, pp. 303-307 (1992)

[20] Y.C. Cheng *"Electronic States at the Silicon-Silicon Dioxide Interface"* Prog. Surface Sci., vol. 8, pp. 181-218 (1977)

[21] C. T. Sah *"Models and Experiments on Degradation of Oxidized Silicon"* Solid-St. Electron., vol. 33, pp. 147-167 (1990)

[22] P.M. Lenahan, P.V. Dressendorfer *"Hole Traps and Trivalent Silicon Centers in Metal/Oxide/Silicon Devices"* J. Appl. Phys., vol. 55, pp. 3495-3499 (1984)

[23] S.M. Sze *"Physics of Semiconductor Devices."* John Wiley & Sons, 1981

[24] J.R. Schwank, P.S. Winokur, P.J. McWhorter, F.W. Sexton, P.V. Dressendorfer, D.C. Turpin *"Physical Mechanisms Contributing to Device 'Rebound'"* IEEE Trans. Nucl. Sci., vol. NS-31, pp. 1434-1438 (1984)

[25] P.S. Winokur *"Radiation-Induced Interface Traps"* in: ed. T.P. Ma, P.V. Dressendorfer *"Ionizing Radiation Effects in MOS Devices and Circuits"* John Wiley & Sons, 1989

[26] Y. P. Tsividis *"Operation and Modeling of the MOS Transistor"* McGraw-Hill, 1987

[27] Y. P. Tsividis *"Moderate Inversion in MOS Devices"* Solid-St. Electron., vol. 25, pp. 1099-1104 (1982)

[28] D. K. Ferry, L.A. Akers, E.W. Greeneich *"Ultra Large Scale Integrated Microelectronics"* Prentice Hall, 1988

[29] J.E. Meyer *"MOS Models and Circuit Simulation"* RCA Review vol. 32, pp. 42-63 (March 1971)

[30] F.M. Klaassen *"A MOS Model for Computer-Aided Design"* Philips Res. Repts, vol. 31, pp. 71-83 (1976)

[31] T. Grotjohn, B. Hoefflinger *"A Parametric Short-Channel MOS Transistor Model for Subthreshold and Strong Inversion Current"* IEEE Trans. Electron Devices, vol. ED-31, pp. 234-246 (1984)

[32] G. Doucet, F. van de Wiele *"Threshold Voltage of Nonuniformly Doped MOS Structures"* Solid-St. Electron., vol. 16, pp. 417-423 (1973)

[33] H. Feltl *"Onset of Heavy Inversion in MOS Devices Doped Nonuniformly near the Surface"* IEEE Trans. Electron Devices, vol. ED-24, pp. 288-289 (1977)

[34] H. C. Pao, C. T. Sah *"Effects of Diffusion Current on Characteristics of Metal-Oxide (Insulator)-Semiconductor Transistors"* Solid-St. Electron., vol. 9, pp. 927-937 (1966)

[35] M. H. White, F. van de Wiele, J-P. Lambot *"High-Accuracy MOS Models for Computer-Aided Design"* IEEE Trans. Electron Devices, vol. ED-27, pp. 899-906 (1980)

[36] M-S. Lin *"The Classical Versus the Quantum Mechanical Model of Mobility Degradation Due to the Gate Field in MOSFET Inversion Layers"* IEEE Trans. Electron Devices, vol. ED-32, pp. 700-710 (1985)

[37] T. J. Krutsick, M. H. White, H-S. Wong, R. V. H. Booth *"An Improved Method of MOSFET Modeling and Parameter Extraction"* IEEE Trans. Electron Devices, vol. ED-34, pp. 1676-1679 (1987)

[38] H-S. Wong, M. H. White, T. J. Krutsick, R. V. H. Booth *"Modeling of Transconductance Degradation and Extraction of Threshold Voltage in Thin Oxide MOSFET's"* Solid-St. Electron., vol.30, pp. 953-968 (1987)

[39] B. El-Kareh, W. R. Tonti, S. L. Titcomb *"A Submicron MOSFET Parameter Extraction Technique"* IBM J. Res. Develop., vol.34, no.2/3, pp. 243-249 (1990)

[40] J. Tihanyi, H. Schloetterer *"Influence of the Floating Substrate Potential on the Characteristic of ESFI MOS Transistor"* Solid-St. Electron., vol. 18, pp. 309-314 (1975)

[41] J. Tihanyi, H. Schloetterer *"Properties of ESFI MOS Transistor Due to the Floating Substrate and the Finite Volume"* IEEE Trans. Electron Devices, vol. ED-22, pp. 1017-1023 (1975)

[42] J. Chen, P. Fang, P.K. Ko, C. Hu, R. Solomon, T-Y. Chan, C.G. Sodini *"Noise Overshoot at Drain Current Kink in SOI MOSFET"* IEEE SOS/SOI Technology Conference, Key West, Florida, USA (1990)

[43] N.D. Arora, M.S. Sharma *"MOSFET Substrate Current Model for Circuit Simulation"* IEEE Trans. Electron Devices, vol. ED-38, pp. 1392-1398 (1991)

[44] R. van Overstraeten, H. de Man *"Measurement of the Ionization Rates in Diffused Silicon p-n Junction"* Solid-St. Electron., vol. 13, pp. 583-608 (1970)

[45] W. Maes, K. de Meyer, R. van Overstraeten *"Impact Ionization in Silicon: a Review and Update"* Solid-St. Electron., vol. 33, pp. 705-718 (1990)

[46] S. Selberherr *"Analysis and Simulation of Semiconductor Devices"* Springer-Verlag, 1984

[47] A.G. Chynoweth *"Ionization Rates for Electron and Holes in Silicon"* Phys. Rev., vol. 109, pp. 1537-1540 (1958)



[48] S. Veeraraghavan, J.S. Fossum *"A Physical Short-Channel Model for the Thin-Film SOI MOSFET Applicable to Device and Circuit CAD"* IEEE Trans. Electron Devices, vol. ED-35, pp. 1866-1875 (1988)

[49] J.P. Colinge *"Reduction of Floating Substrate Effects in Thin-Film SOI MOSFETs"* Electronics Lett., vol. 22, pp. 187-188 (1986)

[50] J.P. Colinge *"Some Properties of Thin-Film SOI MOSFETs"* IEEE Cir. & Dev. M., vol. 3, pp. 16-20 (1987)

[51] Y. Omura, K. Izumi *"Simplified Analysis of Body-Contact Effects for SOI MOSFET/SOI"* IEEE Trans. Electron Devices, vol. ED-35, pp. 1391-1393 (1988)

[52] J-Y. Choi, J.G. Fossum *"Analysis and Control of Floating-Body Bipolar Effects in Fully Depleted Submicrometer SOI MOSFET's"* IEEE Trans. Electron Devices, vol. ED-38, pp. 1384-1391 (1991)

[53] M. Gao, J-P. Colinge, L. Lauwers, S. Wu, C. Claeys *"Twin-MOSFET Structure for Suppression of Kink and Parasitic Bipolar Effects in SOI MOSFETs at Room and Liquid Helium Temperatures"* Solid-St. Electron., vol. 35, pp. 505-512 (1992)

[54] D. Kahng *"A Historical Perspective on the Development of MOS Transistor and Related Devices"* IEEE Trans. Electron Devices, vol. ED-23, pp. 655-660 (1976)

[55] J.S. Kilby *"The Invention of the Integrated Circuit"* IEEE Trans. Electron Devices, vol. ED-23, pp. 648-654 (1976)

[56] L.C. Parrillo *"VLSI Process Integration"* in ed. S.M. Sze *"VLSI Technology"* McGraw-Hill Book Company, 1983

[57] S.M. Sze *"Semiconductor Devices. Physics and Technology."* John Wiley & Sons, 1985

[58] D.M. Brown, M. Ghezzo, J.M. Pimbley *"Trends in Advanced Process Technology - Submicrometer CMOS Device Design and Process Requirements"* Proc. of IEEE, vol. 74, pp. 1678-1702 (1986)

[59] A.C. Adams *"Dielectric and Polysilicon Deposition"* in ed. S.M. Sze *"VLSI Technology"* McGraw-Hill Book Company, 1983

[60] W. Marciniak *"Przyrządy półprzewodnikowe MOS"* Wydawnictwa Naukowo-Techniczne Warszawa, 1991

[61] S. Ogura, P.J. Tsang, W.W. Walker, D.J. Critchlow, J.F.Shepard *"Design and Characteristics of the Lightly Doped Drain-source (LDD) Insulated Gate Field Effect Transistor"* IEEE Trans. Electron Devices, vol. ED-27, pp. 1359-1367 (1980)

[62] R.R. Troutman *"Latchup in CMOS Technology"* IEEE Cir. & Dev. M., vol. 3, pp. 15-21 (1987)

[63] P. Winokur, D. Fleetwood, M. Shaneyfelt, F. Sexton, J. Shwank *"Practical Aspects of Total-Dose Effects and Quality Assurance"* Microelectronic User Group meeting-Radhard Electronics, CERN, 2 June 1992, Geneva

[64] P.S. Winokur, at al. *"Total-Dose Radiation and Annealing Studies: Implications for Hardness Assurance Testing"* IEEE Trans. Nucl. Sci., vol. NS-33, pp. 1343-1350 (1986)

[65] P.V. Dressendorfer *"Radiation-Hardening Technology"* in ed. T.P. Ma, P.V. Dressendorfer *"Ionizing Radiation Effects in MOS Devices and Circuits"* John Wiley & Sons, 1989

[66] W.R. Dawes *"Overview of Radiation Hardening for Semiconductor Detectors"* SAND89-0002C

[67] L. Adams, A. Holmes-Siedle *"Radiation Hardness Assurance of Space Electronics"* Nucl. Instr. & Meth., vol. A314, pp. 335-344 (1992)

[68] C.R. Viswanathan, J. Maserjian *"Model for Thickness Dependence of Radiation Charging in MOS Structures"* IEEE Trans. Nucl. Sci., vol. NS-23, pp. 1540-1545 (1976)

[69] W.R. Dawes, G.F. Derbenwick, B.L. Gregory *"Process Technology for Radiation-Hardened CMOS Integrated Circuits"* IEEE J. of Solid State Cir., vol. SC-11, pp. 459-465 (1976)

[70] E.P. EerNisse, G.F. Derbenwick *"Viscous Shear Flow Model for MOS Radiation Sensitivity "* IEEE Trans. Nucl. Sci., vol. NS-23, pp. 1534-1539 (1976)

[71] E.P. EerNisse *"Viscous Flow of Thermal $SiO_2$"* Appl. Phys. Lett., vol. 30, pp. 290-293 (1977)

[72] F. Eronides, da Silva, Y. Nishioka, T.-P. Ma *"Effects of Trichloroethane During Oxide Growth on Radiation-Induced Interface Traps in Metal/$SiO_2$/Si capacitor"* Appl. Phys. Lett., vol. 51, pp. 1262-1264 (1987)

[73] Y. Wang, Y. Nishioka, T.-P. Ma, C. Barker *"Radiation and Hot-Electron Effects on $SiO_2$/Si Interfaces with Oxide Grown in $O_2$ Containing Small Amounts of Trichloroethane"* Appl. Phys. Lett., vol. 52, pp. 573-575 (1988)

[74] F.N. Coppage, D.J. Allen, P.V. Dressendorfer, A. Ochoa, J. Rauchfuss, T.F. Wrobel *"Seeing Through Latch-up Window"* IEEE Trans. Nucl. Sci., vol. NS-30, pp. 4122-4126 (1983)

[75] G.E. Davis, L.R. Hite, T.G.W. Blake, C.-E. Chen, H.W. Lam, R. DeMoyer *"Transient Radiation Effects in SOI Memories"* IEEE Trans. Nucl. Sci., vol. NS-32, pp. 4432-4437 (1985)

[76] B.-Y. Mao, C.-E. Chen, M. Matloubian, L.R. Hite, G. Pollack, H.L. Hughes, K. Maley *"Total Dose Characterizations of CMOS Devices in Oxygen Implanted Silicon-on-Insulator Structures"* IEEE Trans. Nucl. Sci., vol. NS-33, pp. 1692-1697 (1987)

[77] B.-Y. Mao, C.-E. Chen, G. Pollack, H.L. Hughes, G.E. Davis *"Total Dose Hardening of Buried Insulator in Implanted Silicon-on-Insulator Structures"* IEEE Trans. Nucl. Sci., vol. NS-34, pp. 1692-1697 (1987)



[78] T. Ohno, K. Izumi, M. Shimaya, N.Shiono *"Radiation Hardened n-channel MOSFET Achieved by a Combination of Polysilicon Sidewall and SIMOX Technology"* Electronics Lett., vol. 22, pp. 559-600 (1986)

[79] T. Ohno, K. Izumi, M. Shimaya, N.Shiono *"CMOS/SIMOX Devices Having a Radiation Hardness of 2 Mrad(Si)"* Electronics Lett., vol. 23, pp. 141-143 (1987)

[80] T. Ohno, K. Izumi, M. Shimaya, N.Shiono *"Total-Dose Effects of Gamma-Ray Irradiation on CMOS/SIMOX Devices"* IEEE Cir. & Dev. M., vol. 3, pp. 21-25 (1987)

[81] S.S. Tsao, D.M. Fleetwood, H.T. Weaver, L. Pfeiffer, G.K. Celler *"Radiation-Tolerant, Sidewall-Hardened SOI/MOS Transistors"* IEEE Trans. Nucl. Sci., vol. NS-34, pp. 1686-1690 (1987)

[82] A.C. Ipri *"The Properties of Silicon-on-Sapphire Substrates, Devices, and Integrated Circuits"* Applied Solid State Science, Suppl. 2-Part A, ed. by D. Kahng, Academic Press, New York (1981)

[83] P. Jarron *"SOI process of Thomson TMS studied at CERN."* Microelectronic User Group meeting-Radhard Electronics, CERN, 9 October 1991, Geneva

[84] T.R. Oldham, J.M. McGarrity *"Comparison of $Co^{60}$ Responce and 10 keV X-Ray Responce in MOS Capacitor"* IEEE Trans. Nucl. Sci., vol. NS-30, pp. 4377-4381 (1983)

[85] G.J. Gerardi, E.H. Poindexter, P.J. Caplan, N.M. Johnson *"Interface Traps and $P_b$ Centers in Oxidized $< 100 >$ Silicon Wafer"* Appl. Phys. Lett., vol. 49(6), pp. 348-350 (1986)

[86] Y.Y. Kim, P.M. Lenahan *"Electron-Spin-Resonance Study of Radiation-Induced Paramagnetic Defects in Oxides Grown on (100) Silicon Substrates"* J. Appl. Phys., vol. 64(7), pp. 3551-3557 (1988)

[87] T.R. Oldham, F.B. McLean, H.E. Boesch, Jr. and J.M. McGarrity *"An Overview of Radiation-Induced Interface Traps in MOS Structures"* Semicond. Sci. Technol., vol. 4, pp. 986-999 (1989)

[88] F.B. McLean *"A Framework for Understanding Radiation-Induced Interface States in $SiO_2$ MOS Structures"* IEEE Trans. Nucl. Sci., vol. NS-27, pp. 1651-1657 (1983)

[89] G.W. Hughes *"Interface-States Effects in Irradiated MOS Structures"* J. Appl. Phys., vol. 48(12), pp. 5357-5359 (1978)

[90] C.T. Sah, T.H. Ning, L.L. Tschopp *"The Scattering of Electrons by Surface Oxide Charges and by Lattice Vibrations at the Silicon-Silicon Dioxide Interface"* Surface Sci., vol. 32, pp. 561-575 (1972)

[91] S.C. Sun, J.D. Plummer *"Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces"* IEEE Trans. Electron Devices, vol. ED-27, pp. 1497-1980 (1976)

[92] K.F. Galloway, M. Gaitan, T.J. Russell *"A Simple Model for Separating Interface and Oxide Charge Effects in MOS Device Characteristic"* IEEE Trans. Nucl. Sci., vol. NS-31, pp. 1497-1501 (1984)

[93] P.J. McWhorter, P.S. Winokur *"Simple Technique for Separating the Effects of Interface Traps and Trapped-Oxide Charge in Metal-Oxide-Semiconductor Transistors"* Appl. Phys. Lett., vol. 48(2), pp. 133-135 (1986)

[94] P.S. Winokur, J.R. Schwank, P.J. McWhorter, P.V. Dressendorfer, D.C. Turpin *"Correlating the Radiation Response of MOS Capacitors and Transistors"* IEEE Trans. Nucl. Sci., vol. NS-31, pp. 1453-1460 (1984)

[95] D.M. Fleetwood, M.R. Shaneyfelt, J.R. Schwank, P.S. Winokur, F.W. Sexton *"Theory and Application of Dual-Transistor Charge Separation Analysis"* IEEE Trans. Nucl. Sci., vol. NS-36, pp. 1816-1824 (1989)

[96] K.F. Galloway, C.L. Wilson, L.C. Witte *"Charge-Sheet Model Fitting to Extract Radiation-Induced Oxide and Interface Charge"* IEEE Trans. Nucl. Sci., vol. NS-32, pp. 4461-4465 (1985)

[97] C-T. Sah, W.W-L. Lin, S.C-S. Pan, C.C-H. Hsu *"New Method for Separating and Characterizing Interface States and Oxide Traps on Oxidized Silicon"* Appl. Phys. Lett., vol. 48(12), pp. 782-784 (1986)

[98] S.C. Witczak, J.S. Suehle, M. Gaitan *"An Experimental Comparison of Measurement Techniques to Extract $Si - SiO_2$ Interface Trap Density"* Solid-St. Electron., vol. 35, pp. 345-355 (1992)

[99] Z. Shanfield, M.M. Moriwaki *"Critical Evaluation of the Midgap-Voltage-Shift Method for Determining Oxide Trapped Charge in Irradiated MOS Devices"* IEEE Trans. Nucl. Sci., vol. NS-34, pp. 1159-1165 (1987)

[100] K. Ziegler *"Distinction Between Donor and Acceptor Character of Surface States in the $Si - SiO_2$ Interface"* Appl. Phys. Lett., vol. 32(4), pp. 249-251 (1978)

[101] P.J. McWhorter, P.S. Winokur, R.A. Pastorek *"Donor/Acceptor Nature of Radiation-Induced Interface Traps"* IEEE Trans. Nucl. Sci., vol. NS-35, pp. 1154-1159 (1988)

[102] W. Dąbrowski, M. Kajetanowicz, D. Kidwell, W.A. Rowe, H.F.-W. Sadrozinski, E.N. Spencer, P. Tenenbaum, M. Turala, M. Wilder, H. Spieler *"Noise Measurements on Radiation-Hardened CMOS Transistors"* IEEE Nucl. Sci. Symp., vol. 3, pp. 1536-1540 (1991)

[103] F. Anghinolfi, P. Aspell, M. Campbell, F. Faccio, M. Glaser, E.H.M. Heijne, P. Jarron, F. Lemeilleur, G. Meddeler, G. Rossi, H. Verweij *"A Demonstrator Analog Signal Processing Circuit in a Radiation Hard SOI-CMOS Technology"* CERN/DRDC 92-15, RD9 Status Report, 10 March 1992

[104] G. Borel, F. Faccio, E.H.M. Heijne, P. Jarron, M. Glaser *"Study of Device Parameters for Analog IC Design in a 1.2$\mu m$ CMOS-SOI Technology after* 10 $Mrad$*"* Appendix to CERN/DRDC 92-15, RD9 Status Report, 10 March 1992



[105] B-J. Moon, C-K. Park, K. Lee, M. Shur *"New Short-Channel n-MOSFET Current-Voltage Model in Strong Inversion and Unified Parameter Extraction Method"* IEEE Trans. Electron Devices, vol. ED-38, pp. 592-602 (1991)

[106] P. Dars, G. Merckel, O. Coumar, R. Gaillard, H. Belhaddad *"Radiation Induced Kink Effects on SOI PMOS Transistors"* IEEE SOS/SOI Technology Conference, Key West, Florida, USA (1990)

[107] M. Berger, H. Vogt *"Set of SPICE-Parameters for 3$\mu m$-CMOS-Process"* FhG IMS, Duisburg (December 1990)

[108] M.J. Deen, Z.X. Yan *"A New Method for Measuring the Threshold Voltage of Small-Geometry MOSFETs from Subthreshold Conduction"* Solid-St. Electron., vol. 33, pp. 503-511 (1990)

[109] W. Fichtner, H.W. Poetzl *"MOS Modelling by Analytical Approximation. I. Subthreshold Current and Threshold Voltage"* Int. J. Electronics, vol. 46, pp. 33-55 (1979)

[110] J.R. Brews *"Charge Sheet Model"* Solid-St. Electron., vol. 21, pp. 345- (1978)

[111] J.R. Brews *"Physics of the MOS Transistor"* Applied Solid State Science, Suppl. 2-Part A, ed. by D. Kahng, Academic Press, New York (1981)

[112] R.J. van Overstraeten, G.J. Declerck, P.A. Muls *"Theory of the MOS Transistor in Weak Inversion - New Method to Determine the Number of Surface States"* IEEE Trans. Electron Devices, vol. ED-22, pp. 282-288 (1975)

[113] R.J. van Overstraeten, G.J. Declerck, G.L. Broux *"The Influence of Surface Potential Fluctuations on the Operation of the MOS Transistor in Weak Inversion"* IEEE Trans. Electron Devices, vol. ED-20, pp. 1154-1158 (1973)

[114] D. J. Wouters, J-P. Colinge, H. E. Meas *"Subthreshold Slope in Thin-Film SOI MOSFET's"* IEEE Trans. Electron Devices, vol. ED-37, pp. 2022-2033 (1990)

[115] M. Watanabe, A. Tooi *"Formation of $SiO_2$ Films by Oxygen-Ion Bombardment"* Japan. J. Appl. Phys., vol. 5, pp. 737-738 (1966)

[116] K. Izumi, M. Doken, H. Ariyoshi *"CMOS Devices Fabricated on Buried $SiO_2$ Layers Formed by Oxygen Implantation into Silicon"* Electron. Lett., vol. 14, pp. 593-594 (1978)

[117] J. Belz, G. Burbach, H. Vogt, J. Peter-Weidemann, G. Zimmer *"High Quality Silicon-On-Insulator Substrates by Implanted Oxygen Ions"* Mater. Sc. and Eng., vol. B4, pp. 429-433 (1989)

[118] J. Belz, G. Burbach, H. Vogt, G. Zimmer *"High-Quality SOI-Substrates for CMOS transistors"* Vacuum, vol. 42, pp. 387-388 (1991)

[119] G. Burbach, *private communication*

[120] D. Hill, P. Fraundorf, G. Fraundorf *"The Reduction of Dislocations in Oxygen Implanted Silicon-On-Insulator Layers by Sequential Implantation and Annealing"* J. Appl. Phys., vol. 63(10), pp. 4933-4936 (1988)

[121] T. Aoki, M. Tomizawa, A. Yoshi *"Design Consideration for Thin-Film SOI/CMOS Device Structures"* IEEE Trans. Electron Devices, vol. ED-36, pp. 1725-1731 (1989)

[122] M. Matloubian, C-E.D. Chen, B-Y. Mao, R.Sundaresan, G.P. Pollack *"Modeling of the Subthreshold Characteristic of SOI MOSFET's with Floating Body"* IEEE Trans. Electron Devices, vol. ED-37, pp. 1985-1993 (1990)

[123] D.C. Mayer *"Models of Operation and Radiation Sensitivity of Ultrathin SOI Transistors"* IEEE Trans. Electron Devices, vol. ED-37, pp. 1280-1288 (1990)

[124] S.L. Partridge *"Silicon-On-Insulator Technology"* IEE Proc., Pt.I, vol. 133, pp. 66-76 (1986)

[125] C-E.D. Chen *"SIMOX Devices and Circuits"* Vacuum, vol. 42, pp. 383-386 (1991)

[126] Y. Akasaka *"Three-Dimensional IC Trends"* Proc. of IEEE, vol. 74, pp. 1703-1713 (1986)

[127] C-E.D. Chen, M. Matloubian, R.Sundaresan, B-Y. Mao, C.C. Wei, G.P. Pollack *"Single-Transistor Latch in SOI MOSFET's"* IEEE Electron Device Lett., vol. ED-9, pp. 636-638 (1988)

[128] L.J. McDaid, S. Hall, W. Eccleston, P. Watkinson, J.C. Alderman *"The Influence of Emitter Efficiency on Single Transistor Latch in Silicon-On-Insulator MOSFETs"* IEEE SOS/SOI Technology Conference, Key West, Florida, USA (1990)

[129] J-P. Colinge *"Subthreshold Slope of Thin-Film SOI MOSFET's"* IEEE Electron Device Lett., vol. ED-7, pp. 244-246 (1988)

[130] J.R. Davis, A.E. Glaccum, K. Reeson, P.L.F. Hemment *"Improved Subthreshold Characteristic of n-Channel SOI MOSFET's"* IEEE Electron Device Lett., vol. ED-7, pp. 570-572 (1986)

[131] A. L. McWhorter *"1/f Noise and Germanium Surface Properties"* in Semiconductor Surface Physics, ed. R. H. Kingston Philadelphia: University of Pennsylvania (1972) pp. 207-228

[132] S. Christensson, I. Lundstrom, C. Svensson *"Low Frequency Noise in MOS Transistors-I. Theory"* Solid-St. Electron., vol. 11, pp. 797-812 (1968)

[133] H-S. Fu, C-T. Sah *"Theory and Experiments on Surface 1/f Noise"* IEEE Trans. Electron Devices, vol. ED-19, pp. 273-285 (1972)

[134] A. van der Ziel *"Flicker Noise in Electronic Devices"* Adv. Electron. Electron Phys., vol. 49, pp. 225-297 (1979)

[135] A. van der Ziel *"Noise in Measurement"* John Wiley & Sons, Inc. (1976)

[136] A. van der Ziel *"Noise. Sources, Characterization, Measurement"* Prentice Hall, Inc., Englewood Cliffs, New Jersey (1970)

[137] A. van der Ziel *"Noise in Solid State Devices and Circuits"* John Wiley & Sons, Inc. (1986)



[138] G. Reimbold *"Modified 1/f Trapping Noise Theory and Experiment in MOS Transistor Biased from Weak to Strong Inversion-Influence of Interface States"* IEEE Trans. Electron Devices, vol. ED-31, pp. 1190-1198 (1984)

[139] L. Hasse, L. Spiralski *"Szumy elementów i układów elektronicznych"* WNT, Warszawa (1981)

[140] F.N. Hooge, T.G.M. Kleinpenning, L.K.J. Vandamme *"Experimental Studies on 1/f Noise"* Rep. Prog. Phys., vol. 44, pp. 479-532 (1981)

[141] L.K.J. Vandamme *"Model for 1/f Noise in MOS Transistors Biased in the Linear Range"* Solid-St. Electron., vol. 23, pp. 317-323 (1980)

[142] L.K.J. Vandamme, H.M.M. de Werd *"1/f Noise Model for MOSTs Biased in Nonohmic Range"* Solid-St. Electron., vol. 23, pp. 325-329 (1980)

[143] C. Surya, T.Y. Hsiang *"Surface Mobility Fluctuations in Metal-Oxide-Semiconductor Field-Effect Transistors"* Phys. Rev. B, vol. 35, pp. 6343-6347 (1987)

[144] R. Jayaraman, C.G. Sodini *"A 1/f Noise Technique to Extract the Oxide Trap Density Near the Conduction Band Edge of Silicon"* IEEE Trans. Electron Devices, vol. ED-36, pp. 1773-1782 (1989)

[145] K.K. Hung, P.K. Ko, C. Hu, Y.C. Cheng *"A Unified Model for the Flicker Noise in Metal-Oxide-Semiconductor Field-Effect Transistors"* IEEE Trans. Electron Devices, vol. ED-37, pp. 654-665 (1990)

[146] K.K. Hung, P.K. Ko, C. Hu, Y.C. Cheng *"A Physics-Based MOSFET Noise Model for Circuit Simulator"* IEEE Trans. Electron Devices, vol. ED-37, pp. 1323-1333 (1990)

[147] *"The Fundamentals of Signal Analysis."* Hewlett-Packard, Application Note 243 (1985)

[148] J.H. Scofield, T.P. Doerr, D.M. Fleetwood *"Correlation Between Preirradiation 1/f Noise and Postirradiation Oxide Trapped Charge in MOS Transistors"* IEEE Trans. Nucl. Sci., vol. NS-36, pp. 1946-1953 (1989)

[149] T.L. Meisenheimer, D.M. Fleetwood *"Effect of Radiation-Induced Charge on 1/f Noise in MOS Devices"* IEEE Trans. Nucl. Sci., vol. NS-37, pp. 1696-1702 (1990)

[150] J.H. Scofield, D.M. Fleetwood *"Physical Basis for Nondestructive Tests of MOS Radiation Hardness"* IEEE Trans. Nucl. Sci., vol. NS-38, pp. 1567-1577 (1991)

# Summary

The development of modern elementary particle physics demands a lot of technical effort to design and construct the special equipment for carrying out the experiments which would verify the predictions of a theory. The most general questions which should be answered by those dealing with high energy physics are what the matter is built of and how forces act upon them. Although a so-called standard model explains successfully most of the empirical data, many questions remain unanswered. Such a situation promotes the construction and building of ever more complicated experiments and continuously bigger accelerating facilities. One of them is the ZEUS detector at the HERA electron-proton storage ring at DESY in Hamburg.

The work presented here concerns one of the technical problems which was very important while building the analog readout electronics for the ZEUS uranium calorimeter. This problem concerns the radiation sensitivity of electronic technology applied to building the front-end electronics of a readout system. The two chips of the front-end card were designed and fabricated as ASIC components using the MOS VLSI technology. The front-end cards are mounted in place of the ZEUS detector where the dose rate, due to synchrotron radiation, should not exceed 1 $krad/year$. In some places, near the beam pipe, the dose rate can achieve 10 $krad/year$. Therefore, the radiation hardness of technology planned for application had to be tested. A part of the data gathered by the author while he carried out the test of radiation hardness is presented in this work. The technologies developed by the following factories were tested: IMEC - Louvain, ELMOS - Dortmund, IMS FhG - Duisburg. They are standard, not hardened processes. Special attention was paid to the SOI technology provided by IMS FhG because such a kind of MOS technology is usually considered as more radiation hardened than a bulk technology. The total dose hardness was tested by means of using the caesium source of activity $5Ci$ providing the dose rate on the level of $\approx 2.9$ $krad/h$. The test structures delivered by producers were irradiated.

Chapter 2 discusses the structure of the MOS transistor. Special attention is paid to the nonidealities existent in a real structure of the transistor and which can be created during irradiation. These nonidealities can be divided into two kinds of gate oxide charges: an oxide charge and an interface charge. The definition of several parameters of a MOSFET are discussed:

- threshold voltage $V_{th}$,
- transconductance $\beta$, $g_m$,
- drain conductance $g_d$,
- subthreshold swing $S$,
- kink effect parameter $f$,





- spectral noise power density $S_X(f)$ $(X = N_t; I_{DS}; V_{DS})$.

The biggest problem limiting application of the SOI MOSFETs is the kink effect. The origin of this effect and the method of its prevention are discussed in this chapter.

Chapter 2 deals with the fundamental steps of the MOS technology and the technological and the layout design methods improving the radiation hardness of transistors. Modern technological processes consist of over 300 distinct steps and each of them comprises a large number of individual activities. The following steps are discussed in this work:

- substrate formation (bulk and SIMOX wafer),
- p(n)-well implantation,
- definition of active areas of transistors (LOCOS technique and the oxidation of the whole surface and cutting windows in this oxide),
- chan-stop implantation and field oxide growing,
- gate oxide growing,
- implantations for threshold voltage adjustment,
- high temperature anneal,
- deposition of polysilicon,
- implantations of drain/source regions,
- implantation of LDD regions and deposition of oxide spacer,
- PSG deposition,
- deposition of a protection layer.

All steps listed above of a typical LOCOS process flow are illustrated by the process parameters used on the technological line at IMS FhG in Duisburg. The main difference between bulk and SOI technology is the type of input material. For the SOI technology it is a special wafer called SIMOX which consists of a thick ($380nm$) oxide layer covered by a silicon layer. This buried oxide layer is formed under the surface silicon monocrystalline layer by means of using the implantation of oxygen ions deep into a typical silicon wafer. The procedure for producing SIMOX wafer developed by IMS FhG is described in detail. The transistors are formed in the silicon layer on the top of buried oxide. The SOI transistors can be classified into three groups with respect to the values of two parameters: silicon layer thickness and its doping:

- fully depleted,
- partially depleted,
- intermediate thickness.

The improvement of the radiation hardness of devices is generally associated with gate oxide technology. The thinner oxides are better due to a smaller charge buildup in the oxide volume and at the interface. The thinner gate oxides grow on the silicon surface orientation $< 100 >$ than on $< 111 >$ due to a lower oxidation rate. The cleaning procedure of silicon surface before oxide growing (a dilute HF rinse) is very important because of the rejection of silicon surface defects as stacking faults, edge dislocations and contaminations (iron). Optimal conditions of the thermal growing of gate oxide can be chosen. The optimum growth temperature is around 1000°C for dry-oxygen-grown oxides and in the range of $850 - 925$°C for steam oxides. Argon should be the carrier gas. The contamination of the oxidation ambient by trichloroethane can be advantageous in some conditions. This minimizes the density of

interface states. The high temperature annealing of the gate oxide must be carried out in a temperature below 925°C. This temperature was found as a threshold value. Ion implantation (Al, O, N, Na, Ar) into the gate oxide improves the hardness under a positive gate bias due to the creation of electron traps by the displacement damages in the oxide. The process temperatures after gate oxide growth should be minimized as much as possible. All these steps should be performed below 900°C. This requirement causes a considerable problem when one wants to achieve a sufficient smoothness of topography by P-glass flow (typically 1000 – 1100°C). Processes like a high-temperature die bonding or a package sealing can degrade hardness, too. On the other hand an improvement can be achieved by the appropriate design of an IC layout. This concerns the application of close geometry, guardrings, gate oxide extensions, and chan-stop layers.

Chapter 4 describes physical phenomena occurring in irradiated $SiO_2$ and leading to its radiation degradation:

- energy deposition,
- charge generation,
- recombination of created e-h pairs,
- electron and hole transport,
- hole trapping in the bulk of oxide,
- generation of interface states.

Later sections discuss in detail radiation influence on threshold voltage and transconductance. The extraction methods for these two parameters and methods for separating the two components of threshold voltage are presented. These methods are illustrated by means of using the data obtained from measurements carried out by the author. Two separate sections are devoted to the results of the SOI transistors and to radiation influence on the kink effect.

Chapter 5 contains a review of flicker noise models:

- number-fluctuation model,
- mobility-fluctuation model,
- unified model.

The noise measurement system prepared by the author and the results obtained by means of using it are presented. One of the more interesting results is the observation of kink effect in noise. This effect disappears after irradiation.

The appendices contain the presentation of models of the MOS transistor operated in the weak and strong inversion region. The Langevin method of evaluating the power spectral density of a signal is explained, as well.

# Streszczenie

Rozwój współczesnej fizyki cząstek elementarnych wymaga wielu wysiłków technicznych związanych z projektowaniem i konstrukcją specjalnych urządzeń przeznaczonych do prowadzenia eksperymentów weryfikujących przewidywania teorii. Podstawowe pytania, na które odpowiedzi poszukuje fizyka wysokich energii to: z jakich elementów zbudowana jest materia i w jaki sposób siły działają między nimi. Chociaż tak zwany model standardowy poprawnie wyjaśnia większość danych eksperymentalnych wiele pytań ciągle pozostało bez odpowiedzi. Taka sytuacja w tej dziedzinie nauki zachęca do budowania ciągle większych akceleratorów i ciągle większych eksperymentów. Jednym z nich jest detector ZEUS pracujący na elektronowo-protonowy kolajderze HERA zbudowanym w DESY w Hamburgu.

Prezentowana praca dotyczy jednego z problemów technicznych, który był bardzo ważny podczas budowania analogowej elektroniki odczytu dla kalorymetru uranowego detektora ZEUS. Pytanie to dotyczy wrażliwości radiacyjnej technologii elektronicznej planowanej do zastosowania przy budowie modułu elektroniki front-end systemu odczytu. Dwa układy scalone zastosowane w module front-end zostały zaprojektowane i wyprodukowane jako elementy ASIC (układy scalone specjalnych zastosowań) stosując technologię MOS VLSI. Moc dawki promieniowania synchrotronowego w tych miejscach detektora gdzie zamontowane są moduły front-end nie powinna przekraczać $1krad/rok$. Tylko w niektórych miejscach blisko wiązki moc dawki może osiągać $10krad/rok$. Odporność radiacyjna przewidywanych do zastosowania technologii musiała więc być testowana. Część danych zabranych przez autora podczas prowadzenia testów odporności radiacyjnej jest przedstawiona w tej pracy. Testowane technologie pochodziły z następujących firm: IMEC - Louvain, ELMOS - Dortmund, IMS FhG - Duisburg. Są to standardowe, nie utwardzone radiacyjnie procesy technologiczne. Szczeólną uwagę zwrócono na technologię SOI oferowaną przez IMS FhG ponieważ ten rodzaj technologii MOS jest zwykle uważany za bardziej odporny na promieniowanie niż technologia typu "bulk'. Odporność na całkowitą dawkę była testowana za pomocą źródła cezowego o aktywności $5Ci$ zapewniającego moc dawki około $2.9krad/h$. Naświetlane były struktury testowe dostarczone przez producentów.

Rozdział 2 omawia strukturę tranzystora MOS. Szczególną uwagę zwrócono na niedoskonałości rzeczywistej struktury tranzystora, które mogą byc generowane podczas naświetlania. Tymi niedoskonałościami są dwojakiego rodzaju ładunki w tlenku bramkowym: ładunek w głębi tlenku i ładunek na powierzchni rozdziału krzem-dwutlenek krzemu. Omówiono także kilka parametrów tranzystora MOS:

- napięcie progowe $V_{th}$,
- transkonduktancja $\beta$, $g_m$,







- konduktancja drenu $g_d$,
- odwrotne nachylenie charakterystyki podprogowej $S$,
- parametr efektu kinku $f$,
- gęstość widmowa mocy szumów $S_X(f)$ $(X = N_t; I_{DS}; V_{DS})$.

Największym problemem ograniczającym zastosowanie tranzystorów MOS SOI jest efekt kinku. Omówiono mechnizm odpowiedzialny za powstawanie tego efektu i metody jego eliminacji.

Rozdział 3 opisuje podstawowe etapy procesu technologicznego tranzystorów MOS oraz technologiczne sposoby i metody projektowania topologii układu scalonego poprawiające odporność radiacyjną tranzystorów. Współczesne procesy technologiczne składają się z ponad 300 różnych etapów i każdy z nich obejmuje liczne, indywidualne czynności. Następujące etapy są dyskutowane w tej pracy:

- otrzymywanie materiału wyjściowego (płytki krzemu typu "bulk" i SIMOX),
- implantacja studni p(n),
- określenie obszarów aktywnych tranzystorów (technika LOCOS i wycinanie okien w grubym tlenku wytworzonym na całej powierzchni),
- implantacja warstwy chan-stop i wytwarzanie grubego tlenku,
- wytwarzanie tlenku bramkowego,
- implantacje dostrajające napięcie progowe,
- wygrzewanie wysokotemperaturowe,
- nanoszenie krzemu polikrystalicznego,
- implantacje obszarów drenu i źródła,
- implantacja obszarów LDD i nanoszenie tlenku separującego bramkę i obszar drenu,
- nanoszenia PSG,
- nanoszenie warstwy ochronnej.

Wszystkie wymienione powyżej etapy typowego procesu LOCOS są zilustrowane parametrami technologicznymi stosowanymi na lini technologicznej w IMS FhG w Duisburgu. Główną różnicą między technologią "bulk" i SOI jest rodzaj materiału wyjściowego. Dla technologii SOI jest to specjalna płytka krzemu zwana SIMOX, która składa sie z grubej warstwy tlenku ($380nm$) przykrytej warstwą krzemu. Ta zagrzebana warstwa tlenku jest formowana pod powierzchniową warstwą krzemu za pomocą implantacji jonów tlenu w głąb typowej płytki krzemu. Szczegółowo opisano procedurę otrzymywania płytek typu SIMOX opracowaną w IMS FhG. Tranzystory są formowane w warstwie krzemu położonej na zagrzebanym tlenku. Tranzystory typu SOI mogą być sklasyfikowane w trzech grupach według wartości dwóch parametrów: grubości warstwy krzemu i jej domieszkowania:

- całkowicie zubożone,
- częściowo zubożone,
- pośredniej grubości.

Polepszenie odporności radiacyjnej elementu jest głównie związane z technologią tlenku bramkowego. Cieńsze tlenki są lepsze ze względu na mniejszą akumulację ładunku w objętości tlenku i przy jego powierzchni. Cieńszy tlenek narasta na powierzchni krzemu o orientacji krystalograficznej $< 100 >$ niz na $< 111 >$ z powodu

mniejszej prędkości utleniania. Procedura czyszczenia powierzchni krzemu przed utlenianiem (plukanie rozpuszczonym HF) jest bardzo ważna ze względu na usuwanie błędów ułożenia, dyslokacji krawędziowych i domieszek (żelazo). Optymalne warunki termicznego wzrostu tlenku bramkowego mogą być dobrane. Optymalna temperatura wzrostu jest około 1000°C dla tlenków wytwarzanych w suchym tlenie i w zakresie 850 – 925°C dla tlenków wytwarzanych w obecności pary wodnej. Gazem nośnym powinien być argon. Kontaminacja otoczenia utleniającego przez trójchloroetan w pewnych przypadkach może być korzystna minimalizując gęstość stanów powierzchniowych. Wysokotemperaturowe wygrzewanie tlenku bramkowego musi być prowadzony w temperaturze poniżej 925°C. Stwierdzono, że jest to temperatura progowa. Implantacja jonów (Al, O, N, Na, Ar) wgląb tlenku bramkowego poprawia odporność w warunkach dodatniej polaryzacji bramki dzięki generacji pułapek elektronowych powstających na zniszczeniach sieci krystalicznej tlenku. Temperatury procesu technologicznego w etapach następujących po wytworzeniu tlenku bramkowego powinny być tak niskie jak to tylko możliwe. Wszystkie te etapy technologiczne powinny być prowadzone poniżej temperatury 900°C. Wymaganie to powoduje znaczne problemy z osiągnięciem wystarczającej gładkości topografii układu scalonego w procesie płynięcia szkła fosforowego (typowo stosowana jest temperatura 1000 – 1100°C). Procesy takie jak wysokotemperaturowy bonding krzemu do metalowej lub ceramicznej obudowy lub zamykanie obudów mogą pogarszać odporność radiacyjną. Polepszenie może być także osiągnięte przez odpowiednie projektowanie topologii układu scalonego. Dotyczy to stosowania zamkniętej geometrii, pierścieni ochronnych, przedłużeń tlenku bramkowego i warstw ograniczających szerokość kanału.

Rozdział 4 opisuje zjawiska fizyczne zachodzące w naświetlanym dwutlenku krzemu i prowadzące do jego radiacyjnej degradacji:

- depozycja energii,
- generacja ładunku,
- rekombinacja wykreowanych par elektron-dziura,
- transport elektronowy i dziurowy,
- pułapkowanie dziur w objętości tlenku,
- generacja stanów powierzchniowych.

Następnie szczegółowo dyskutowany jest wpływ promieniowania na napięcie progowe i transkonduktancję. Zaprezentowano metody ekstrakcji tych parametrów i podziału napięcia progowego na dwie składowe. Metody te zilustrowane są za pomocą własnych pomiarów. Dwa oddzielne podrozdziały poświęcone są rezultatom dotyczącym tranzystorów SOI i wpływu promieniowania na efekt kinku.

Rozdział 5 zawiera przegląd modeli szumu migotania:

- model fluktuacji liczby nośników,
- model fluktuacji ruchliwości,
- model zunifikowany.

Przedstawiono układ pomiaru szumów i uzyskane przy jego użyciu rezultaty. Jednym z ciekawszych pomiarów jest obserwacja szumowego efektu kinku. Efekt ten znika po naświetleniu.

W dodatkach przedstawiono modele tranzystora MOS pracującego w słabej i silnej inwersji. Wyjaśniono także metodę Langevina obliczania widmowej gęstości mocy sygnału.

# Acknowledgements

I am very indebted to Prof. Kazimierz Korbel who directed this thesis. Especially, I feel very grateful for our scientific discussions, his patience and moral support.

For seventeen months during the last two years I enjoyed working at DESY in Hamburg for the ZEUS collaboration as a part of my postgraduate study at the Faculty of Physics and Nuclear Technique of the Academy of Mining and Metallurgy in Cracow. I would like to thank Dr. Ulrich Koetz for giving me this opportunity, both for his support and for advice which helped me in many ways as he supervised my work during my stay at DESY.

I would like to thank Dr. Władysław Dąbrowski for his advice and friendly discussions about the measurements technique and results analysis.

I am very grateful to Dr. Gert Burbach for giving me his time during my several visits at the Fraunhofer Institute of Microelectronic Systems and Circuits (IMS FhG) in Duisburg. Thanks to him I had the opportunity to learn about practical details of the MOS technology and to watch a technological line. His assistance proved very beneficial to me and gave me a chance to get the test structures.

I am also very grateful to Prof. Andrzej Kotański who helped me to get started on the VME computer, OS-9 operating system and HPIB interface. Thanks to Dr. Zbigniew Jakubowski who dedicated to me much of his time, I became acquainted with the big computer systems at DESY (big IBM, VAX cluster, and Apollo cluster). Thanks to him I mastered the LaTeXdocument preparation system and the postscript graphics.

I must offer my particularly thanks to my German friends Carsten Coldewey and Stephan Boettcher. We spent many day- and night-hours in the laboratory together. Their help and encouragement was very important to me especially when I was tired and full of doubts.

While I was working on the study presented above, I had the opportunity to get to know, personally or via computer networks, many people at DESY and at CERN who were very supportive. I would like to thank them, too.

Finally and because any product is only as good as its cover, I am very grateful to all these people who helped me to improve my English up to the level that I could write and publish my dissertation in this language.