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Study of the Radiation Damage in Analog CMOS Pipelines, MOS Transistors, and MOS Capacitors

by

S. Böttcher

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Dissertation
zur Erlangung des Doktorgrades
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Zusammenfassung

Im Experiment ZEUS am Teilchenbeschleuniger HERA werden kundenspezifische Analog-Pipeline Speicher eingesetzt, welche mit einem 2 μm CMOS-Prozess hergestellt wurden. Diese Pipeline Speicher werden benötigt, um die Detektorsignale des hochauflösenden Uran-Szintillator-Kalorimeters während der Latenzzeit der 1. Triggerstufe zu speichern. Die Bausteine sind innerhalb des Detektors montiert, wo sie radioaktiver Hintergrundstrahlung ausgesetzt sind.

Um die Strahlenhärte der Schaltung zu gewährleisten, wurde ein strahlenfestes n-Kanal Transistorlayout verwendet, mit Dünnoxid-Erweiterung und *guardband*-Implantation.

Die Funktionsparameter der Analog-Pipeline, sowie Kennlinien diskreter Transistoren und Kondensatoren, wurden vor und nach Bestrahlung mit ionisierende Strahlung einer Cs^{137}-Quelle gemessen. Alle Bauteile wurden mit demselben Prozeß hergestellt.

Es wurden Strahlendosen bis 212 krad für die diskreten Bauelemente und bis 500 krad für die integrierte Schaltung erreicht.

Die Analog-Pipeline zeigt geringfügige Veränderungen der Funktionsparameter nach Bestrahlung mit 500 krad. Die dominanten Effekte sind: Zellenleckströme in der Größenordnung 1 pA, *pedestal*-Verschiebung um $\Delta p = 25$ mV und eine Abnahme der Geschwindigkeit der Ausleseverstärker, was zu einer effektiven Verminderung der Pipeline-Verstärkung um 1.5 % führt.

Der Zellenleckstrom entsteht gleichförmig in allen Zellen. In diesem Fall sind Ströme der genannten Größenordnung tolerierbar.

Die Verschiebung des *pedestals* kann durch Änderung des Schaltverhaltens eines *transmission gates* im Signal-Pfad durch Schwellenspannungsverschiebung erklärt werden. Die Abnahme der Ausleseverstärker-Geschwindigkeit kann auf eine Abnahme des Bias-Stromes in der ersten Vertärkerstufe zurückgeführt werden, wiederum durch Schwellenspannungsverschiebung eines kritischen Transistors in der Stromquelle. Beide Effekte sind unkritisch für die Anwendung im ZEUS-Kalorimeter.

Verschiedene Techniken zur Messung von Grenzflächenzustandsdichten wurden angewendet, unter Verwendung von Transistorkennlinien und Kleinsignal-Admittanz Kennlinen von MOS-Kondensatoren. Eine neue Methode zur Bestimmung von Eigenschaften der Grenzflächenzutände unter Verwendung von Kapazitäts-Frequenz-Kurven wurde entwickelt. Die beobachteten Grenzflächenzustandsdichten sind gering: $D_{it} < 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

Der wesentliche Strahleneffekt ist die Erzeugung von fixierten Oxidladungen, was zu Transistor-Schwellenspannungsverschiebungen um $-6\,\mathrm{mV/krad}$ führt, bei Bestrahlung mit einem *gate*-Bias $V_{gs} = +5\,\mathrm{V}$. Der Beitrag der Grenzflächenzustände zur Schwellenspannungsverschiebung liegt unter 10 %.

Abstract

The ZEUS experiment at HERA employs custom made analog pipeline memories, manufactured with a 2 μm CMOS process. These memories are used to store the signals from the high resolution uranium scintillator calorimeter during the latency of the first level trigger, and are mounted inside of the detector where they are exposed to background radiation.

To improve the radiation hardness, *thin oxide extension* and *guard bands* were added to the layout of the NMOS transistors.

Performance parameters of the pipeline and characteristics of discrete transistors and MOS capacitors were studied before and after irradiation with ionizing radiation from a Cs^{137} source with doses up to 212 krad for the discrete components and 500 krad for the integrated circuit. The discrete devices were made with the same process as the integrated pipeline memory.

The pipeline memories showed minor performance degradation after exposure of up to 500 krad. The dominant effects were the development of storage cell leakage current of the order of 1 pA, pedestal shifts of the output voltage $\Delta p = 25$ mV, and a decrease of the speed of the readout amplifier, leading to an effective gain reduction by 1.5 %.

The cell leakage appears uniformly in all cells of the device. In this case, currents of the observed magnitude are tolerable.

The pedestal shift could be due to a changing switching characteristic of a transmission gate in the signal path caused by threshold voltage shifts. The speed degradation of the readout amplifier can be explained by the reduction of the bias current in the input stage of the amplifier, again due to a threshold voltage shift of a critical transistor in the current source. Both effects are uncritical for the application in the ZEUS calorimeter.

Several techniques were used to measure interface trap densities, using transistor characteristics as well as small signal admittance data from MOS capacitors. A new method to extract interface trap properties from capacitance–frequency curves of a MOS capacitor biased in depletion was developed. The observed interface trap densities were small, $D_{it} < 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$.

The main radiation effect was the accumulation of fixed oxide charge, resulting in transistor threshold voltage shift of $-6\,\mathrm{mV/krad}$ when irradiated with a gate bias of $+5\,\mathrm{V}$. Interface traps contribute less than 10 % to the shift.

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Glossary of physical symbols

C_D	Depletion layer capacitance
C_m	MOS capacitance per unit area, after series resistance correction
C_{ox}	Oxide capacitance, $C_{ox} = \varepsilon_{SiO_2}/d_{ox}$
c_p	Hole capture probability
C_{it}	Interface trap capacitance, $C_{it} = q^2 D_{it}$
C_R	Pipeline readout capacitor
C_S	Semiconductor capacitance per unit area
C_S	Pipeline cell storage capacitor
C_T	Single level interface trap capacitance
D	Radiation dose
$\dot{D}$	Doserate
D_{it}	Interface trap density counted per eV in the silicon bandgap and per cm^2
d_{ox}	Oxide thickness
E'	Name of a hole trap center in SiO_2
E_C	Energy level of the conduction band edge
E_F	Fermi energy. A DC-biased MOS capacitor is to a very good approximation in thermal equilibrium, since there is almost no current flow, due to the high resistivity of the silicon oxide.
E_{gap}	Width of the silicon bandgap $E_{\text{gap}} = E_C - E_V$

E_i	Intrinsic level, potential at which $N_A = N_D = n_i$. This is approximately in the middle of the silicon bandgap
E_T	An interface traps energy level
ε_{Si}	The dielectric constant of silicon, $\varepsilon_{Si} = 1.04{\cdot}10^{-12}\,\text{F/cm}$
ε_{SiO_2}	The dielectric constant of silicon oxide, $\varepsilon_{SiO_2} = 3.4{\cdot}10^{-13}\,\text{F/cm}$
E_V	Energy level of the valence band edge
f_o	Trap occupancy probability
F_{ox}	Electric field in the gate oxide
F_s	Electric field at the semiconductor surface
f_s	Dimensionless electric field at the semiconductor surface, $F_s = \frac{kT}{q\lambda_i} f_s$
g	Gain parameter of the pipeline memory response
g_m	Transconductance of a MOS transistor, $g_m = dI_d/dV_{gs}$
G_m	Conductance of the proper MOS capacitor after series resistance correction
G_p	Hole capture and emission conductance
G_S	Semiconductor parallel conductance
I_d	Drain current of a MOS transistor
I_{DDA}	Pipeline analog supply current
I_{DDD}	Pipeline digital supply current
I_{leak}	Pipeline cell leakage current
I_{REF}	Pipeline amplifier bias reference current
kT	Absolute temperature in energy units
λ_i	Intrinsic Debye length, $\lambda_i = \sqrt{\frac{\varepsilon_{Si} kT}{2q^2 n_i}}$
λ_p	Extrinsic Debye length in p-type silicon, $\lambda_p = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_A}}$

N_A	Acceptor density, number of dopands per unit volume in p-type silicon
N_D	Donor density, number of dopands per unit volume in n-type silicon
n_i	Intrinsic electron/hole density, $n_i \approx 10^{10}\,\mathrm{cm}^{-3}$ at $T = 300\,\mathrm{K}$
N_{it}	Interface trap surface density
N_T	Single level interface trap density
p_S	Hole density at the silicon surface
φ	Potential, Fermi-level relative to the intrinsic level E_i (midgap)
φ_B	Fermi-level in the silicon bulk relative to the intrinsic level E_i
$\mathcal{P}$	Distribution of the band bending fluctuations
ψ_s	Surface potential, Fermi-level at the surface relative to its position at flatbands
ψ	Fermi-level relative to its position at flatbands
p	Pedestal (or offset) parameter of the pipeline memory response
q	Elementary charge unit, $q = 1.6022{\cdot}10^{-19}\,\mathrm{As}$
Q_{if}	Charge density at the interface, including the equivalent interface charge for the present fixed oxide charges
ϱ	Charge density in the semiconductor
R_S	Series resistance of the semiconductor bulk and the contacts
σ_s	Width of the distribution of the band bending fluctuations
S	Sub-Threshold slope of an I_d–V_{gs} characteristic
$S^{(\mathrm{irr})}$	Sub-Threshold slope after irradaition
$S^{(\mathrm{pre})}$	Prerad sub-threshold slope
τ_p	Hole capture time constant
t_s	Pipeline cell storage time, when charge is stored in a pipeline cell

V_{bias}	Gate bias voltage
V_{bs}	Bulk-source voltage of a MOS transistor
V_{DDA}	Pipeline analog supply voltage
V_{DDD}	Pipeline digital supply voltage
V_{ds}	Drain-source voltage of a MOS transistor
V_{gs}	Gate-source voltage of a MOS transistor
V_{osc}	Oscillator amplitude, AC-component of the bias voltage for admittance measurements
V_{REF}	Pipeline amplifier bias reference voltage
V_{fb}	Gate bias voltage at flatbands
V_{IN}	Pipeline input voltage
V_{in}	Gate bias voltage at the onset of strong inversion
V_{mg}	Gate bias voltage at midgap
V_{OUT}	Pipeline output voltage
V_{SS}	Pipeline negative supply voltage
V_{th}	MOSFET Threshold voltage
v_s	Dimensionless surface potential, $\psi_s = \frac{kT}{q} v_s$
w_D	Width of the depletion layer. In depletion $w_D = \varepsilon_{Si}/C_D$
Y_{it}	Interface trap admittance, $Y_{it} = Y_S - C_D$
Y_S	Semiconductor admittance, $Y_S = j\omega C_S + G_S$
Y_m	MOS admittance

Introduction

The electron–proton collider HERA at DESY in Hamburg delivers colliding beams since 1992. Two experiments, named H1 and ZEUS, observe the reactions of protons of 820 GeV colliding head on with electrons with an energy of 27.5 GeV.

The 'heart' of the ZEUS detector is a high resolution calorimeter made of depleted uranium with scintillator readout. In spite of its large size it is a very precise instrument to measure the energy, scattering angle and arrival time of the scattered electron and the hadronic energy flow of inelastic *ep* reactions. It has, therefore, played a decisive role in, practically, all investigations, such as measurements of the proton and photon structure functions, the discovery of diffractive processes in deep inelastic scattering, and new QCD tests that were made possible by the large center of mass energy of the HERA machine.

The readout of the ZEUS detector has to deal with challenging constraints, due to the HERA beam structure. The particle bunches of the beam arrive at the interaction point at a frequency of about 10 MHz. To select potentially interesting events, the ZEUS experiment uses an elaborate three stage trigger. The first stage requires 4.5 μs to reach a decision whether to read out the signals of the detector for a specific bunch crossing. Therefore, all detector signals are stored during this time in pipeline memories.

The signals from the 11836 readout channels of the calorimeter are stored in custom-designed integrated analog pipeline memories. These circuits are mounted within the experimental area of the detector, where they are exposed to background radiation from the circulating beams, which are designed to reach currents of 50 mA for electrons and 150 mA for the proton beam. In 1995 running period currents of about 20 mA and 40 mA, respectively, were reached.

The radiation hardness of the pipeline memory circuits was, therefore, a major design issue of the calorimeter readout.

The radiation levels, at the future Large Hadron Collider (LHC) at CERN,

will be several orders of magnitude higher than at HERA experiments [3]. Careful evaluation of the radiation hardness of the employed electronics will be the more important in that environment.

Outline of the thesis

This thesis deals with the radiation hardness of the ZEUS analog pipeline memory circuits.

The first chapter describes the ZEUS experiment, the calorimeter and its front-end electronics, the pipeline memory circuits and the radiation levels in the experiment.

The second chapter is a brief summary of *Metal Oxide Semiconductor* (MOS) device physics, the effects of radiation on devices built of MOS transistors, and the processing technology, used to make the ZEUS pipeline memories.

Chapter 3 describes the irradiation and measurement procedures.

The following three chapters give the results of measurements with three kinds of devices: transistors, MOS capacitors, and the pipeline memory circuit.

Finally, the results and their implications for the performance of the circuit in the ZEUS experiment are discussed in chapter 7.

Chapter 1

The ZEUS experiment at HERA

1.1 Description of the detector

HERA provides a huge electron microscope to look at the structure of the proton. The two collider experiments H1 and ZEUS are the imaging devices of this microscope. The HERA electron beam illuminates the protons in the HERA proton beam in the center of these detectors, the interaction points, where both beams are focused to a small area. The two interaction points are surrounded by a set of detectors to detect the radiation which is scattered from the illuminated proton and the electron. The scattered radiation consists of all kinds of high energetic particles, like hadrons, photons, charged leptons, and neutrinos. The purpose of the detectors is to measure the nature, energy and direction of emission of all these particles (except the neutrinos).

The ZEUS detector conforms to the general structure of colliding beam experiments: The interaction point is surrounded by several layers of subdetectors, covering the solid angle as completely as possible. The main subdetectors are, from inside to outside: the tracking detectors, the calorimeters and the muon spectrometers. A longitudinal cut through the ZEUS detector is shown in Fig. 1.1.

The following description refers to the *forward direction* as the direction of the proton beam.

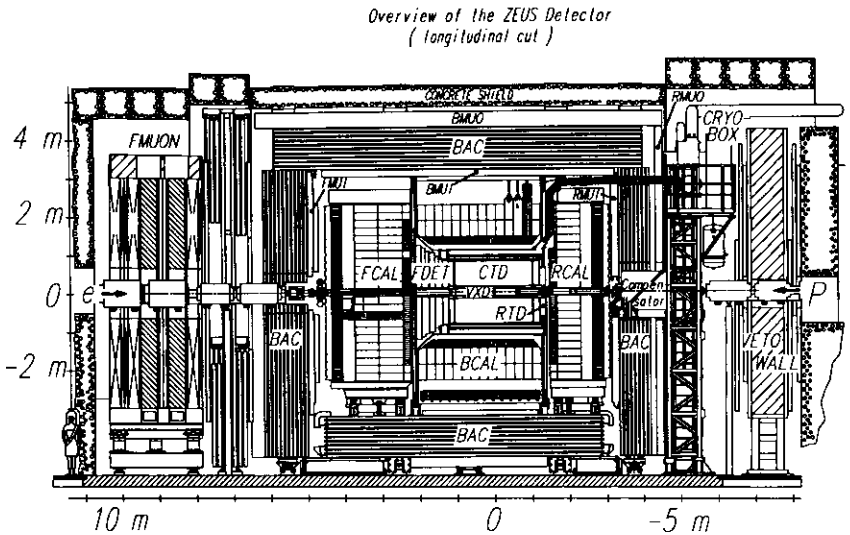


Figure 1.1: Longitudinal cut through the ZEUS detector. The electrons enter from the left-hand side, the protons from the right one. The interaction point is marked in the center. The labeled subdetectors and components are: **VXD:** Vertex detector. **CTD:** Central drift chamber. **RTD:** Rear tracking detector. **FDET:** Forward detector, comprising three forward tracking detector modules (FTD) and two transition radiation detector modules (TRD). **FCAL, BCAL, RCAL:** Forward, barrel and rear calorimeters. **BAC:** Iron yoke with the backing calorimeter. **RMUI, BMUI, RMUI:** Inner muon chambers. **RMUO, BMUO:** Outer muon chambers. **FMUI, FMUON:** Forward muon spectrometer. **CRYO-BOX:** Liquid helium infrastructure for the superconducting SOLENOID (not labeled). **Compensator:** Superconducting magnet to compensate the influence of the main solenoid on the beams. **VETOWALL:** Vetowall to detect proton beam halo particles. **CONCRETE SHIELD:** Concrete blocks surrounding the whole detector.

1.1.1 Tracking detectors

The tracking of charged particles in ZEUS is performed by the vertex detector (VXD), the central drift chamber (CTD), the forward and rear tracking detectors (FTD, RTD) and the transition radiation detector (TRD). The aim of tracking is to determine the momenta of charged particles, with high precision, by measuring the bending radius in the strong magnetic field (1.43 T) of the surrounding superconducting solenoid (SOLENOID). The transition radiation detector allows to distinguish between electrons and hadrons.

VXD: The ZEUS VerteX Detector is a high precision drift chamber that surrounds the beampipe, with a length of 159 cm, with 120 cells that consist of twelve sense wires, each parallel to the beam. Its main purpose is the detection of short lived particles and to improve the momentum and angular resolution of charged tracks, detected by the central drift chamber. The position resolution of the VXD ranges from $\sigma = 50$–$150\,\mu$m in the xy-plane.

CTD: The Central Drift Chamber surrounds the beam pipe and the vertex detector. It has an inner radius of 16.2 cm, an outer radius of 82.4 cm and an overall length of 240 cm. The inner structure of the CTD consists of nine super-layers of drift cells, with eight sense wires in each cell. Five super-layers are parallel to the beam and four are titled to allow a measurement of the z-position of the tracks. The CTD resolution is $\sigma \approx 280\,\mu$m in the xy-plane and about 2 mm in z.

FTD, RTD: Forward and Rear Tracking Detectors are designed to enhance the tracking at low angles in electron and proton direction. FTD and RTD are instrumented with planar drift chambers covering the angular range from 8°–28° (FTD) and 10°–20° (RTD, with respect to the electron beam).

TRD: The Transition Radiation Detector detects charged particles in the forward direction by their energy loss from transition radiation. It consists of layers of polypropylene fibers in which transition radiation is produced, followed by a drift chamber, to detect the transition radiation. Since the amount of produced transition radiation depends on the charge/mass ratio of the traversing particle, the TRD allows to distinguish between electrons and pions.

SOLENOID: The superconducting Solenoid surrounds the tracking devices and produces an inner field of 1.43 Tesla. To minimize energy loss for traversing particles the solenoid has a thickness of only 0.9 radiation length.

1.1.2 Calorimetry

Calorimeters in high energy physics measure the energy of particles. They may also determine their impact position and separate electrons from hadrons and muons.

The main ZEUS calorimeter is a sampling calorimeter, built as a sandwich structure of steel clad depleted uranium (DU) plates as absorber (3.3 mm

DU = 1 electromagnetic radiation length), and scintillator tiles (SCSN-38, 2.6 mm thickness) as readout material.

The calorimeter is subdivided into three parts, the barrel calorimeter (BCAL) which surrounds the tracking devices and the solenoid, and the forward and rear calorimeters (FCAL, RCAL) which close the two ends of the barrel calorimeter. Each of the three calorimeter parts consist of a number of modules, with a width of 20 cm. FCAL and RCAL modules are box shaped, whereas the BCAL modules have a trapezoid longitudinal cross-section. The functional design of all calorimeter modules is similar.

A module is longitudinally segmented into an electromagnetic calorimeter (EMC) and one (RCAL) or two (FCAL, BCAL) hadronic calorimeters (HAC1, HAC2), each of which is read out on both sides by plastic wavelength shifter plates (WLS, 2 mm thick), light guides and associated photomultipliers. Signals from the photomultipliers are fed into the calorimeter readout electronics.

The smallest structure of the ZEUS uranium calorimeter is a cell. A cell is defined as the area read out by two photomultipliers. Its size varies from $5 \times 20\,\text{cm}^2$ in the FCAL EMC to $20 \times 20\,\text{cm}^2$ in the hadronic parts of the calorimeter. EMC cells in RCAL have a cross-section of $10 \times 20\,\text{cm}^2$.

The relative energy resolution of the ZEUS calorimeter is $18\%/\sqrt{E\,[\text{GeV}]}$ for electromagnetic showers and $35\%/\sqrt{E\,[\text{GeV}]}$ for hadronic showers, under test beam conditions. Electromagnetic and hadronic showers of the same energy produce on average the same amount of light in the scintillators. This is achieved by compensating for the energy loss of hadronic showers in the DU absorber, due to production of many neutrons (fission and decay of uranium nuclei in hadronic showers), that in turn have a large energy transfer to protons in the scintillator (SCSN-38 is a carbon hydrogen polymer). The thickness of the scintillator was optimized to achieve compensation. Compensation is the key to the precise energy measurement with good resolution for hadronic showers in the ZEUS calorimeter.

1.1.3 Muon spectrometers and backing calorimeter

Surrounding the high resolution calorimeter is the iron yoke which serves three purposes:

- Return the magnetic flux of the solenoid magnet.
- Gaps within the yoke are instrumented with Al proportional tubes filled with Ar–CO_2, to make it a backing calorimeter, to detect and measure

events where very high energetic particles are not completely absorbed in the uranium calorimeter.

- The yoke is magnetized, to provide bending power for the muon spectrometer.

Muon chambers are mounted inside and outside the yoke to measure the deflection of muons in the magnetic field within the yoke. For muons, emitted in the proton direction, there is a forward muon spectrometer, with two large massive iron toroids to provide the necessary bending power, in addition to the iron yoke.

The *ZEUS status report* [4] gives a complete description of the ZEUS detector.

1.1.4 ZEUS three level trigger

The detectors and the readout electronics in the HERA experiments have to comply to a challenging constraint imposed by the accelerator: the colliding particles arrive in bunches, which meet at the interaction point every 96 ns. Most often the particle bunches pass each other without any observable interaction. About 100 thousand times per second the beams cause observable signals in the detectors, but very few of these events are actually interesting electron proton scattering events.

The ZEUS experiment uses a three-stage trigger. The first trigger level looks at detector signals, which are digitized at high speed and, for some detectors, with limited resolution. This trigger works deadtime free. It accepts and processes data at the rate of the HERA clock every 96 ns, The individual trigger decision for any bunch crossing takes about 4.5 μs. Therefore, all signals from the detector must be stored for 4.5 μs in either digital or analog pipeline memories, until a decision on their fate is reached.

The trigger is designed to use algorithms which accept no more than thousand events per second.

When the first trigger level reaches a positive decision, the data are read from the pipeline memories, digitized if necessary, and transferred to the second level trigger, which uses data with full granularity and precision. No more than one out of ten events should pass this trigger level.

The events that pass the second trigger are compiled into a common data structure and transfered to the third level trigger, which does a complete reconstruction of the event. The third level trigger is a farm of fast computers

of sufficient size to reconstruct up to hundred events per second. The final trigger rate is limited to 15 events per second, resulting in a data stream of one million bytes of data per second, which is stored on computer tapes for later analysis.

1.2 The calorimeter read out electronics

The ZEUS high resolution uranium–scintillator calorimeter employs an analog CMOS switched capacitor pipeline memory and a similar buffer memory with an integrated analog multiplexer to store the detector signals during the first level trigger latency of 4.5 μs. Both circuits were specifically designed for this purpose by the Fraunhofer Institut für Mikroelektronische Bauteile und Systeme in Duisburg, Germany [5].

The circuits are mounted within the detector on the back of the calorimeter on the *analog front-end cards*. Fig. 1.2 shows a block diagram of the circuit on the analog card.

Each pipeline memory circuit has four channels with 58 storage cells each. The buffer/multiplexer circuit features twelve buffer memories with eight cells each.

The signals from the photomultiplier tubes are fed with different gains into two shapers. The shapers are analog filters which a δ-pulse response $h(t)$ as shown in Fig. 1.3. The pipeline memories sample the outputs of the shapers synchronous to the HERA bunch clock, every 96 ns the voltage of the signals are stored into analog storage cells.

When the first level trigger sends an accept signal, the data from five consecutive cells in the pipeline, which cover the shapes of pulses corresponding to the triggered HERA bunch crossing are transfered into buffer memories. For this purpose the pipeline is stopped and switched to read mode. After the transfer, the pipelines resume sampling the detector signals, while the data in the buffers are sent at lower rate (0.8 MHz), over 60 m of cable, out of the detector for digitization. The data from twelve buffer memories are multiplexed to one line.

The multiplexers have twelve additional (unbuffered) inputs. Six of these inputs are used to read out uranium current, the remaining inputs are used to read diagnostic voltages from the analog card.

The uranium current signals are obtained with analog integrators, which integrate the signals from the photomultiplier tubes with a time constant of 20 ms. The natural radioactivity of the depleted uranium gives a constant

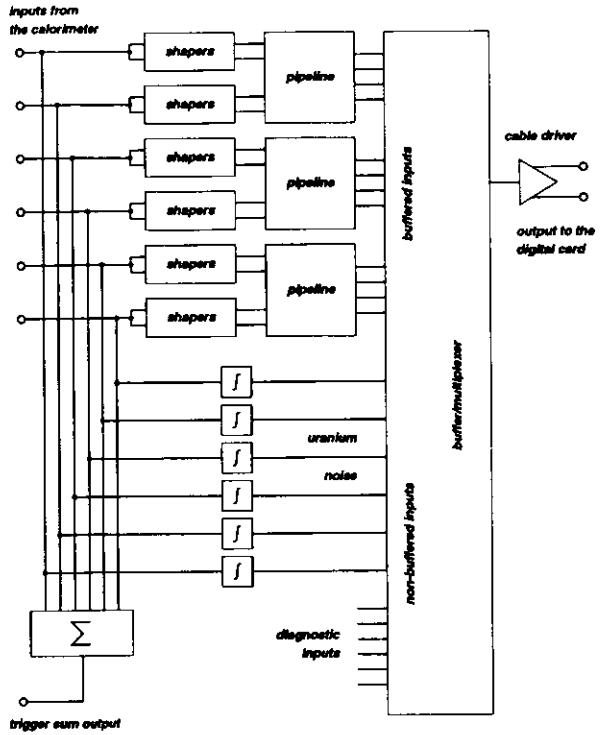


Figure 1.2: Block diagram of the ZEUS calorimeter read out analog card. Each card features two of the shown circuits. The analog cards are mounted on the back of the calorimeters within the ZEUS detector. The inputs are connected to the outputs of the photomultiplier tubes. The input signals are split into three ways: 1) They are fed for the precision readout via shapers into pipeline memories. 2) The signals are integrated with a time constant of 20 ms to measure the uranium current via non-buffered multiplexer inputs. 3) Groups of three to four inputs are summed to provide inputs for the calorimeter first level trigger, which operates with reduced granularity (for simplicity, all shown inputs are summed together in this picture). The two shapers provide output signals with different amplification to increase the dynamic range of the readout. Both channels are samples by the pipeline memory and, upon a first level trigger accept, the information is transfered to buffers in the buffer/multiplexer chip. The pipeline resumes sampling the input signals while the information in the buffers is time-multiplexed to the cable driver and sent via 60 m of twisted pair cable to digital cards outside the detector, where the signals are digitized and stored for further processing. When an overflow occurs, during digitization, on the high gain channel, the low gain channel is used. The uranium current signals and some diagnostic voltages are readout through the same multiplexer channel.

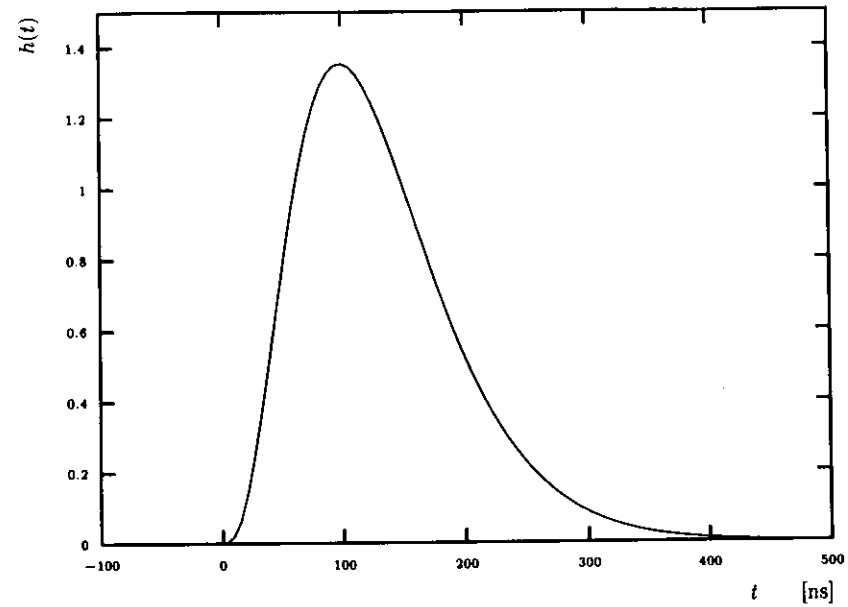


Figure 1.3: Pulse response of the shaper filters. The pulse response $h(t)$ is the output of the filter in response to a $\delta(t)$-pulse at the input.

background light to the photomultipliers. Measuring the output current, generated by this light, provides an excellent means to calibrate and monitor the calorimeters energy scale.

The ZEUS calorimeter has 11836 channels. The readout requires 5918 pipeline memory chips and 1972 buffer/multiplexer circuits.

For a detailed description of the calorimeter readout refer to [6, 7].

1.2.1 The ZEUS analog pipeline memory chip

Circuit description

The analog pipeline memory circuit is built in switched capacitor CMOS technology. Fig. 1.4 shows the circuit diagram of the whole memory chip. Each of the four channels is built of 58 storage cells, a readout amplifier, four READ/WRITE mode switches and a digital shift register to select one storage cell at a time in a circular mode.

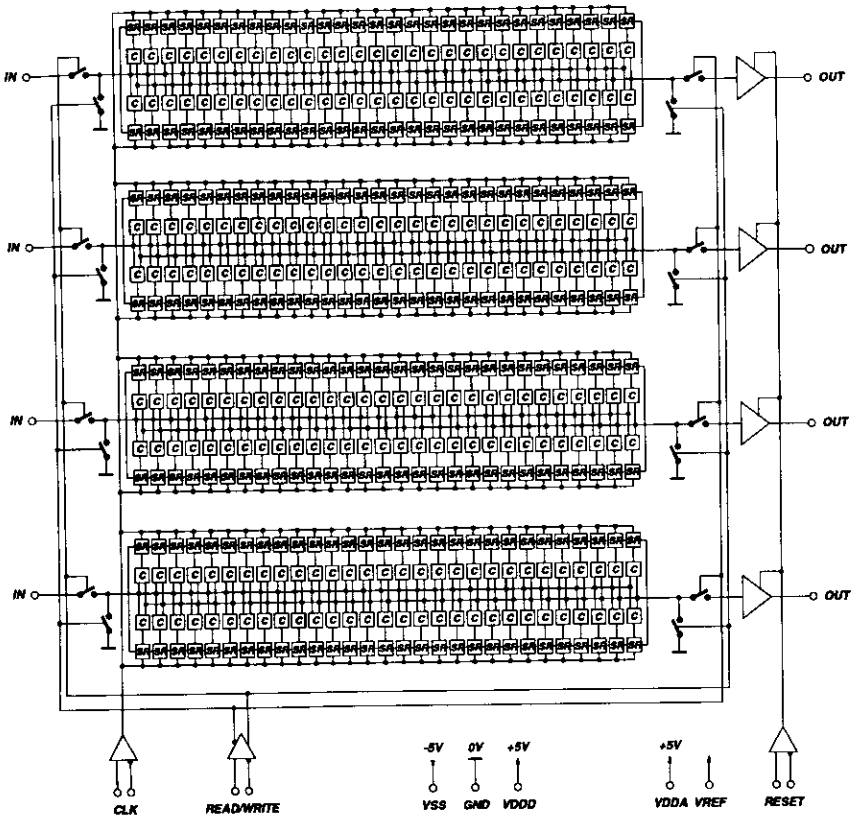


Figure 1.4: Circuit diagram of the whole pipeline memory chip. The pipeline chip features four channels with 58 storage cells each. Three control signals, READ/WRITE, CLK and RESET, are fed into the circuit via differential input comparators. The READ/WRITE signal switches between read and write mode. In both modes, access to the storage cells C is controlled by a digital shift register with one shift register cell SR for each storage cell. Only one cell in each channel is active at any time, a pulse on the CLK input shifts the active bit from one SR cell to the next. The readout is done via readout amplifiers, which need to be reset before reading each cell with the RESET input.

The diagrams in Figs. 1.5 and 1.6 illustrate the analog signal path of one pipeline channel. Fig. 1.5 shows the switches with their naming scheme while Fig. 1.6 has the generic switch symbols replaced by the transistor composition.

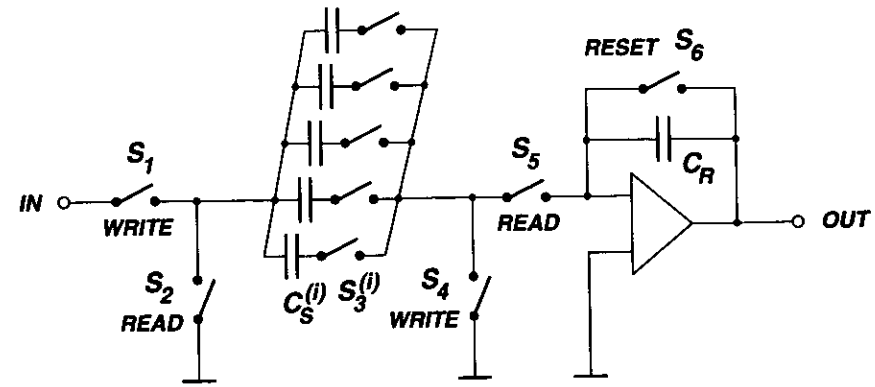


Figure 1.5: The analog signal path of the pipeline with generic switches. Only five of 58 storage cells ($C_S^{(i)}$–$S_3^{(i)}$) are drawn in this diagram.

A storage cell consists of a storage MOS capacitor $C_S^{(1...58)}$ and a transmission gate switch $S_3^{(1...58)}$ which is controlled by a corresponding cell in the shift register SR.

The capacitors $C_S^{(1...58)}$ are built on n-wells, with a gate oxide dielectric and a polysilicon layer on top. The capacitance is $C_S = 1\,\mathrm{pF}$. The polysilicon plates of the capacitors are facing the switches $S_3^{(1...58)}$.

The feedback path of the readout amplifier consists of the readout capacitor C_R and the RESET switch S_6, both with identical layout, as used for the storage cells. The bias current of the amplifier is set via a current mirror by an external reference voltage V_{REF}.

The READ/WRITE mode switches S_1, S_2, S_4 and S_5 are large NMOS transistors.

The pipeline memory is used with negative input voltage between zero and $-2\,\mathrm{V}$, thus, avoiding depletion/inversion of the MOS storage/readout capacitors and operating the READ/WRITE switches with sufficiently low resistance in the *on*-state.

Three digital control signals READ/WRITE, CLK and RESET are fed into the IC, via differential comparators. The bias currents of these are controlled by the same reference V_{REF} as for the readout amplifiers.

The readout amplifiers are supplied by a power supply V_{DDA} separate from the digital power supply V_{DDD}.

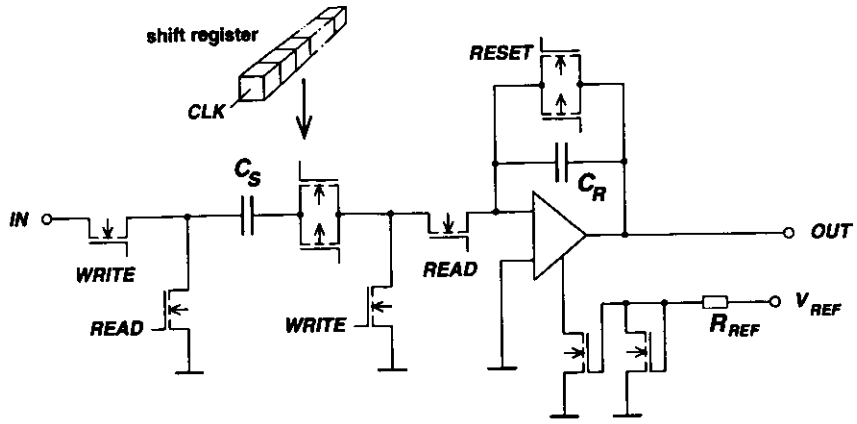


Figure 1.6: The analog signal path of a pipeline channel with the switches drawn as transistors. Only one storage cell C_S is shown.

Operation

The pipeline memory runs in two modes: In WRITE mode the input voltage is clocked into successive cells at a nominal CLK frequency of 10.4 MHz. In READ mode, successive cells are read out at a rate of up to 1 MHz, using the RESET switch to discharge the readout capacitor, before reading each cell. The signal sequence of the three control inputs READ/WRITE, CLK and RESET are drawn in Fig. 1.7.

The first CLK pulse after switching from READ to WRITE mode initializes the circular shift register to select the first storage cell, and deselect all the others. Any successive CLK pulse will push the selecting bit to the next cell of the shift register. This remains true when switching from WRITE to READ after receiving a trigger in the experiment. The information in the currently selected cell is lost during the switch to READ mode. The first cell to be read out is the one that has been written 47 CLK pulses, or 4.5 μs ago.

Writing the input voltage into the cells works as follows: The n-well plates of all storage cells are connected to the analog input via S_1. The polysilicon side of the selected cell is switched to the analog ground level via S_4. On the active edge of the CLK pulse, the cell switch S_3 is opened, thus, freezing the charge on the storage capacitor C_S. The next cell is selected, by closing its switch, allowing the capacitor to collect charge until the next CLK pulse arrives 96 ns later. The integration time constant of the cells is a few nanoseconds.

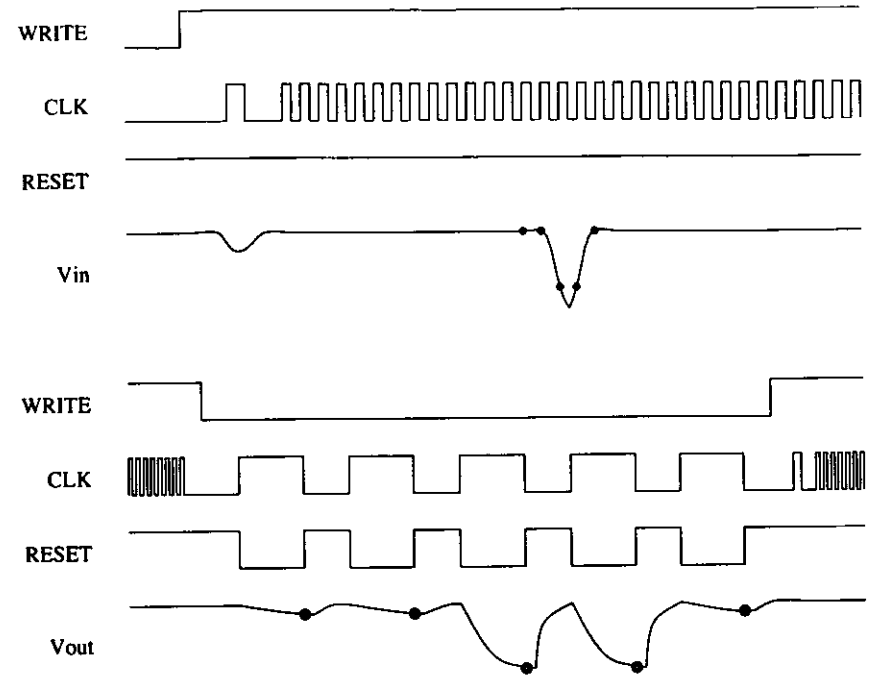


Figure 1.7: Pipeline operation signal sequences. The upper sequence shows the three pipeline control signals during the switch from READ to WRITE mode, with an event pulse on the input. The lower sequence shows how that event is read out. Please note that the time scales of the upper and the lower sequence are different.

In READ mode, the n-well plates of the storage capacitors are switched to ground via S_2. Upon a CLK pulse, a cell is selected by closing the cell switch S_3. The charge on the cell capacitor flows through S_5 to the readout capacitor C_R. The readout capacitor is now in exactly the same state as the cell capacitor was during WRITE. The polysilicon plate is grounded on the virtual ground, at the input of the readout amplifier, and the n-well plate reproduces the sampled input voltage at the output. This requires that the readout capacitor was discharged via the RESET switch S_6 prior to selecting the cell.

1.2.2 Radiation environment at ZEUS

The analog front-end cards, with the memory circuits, are mounted at the back of the calorimeter, to allow for short cables to connect to the photo multiplier tubes. This location is shielded from the interaction point by the calorimeter itself, and from the back, by the iron yoke, concrete blocks, and other detector components. Nevertheless, there is a substantial amount of background radiation.

One source of radiation is the natural radioactivity of the uranium. When the detector is in operation, the electronics are shielded from the uranium by the calorimeters steel support structure. But, during maintenance periods and while beams are injected into HERA, the two halves of the forward and the rear calorimeters are moved apart. In this case radiation from the surfaces of the inner calorimeter modules reaches the electronics. From measurements with *background radiation monitors* (BRM), mounted near to the electronics, this radiation amounts to 14 mrad/d, in the worst case [8]. This is negligible.

Stable beams in HERA cause background radiation from synchrotron radiation, beam halo particles and beam–gas interactions from the electron and proton beams. The highest radiation levels are expected during unstable proton beam conditions or beam losses.

The total dose measured with the BRM during 1992 was 24 rad. This dose is low because the HERA beam currents were two orders of magnitude below design value, although there were some serious beam losses during that period. The radiation level at design luminosity is expected to be below 25 rad/d during the running period. The total dose in the anticipated lifetime of ZEUS may reach 50 krad in some components located near to the beampipe.

1.2.3 Radiation hardness of the pipeline memory

The first versions of the pipeline and buffer memories were produced using a standard CMOS process, with no precaution for radiation hardness. These devices failed to work after receiving an ionizing irradiation dose of less than 10 krad [9]. Details are discussed in chapter 2, where the basic mechanisms of irradiation damage in MOS circuits are explained.

The circuits were replaced by an improved version, produced with a similar standard CMOS process, but employing a radiation-hard transistor layout, with *thin oxide extension* and *guard bands* [10].

The improved circuits were produced by the *Fraunhofer Institut für Mikroelektronische Bauteile und Systeme* in Duisburg, Germany. These devices were used for the studies presented in this thesis.

Chapter 2

Radiation hardness of CMOS electronics

2.1 Physics of the MOS structure

A MOS device is a structure made of three layers: a *Metal* electrode, a thin insulating *Oxide* layer, and the *Semiconductor* bulk. A MOS capacitor is a passive MOS device with no further lateral structure in the semiconductor. This section introduces the basic terms that describe a MOS capacitor with a DC-bias voltage applied to its two terminals: the metal gate and the semiconductor bulk.

2.1.1 The silicon MOS capacitor

To make a silicon MOS device, a thin silicon dioxide layer is formed on a monocrystalline silicon substrate, by heating the substrate to about $1000°C$ in an atmosphere which contains oxygen. The metal gate electrode is afterwards deposited on top of the oxide. Commonly used materials for the gate are aluminum or polysilicon. All MOS devices, used for this work, are made with polysilicon gates. Fig. 2.1 shows the structure of a basic MOS capacitor.

I will now describe the material properties which define the behavior of the MOS device.

The only property of the gate metal, with an influence on the device characteristics, is its workfunction. The workfunction is the energy which is needed to move an electron out of the metal. This is usually expressed as the *workfunction difference*, the difference of the workfunctions of the gate metal

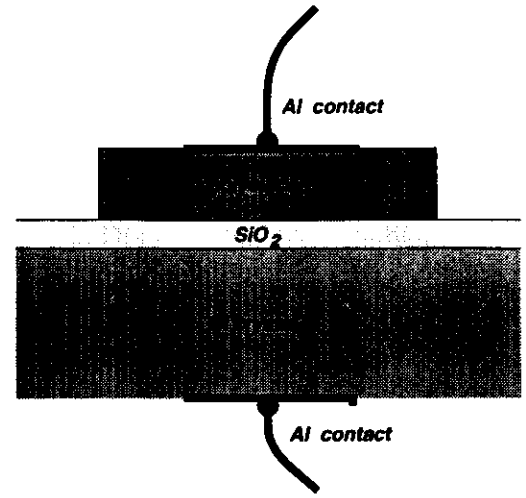


Figure 2.1: Structure of a basic MOS capacitor.

and the semiconductor. The workfunction difference gives a constant offset to the bias voltage applied to the device. This offset is indistinguishable from other offsets like fixed oxide charges or an inhomogeneous impurity density in the semiconductor (see below).

The parameters that describe the oxide are its thickness d_{ox}, the dielectric constant $\varepsilon_{SiO_2} = 3.4{\cdot}10^{-13}\,\mathrm{F/cm}$ and its quality. The quality depends on the temperature, atmosphere, and duration of the oxidation process, any subsequent high temperature treatment, gate metal deposition and composition, the crystal orientation of the substrate, luck, and the irradiation history. Typical sources of radiation are X-ray or electron beam lithography or ion implantation in subsequent processing, hot electrons during operation of the device, or external radiation in the storage or operation environment. Measurable expressions of the oxide quality are the densities of fixed oxide charges and interface traps, and the radiation hardness. Fixed oxide charges are mostly holes, and, possibly, some electrons which are trapped within the bulk of the oxide, most of them near the interface to the silicon substrate. Interface traps are electronic states at the interface, with energy levels within the silicon band gap. The radiation hardness, in turn, is how irradiation changes the fixed oxide charge and interface trap densities. Radiation comes in several kinds, with any energy spectrum, intensity, and duration, with different effects, depending on the samples' temperature and bias condition. That is one reason why radiation hardness is such a complex issue.

Fixed oxide charges contribute to the constant offset to the applied bias voltage, depending on the location within the oxide. With the distance x from the gate metal ($x = 0$ at the metal/oxide interface, and $x = d_{ox}$ at the oxide/silicon interface) and the charge density $\varrho(x)$ in the oxide, the offset voltage due to oxide charges is

$$\Delta V_{\text{bias}} = -\frac{1}{\varepsilon_{SiO_2}} \int_0^{d_{ox}} \mathrm{d}x \, x\varrho(x). \tag{2.1}$$

Interface traps change their charge state depending on their energy level and the bias condition.

The main property of the silicon substrate is the impurity concentration as a function of space. A reasonably large capacitor can be considered homogeneous over the surface area, but the impurity concentration usually depends on the depth into the substrate, especially when dopant ions were implanted after the substrate crystal was grown. The oxidation and other high temperature processing cause impurities to diffuse into or out of the substrate. Inhomogeneities in impurity concentration create internal electric fields in the substrate, which contribute another offset to the bias voltage.

The area A of the capacitor will not appear in the following discussions, since all variables that scale with the area are normalized to the unit area.

The dielectric constant of silicon is $\varepsilon_{Si} = 1.04 \cdot 10^{-12}\,\mathrm{F/cm}$.

2.1.2 Bias voltage regimes

The semiconductor of a MOS capacitor, with a DC-bias applied, is in thermal equilibrium, because there is no current flow. It is a very good approximation to consider the resistivity of the oxide to be infinite.

The applied voltage divides into three parts, the voltage across the oxide, the voltage across the semiconductor, and the work function difference of the contacts. For simplicity, we will now assume that the impurity concentration in the semiconductor is homogeneous, that the oxide is free of charges, and that there is no work function difference at the two contacts.

The voltage across the oxide is the width of the oxide d_{ox} times the electric field in the oxide.

When the bias voltage is set to the capacitors *flatbands* voltage V_{fb}, the charge density in the semiconductor is zero and so is the electric field. The valence and conduction band edges in the semiconductor run parallel to the Fermi energy. That is why this state is called flatbands. With our ideal

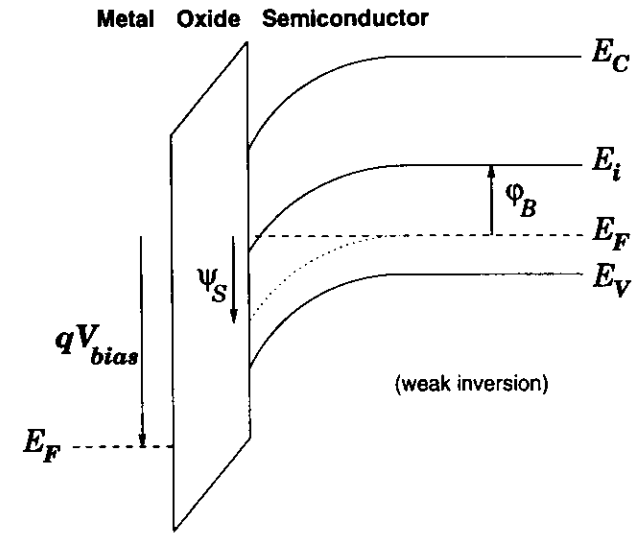


Figure 2.2: Energy band diagram, to illustrate the definition of the surface potential ψ_s in a MOS capacitor. The semiconductor is p-type, biased in weak inversion. In the semiconductor part the edges of the valence and conduction band, E_V and E_C are shown, also the intrinsic energy level E_i and the Fermi level E_F. The difference of the Fermi level in the semiconductor and the metal is the applied bias voltage V_{bias}. The potential ψ in the semiconductor is defined as the difference of E_F and its position in the band structure in the bulk. ψ_s is the potential at the surface.

capacitor, this happens at $V_{fb} = 0\,\mathrm{V}$. A nonzero workfunction difference, fixed oxide charges and interface traps will change the capacitors flatbands voltage. When the impurity concentration in the semiconductor is inhomogeneous it is not even easy to define a flatbands condition, since the bands are never flat. At flatbands, the silicon under the surface is in the same state as in the bulk.

I will restrict the following to p-type MOS capacitors, since all samples, used in this thesis, were of this type. In p-type silicon the impurities are acceptors and their density is called N_A. Acceptors create electronic states next to the valence band, near enough to ensure that all these states are occupied by electrons. Those electrons are missing in the valence band, for each negatively ionized acceptor there is one hole. The density of holes p is equal to $N_A + n$, but the density of electrons in the conduction band n is negligible. To be precise, the product of the electron and hole density is constant $np = n_i^2$, with $n_i \approx 10^{10}\,\mathrm{cm}^{-3}$ at room temperature. The large hole

density moves the Fermi energy level E_F into the lower part of the silicon bandgap

$$E_F = E_i + \frac{kT}{2} \ln \frac{n}{p} = E_i + kT \ln \frac{n_i}{p}, \tag{2.2}$$

e. g., with $p = N_A = 10^{16}\,\mathrm{cm}^{-3}$, the Fermi level is 0.35 eV below E_i, which is the intrinsic energy level about in the middle of the bandgap. E_i is defined by Eq. (2.2) to be the Fermi level, when the hole density equals the electron density $p = n = n_i$.

We call the location of the Fermi level deep in the neutral bulk of the semiconductor $\varphi_B = E_F - Ei$. φ_B is negative in p-type silicon. When an electric field is present in the semiconductor, the band structure bends up or down in space. Fig. 2.2 is the energy band diagram of a MOS capacitor, with a moderate positive bias applied, which causes the bands to bend down near the interface to the oxide. The assumption that the band structure in the semiconductor remains the same in the presence of an electric field, only shifted in energy, is called *band bending approximation.*

The states of a biased MOS capacitor are divided into four regimes, depending on the amount by which the bands are bent on the interface of the semiconductor to the oxide. This amount of bending is called the surface potential ψ_s, which is zero at flatbands.

I measured the potential in energy units, others use electric potential units [V]. This makes no difference in the numeric value, since the used energy unit is the electron-Volt [eV], save for factors q, the elementary charge unit, in my formulas.

Accumulation

When the bias voltage is below V_{fb}, the hole (majority carrier) density at the surface is larger than in the bulk $n < n_i < N_A < p$. This regime is called accumulation.

Depletion

The *midgap* voltage V_{mg} is the bias voltage which moves the band structure so far that the Fermi level at the surface is in the middle of the bandgap, or, more precisely, at the intrinsic level E_i. At this point, the hole and electron densities are the same $p = n = n_i$. The bias regime between flatbands and midgap is called *depletion*, because the majority carriers are depleted $n < n_i < p < N_A$.

Inversion

If V_{bias} is increased further, there is a point where the electron (minority carrier) density at the surface becomes as large as the hole density in the bulk $n = N_A$. This is called the *onset of strong inversion.* With V_{bias} between V_{mg} and the onset of strong inversion V_{in} the electron density is larger then the hole density, but lower than the acceptor density $p < n_i < n < N_A$. This is the regime of *weak inversion.* The ratio of the hole to the electron density is inverted. The bias regime beyond V_{in} is called *strong inversion*, because the minority carrier density exceeds the majority acceptor density at flatbands $p < n_i < N_A < n$.

2.1.3 Low frequency MOS capacitance

With the assumptions of the previous section for an ideal MOS capacitor, it is possible to integrate the Poisson equation for the potential in the silicon bulk. This yields a relation between the applied bias voltage V_{bias} and the surface potential ψ_s, and the low frequency capacitance.

Solving the Poisson equation

The Poisson equation in one dimension for the potential ψ (measured in energy units $[eV]$) is

$$\frac{1}{q} \frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = -\frac{\varrho}{\varepsilon_{\mathrm{Si}}} \tag{2.3}$$

with

$$\varrho = (p - n + N_D - N_A)q \tag{2.4}$$

$$p = N_A \exp(-\frac{\psi}{kT}) \qquad n = \frac{n_i^2}{p} \qquad N_D = \frac{n_i^2}{N_A}. \tag{2.5}$$

The term N_D for the donor density is included to ensures charge neutrality in the silicon bulk. When we integrate Eq. (2.3) we get an expression for the electric field F as a function of the potential ψ. We switch to dimensionless variables v, w, N, and f

$$\psi = kT\, v \tag{2.6}$$

$$x = \lambda_i\, w \tag{2.7}$$

$$N_A = n_i\, N \tag{2.8}$$

$$F = \frac{1}{q} \frac{\mathrm{d}\psi}{\mathrm{d}x} = \frac{kT}{q\lambda_i} \frac{\mathrm{d}v}{\mathrm{d}w} = \frac{kT}{q\lambda_i} f \tag{2.9}$$

with the intrinsic Debye length in silicon

$$\lambda_i = \sqrt{\frac{\varepsilon_{Si} kT}{2q^2 n_i}}. \tag{2.10}$$

The dimensionless Poisson equation becomes

$$\frac{\mathrm{d}^2 v}{\mathrm{d}w^2} = -\frac{1}{2}\left(N(e^{-v} - 1) - \frac{1}{N}(e^{v} - 1)\right). \tag{2.11}$$

This formula is symmetric in the semiconductor type, with $N > 1$ for p-type silicon and $N < 1$ for n-type. Using the identity

$$\frac{\mathrm{d}}{\mathrm{d}w}\left(\frac{\mathrm{d}v}{\mathrm{d}w}\right)^2 = 2\frac{\mathrm{d}v}{\mathrm{d}w}\frac{\mathrm{d}^2 v}{\mathrm{d}w^2} \tag{2.12}$$

we obtain

$$\mathrm{d}(f^2) = -\left(N(e^{-v} - 1) - \frac{1}{N}(e^{v} - 1)\right)\mathrm{d}v. \tag{2.13}$$

Now, we integrate Eq. (2.13) from the neutral bulk where $v = f = 0$, to the surface, where the potential is $v = v_s$. With the proper sign convention, the electric field at the surface becomes

$$f_s = -\mathrm{sgn}(v_s)\sqrt{N(e^{-v_s} - 1 + v_s) + \frac{1}{N}(e^{v_s} - 1 - v_s)}. \tag{2.14}$$

The bias voltage

With the knowledge of the electric field F_s and the potential ψ_s at the semiconductor surface, we can calculate the applied bias voltage V_{bias} as the sum of the surface potential ψ_s and the voltage across the oxide

$$V_{\mathrm{bias}} = \frac{\psi_s}{q} - \frac{\varepsilon_{Si}}{C_{ox}}F_s, \tag{2.15}$$

with $\varepsilon_{SiO_2} F_{ox} = \varepsilon_{Si} F_s$, and the oxide capacitance

$$C_{ox} = \frac{\varepsilon_{SiO_2}}{d_{ox}}. \tag{2.16}$$

The differential low frequency capacitance

The differential low frequency MOS capacitance C_m is defined as

$$C_m = \frac{\mathrm{d}Q}{\mathrm{d}V_{\mathrm{bias}}}, \tag{2.17}$$

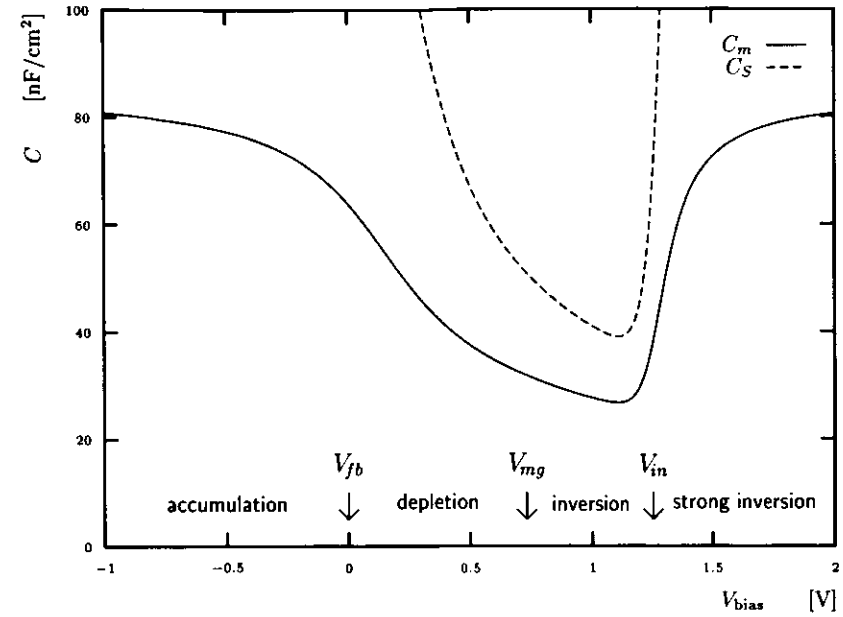


Figure 2.3: Calculated low frequency C-V curve. The parameters are the acceptor density $N_A = 10^{16}\,\mathrm{cm}^{-3}$ and the oxide capacitance $C_{ox} = 85\,\mathrm{nF/cm}^2$.

and from Gauß law we know that the total surface charge density in the semiconductor Q is proportional to the electric field at the surface

$$Q = -\varepsilon_{Si} F_s. \tag{2.18}$$

In this context *low frequency* means that the capacitance is measured at a frequency which is low enough to keep the capacitor in thermal equilibrium all the time.

Using Eq. (2.15) to substitute for V_{bias} gives

$$C_m = \frac{C_{ox} C_S}{C_{ox} + C_S} \tag{2.19}$$

with the semiconductor capacitance C_S

$$C_S = -\frac{1}{q}\frac{\mathrm{d}F_s}{\mathrm{d}\psi_s}. \tag{2.20}$$

The MOS capacitance C_m is the series combination of the oxide capacitance C_{ox} and the silicon capacitance C_S.

By differentiating Eq. (2.14) we obtain the expression

$$C_S = -\frac{\varepsilon_{Si}}{\lambda_i}\frac{1}{2} f^{-1}\left(N(1-e^{-v}) + \frac{1}{N}(e^{v}-1)\right). \tag{2.21}$$

If we take Eqs. (2.15 and (2.21), we get the C-V curve using the surface potential ψ_s as a parameter, running from the valence band to the conduction band. Fig. 2.3 gives an example. The dashed curve is the semiconductor capacitance C_S, with $N_A = 10^{16}\,\mathrm{cm}^{-3}$ ($N = 10^6$). The solid curve is the MOS capacitance C_m, with $C_{ox} = 85\,\mathrm{nF/cm}^2$. The bias voltages corresponding to V_{fb}, V_{mg}, and V_{in} are marked on the x-axis.

Left of V_{fb} is the accumulation regime. The nominator of Eq. (2.21) is dominated by the term Ne^{-v_s}, which stands for the rapidly growing majority carrier density at the interface. On the other end, right of V_{in} in strong inversion, the term describing the inversion layer of minority carriers $1/N\, e^{v_s}$, dominates. Both the accumulation charge layer and the inversion layer have an almost infinite capacitance because of the high density of states on the edges of the valence and conduction bands respectively. When the surface field changes, more charges appear at the interface without the need to change the potential. The MOS capacitance approaches the oxide capacitance in both of these cases.

In the intermediate regimes the charge in the semiconductor is dominated by the ionized acceptors in the depletion layer

$$Q \approx qN_A w_D, \tag{2.22}$$

with the depletion layer width w_D. Solving the Poisson equation as above, but with $\varrho = qN_A$, gives

$$C_S = \frac{\varepsilon_{Si}}{w_D}, \tag{2.23}$$

which is a capacitor with a silicon dielectric of width w_D.

While increasing the bias voltage, the depletion layer grows until the inversion layer builds up. w_D reaches a maximum and remains constant in strong inversion.

High frequency C-V curve

The majority carriers follow a change of the bias voltage instantaneously for all reasonable frequencies. But an inversion layer in a MOS capacitor is completely insulated by the oxide and the depletion layer, and the mechanisms to generate and recombine minority carriers are slow. Depending on

the temperature and impurities in the silicon bulk, even $f = 1\,\mathrm{Hz}$ may be considered a *high frequency*, since the minority carriers can not maintain thermal equilibrium.

The *high frequency* MOS *capacitance* is measured with the capacitor in thermal equilibrium, according to the DC-bias, but, at a frequency that is high enough, to prevent the minority carrier density to change altogether. The high frequency capacitance differs from the low frequency capacitance only when there *are* minority carriers, that is in strong inversion. The high frequency C-V curve does not show a minimum, and the capacitance is constant in strong inversion, according to the maximum depletion layer width.

Deep depletion

Immediately after the DC-bias is switched to strong inversion, there is no inversion layer. Instead, the depletion layer extends further into the substrate than is possible in thermal equilibrium. This state is called *deep depletion*.

2.2 Basic effects of ionizing irradiation in MOS devices

An ionizing particle, traversing the insulator or semiconductor layers of a MOS device, leaves a track of electron–hole pairs along its trajectory. In the gate metal, electrons are excited within the conduction band or even raised to higher bands, but they cool down afterwards, without causing further effects.

In the semiconductor the additional charges may end up on a sensitive node of the circuit, possibly causing two kinds of errors:

- Information, stored on that node, may be changed, causing a soft error that may propagate through the circuit and produce wrong output. A proper *reset* of the circuit will eliminate the error. This sort of event is called *single event upset* (SEU).
- The circuit may enter a state which cannot occur in normal operation. When this involves opening parasitic current paths between power supply terminals, a part of the circuit may be destroyed permanently. This is called *single event latchup* (SEL).

These phenomena are not subject of this thesis. In most cases the generated electron–hole pairs recombine in the semiconductor without leaving any trace.

2.2.1 Trapped oxide charge

The ionization in silicon dioxide is what causes the *total dose effects* in CMOS circuits. Electrons are very mobile, and there are very few electron traps in thermally grown silicon dioxide. The free electrons, that did not recombine immediately, leave the oxide within picoseconds, leaving behind the holes, which drift slowly in the electric field. Eventually, the holes leave the oxide as well, or they get trapped in hole traps near the surface. In the case of the gate oxide of a MOSFET or a MOS capacitor, with a positive bias voltage applied to the gate, the holes move towards the silicon–silicon dioxide interface and a fraction of them gets trapped within a few nanometers from the surface. When irradiation proceeds, a layer of *trapped oxide charge* accumulates.

Electron Spin Resonance (ESR) techniques revealed that the holes are trapped in what is called the E'-center [11, 12, 13]. The E'-center is generated when a hole meets a bridging oxygen vacancy. This is a place where two silicon atoms are bonded together, without an oxygen atom in between. The hole recombines with one of the electrons in the bonding orbital. The remaining electron stays with one of the silicon atoms while the other is lacking one electron, and thus constitutes a fixed positive charge in the oxide.

The transition of the crystal structure, from silicon to silicon dioxide, takes place within one atomic layer. However, the first few nanometers of the oxide are enriched with strained bonds and oxygen vacancies that encourage hole trapping.

Trapped oxide charges are not stable, especially at elevated temperature. The process of removing hole traps, by waiting and/or heating, is called *annealing*.

2.2.2 Interface traps

The second effect of ionizing irradiation in MOS devices is the generation of *interface traps*. These are electronic states *at* the interface between the oxide and the semiconductor. Since these states are in direct contact with the silicon, they can acquire or release an electron, depending on their energy level and the surface potential.

Interface traps can be donors or acceptors, depending on whether they are neutral with or without an electron. It is difficult to distinguish these two natures experimentally. A common working hypothesis is to assume all interface traps above midgap to be acceptors and those below midgap to be donors. In this case all interface traps are neutral when the Fermi energy

coincides with the midgap level at the interface. However, I did not find any conclusive proof of this assumption.

Still, very little is known about the microscopic nature of interface traps. What we know definitely is that there are no distinguished energy levels. The interface trap energy distribution is continuous, throughout the silicon band gap. Their density is expressed by the interface trap level density $D_{it}(\psi_s)$, counting the number of interface traps per unit area and per energy unit, with energy levels near the Fermi level when the surface potential is ψ_s.

Another important property of interface traps is their interaction rate. In thermal equilibrium the electron capture rate and the hole capture rate are the same. Since we will not discuss significant deviations from the equilibrium state, one parameter is sufficient to describe the "speed" of the interface traps. We introduce the *hole capture probability* c_p, which can be viewed as a cross section of an interface state for capturing a hole. The time constant of the interface trap response is

$$\tau_p = \frac{1}{c_p p_S} \tag{2.24}$$

with the density of holes at the interface p_S.

Interface traps are present on any semiconductor surface. Their initial density, in a MOS system, depends on many details of the manufacturing process. Ionizing irradiation creates additional interface traps.

An excellent book about radiation effects in CMOS devices is [14].

2.3 Irradiation response of MOS-transistors

Figs. 2.4 and 2.5 show the layout and cross sections through an NMOS transistor in a standard n-well CMOS circuit.

Silicon dioxide appears not only as the gate oxide of the transistors, but also serves as electrical insulation. The whole area of the silicon chip, apart from the active areas, is covered by a *field oxide*, which is an order of magnitude thicker than the gate oxide.

To make a transistor, a rectangular hole is is left in the field oxide. The gate oxide is grown by thermal oxidation of the silicon surface inside that hole. A polysilicon strip is deposited across the gate oxide with sufficient overlap on the field oxide. Afterwards, the source and drain regions are defined by ion beam implantation, with the field oxide and the polysilicon strip serving as masks.

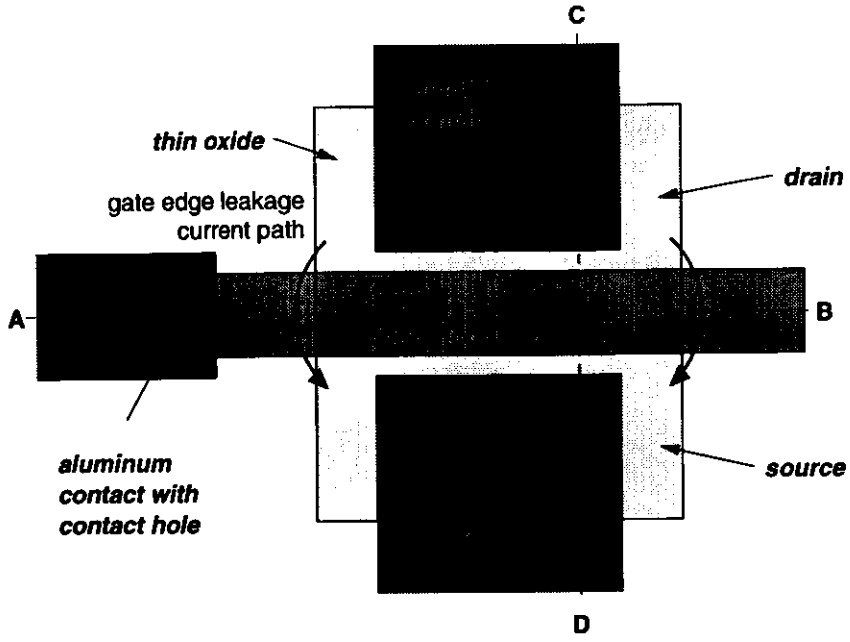


Figure 2.4: Layout of a standard MOS transistor. Cross sections A–B and C–D are shown in Fig. 2.5. A thin gate oxide was grown in a rectangular hole in the field oxide. The polysilicon gate was deposited across the thin oxide. The drain and source were made by ion beam implantation through the thin oxide, with the polysilicon gate and the field oxide serving as masks to define the areas. Aluminum leads are connected to the device contact hole through the intermediate oxide layers. Arrows indicate the gate edge leakage current path, the major failure mechanism of standard CMOS transistors after irradiation.

Source and drain are insulated from the substrate and from each other by *pn* junctions. By applying a voltage between the polysilicon gate and the source contact which exceeds the *threshold voltage* of the transistor, an inversion layer is generated under the gate, which connects the source and the drain. The transistor is switched on.

The characteristics of MOS transistors are changed during irradiation by the accumulation of charges in the gate oxide as well as in field oxide near to the device.

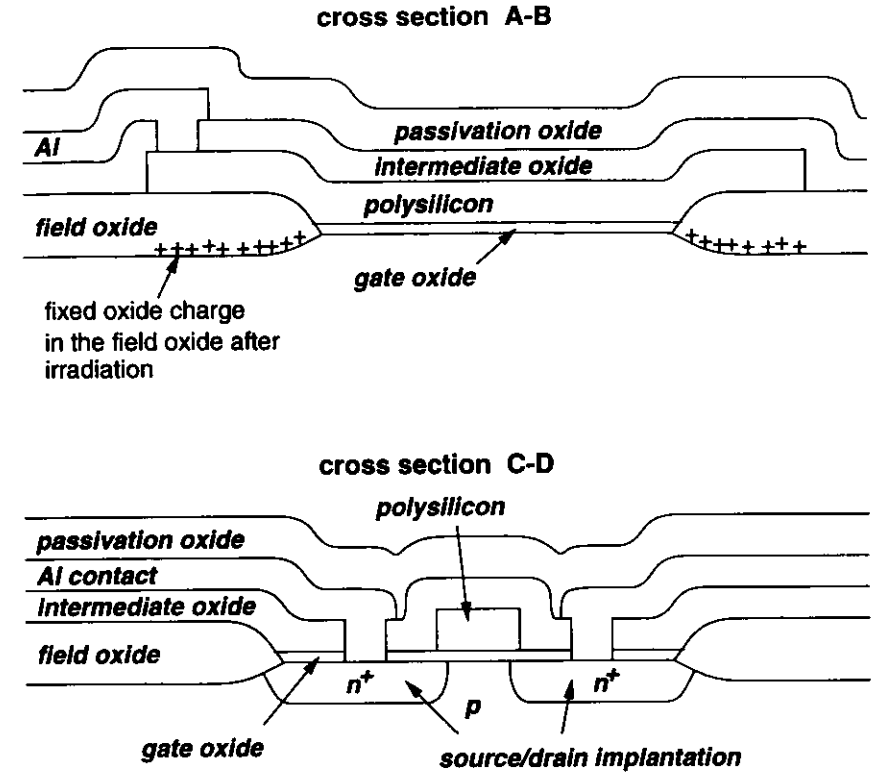


Figure 2.5: Cross sections through the transistor in Fig. 2.4. The intermediate oxide insulates the layer of aluminum leads from the polysilicon layer. The whole integrated circuit is covered by a passivation oxide for protection against contaminations from the environment. The critical place in the field oxide, where fixed oxide charges accumulated during irradiation, is marked by '+' symbols. These charges eventually cause the development of an inversion layer in the semiconductor at the edges of the gate, which form the gate edge leakage current path which connect drain and source of the transistor.

2.3.1 Threshold voltage shift

Any charge that is present in the gate oxide or at the interface of a MOS device causes the gate voltage characteristic of the device to shift, according to the electric field that the charges induce in the oxide.

Positive fixed oxide charges act like an addition to the applied gate voltage, and a less positive gate voltage is required to obtain the same effect, as

without the charges. The presence of fixed oxide charges causes a parallel shift of the characteristics to more negative gate voltages.

The interface trap charge depends on the surface potential. The more positive the surface potential is, the more interface traps fall below the Fermi level, and the more negatively charged is the interface. If the gate voltage is raised, the effect is partly compensated by the capture of electrons in interface traps. Any characteristic becomes broader by introducing more interface traps.

On a MOSFET the gate voltage, at the onset of strong inversion, is called the *threshold voltage* V_{th}. That is the voltage where the transistor switches from *off* to *on* state. The generation of both fixed oxide charges and interface traps will change the threshold voltage. Usually, there are donor traps as well as acceptor traps at the interface. When an n-channel transistor is biased at the threshold, the Fermi level is in the upper part of the bandgap, so that the donors are mostly neutral and the acceptors are negatively charged. The threshold voltage shift, due to positive fixed oxide charges, tends to be compensated by the interface traps. In a PMOS transistor at the threshold, the Fermi level is in the lower half of the bandgap, the donor traps are positively charged and the acceptors are neutral. In this case the interface traps add to the threshold voltage shift of the fixed oxide charges.

2.3.2 Gate edge leakage current

The threshold voltage shift, during irradiation, is approximately proportional to the square of the oxide thickness. The number of generated electron-hole pairs is proportional to the volume of the oxide, and the effect of the holes, which are trapped near the interface, on the threshold voltage, is again proportional to the oxide thickness.

The field oxide is at least an order of magnitude thicker than the gate oxide and, without further precautions, an inversion layer may appear under the field oxide at a low radiation dose. The inversion layer may form the channel of parasitic MOS transistors between normally isolated parts of the circuit, causing leakage currents and other malfunctions. One type of parasitic transistor is present in any standard n-channel transistor described above: on both sides of the gate, where the channel is normally limited by the field oxide, there are gate edge transistors parallel to the main transistor. The current through these transistors, when the main transistor is still turned off, is called *sub-threshold leakage* or *gate edge leakage.*

There are several techniques to avoid gate edge leakage. The method,

which was employed for the radiation hardness improved ZEUS pipeline, is called *thin oxide extension* with *guard bands* (see section 2.4.1 for the transistor layout). The thin oxide extension is the extension of the gate oxide beyond the active area of the transistor, separating the field oxide from the transistor. Guard bands are additional implantations in the field region, to make the initial threshold voltage of parasitic transistors, high enough to prevent inversion, after irradiation. These methods require additional surface area on the chip, which is considered too costly in modern radiation hardened applications.

2.3.3 Mobility degradation

Charged interface traps are scattering centers for minority carrier in an inversion layer of a MOS device. The generation of interface traps leads to degradation of the mobility of electrons in the channel of an n-MOS transistor (See also section 4.2.2).

2.4 Implementation of the pipeline memory circuit

2.4.1 Radiation tolerant transistor layout

The radiation hardness of the circuit was improved by using a transistor layout with *thin oxide extension* for the NMOS transistors, together with a highly p-doped field region, providing guard rings. These means prevent gate edge leakage and parasitic transistor leakage.

The modified layout is drawn schematically in Fig. 2.6, and a photograph of a real example is in Fig. 2.7. The source and drain implantation is no longer limited by the field oxide, instead an additional lithographic mask is required to leave 1 μm of space around the implanted region.

The thin oxide is further extended on both sides of the gate onto a part of the silicon substrate, where the guard band implantation was made before the field oxide was grown. The guard band is a strong p^{++} implantation into the otherwise lightly p doped substrate. The threshold voltage of any parasitic transistor on the guard band is very high, giving an extra safety margin before threshold voltage shift causes malfunction of the circuit.

The field oxide is completely separated from the transistor, thus, eliminating any risk of gate edge leakage.

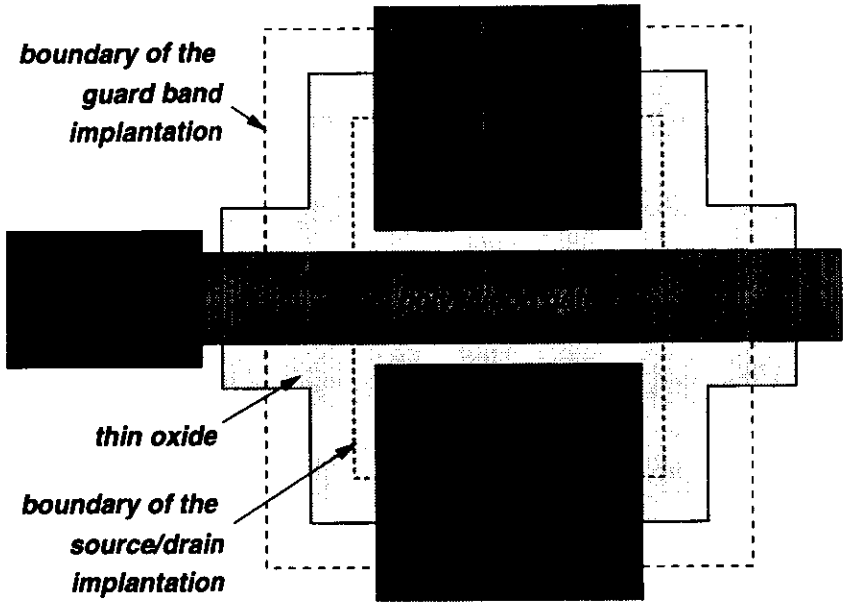


Figure 2.6: Modified transistor layout with thin oxide extension. Compare with the standard layout in Fig. 2.4. The whole field region of the chip is covered by the guard band implantation, except for a safety margin around the active areas. The thin oxide is extended to the guard band region. The source/drain regions are separated from the field oxide by an additional lithographic mask.

2.4.2 The process technology

The memory circuits were produced with a standard 2 μm self aligned polysilicon gate, n-well bulk CMOS process on a 15 μm EPI p-substrate. I will repeat that in slow motion:

standard: The process was not optimized for radiation hardness.

2 μm: The nominal minimum gate length of the transistors is 2 μm. This allows safe operation of CMOS logic with a power supply voltage of 5 V. Since the pipeline runs with a power supply of 10 V, the minimum gate length actually used is 3.5 μm.

self aligned: The gate metal is deposited before the source/drain implantation, and the gate itself was used as a mask for the dopant ions.

polysilicon gate: The gate metal is polycrystalline silicon.

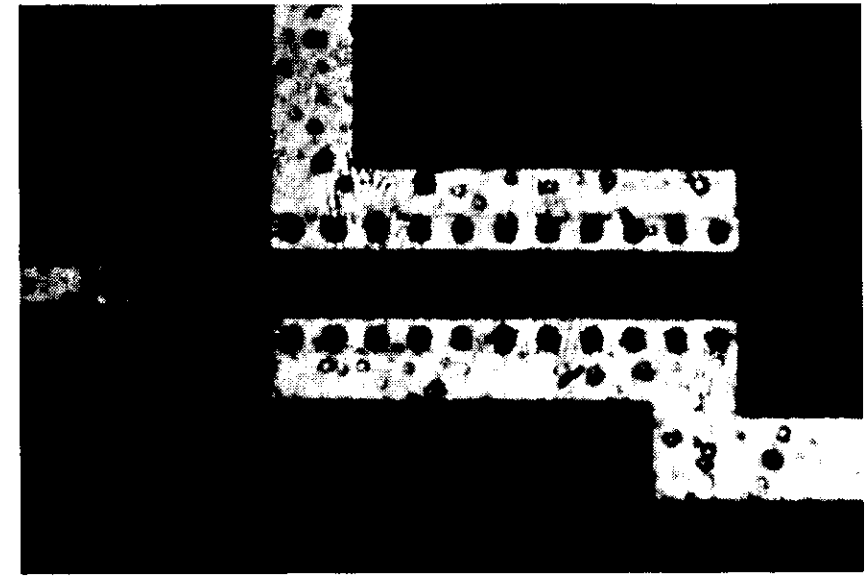


Figure 2.7: Picture of a MOS transistor. The gate length of this transistor is 5 μm, the width is 50 μm. The thin oxide extension is visible on both sides of the gate.

n-well: The NMOS transistors are produced in the p-substrate, while the PMOS transistors need an n-well for their bulk contact.

bulk: The components are insulated by pn-junctions from each other and from the substrate. There is no buried insulation layer in the wafer, as in SOI technologies.

CMOS: Complementary Metal Oxide Semiconductor logic. This type of digital electronics requires both NMOS and PMOS transistors. The advantage is, that the static power consumption is zero, because the logic states are maintained by running one of the transistors in a low impedance state while the other is turned off, preventing any current to flow from the power supply terminals.

15 μm EPI: On top of a silicon wafer with very low resistivity, a 15 μm thin layer of silicon has been deposited, with the same type, but much lower density of dopants, to allow to manufacture proper transistor devices.

p-substrate: The wafer material is p-type silicon. Since the negative power supply of the circuit is distributed through the substrate of the chip, a

Table 2.1: Process parameter.

substrate		$5{\cdot}10^{18}\,\mathrm{cm}^{-3}$	boron
EPI layer	$15\,\mu\mathrm{m}$	$4{\cdot}10^{14}\,\mathrm{cm}^{-3}$	boron
gate oxide	40 nm	wet grown	
field oxide	770 nm	wet grown LOCOS	
gate metal	460 nm	polysilicon	$15\,\Omega\mathrm{cm}$
intermediate oxide	750 nm	PECVD	2 % boron, 4 % phosphorus
passivation oxide	750 nm	PECVD	2 % phosphorus

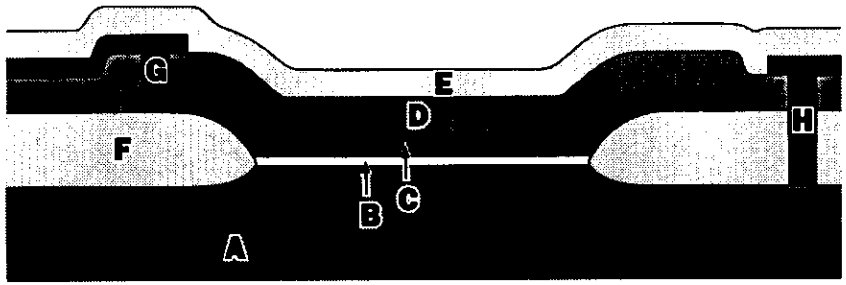


Figure 2.8: Schematic cross section of a MOS capacitor. **A:** EPI substrate, **B:** gate oxide, **C:** polysilicon gate, **D:** intermediate oxide, **E:** passivation oxide, **F:** field oxide, **G:** aluminum contact to the gate, **H:** aluminum contact to the substrate.

low resistivity of the basic wafer material is required.

The information that I got from the manufacturer about the process parameters is compiled in Table 2.1. Fig. 2.8 shows a schematic cross-section through a MOS capacitor, to illustrate all the layers of material, which are created during the processing.

2.4.3 The test insert chip

Both the pipeline memory and the buffer multiplexer circuits where produced together on the same wafers, where the actual masks (reticles) for the lithography covered nine chips: two buffer multiplexer and six pipelines on the outer positions, and the slot in the middle was used to produce a test insert chip.

This test insert features discrete components, various MOS transistors, and five MOS capacitors. Additionally, a pipeline readout amplifier and a

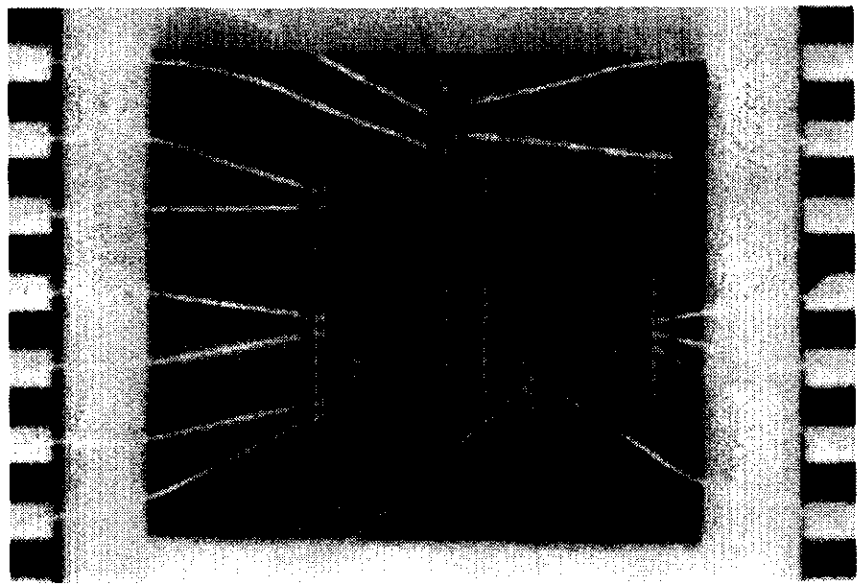


Figure 2.9: Test insert chip, bonded into a DIL 40 package. On the left are three large area capacitors, size 1 × 1 mm, the lower one with an aluminum gate on field oxide, the one in the middle with polysilicon on field oxide, and the upper with polysilicon on gate oxide. The latter is the device, most of the measurements for this thesis were done with. In the upper center there are two smaller capacitors, both polysilicon on gate oxide, but one of them was masked during the implantation for threshold voltage adjustment. On the right and lower center are contacts to two NMOS transistors. The bright vertical columns are the aluminum bonding pads, the devices are located in between. The structures on the bottom are amplifiers copied from part of the pipeline circuit.

digital input signal comparator are provided.

The test inserts were produced to monitor the production process, and to test the discrete components of the circuit for their fitness in the application, especially the radiation hardness. The surface of the test insert chip is covered mostly with aluminum bonding pads, with a couple of transistors in between. Additionally, there are five large capacitors and two amplifier circuits (see Fig. 2.9).

The Fraunhofer Institut kindly agreed to bond 20 of the chips into 40-pin DIL (*Dual In Line*) packages, with contacts to all the capacitors and additionally to two large NMOS transistors, sized $50/5\,\mu\mathrm{m}$ and $50/50\,\mu\mathrm{m}$ (Width/Length).

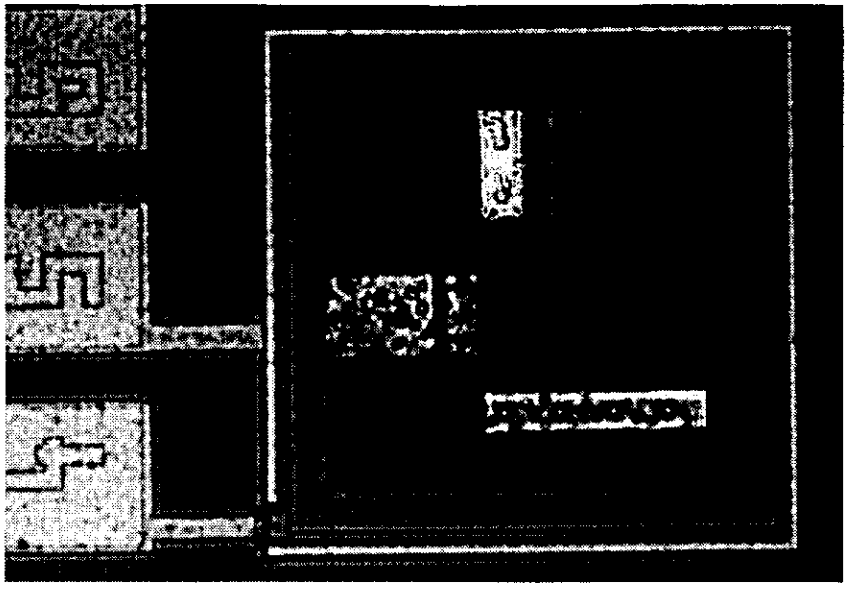


Figure 2.10: Layout of a capacitor. On the left are bonding pads with aluminum leads to the polysilicon gate (4) and to a ring of contacts to the silicon bulk all around the capacitor area (5). The size of the gate oxide area is $300 \times 300\,\mu$m. A close look at the capacitors edge reveals the border of the field oxide a small distance into the polysilicon, and on the bonding pads, the boundary of the hole in the passivation oxide for bonding is visible. The insert is a magnified view on the gate contact region. There are three contact holes from the aluminum layer through the intermediate oxide to the polysilicon gate. Similar holes can be seen from the bulk contact ring through the intermediate and field oxides to the silicon bulk.

Table 2.2 summarizes the parameters of the five MOS capacitors on the test insert. All of them are made on the p substrate, different to the capacitors in the storage cells of the memory circuits, which are made on n-wells. The area of the capacitors is either 1×1 mm or $300 \times 300\,\mu$m. The capacitors differ in the oxide dielectric, which is either the field oxide or the gate oxide. The processing of the gate oxide capacitors is exactly the same as for the NMOS transistors in the CMOS circuit, including the threshold voltage adjustment implantation. One of the smaller gate oxide capacitors was masked during this implantation.

For this thesis, measurements of one large gate oxide capacitor were used. The field oxide capacitors require high gate voltages, because of the guard band implantation. The smaller capacitors had a higher signal to noise ration.

Table 2.2: The capacitors on the test insert.

gate	oxide		size	substrate
polysilicon	gate	40 nm	$1\times1\,\text{mm}^2$	$N_A \approx 3.5{\cdot}10^{16}\,\text{cm}^{-3}$
polysilicon	gate	40 nm	$0.3\times0.3\,\text{mm}^2$	$N_A \approx 3.5{\cdot}10^{16}\,\text{cm}^{-3}$
polysilicon	gate	40 nm	$0.3\times0.3\,\text{mm}^2$	$N_A \approx 8{\cdot}10^{14}\,\text{cm}^{-3}$
polysilicon	field	770 nm	$1\times1\,\text{mm}^2$	$N_A \approx 8{\cdot}10^{14}\,\text{cm}^{-3}$
aluminum	field	770 nm	$1\times1\,\text{mm}^2$	$N_A \approx 8{\cdot}10^{14}\,\text{cm}^{-3}$

Fig. 2.10 is a picture of one of the smaller ($300 \times 300\,\mu$m) capacitors. The layout of the capacitor that was actually used is identical.

A picture of the NMOS transistor on the test insert, which was used for the measurements, is shown in Fig. 2.11.

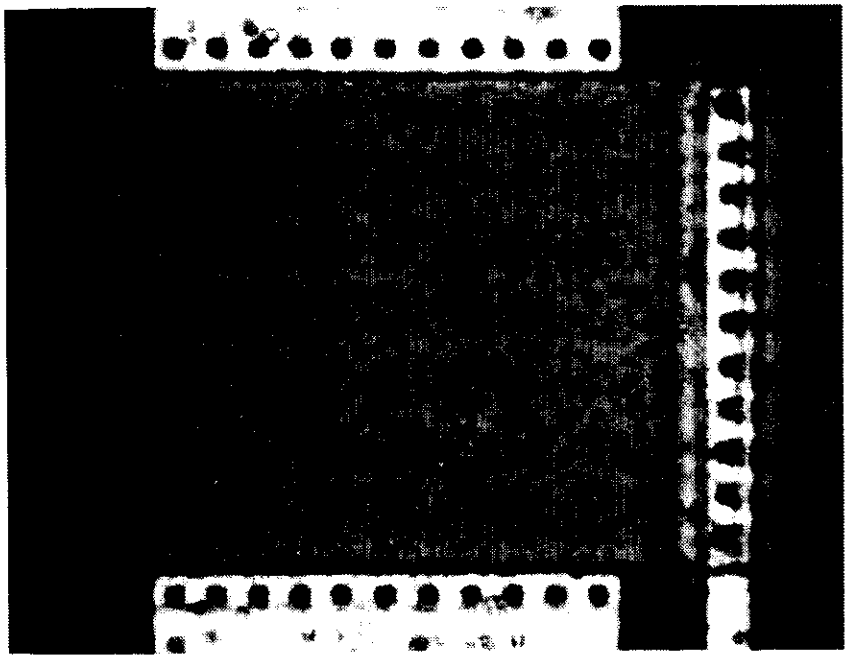


Figure 2.11: Picture of the NMOS transistor which was used for the measurements. The gate length and the width of this square transistor is $50\,\mu\mathrm{m}$.

Chapter 3

Irradiation and measurement procedures

When the first pipeline memory and buffer/multiplexer circuits became available in 1989, special test equipment was built to measure the performance of these samples [6, 9, 15]. Software tools, measurement procedures, and analysis programs were developed. A huge amount of data were generated, analyzed, stored on floppy disks, lost and found, and became finally unreadable, because the last disk drive that could read those floppy disks, died.

To produce data for this thesis, I decided to repeat an irradiation experiment to get a well documented data set. This is the reason why all pipeline memory data, used here, originates from one single sample. The results agree well with old data from the first radiation hardened pipelines.

This pipeline chip was produced by the Fraunhofer Institute in Duisburg, Germany, batch N° 300. This was one of the last batches run with the final, radiation hardness improved design. The chip was housed in a plastic chip carrier package.

3.1 Irradiation

In addition to the pipeline memory circuit, nine test inserts bonded into DIL 40 packages, were irradiated, with different bias conditions on the devices, and with different final doses.

3.1.1 Source

The samples were irradiated one by one, in front of a ^{137}Cs γ-source, borrowed from the DESY radiation safety group.

The distance of the chip to the source was 15 mm. The position of the socket was reproducible with an accuracy of ≈ 0.5 mm.

To measure the doserate at the place of the chip, one test insert sample was opened, the chip was partly removed and replaced by two small cylindrical glass dosimeters. One of them (N° 1) placed along the bottom edge in Fig. 2.9, the other one along the top (N° 2). A third dosimeter was placed on top of the package cover, about 1 mm above the chip surface, parallel to the other two. The whole thing was then irradiated during 3.78 hours, in the same position as all the real samples.

Table 3.1: Doserates obtained from glass dosimeters. The irradiation time was 3.78 h. A correction factor was applied to dosimeter No. 3, because it was displaced about 1 mm towards the source.

No.	dose	corr.	doserate
1	7.5 krad	1	1.98 krad/h
2	6.0 krad	1	1.59 krad/h
3	7.6 krad	0.87	1.75 krad/h
			1.77 ± 0.16 krad/h

The dosimeters were provided and afterwards analyzed by the radiation safety group *(Strahlenschutzabteilung)* of DESY. Table 3.1 lists the results. The dose from the third dosimeter was corrected for the fact that it was placed nearer to the source by a factor $(14/15)^2 = 0.87$. The best estimate for the doserate on the surface of the chip is

$$\dot{D} = 1.77 \pm 0.16 \,\text{krad/h}.$$

3.1.2 Test insert irradiation

The test insert devices were placed into a socket, with all bulk, source, and drain contacts connected to ground and all gates connected to a power supply, to maintain a constant gate bias voltage during irradiation. Irradiations with zero bias were done with all contacts connected.

Nine samples were irradiated. Table 3.2 summarizes the obtained total dose and the bias conditions during irradiation. Two series of samples were

irradiated for 66 h and 120 h (117 krad and 212 krad) respectively, and two more chips were irradiated at $V_{bias} = +5\,V$.

Table 3.2: Total dose and irradiation bias of the samples.

irr. time:	16 h	48 h	66 h	120 h
dose:	28 krad	85 krad	117 krad	212 krad
V_{bias}				
−5 V			N° 07	N° 09
0 V			N° 10	N° 15
+5 V	N° 14	N° 13	N° 05	N° 11
+10 V			N° 16	

3.1.3 Pipeline memory irradiation

The pipeline chip was placed in a test socket in front of the source, in roughly (±1 mm) the same position where the test inserts were irradiated. The doserate was, therefore, assumed to be the same in both cases: $\dot{D} = 1.8\,krad/h$.

The test socket was connected to a stand-alone pipeline clock generator, which produces the control signals to run complete WRITE/READ cycles at about half the design frequency. The generator was configured to repeat a cycle of 127 write-clocks at 5 MHz and 8 read clocks at 312.5 kHz, which gives a WRITE/READ clock ratio of 50 %.

The power supply was set to the nominal voltage of ±5 V. The reference voltage V_{REF} was connected to the positive power supply, via a resistor $R_{REF} = 24\,k\Omega$.

The current into both the analog and the digital power supply nodes, as well as the voltage across R_{REF}, was measured with a digital multimeter whenever the chip was accessed.

The input voltage off the four pipeline channels was set to −2 V during the first two days of irradiation, (87 krad). Afterwards channels 3 and 4 were kept floating. This gives four different conditions in the storage cells, because nine cells got selected during READ-mode and were discharged during part of the cycle.

- Channel 1 and 2, cells not read out: were constantly charged with −2 V.

- Channel 1 and 2, cells selected during READ: were charged with −2 V and discharged between 6 % and 50 % of the time during the cycle.
- Channel 3 and 4, cells not read out: were floating.
- Channel 3 and 4, cells selected during READ: were discharged during the whole cycle.

3.2 Measurements with the pipeline memory

The measurement of the pipelines performance parameters was done with a selfmade test equipment. The hardware consists of five parts:

- A board with a socket for the *device under test* (DUT), and some auxiliary electronics, like logic converters, amplifiers, and power supply regulators, which needs to be placed next to the DUT.
- A selfmade digital signal generator, in fact a small programmable processor, which generates the pipeline control clock with high accuracy at the full nominal speed. The generator also produces two analog voltages used to set the pipeline input voltage and the bias reference current I_{REF}.
- An *analog/digital-converter* (ADC) card AD 9500 D within a VME crate. This ADC is used to read the pipeline output voltage as well as several analog parameters, like supply and reference current and voltages, and the pipeline input voltage. The input voltage range of the ADC is ±5 V, which is converted to a twelve bit number. One *least significant bit* (LSB) corresponds to 2.5 mV.
- A digital parallel input/output unit MVME 201 in the VME crate, used to program and control the signal generator.
- A micro processor board MVME 147 running the real-time multiuser/multitasking operating system OS 9. This computer is equipped with a harddisk drive and is connected to the DESY *local area network* (LAN).

The program which is running on the VME computer during the measurements performs several tasks:

- Commands are read from the keyboard and from command files, which specify the sequence of measurements to be performed.

- The ADC is configured.
- A program is loaded into the signal generator and started.
- Digitized data is read from the ADC card. Some handshake between the CPU and the signal generator is necessary for this.
- After the measurements are completed, the data is written into binary data files on the hard-disk.

An analog circuit, as complex as the ZEUS pipeline, has a large number of performance parameters. To measure a comprehensive subset of them, I ran a standard procedure using several command scripts. This is roughly what was measured:

- The output voltage of the pipeline at various DC-input voltages, covering more than the nominal input voltage range, was measured with high precision.
- Some special measurements which involved running the pipeline in modes that are not encountered in normal operation:
  - Reading empty cells, that is, doing a complete turn of READ-clocks, thereby discharging all cells, and then continue to read and digitize the output.
  - Reading the output while keeping the circuit in WRITE-mode.
  - Reading the output with the RESET-switch of the readout amplifiers closed.
- The output curve of the readout amplifiers versus time, was scanned by shifting the trigger pulse for the ADC relative to the active CLK-edge in steps of 100 ns. This is done at the nominal full scale input voltage of $V_{IN} = -2\,V$ and with several settings of the reference current I_{REF}.
- The response of the pipeline when the charges are stored for an enhanced period of time in the storage cells. This is accomplished by stopping the clocks after switching from WRITE into READ-mode for a period of either 10 ms or 1 s, before continuing with the readout. For proper comparisons there is always a measurement done with exactly the same settings except for the delay. The input voltage was set to either zero or to $-2\,V$.

Table 3.3: Definition of the columns in the pipeline data files.

1. Measurement id-number. This is the approximate number of hours the chip was irradiated so far.
2. Channel number (0..3).
3. Cell number (0..57).
4. Cell gain $g = (V_{OUT}(0\,V) - V_{OUT}(-2\,V))/2\,V$.
5. Difference of the cell gain to the channel average.
6. Cell pedestal $p = V_{OUT}(0\,V)$.
7. Difference of the cell pedestal to the channel average.
8. Cell nonlinearity. Maximal deviation of the output voltage from the line defined by g and p, measured in fractions of the input voltage.
9. Output amplifier baseline, output voltage measured after closing the RESET-switch after reading this cell. Should be the same for all cells, plus noise.
10. Empty cell output, read in the second turn, after clocking through all cells in read mode at least once.
11. Output voltage read in WRITE mode, while applying RESET-pulses as during READ-cycles. Should be the same for all cells, plus noise.
12. Output voltage shift after 10 ms storage time, input voltage set to $V_{IN} = -2\,V$,
13. after 10 ms, with the input voltage $V_{IN} = 0\,V$,
14. after storing the charge for one second, $V_{IN} = -2\,V$,
15. after one second, with $V_{IN} = 0\,V$.
16. Readout settling error. Difference of the reading at the nominal readout settling time of 900 ns after the READ-clock edge compared to the reading after 3 μs, measured with nominal full scale input $V_{IN} = -2\,V$.
17. Reset speed. Output voltage read about 300 ns after applying the RESET-pulse, again at $V_{IN} = -2\,V$.
18. ...Some RMS values of the readings during measurement. Because the resolution of the ADC is far worse than the noise levels in the pipeline, these numbers are of little use.

Only a subset of the data was used for analysis. The binary data files were run through an analysis program, which generates an output file with 21 columns of numbers, one line of output for each storage cell in the pipeline circuit. See Table 3.3 for the meaning of those columns.

3.2.1 Dataset

The measurement procedure was run 13 times:

- two times before irradiation,

- eight times after 21, 49, 70, 96, 147, 189, 239, and 302 hours of irradiation, and
- three times, 6, 30, and 55 hours after the end of irradiation, keeping the pipeline in the irradiation setup under power and clocks in the mean time.

The total dose after 302 hours of irradiation was 535 krad.

Additionally, the power consumption in the irradiation setup was measured before irradiation and whenever the chip was taken out to do the main measurements. Plus once, half an hour after the irradiation was finished, the main measurement was done and the chip was reinserted into the irradiation socket for annealing. The measured quantities were:

- the analog supply current I_{DDA},
- the digital supply current I_{DDD} while the clock-pattern was applied,
- the digital supply current with the clocks stopped in READ-mode,
- the digital supply current with the clocks stopped in WRITE-mode, and
- the bias reference current I_{REF}.

3.3 Measurements on MOS transistors

Due to geometrical constraints, only two of the transistors on the test insert got its contacts bonded to pins of the DIL-40 package. I choose the largest available NMOS transistor, with a width/length of $50/50\,\mu m^2$. This n-channel device is directly comparable to the p-substrate capacitors. Due to the large size "surface effects" from the channel edges are reduced.

Measurements were done for two reasons:

1. To study parameter changes during/after irradiation.
2. To monitor the irradiation procedure, to detect possible errors in the setup.

For this purpose it is sufficient to measure the drain current versus gate-source voltage characteristic (I_d–V_{gs}) in the linear mode of the transistor.

Table 3.4: Irradiated transistor measurements. The table includes the sample number, the irradiation bias and the γ-dose where measurements were performed during irradiation including the final dose. A further measurement was done six month after irradiation.

N°	V_{bias}	dose [krad]
05	5 V	0, 35, 78, 117
07	−5 V	0, 42, 89, 117
09	−5 V	0, 85, 156, 212
10	0 V	0, 39, 71, 117
11	5 V	0, 212
13	5 V	0, 48, 85
14	5 V	0, 28
15	0 V	0, 133, 212
16	10 V	0, 32, 64, 117

3.3.1 Measurement setup

The measurement was done with a component analyzer HP 4145 B, controlled via a VME laboratory computer. The sample was connected to four source/measurement leads of the component analyzer with short wires clamped to pins, inside an electrically sealed box which was supplied for this purpose with the instrument. The HP 4145 B was programmed to

- set the bulk-source voltage $V_{bs} = 0\,V$,
- measure two characteristics, with the drain-source voltage set to $V_{ds} = 100\,mV$ and 3 V. With $V_{ds} = 100\,mV$ the transistor is in the linear region, while $V_{ds} = 3\,V$ was chosen to be well in the saturated region without stressing the transistor with high oxide fields,
- sweep the gate-source voltage from $V_{gs} = -3\,V$ to 2 V in steps of 10 mV,
- read the drain current I_d, repeating each reading 256 times to compute the average.

Running this setup results in a data file, containing three columns of numbers (V_{gs}, V_{ds}, I_d), a total of 1002 lines, 501 each for the two characteristics.

3.3.2 Dataset

The I_d–V_{gs} characteristics of the samples were measured:

- before irradiation,
- several times in between, interrupting the irradiation for this purpose,
- immediately after irradiation, and
- about six months later, after the samples were shipped to Tel Aviv University, where measurements on the capacitors were performed, put aside (stored at room temperature), and shipped back to DESY.

All data files were transfered to a VAX computer, where they were visually checked using the program PAW (*Physics Analysis Workstation*) developed at CERN. No hints of trouble were observed, except for the fact that a second transistor, which was supposed to be contacted to pins and was measured routinely, gave consistently distorted characteristics on all samples. This second transistor features a ten times shorter channel length of 5 μm, was intended as a backup, and its data was not used further.

Table 3.4 is a list of all measurements, performed on the irradiated samples.

3.4 Measurements on MOS capacitors

There are two kinds of methods, using either transients after the MOS system was set into a non-equilibrium state, or the response to small signal deviations from equilibrium. Transient methods require large area capacitors to obtain reasonable signal amplitudes, while admittance measurements may be more sensitive.

I used only small signal methods to study radiation effects on the MOS capacitors on the test insert. For this purpose I measured the admittance of the capacitors as a function of the signal frequency and the DC-bias.

Nine test inserts were irradiated during February 1995. The measurement procedure described in this section was applied before irradiation to five of these samples. After the irradiation at DESY, the samples where shipped back to Tel Aviv, and the measurements on the capacitors were repeated on all irradiated samples. All three capacitors with gate oxide dielectrics were measured but the data, obtained from the capacitors with the smaller area of 300 x 300 μm, were not studied in detail, because the signal to noise ratio was too bad.

3.4.1 Measurement setup

Measurements were performed with a low frequency impedance analyzer HP 4192A, where *low frequency* means 5 Hz to 13 MHz. A program, running on a personal computer, did the setup of the instrument and received the data to write them to a disk file.

The samples were clamped with short wires, about 7 cm long, to the test leads of the instrument.

The DC-bias range was individually adjusted to the samples irradiation condition, to cover the whole region between flatbands and inversion, in small steps, 25 mV for most measurements. The measurements before irradiation were done with fewer points, in steps of 50 mV.

The admittance was measured, by superimposing a harmonic signal on the DC-bias. The oscillator amplitude was set to 100 mV.

For each selected DC-bias point the frequency range from 100 Hz to 10 MHz was scanned in logarithmic steps, 20 measurements per frequency decade.

The instrument was switched to *average mode*, causing every data point to be measured several times and to compute the average.

A typical run, covering a bias range of 4 V, resulted in 16000 data points, each giving one line in the output data file, with four columns: bias, frequency, capacitance and conductance. To run this procedure takes about six hours for each capacitor.

Chapter 4

Radiation effects in NMOS-transistors

MOS transistors are not the most basic devices to study radiation effects, since they feature four contacts: in addition to the gate and bulk as in a basic MOS structure there are the source and drain contacts. When a voltage is applied to these contacts, the surface potential varies along the channel, and the semiconductor is no longer in thermal equilibrium. Nevertheless, there are several reasons to study transistors:

- Transistors are what an integrated circuit is made of.
- Transistors occupy a small surface area on a chip.
- There are fast, simple, and well established measurement and analysis procedures available, using static transistor characteristics.

The most important parameter of a MOSFET, that is affected by radiation is the threshold voltage, as it defines the gate voltage required to switch the transistor from the high impedance off state to the low impedance on state. The threshold voltage shift is a result of both fixed oxide charge and interface trap generation.

Another affected parameter is the carrier mobility in the transistor channel, which has an influence on the switching speed. The mobility is affected by interface traps only [16]. Switching speed is of little concern in the pipeline memories, because they are used at frequencies well below the limits of the digital part of the circuit.

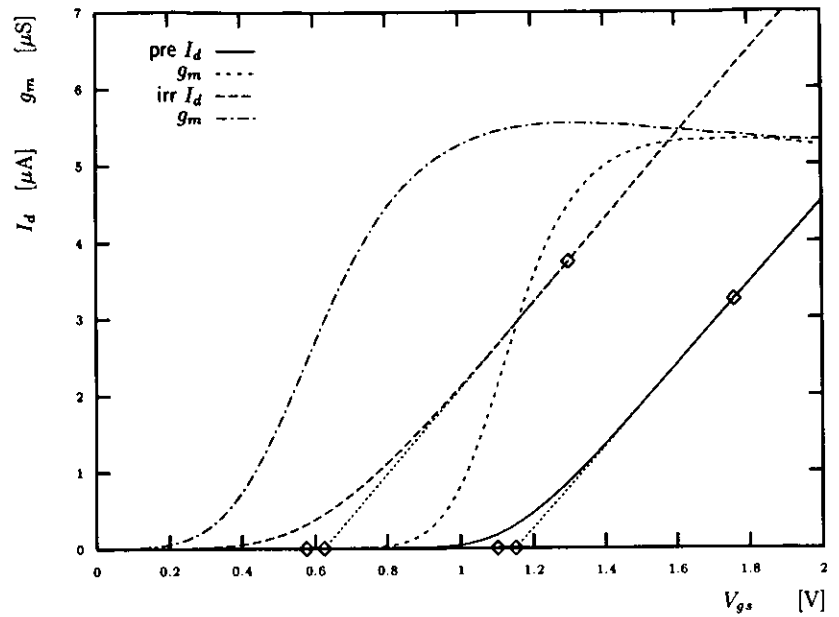


Figure 4.1: I_d-V_{gs} characteristics, to illustrate the definition of the threshold voltage V_{th} of a MOS transistor. The data is from sample No. 13, non-irradiated and irradiated with 85 krad at $V_{\text{bias}} = +5\,\text{V}$.

4.1 Threshold voltage shift

The first thing to do is to choose a method to measure the threshold voltage V_{th}. Since I want to compare with results obtained from MOS capacitors, a method, using characteristics in the linear region, is better suited, compared to running the transistor in the saturated region, which involves substantial inhomogeneities and deviation from the thermal equilibrium.

4.1.1 Practical definition of V_{th}

The theoretical definition of the threshold voltage is the gate bias, at the onset of strong inversion. What we need is a practical definition. One choice is to define the threshold voltage V_{th} as follows:

We use the I_d-V_{gs} characteristic in the linear region.

The static transconductance g_m is the slope of this characteristic, obtained

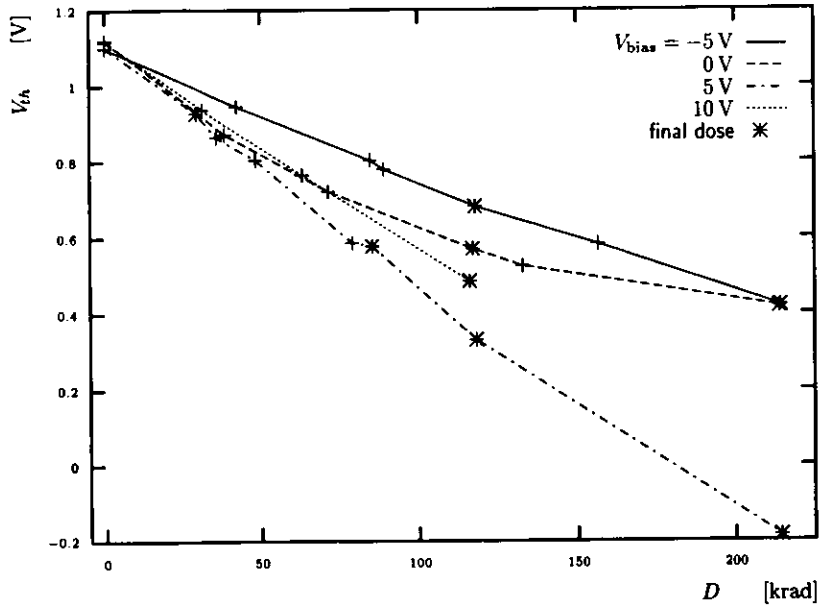


Figure 4.2: Threshold voltage vs irradiation dose.

by numerical differentiation of the measured I_d–V_{gs} characteristic.

$$g_m = \frac{\mathrm{d}I_d}{\mathrm{d}V_{gs}}. \tag{4.1}$$

The threshold voltage is obtained with the following procedure:

1. Find the gate voltage $V_{gs}^{(\max)}$ where the static transconductance reaches the maximum $g_m^{(\max)}$.
2. The value of the drain current at this point is $I_d^{(\max)}$.
3. Draw the tangent to the I_d–V_{gs} curve at that point.
4. Take the intersection of that tangent with the gate voltage axis, and subtract half of the drain–source voltage V_{ds} to get the threshold voltage V_{th}.

This is equivalent to the formula

$$V_{th} = V_{gs}^{(\max)} - \frac{I_d^{(\max)}}{g_m^{(\max)}} - \frac{V_{ds}}{2}. \tag{4.2}$$

Fig. 4.1 illustrates the procedure.

4.1.2 Bias dependence

Every characteristic, measured during the irradiation procedures, gives one data point V_{th} vs dose in Fig. 4.2, with lines connecting data points obtained with the same bias during irradiation.

As long as the electric field in the oxide is not too strong, the threshold voltage shift is expected to be the faster, the more positive the field is from the gate to the substrate. A negative field pulls the holes away from the oxide–substrate interface, whereas a positive field pushes the holes to the interface, where a larger fraction of them gets trapped.

This is confirmed by the data: the initial shift rate is -3.6, -5.3, and $-6.4\,\mathrm{mV/krad}$ for the samples irradiated at $-5\,\mathrm{V}$, $0\,\mathrm{V}$ and $5\,\mathrm{V}$, respectively.

On the transistor, irradiated with 10 V across the gate oxide, the threshold voltage shifts less: $-5.6\,\mathrm{mV/krad}$ compared to $-6.4\,\mathrm{mV/krad}$ at 5 V. The reason could be that the holes traverse the oxide too fast to get trapped.

4.1.3 Dose dependence

Except for the samples irradiated at zero bias, the threshold voltage shift proceeds at an almost constant rate, up the highest applied dose of 212 krad.

Samples, that were irradiated with zero bias, exhibit almost the same initial threshold voltage shift as those with $V_{gs} = 5\,\mathrm{V}$. However, the rate decreases rapidly with increasing dose and seems to saturate after a shift of $\Delta V_{th} \approx -0.7\,\mathrm{V}$ at about 200 krad.

There are two possible reasons for this:

1. Compensation of the oxide trapped charges by interface traps. We will later see that the interface trap generation is most prominent during irradiation with zero bias. But this cannot account for the full magnitude of the effect.
2. Repulsion of the holes by the accumulated fixed oxide charge layer. The externally applied voltage is zero, but the accumulation of trapped holes in the vicinity of the oxide–substrate interface causes substantial internal fields, which drive the holes approaching from both directions away from this area.

At an irradiation dose of 212 krad the total threshold voltage shift, at zero bias, becomes comparable to the shift obtained with an irradiation bias of $-5\,\mathrm{V}$. This indicates that a substantial contribution of the threshold voltage shift, under negative bias, may originate from processes at or near the interface.

4.2 Interface trap generation

There are several methods to obtain information about interface trap generation from transistor characteristics. This section presents two methods using two, completely different, effects:

1. The sub-threshold slope method measures the change of the interface charge, while changing the gate bias. This gives the interface trap level density in weak inversion.

2. The transconductance method measures the mobility degradation in the channel, due to interface trap charges. This gives the density of those interface traps which are charged in inversion.

4.2.1 The sub-threshold slope method

While increasing the gate voltage of a MOS structure, the Fermi level at the interface rises in relation to the silicon band levels. All interface traps crossed by the Fermi level, acquire an electron. The total amount of charge at the interface becomes more negative, compensating part of the rise of the gate voltage. The consequence is, that any function of the gate bias becomes broader in the presence of interface traps.

By measuring the slope of the sub-threshold current, we can obtain the increase of the interface trap level density in the upper part of the silicon band gap (for NMOS transistors).

The sub-threshold drain current is essentially proportional to the minority carrier concentration in the channel region, which depends roughly exponentially on the surface potential or the gate voltage V_{gs}. We define the sub-threshold slope S as

$$S = \frac{\mathrm{d}V_{gs}}{\mathrm{d}(\ln I_d)} \tag{4.3}$$

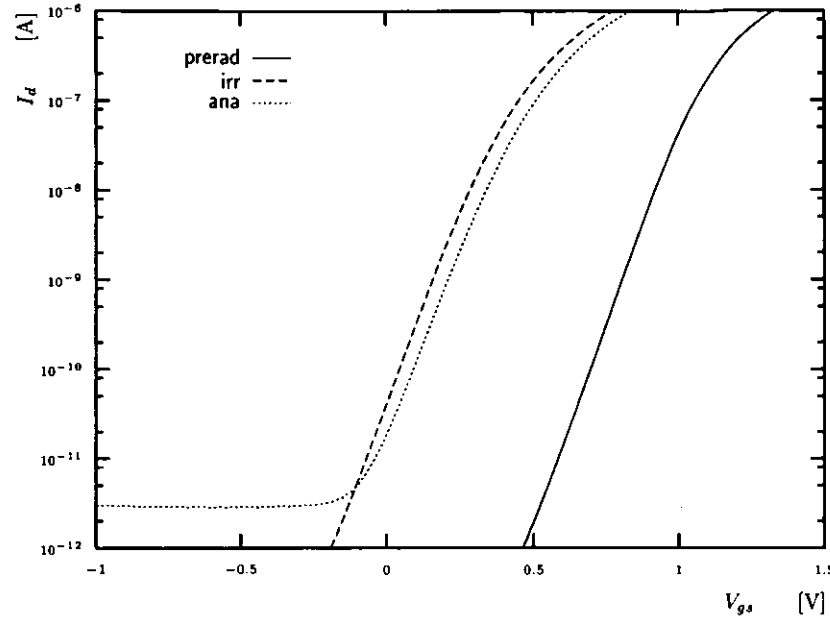


Figure 4.3: I_d–V_{gs} characteristics of sample N° 13, before and after irradiation with 85 krad, and six month later.

A good approximation which includes interface traps is

$$S = \frac{kT}{q}\left(1 + \frac{C_S}{C_{ox}} + \frac{q^2 D_{it}}{C_{ox}}\right) \tag{4.4}$$

[14, section 1.2.3.5].

The radiation induced increase of the interface trap level density D_{it} is obtained by comparing the slope after irradiation $S^{(\mathrm{irr})}$ with the value $S^{(\mathrm{pre})}$ before irradiation

$$\Delta D_{it} = \frac{C_{ox}}{qkT}(S^{(\mathrm{irr})} - S^{(\mathrm{pre})}). \tag{4.5}$$

Fig. 4.3 shows a measured C-V characteristic from sample N° 13, irradiated with $V_{\mathrm{bias}} = 5\,\mathrm{V}$ to 85 krad. The sub-threshold slope S was estimated by a linear regression to the logarithm of the drain current I_d between 10^{-10} and $10^{-8}\,\mathrm{A}$. The results are plotted in Fig. 4.4 using the curves, measured immediately after the samples reached the final dose, and Fig. 4.5 for data measured six months later. Both are compared to the state before irradiation.

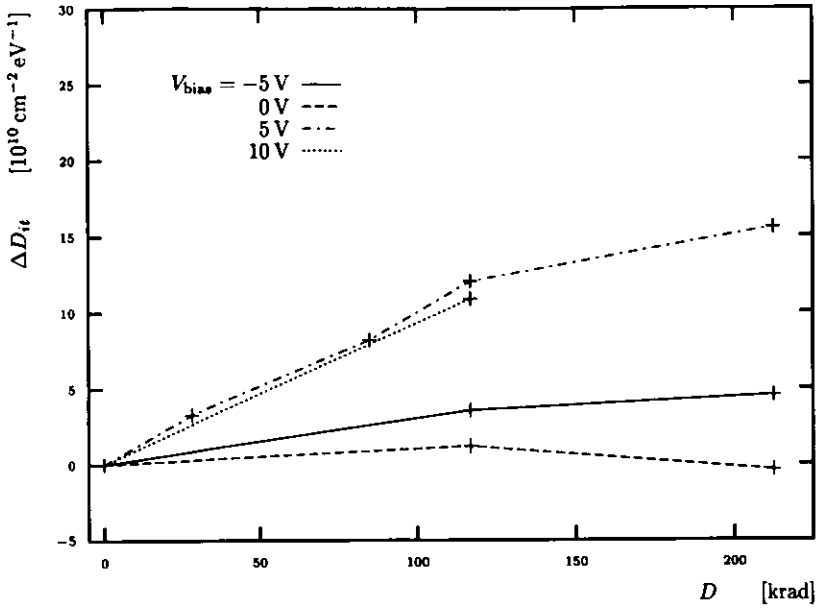


Figure 4.4: Interface trap level density in the upper part of the bandgap obtained from the sub-threshold slope method, immediately after irradiation, as a function of the total dose.

Immediately after irradiation, in this context, means about ten to twenty minutes after the source was closed. This time was needed to take the sample out of the source and take it to the measurement setup. The measurement itself took several minutes, and the irradiation took several days.

A substantial increase of the interface trap density during the six month period of shelf annealing, is observed.

Schwank et. al. [17, 18] found three components of interface trap buildup in polysilicon devices:

- An immediate component, within the first second following irradiation pulses,
- A delayed component, which lasts between seconds to some thousands of seconds, and
- after a delay of up to several month, a latent buildup sets on, which further increases the interface trap density.

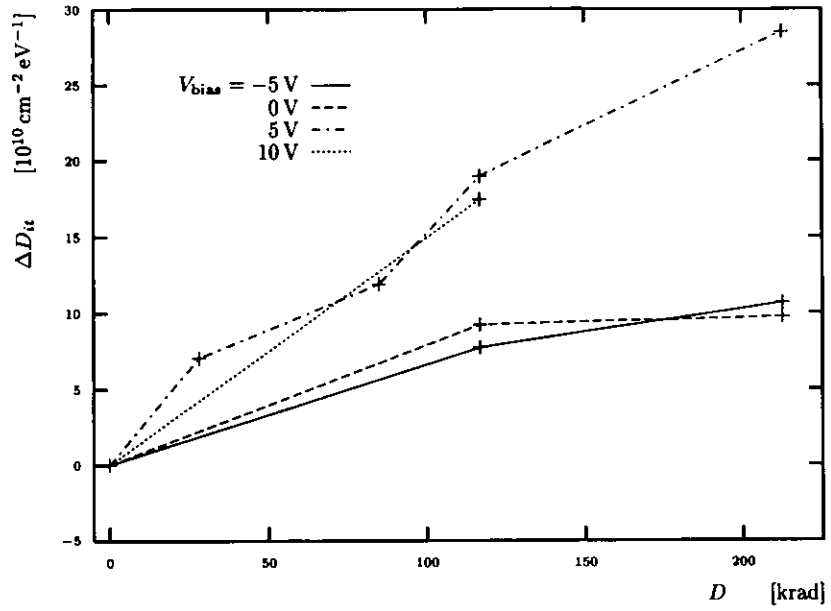


Figure 4.5: Interface trap level density in the upper part of the bandgap obtained from the sub-threshold slope method, six months after irradiation, compared to before irradiation.

The observed increase might be the result of this latent interface trap buildup.

4.2.2 Static transconductance degradation

The presence of charged centers at the interface reduces the mobility of minority carriers in the inversion layer channel of a MOSFET.

There is an empirical model of how the minority carrier mobility μ in the channel degrades, by introducing interface traps

$$\frac{\mu^{(irr)}}{\mu^{(pre)}} = \frac{1}{1 + \alpha \Delta N_{it}} \tag{4.6}$$

where the parameter α was fitted to data obtained with all kinds of devices, giving $\alpha = 8{\cdot}10^{-13}\,cm^2$ [16].

Assuming that the static transconductance g_m depends linearly on the mobility, I used the peak of g_m in the I_d–V_{gs} characteristic (see Fig. 4.1) as

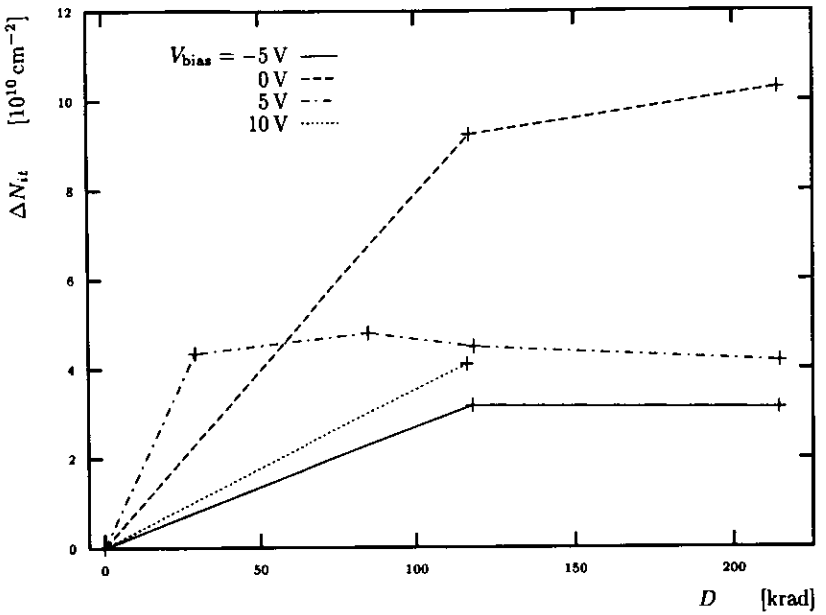


Figure 4.6: Interface trap surface density obtained from the transconductance. This analysis was done with data taken after six month after irradiation.

a measure for μ to estimate ΔN_{it}

$$\Delta N_{it} = \frac{\frac{g_{m,pre}^{(max)}}{g_{m,irr}^{(max)}} - 1}{\alpha}. \tag{4.7}$$

A close look at Fig. 4.1 reveals that g_m did not decrease during irradiation, in fact, most samples exhibit a slight increase. Only after shelf annealing, the static transconductance showed a substantial decrease, which translates into interface trap densities shown in Fig. 4.6.

An interpretation of this behavior is, that the immediate and delayed components create mostly donor type interface traps, whereas the latent interface trap buildup create acceptor type traps, the latter are charged while the former are neutral, in an NMOS transistor operated beyond threshold.

The interface trap density generation was largest when irradiation was done with zero bias. This is consistent with results from MOS capacitors in Chapter 5.

Chapter 5

Radiation effects in MOS capacitors

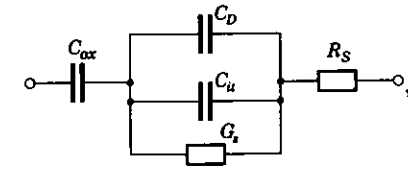
MOS capacitors are ideal devices to study the properties of MOS systems and the silicon dioxide-silicon interface, in particular. The two main reasons are:

- Capacitors are easy to fabricate in large size to obtain reasonable signal amplitudes.
- The semiconductor, up to and including the interface, is in thermal equilibrium when a DC-bias is applied. Perturbative *small signal* models are comparatively well understood.

The measured admittance data, used to obtain the properties of the capacitors, like the series resistance of the substrate R_S, the oxide capacitance C_{ox} and the impurity concentration of the semiconductor N_A. The results are used to obtain the relationship between the applied bias voltage V_{bias} to the surface potential ψ_s at the oxide/semiconductor interface. Finally, several methods to obtain interface trap and oxide charge densities, are used to study radiation effects.

5.1 Static capacitor properties

An equivalent circuit of the capacitor samples is



(5.1)

with the oxide capacitance $C_{ox} = \varepsilon_{SiO_2}/d_{ox}$, the semiconductor admittance $Y_S = G_S + j\omega C_D + j\omega C_{it}$, and the series resistance of the substrate R_S. (In electronics engineering j is used for the imaginary unit $j = \sqrt{-1}$, and $\omega = 2\pi f$, is the small signal frequency.) The interesting physics is contained in the semiconductor admittance Y_S, which is modeled here by the following components: The depletion layer capacitance C_D, the interface trap capacitance C_{it}, and the parallel conductance G_S. The last two terms are introduced by the presence of interface traps, which contribute an electrical branch, parallel to the depletion layer capacitance

$$Y_{it} = G_S + j\omega C_{it}. \tag{5.2}$$

The imaginary part of the semiconductor admittance is

$$C_S = C_D + C_{it}. \tag{5.3}$$

The three terms of the semiconductor admittance depend on the applied DC-bias voltage and on the small signal frequency.

The oxide capacitance and the series resistance do not depend on the frequency and the bias, nor on the irradiation history.

The measured quantity is the samples admittance $Y = G + j\omega C$

$$\frac{1}{Y} = \frac{1}{j\omega C_{ox}} + \frac{1}{Y_S} + R_S. \tag{5.4}$$

By subtracting the series resistance we get the admittance of the proper MOS capacitor Y_m

$$\frac{1}{Y_m} = \frac{1}{j\omega C_{ox}} + \frac{1}{Y_S}. \tag{5.5}$$

5.1.1 Series resistance correction

The resistance of the semiconductor bulk R_S should not be neglected in my samples. Therefore, the first step in the analysis is to subtract R_S from the

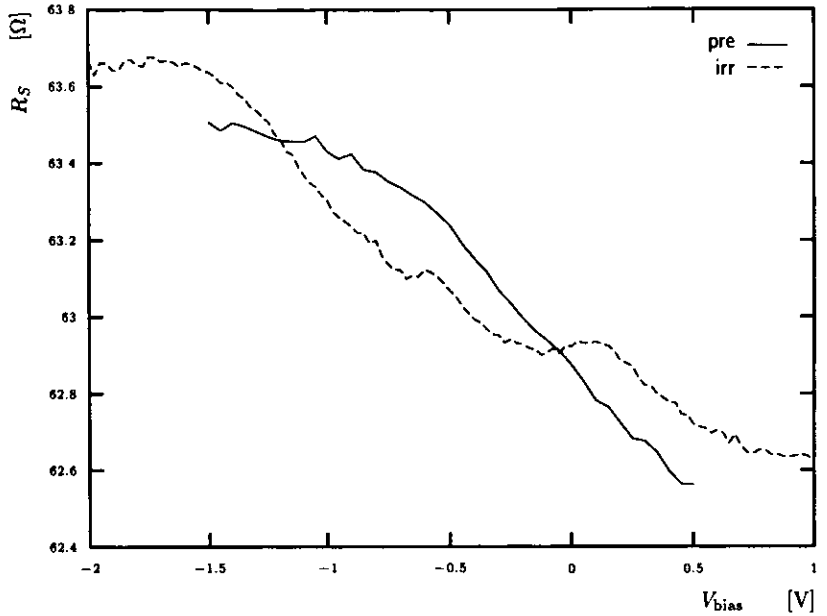


Figure 5.1: Series resistance R_S vs bias voltage obtained from the admittance averaged over the frequency range $f = 3.0$ to 5.0 MHz according to Eq. (5.7). The data is from sample No. 05, before and after irradiation up to 117 krad.

measured MOS impedance

$$\frac{1}{Y} = \frac{1}{Y_m} + R_S. \tag{5.6}$$

To obtain the series resistance from the data we assume that, at very high frequencies, the measured conductance is dominated by the series resistance, neglecting the real part of the MOS admittance G_S

$$R_S = \mathrm{Re}\left(\frac{1}{Y}\right), \qquad \omega \to \infty \tag{5.7}$$

Fig. 5.1 shows R_S, obtained from Eq. (5.7), averaged over the frequency range $f = 3.0$ to 5.0 MHz. The obtained resistance value changes in the order of 2 %, depending on the value of the capacitance. The average of R_S over the available bias range is used for the final corrections.

Once R_S is known, the MOS admittance Y_m results from solving Eq. (5.6)

$$Y_m = \frac{Y}{1 - R_S Y} = \frac{G - G^2 R_S - \omega^2 C^2 R_S + j\omega C}{1 - 2GR_S + (G^2 + \omega^2 C^2) R_S^2}. \tag{5.8}$$

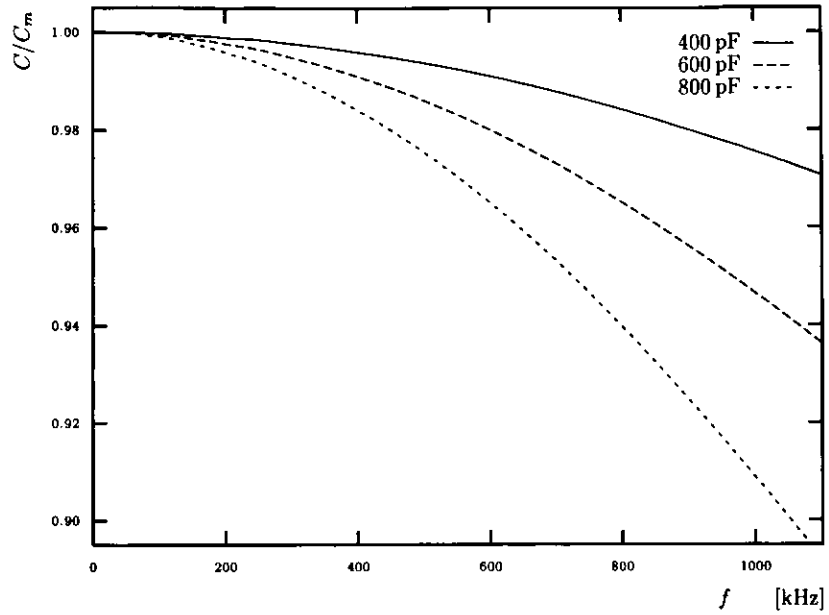


Figure 5.2: Error on the MOS capacitance, due to the presence of a series resistance $R_S = 63\,\Omega$, for three typical capacitance values. The curves show the ratio of the capacitance as measured on samples C to the capacitance of the proper MOS capacitor C_m.

The correction due to R_S to the capacitance C can be as large as ten percent at $f = 1$ MHz, as shown in Fig. 5.2.

5.1.2 Oxide capacitance

The information we are seeking is in the silicon admittance Y_m. We need to subtract the oxide capacitance, which is measured in series with the silicon admittance.

With the gate oxide thickness $d_{ox} = 40$ nm and $\varepsilon_{SiO_2} = 3.4{\cdot}10^{13}$ F/cm, the nominal oxide capacitance is

$$C_{ox} = \frac{\varepsilon_{SiO_2}}{d_{ox}} = 85\,\mathrm{nF/cm^2}. \tag{5.9}$$

To obtain the real oxide capacitance for each capacitor, I measured the capacitance in accumulation, at $V_{bias} = -10$ V and $f = 100$ kHz. In this bias

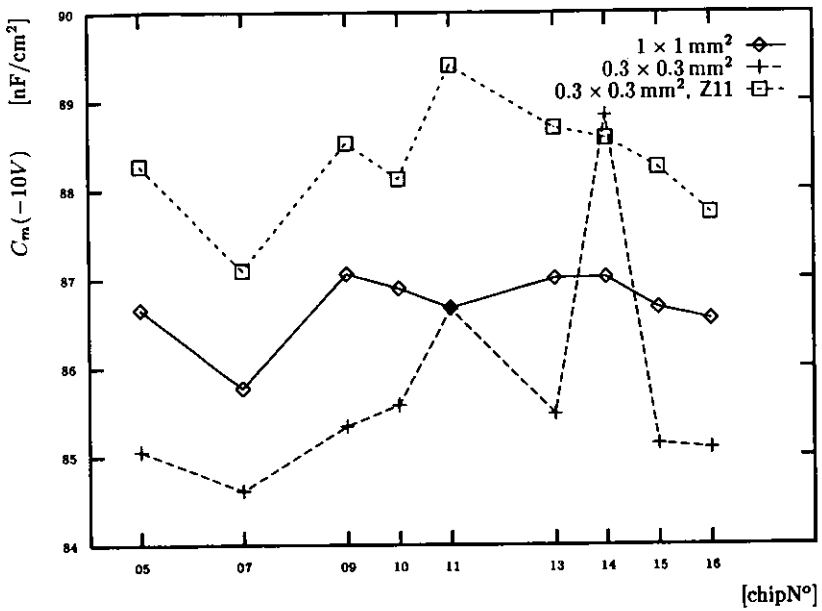


Figure 5.3: MOS capacitance at $V_{\text{bias}} = -10\,\text{V}$ and $f = 100\,\text{kHz}$ versus sample number. All three gate oxide capacitors are included in this graph.

condition, the semiconductor capacitance C_D is very large, giving

$$C_{ox} \approx C_m(V_{\text{bias}} = -10\,\text{V}). \tag{5.10}$$

The results are plotted in Fig. 5.3. There is some correlation between the three capacitors, located on the chips, providing some confidence that the fluctuations are not dominated by noise but by oxide thickness variations over the wafer, or from wafer to wafer. Capacitors on the same sample should have almost the same oxide thickness, but variations may occur from chip to chip.

Comparing with a theoretical CV-curve, the capacitance at $V_{\text{bias}} = -10\,\text{V}$ is 0.7% below the oxide capacitance. In the the following I will use the measured capacitance at $V_{\text{bias}} = -10\,\text{V}$, adjusted by the factor 1.007, for the oxide capacitance

$$C_{ox} = 1.007 \times C_m(-10\,\text{V}). \tag{5.11}$$

With the knowledge of the oxide capacitance we can calculate the semicon-

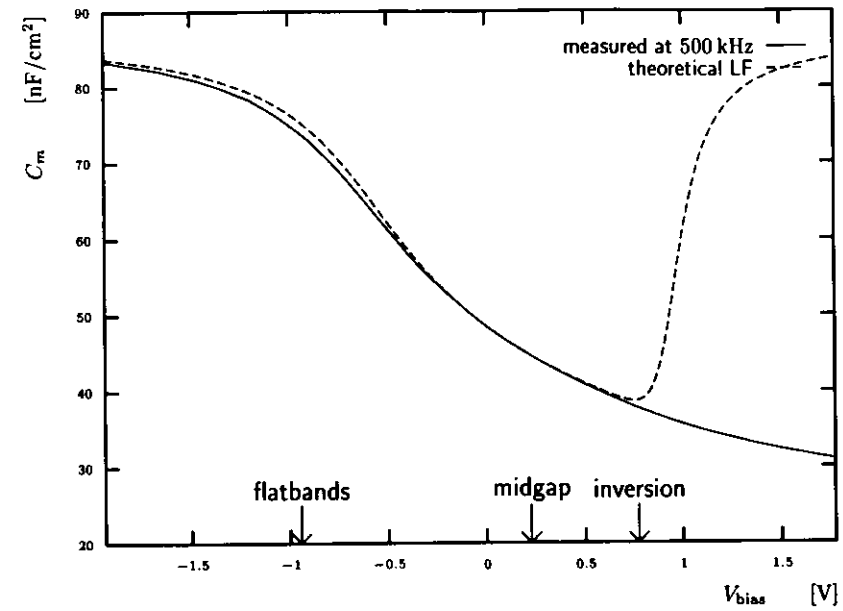


Figure 5.4: CV-curve of a non-irradiated capacitor measured at $f = 500\,\text{kHz}$, together with a theoretical LF curve. The parameters of the theoretical curve are: $C_{ox} = 87.50\,\text{nF/cm}^2$ and $N_A = 3.5{\cdot}10^{16}\,\text{cm}^{-3}$. The curve was shifted along the bias voltage axis to match the measured curve at midgap.

ductor admittance Y_S from the MOS admittance $Y_m = G_m + j\omega C_m$

$$Y_S = \frac{j\omega C_{ox}^2 G_m + j\omega^3 C_{ox} C_m (C_{ox} - C_m) - j\omega C_{ox} G_m^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}. \tag{5.12}$$

5.1.3 Substrate impurity concentration

In section 5.2 we need to know the acceptor density N_A in the bulk material, in order to get a relationship between the applied bias voltage V_{bias} and the surface potential ψ_s.

To obtain a doping profile from a CV-curve is quite easy, if the interface traps are negligible. We consider a MOS capacitor on p-substrate biased in depletion. The width of the depletion layer is

$$w_D = \frac{\varepsilon_{Si}}{C_S} = \varepsilon_{Si}\left(\frac{1}{C_m} - \frac{1}{C_{ox}}\right). \tag{5.13}$$

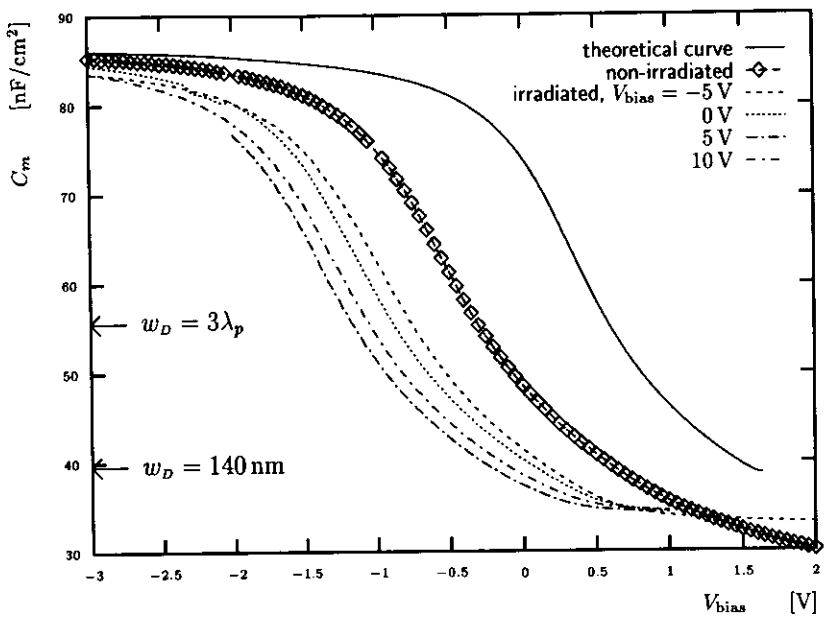


Figure 5.5: The CV-curves, from which the doping profiles in Fig. 5.6 were obtained. The capacitance was measured at $f = 500$ kHz, and was corrected for series resistance effects. The marks at the capacitance axis indicate the depletion layer width w_D on the limits for obtaining the acceptor density.

The displacement charge Q on the silicon side of the capacitor is assumed to consist entirely of the bare acceptor ions, in the depletion layer. Any change in Q is caused by a change in w_D:

$$\mathrm{d}Q = -qN_A\mathrm{d}w_D = C_m\mathrm{d}V_{\mathrm{bias}}. \tag{5.14}$$

From Eq. (5.13) we get

$$\mathrm{d}w_D = \varepsilon_{\mathrm{Si}}\mathrm{d}\left(\frac{1}{C_m}\right). \tag{5.15}$$

Putting this together and solving for N_A, gives the acceptor density, at a distance $x = w_D$ from the interface

$$N_A = -\frac{2}{q\varepsilon_{\mathrm{Si}}}\frac{1}{\frac{\mathrm{d}}{\mathrm{d}V_{\mathrm{bias}}}C_m^{-2}}. \tag{5.16}$$

This method, like most other methods, is limited to $w_D > 3\lambda_p$, with the

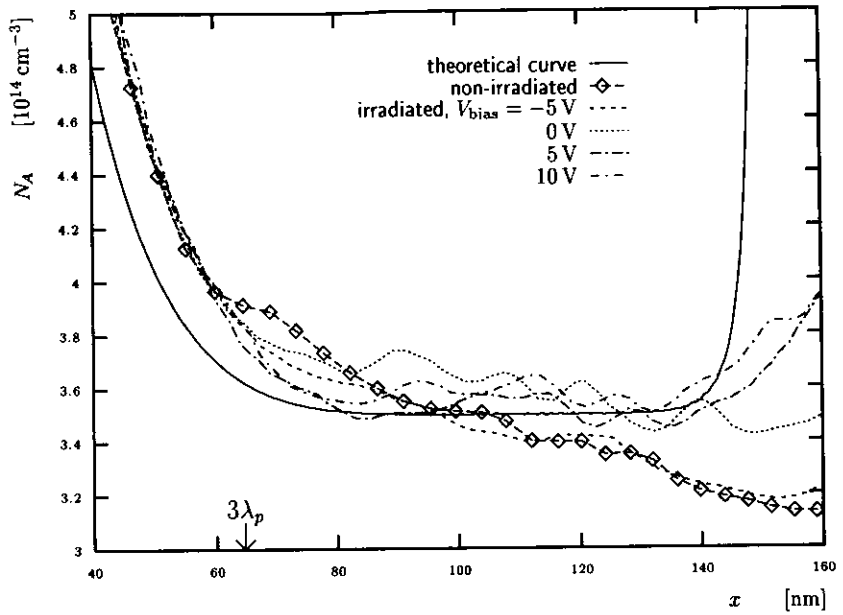


Figure 5.6: Doping profiles measured on MOS capacitors. The acceptor density is shown as a function of the distance form the interface x. The various curves were obtained from a theoretical C-V curve (solid line) and from measured high frequency curves in Fig. 5.5, non-irradiated and irradiated at different bias conditions, with a total dose of 117 krad. The theoretical curve was calculated with a homogeneous acceptor density $N_A = 3.5{\cdot}10^{16}$ cm^{-3} and is included to show the theoretical limits of the distance x, with this method.

extrinsic Debye length in p-type silicon

$$\lambda_p = \sqrt{\frac{\varepsilon_{\mathrm{Si}}kT}{q^2N_A}}, \tag{5.17}$$

since next to the interface, most of the assumptions fail. At the far end, the limit is the onset of inversion.

To apply this method, the measured capacitance at $f = 500$ kHz was extracted from the data files, with corrections for the series resistance contribution (Fig. 5.5). The resulting doping profiles are plotted in Fig. 5.6.

The acceptor density is, obviously, not homogeneous, as in fact expected, because of the threshold voltage adjustment implantation, which made a fairly thin doping layer under the gate oxide. From Table 2.1 we know that

the acceptor density, in the EPI layer of the substrate, is about two orders of magnitude lower than near to the interface. Fig. 5.6 shows that the transition to the EPI layer density is beyond the maximum depletion layer width $w_D^{(max)}(\approx 140\,\mathrm{nm})$. This allows to approximate the doping density by a homogeneous distribution of acceptors. The electric field, in the transition between the high acceptor density near the interface to the EPI layer, gives a constant shift of the CV-curve along the bias voltage axis, as well as a constant threshold voltage shift for the transistors. The shape of the characteristics is not affected, since the transition region is not depleted in strong inversion.

Fig. 5.6 includes a profile which is obtained with the same method from a theoretical CV-curve, which was calculated with the assumption of a homogeneous acceptor density $N_A = 3.5{\cdot}10^{16}$. This curve illustrates the theoretical limits of the method. The same theoretical CV-curve will be used in the next section to relate the applied bias voltage to the surface potential.

5.2 Surface potential

In this section, the relation between the applied bias voltage V_{bias} and the surface potential ψ_s, will be established.

5.2.1 Mapping the surface potential through the capacitance

We assume interface traps to be negligible, and the acceptor density profile to be homogeneous, and calculate a theoretical CV-curve, putting in a reasonable estimate for the acceptor density from section 5.1.3 and the oxide capacitance obtained, for each sample, in section 5.1.2. When I further assume the silicon capacitance to be a direct function of the surface potential alone, I can map the bias voltage via the silicon capacitance to the known surface potential from the theoretical calculations. Fig. 5.7 illustrates the procedure. A high frequency characteristic must be used to make sure that the errors, due to interface traps, are kept small. At low frequencies the interface trap charge will contribute to the semiconductor capacitance, resulting in a systematic error.

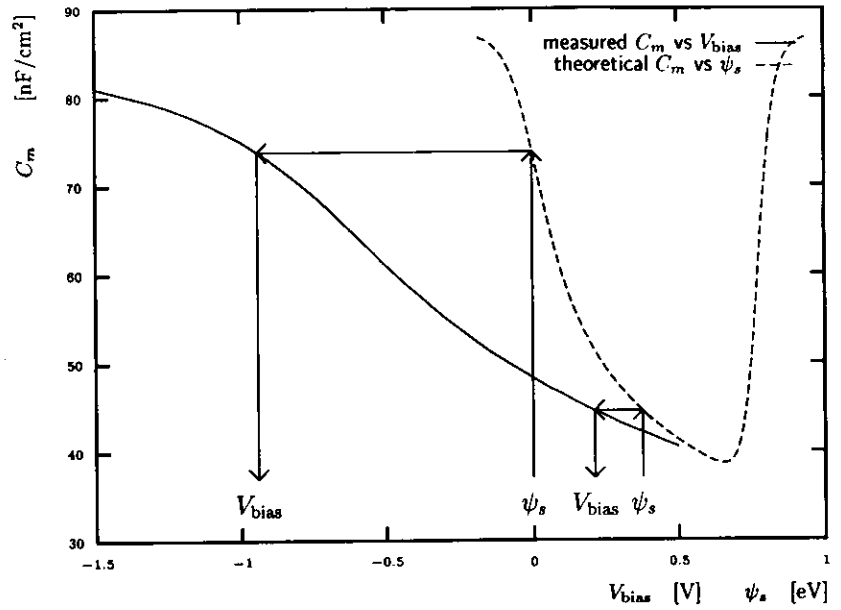


Figure 5.7: Mapping the bias voltage to the surface potential. The solid curve is the measured capacitance at $f = 500\,\mathrm{kHz}$ vs bias voltage. The dashed line is the low frequency capacitance, calculated from the oxide capacitance and the estimated average acceptor density.
The arrows show the way to obtain the bias–surface potential relationship. For a given surface potential ψ_s, the corresponding capacitance is obtained from the theoretical curve. The bias voltage V_{bias}, where the the real capacitor has the same capacitance, corresponds to the given surface potential. The two shown examples correspond to flatbands ($\psi_s = 0$) and midgap ($\psi_s = 0.38\,\mathrm{eV}$).

5.2.2 Surface potential from integrating the CV-curve

Another way to obtain a relation between bias voltage and surface potential is to integrate the CV-curve, obtaining the shape of the function $\psi_s(V_{\mathrm{bias}})$. The integration constant must be obtained in another way.

The MOS capacitance is defined as

$$C_m = \frac{\mathrm{d}Q}{\mathrm{d}V_{\mathrm{bias}}} \quad \text{or} \quad Q = \int \mathrm{d}V_{\mathrm{bias}}\, C_m. \tag{5.18}$$

From Gauß law, the charge Q is proportional to the electric field in the oxide, and, by multiplying with the oxide thickness, we get the voltage across

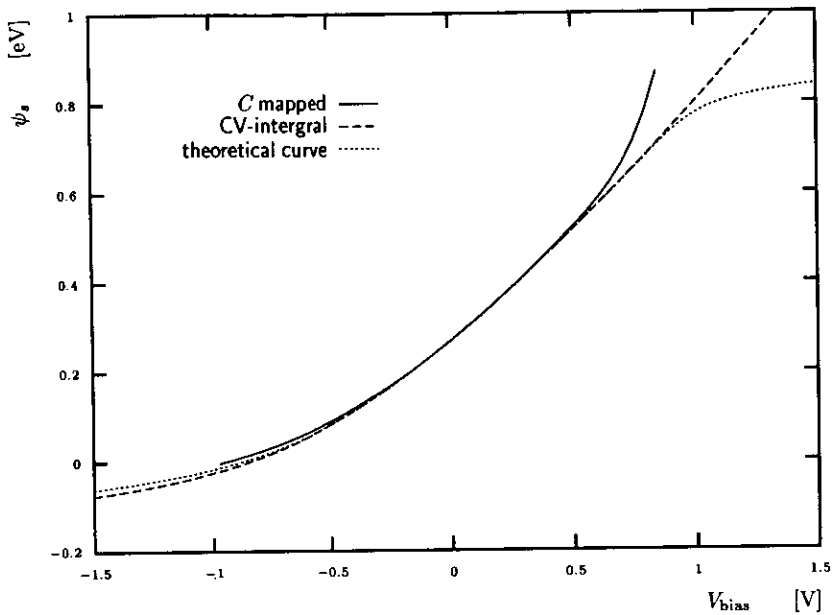


Figure 5.8: Various ψ_s vs V_{bias} curves for a non-irradiated sample. The solid line is obtained with the method of section 5.2.1. The dashed line is from Eq. (5.19), matched to the first one at midgap. The dotted line is a theoretical curve (see text).

the oxide. Subtracting this from the applied bias voltage leaves the electric potential on the surface

$$\frac{\psi_s}{q} = V_{\text{bias}} - \frac{d_{ox}}{\varepsilon_{SiO_2}} \int \mathrm{d}V_{\text{bias}}\, C_m = \int \mathrm{d}V_{\text{bias}} \left(1 - \frac{C_m}{C_{ox}}\right). \qquad (5.19)$$

This requires a low frequency CV-curve where all charges, including interface traps, follow the AC-cycle. I used CV-curves at $f = 1\,\text{kHz}$ to demonstrate this method in Fig. 5.8, where both the surface potential from the previous section, and from Eq. (5.19) are drawn, with the integration constant of the latter, chosen to match both curves at midgap. The theoretical curve, for a homogeneous impurity concentration, is also shown. This graph was obtained from a non-irradiated sample.

Fig. 5.9 shows the differences between the potentials obtained by the two methods from all measurements on irradiated samples and one non-irradiated sample. The agreement of the two methods is better than $\Delta\psi_s < 1kT = 0.025\,\text{eV}$ between $0 < \psi_s < 0.6\,\text{eV}$, and from Fig. 5.8 we see that the

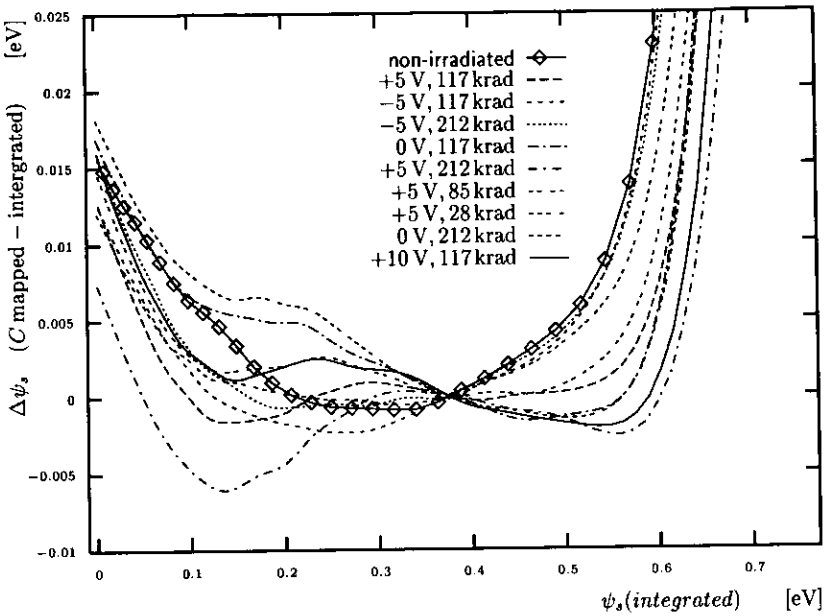


Figure 5.9: Difference between the surface potentials, obtained by the two methods: capacitance matching with a theoretical curve and integration of a LF CV-curve. Data for all irradiated samples and one non-irradiated sample is shown.

capacitance integral method agrees well with the theoretical prediction even beyond this range almost up to the onset of inversion at $\psi_s = 0.75\,\text{eV}$.

5.3 Radiation effects

5.3.1 Interface trap density from the surface charge gradient

With the results from the previous section, we can estimate the additional charge at the interface generated during irradiation, just by subtracting the bias voltage before irradiation from the bias voltage after irradiation, for a given surface potential

$$\Delta Q_{if}(\psi_s) = -\left(V_{\text{bias}}^{(\text{irr})} - V_{\text{bias}}^{(\text{noi})}\right) C_{ox}. \qquad (5.20)$$

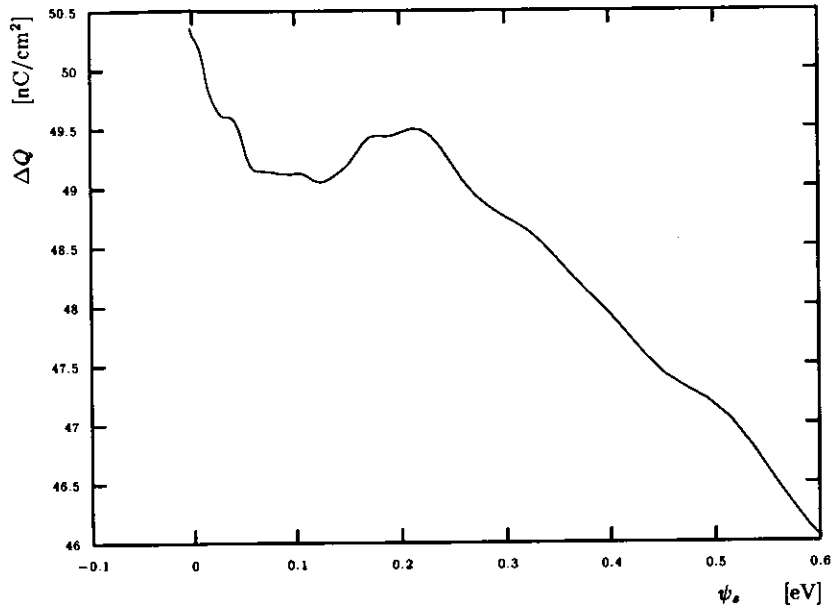


Figure 5.10: Change of the interface charge density by irradiation with 117 krad versus surface potential on sample N° 10.

Interface charge means: charges in interface traps plus the effect of the trapped oxide charges, projected to the interface. Trapped oxide charges contribute only by the fraction of the oxide where they contribute to the electric field at the gate interface. But, since most oxide traps are located near to the interface compared to the oxide thickness, we will assume all charges to be located at the interface.

Fig. 5.10 shows Q_{if} from Eq. (5.20) versus surface potential, that appeared after irradiation on sample N° 10, that was irradiated at $V_{\text{bias}} = 0\,\text{V}$ with 117 krad. The data, between flatbands and close to midgap $\psi_s = 0 \ldots 0.2\,\text{eV}$, show that interface traps may *not* be negligible in this region, where the interface trap response is comparable to the frequency $f = 500\,\text{kHz}$, used for this measurement.

The radiation induced interface charge ΔQ_{if} in Fig. 5.10 decreases with rising ψ_s, since more and more interface traps capture electrons. The slope

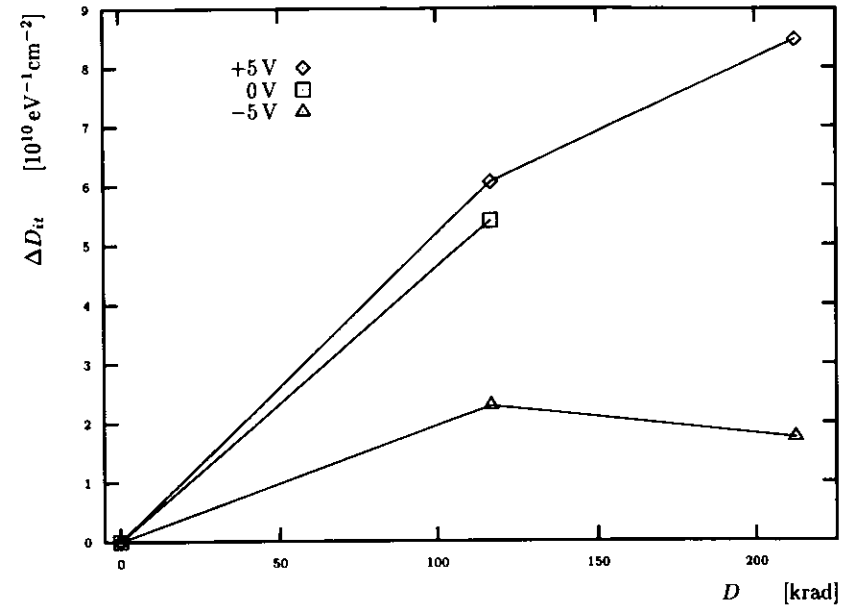


Figure 5.11: Excess interface trap level density after irradiation calculated from Eq. (5.21). Five samples, which were measured before and after irradiation are shown.

translates into the interface trap level density, introduced by radiation

$$\Delta D_{it} = \frac{1}{q}\frac{\partial \Delta Q_{if}}{\partial \psi_s}. \tag{5.21}$$

Results are shown in Fig. 5.11 for five samples on which measurements were performed prior to irradiation.

Flatbands, midgap and inversion shift

Similar to the threshold voltage shift measurement on MOS transistors, we can select energy levels in the silicon band gap and measure the bias voltage, corresponding to these levels. Three curves in Fig. 5.12 show the bias voltage, corresponding to flatbands, midgap, and the onset of strong inversion, versus irradiation dose. The samples were irradiated with $V_{\text{bias}} = +5\,\text{V}$. The threshold voltage V_{th} of the transistors on the same samples, are shown, for comparison.

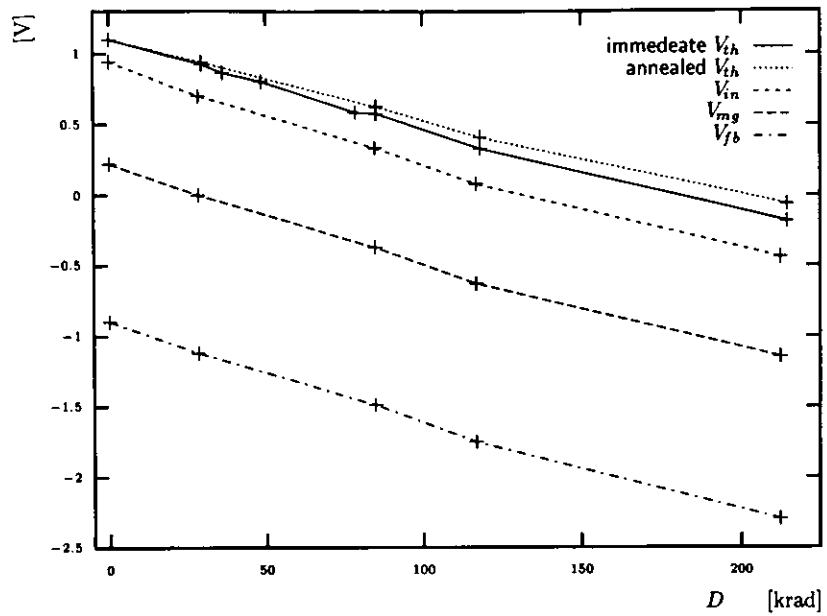


Figure 5.12: MOS capacitor flatbands, midgap, and inversion voltage, and the transistor threshold voltage shift, versus γ-dose. The samples were irradiated at $V_{\text{bias}} = 5\,\text{V}$. The inversion, midgap, flatbands voltage, V_{fb}, Vmg, and V_{in}, of the capacitor are drawn with short-dashed, dashed, and dot-dashed lines. The threshold voltages V_{th}, measured during (six months after) irradiation, are plotted with solid (dotted) lines.

The curves run neatly parallel, within about 50 mV. The generation of interface traps should cause the curves to spread apart in this graph. The small spread translates into interface trap densities $N_{it}^{(a)}$ above, and $N_{it}^{(b)}$ below midgap

$$N_{it}^{(a)} = \frac{C_{ox}}{q}\left(V_{in}^{(irr)} - V_{mg}^{(irr)} - V_{in}^{(pre)} + V_{mg}^{(pre)}\right) \tag{5.22}$$

$$N_{it}^{(b)} = \frac{C_{ox}}{q}\left(V_{mg}^{(irr)} - V_{fb}^{(irr)} - V_{mg}^{(pre)} + V_{fb}^{(pre)}\right) \tag{5.23}$$

The results of these calculations are plotted in Fig. 5.13, using the data from Fig. 5.12. The pre–rad bias $V_{xx}^{(pre)}$ was estimated as the average from five samples, which were measured before irradiation.

Obviously, we do not see any generation of interface traps above midgap with this method. Below midgap there is a small increase of the total number

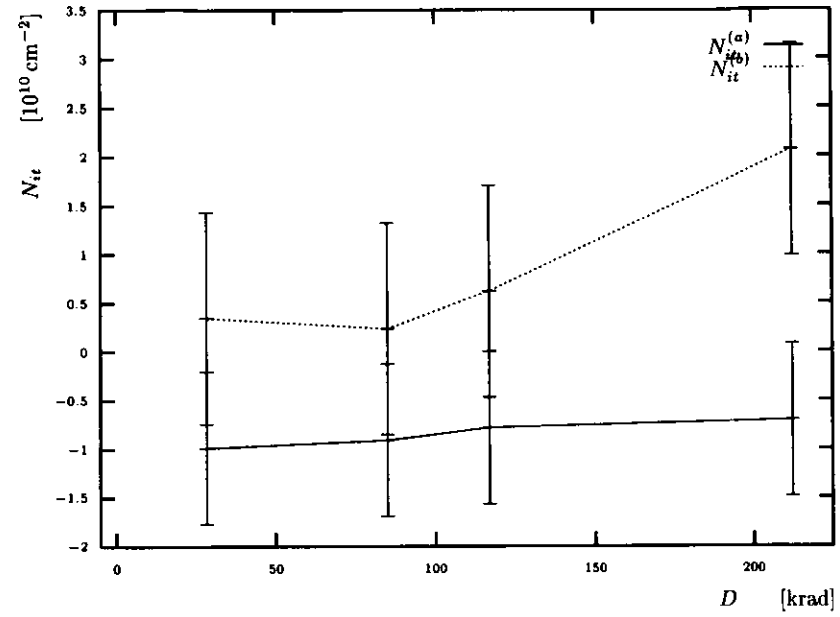


Figure 5.13: Interface trap densities $N_{it}^{(a)}$, between midgap and inversion (0.38 eV above midgap), and $N_{it}^{(b)}$ between flatbands (0.38 eV below midgap) and midgap, obtained from the spread of C-V curves at $f = 500\,\text{kHz}$.

of interface traps.

5.4 Interface trap admittance

To describe the signature of interface traps in the measured MOS admittance, I will use a model for the frequency dependence of the interface trap admittance, which is described by Nicollian and Brews in [19]. In this section I will first introduce this model, describe the procedure to fit the measured data to the model, and give my results.

5.4.1 Interface trap admittance model

There are a couple of assumptions about interface traps, which go into the model:

- We can apply the *Shockley-Read-Hall* (SRH) model, allowing to characterize interface traps electrically by their level density and their hole and electron capture time constants,
- Interface traps are well separated in space on the interface,
- but closely packed in energy throughout the silicon bandgap.
- The density and capture probabilities vary slowly with the energy level.
- The model is restricted to depletion, thus we assume the minority carrier density at the interface, to be negligible.

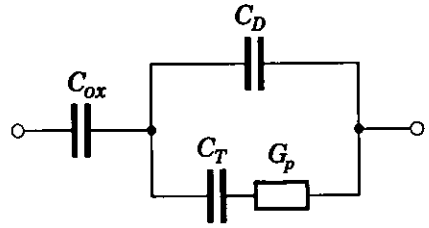
The system we are looking at is a MOS capacitor with a DC-bias applied and a small harmonic AC-signal superimposed. The semiconductor and the interface are in thermal equilibrium, according to the DC-bias, with small harmonic disturbances, due to the AC-signal. The disturbances are described in terms of small signal equivalent circuits, with components which depend on the applied DC-bias and the frequency $f = \omega/2\pi$ of the signal.

Single level interface traps

We start with only one kind of interface trap, located at the energy E_T, with a density N_T per unit area. In thermal equilibrium the probability, that such a trap is occupied, is given by the Fermi-Dirac distribution

$$f_o(E_T) = \frac{1}{1 + e^{(E_T - E_F)/kT}} \tag{5.24}$$

When neglecting minority carriers, the interface traps contribute an electrical branch from the interface to the majority carrier band (valence band for p-type silicon) of the semiconductor, consisting of a capacitor C_T and a conductance G_p in series, giving a small signal equivalent circuit for the MOS capacitor like



(5.25)

where C_{ox} is the oxide capacitance and C_D is the capacitance of the depletion layer.

The capacitance C_T measures the change of trap occupancy when the surface potential changes while maintaining thermal equilibrium

$$C_T = \frac{\mathrm{d}(-q f_o N_T)}{\mathrm{d}(E_T/q)} = \frac{q^2}{kT} N_T f_o (1 - f_o). \tag{5.26}$$

The conductance G_p governs the speed, at which the equilibrium is approached, which is (for p-type silicon) proportional to the number of filled traps $f_o N_T$, the number of available holes p_S, and the hole capture probability of the traps c_p

$$G_p = \frac{q^2}{kT} N_T c_p p_S f_o. \tag{5.27}$$

In thermal equilibrium, the hole capture and emission rates are the same, and, since we look at small deviations from the equilibrium state, the speed of the interface trap response is sufficiently parameterized by the capture process alone.

The temperature dependence enters, because the small signal variations of the potential act in units of kT, while they are measured in eV, giving the factor kT/q in the denominator. That means that a small change of the potential causes a larger deviation from equilibrium, at lower temperatures.

The term $f_o(1 - f_o)$ in the capacitance reduces the influence of the traps to situations, where the Fermi energy is within a few kT of the trap level E_T.

Omitting the oxide capacitance C_{ox}, which is in series with the silicon admittance Y_S, we write down the equivalent circuit in terms of

$$Y_S = j\omega C_D + \frac{j\omega C_T G_p}{j\omega C_T + G_p} \tag{5.28}$$

Separating the real and imaginary parts of $Y_S = j\omega C_S + G_S$

$$C_S = C_D + C_T \frac{1}{1 + (\omega\tau)^2} \tag{5.29}$$

$$\frac{G_S}{\omega} = C_T \frac{\omega\tau}{1 + (\omega\tau)^2} \tag{5.30}$$

where the time constant

$$\tau = \frac{C_T}{G_p} = \frac{f_o}{c_p p_S} \tag{5.31}$$

depends on the applied bias, through the trap occupancy f_o and the hole density on the surface p_S.

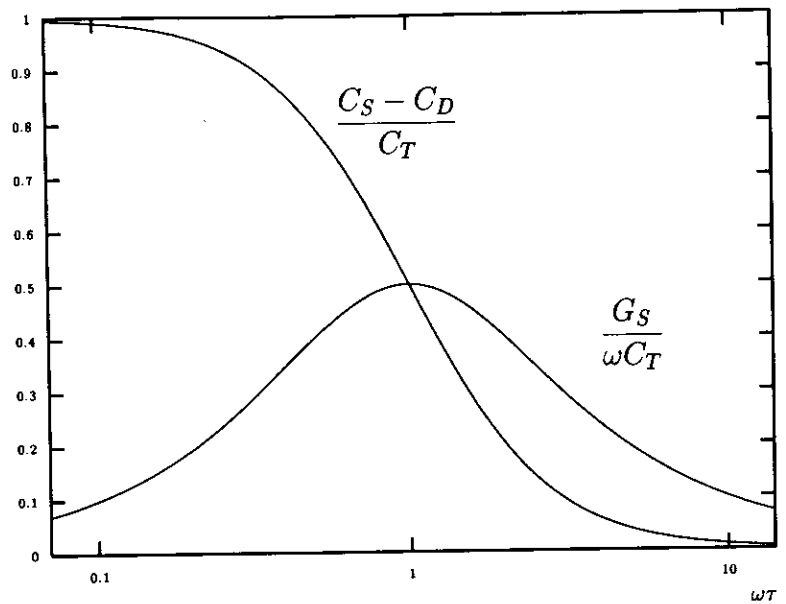


Figure 5.14: Frequency dependence of the single trap level admittance, from Eqs. (5.29 and (5.30).

The frequency dependence of these formulas is shown in dimensionless form, in Fig. 5.14. When the frequency is sufficiently low for the interface traps to follow the AC-cycle, to maintain thermal equilibrium, the interface traps just add to the capacitance, according to the change in occupancy of the traps, with the small signal potential. At high frequency, the interface traps can not follow the signal altogether, and the admittance vanishes. For intermediate frequencies, the traps follow partly the AC-signal, and the delay in their response causes energy loss, giving a nonzero real part of the admittance.

Admittance of a dense interface trap distribution

On real MOS capacitors there are no discrete interface trap levels. Interface traps are distributed so closely within in the silicon bandgap, that it is impossible to separate single levels in a measurement.

On the other hand, as long as the interface trap density is not extremely

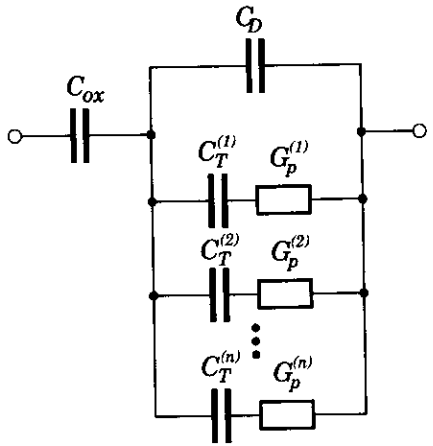


Figure 5.15: Equivalent circuit for multiple interface trap levels.

high, there is no direct interaction between the traps, because they are well separated in space. The interface traps do not form a band.

As a consequence, each trap level $^{(i)}$ can be put into the model as one independent branch $C_T^{(i)}$–$G_p^{(i)}$, parallel to the others, as in Fig. 5.15. All trap levels follow the AC-signal with their own time constant.

For a continuum of interface traps, the single level trap density per unit area N_T is replaced by the interface trap level density $D_{it}(E_T)dE_T$, which is the number of interface traps per unit area with energy levels between E_T and $E_T + dE_T$.

All that remains is to add all interface trap branches

$$Y_{it} = \sum_i \frac{j\omega C_T^{(i)} G_p^{(i)}}{j\omega C_T^{(i)} + G_p^{(i)}}, \tag{5.32}$$

putting in Eqs. (5.26 and (5.27), we get the integral

$$Y_{it} = \frac{q^2}{kT} \int_{E_V}^{E_C} D_{it} \mathrm{d}E_T \, \frac{j\omega c_p p_S f_o (1 - f_o)}{j\omega (1 - f_o) + c_p p_S}. \tag{5.33}$$

Now we need the assumption that interface trap properties do not vary fast with the energy level. The integrand, to be precise, the term $f_o(1 - f_o)$, has a sharp peak at $E_T = E_F$. Interface traps far from the Fermi level do not contribute. Therefore, we take the interface trap properties D_{it} and c_p at

the Fermi level, and keep them constant in the integration. We change the integration variable $df = d(1-f_o) = f(1-f)dE_T/kT$ and introduce the interface trap response time constant $\tau_p = 1/(c_p p_S)$, the integral becomes

$$Y_{it} = q^2 D_{it} \left(j\omega \int_0^1 \mathrm{d}f \, \frac{1}{(\omega\tau_p f)^2 + 1} + \omega \int_0^1 \mathrm{d}f \, \frac{\omega\tau_p f}{(\omega\tau_p f)^2 + 1} \right) \tag{5.34}$$

and we obtain an upgrade for the single trap level Eqs. (5.29 and (5.30):

$$C_S = C_D + C_{it} \frac{\arctan(\omega\tau_p)}{\omega\tau_p} \tag{5.35}$$

$$\frac{G_S}{\omega} = C_{it} \frac{\ln\left(1 + (\omega\tau_p)^2\right)}{2\omega\tau_p} \tag{5.36}$$

with the interface trap capacitance $C_{it} = q^2 D_{it}$.

The admittance of a continuum of interface traps is drawn in Fig. 5.16, together with the curves for a single trap level Eqs. (5.29 and (5.30), with $\tau = \tau_p$ and $C_T = C_{it}$. The interface trap continuum leads to a conductance peak at $\omega = 1.98/\tau_p$, which is near to the naive expectation of a peak at $\omega = 2/\tau_p$, from the fact that the time constant of a single level trap at the Fermi energy is $\tau = \frac{1}{2}\tau_p$.

The time constant dispersion from a continuum of trap levels makes the conductance peak wider and flatter than the single level curves. The capacitance curve is less steep.

A major difference between single trap level and a continuum, apart from the frequency dependence, is the replacement of C_T by C_{it}, the former a sharply peaked function of the surface potential, the latter proportional to the interface trap level density and, therefore, from all experimental evidence, almost independent from the bias condition.

Band bending fluctuations

Comparing measured data to the model with a continuum of interface traps, Fig. 5.17, reveals that the data is not in good agreement with the model. The measured capacitance curve is spread out more than predicted and the conductance peak is less high. This leads to the assumption that there is an additional source of time constant dispersion present.

This time constant dispersion is believed to originate from short range spatial *band bending fluctuations*. Charges, trapped at the interface or in

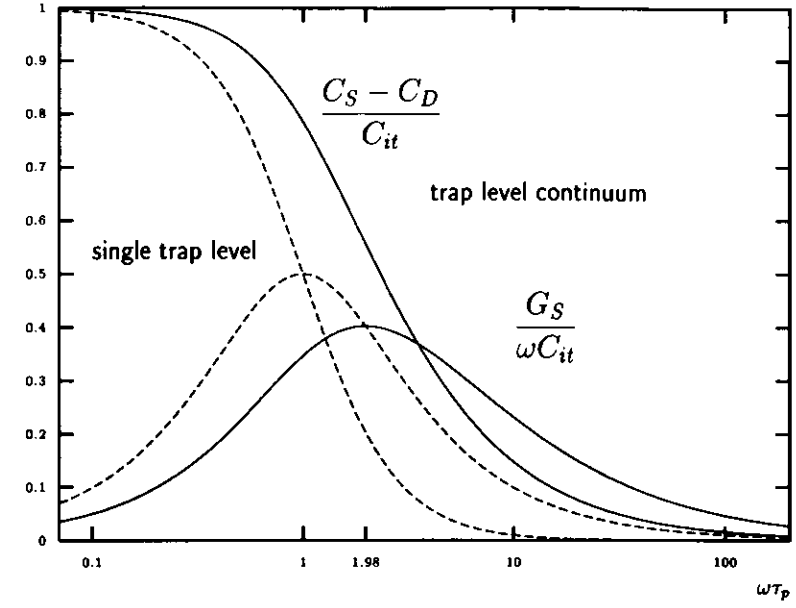


Figure 5.16: Frequency dependence of the admittance of a continuum of interface traps. The dashed graphs are the single trap level results as in Fig. 5.14. The solid lines are the plots of Eqs. (5.35 and (5.36), normalized to the low-frequency interface trap capacitance C_{it}.

the oxide, are distributed inhomogeneously or even clustered, causing local variations of the surface potential. *Short range* means, that fluctuations, which extend to an area larger than the square of the depletion layer width are very improbable, so that the depletion layer capacitance C_D can be assumed to be constant at an average value.

The interface trap response time constant depends, through the majority carrier density, exponentially on the surface potential. Small inhomogeneities of the surface potential ψ_s, of the order of some kT, have a dramatic effect.

To include the band bending fluctuations into the model, the capacitor is cut into small patches, each with its local surface potential $\psi_s + \Delta\psi_s$, which fluctuates around the mean value ψ_s with a distribution $\mathcal{P}(\Delta\psi_s)$. The depletion layer capacitance $C_D(\psi_s)$ is assumed to be the same for all patches, according to the mean surface potential. The interface trap admittance Y_{it} is modeled, for each patch, independently. Finally, all patches are connected

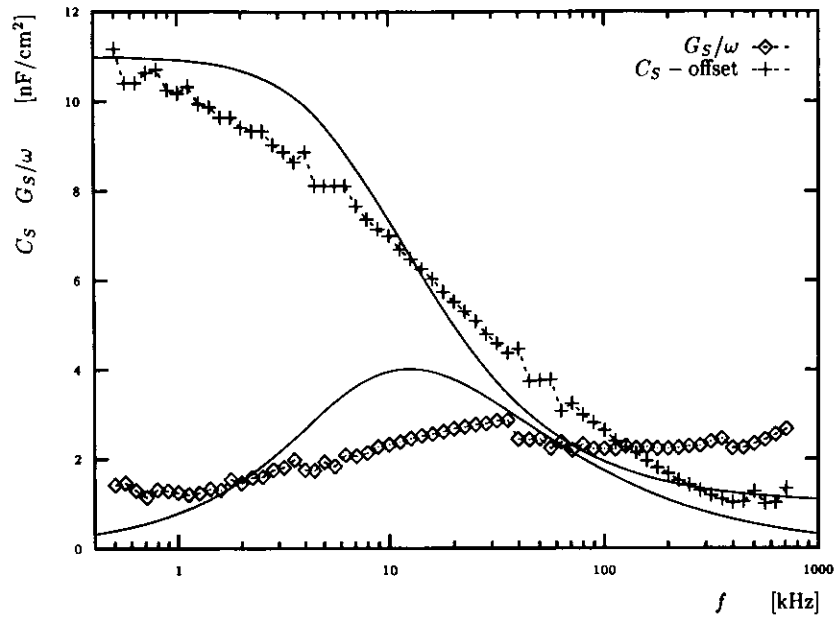


Figure 5.17: Frequency dependence of the admittance of an irradiated MOS capacitor (data points), irradiated up to 117 krad, with zero bias applied. The surface potential, during the measurement, was $\psi_s = 0.17\,\mathrm{eV}$. To show both curves in one picture, an arbitrary offset was subtracted from the capacitance. The solid lines are calculated from Eqs. (5.35 and (5.36), with $C_{it} = 10\,\mathrm{nF/cm^2}$ and $1/\tau_p = 1\,\mathrm{kHz}$

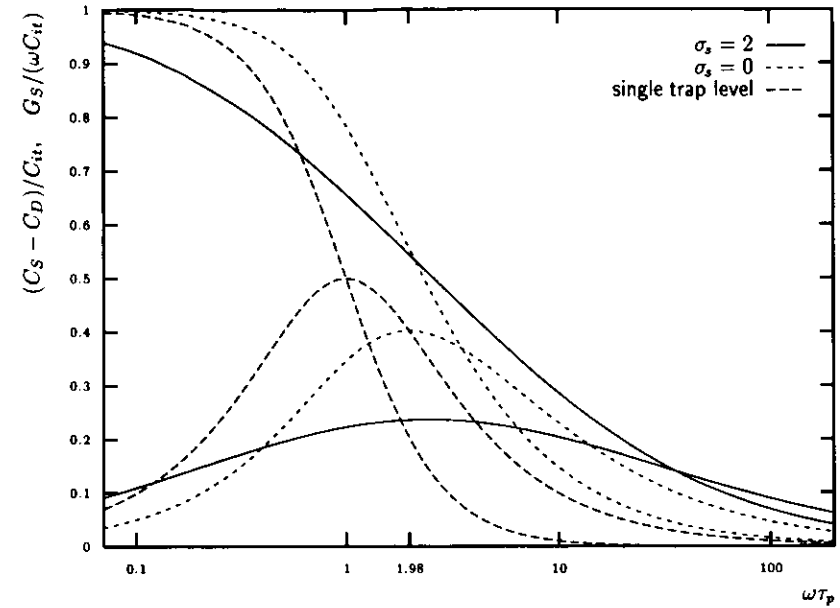


Figure 5.18: Frequency dependence of the interface trap admittance including band bending fluctuations. The dashed curves again represent the single trap level case, and the dotted lines are calculated with $\sigma_s = 0$, that is the case without band bending fluctuations, as in Fig. 5.16. The solid graphs are calculated from Eq. (5.41), with $\sigma_s = 2$.

in parallel

$$Y_S = j\omega C_D(\psi_s) + \int_{-\infty}^{\infty} \mathrm{d}\Delta\psi_s\, \mathcal{P}(\Delta\psi_s) Y_{it}(\psi_s + \Delta\psi_s). \tag{5.37}$$

We assume a normal distribution of the band bending fluctuations

$$\mathcal{P}(\Delta\psi_s) = \frac{1}{\sqrt{2\pi\sigma_s^2}} e^{-\frac{1}{2\sigma_s^2}\left(\frac{\Delta\psi_s}{kT}\right)^2}, \tag{5.38}$$

where σ_s is the width of the distribution, in units of kT.

To perform the integration we assume, once again, that the interface trap parameters do not vary within some kT in energy, keeping D_{it}, c_p, and σ_s constant, at their average value. In the following, τ_p is the time constant

according to the average majority carrier (hole) density

$$\tau_p = \frac{1}{c_p p_S} = \frac{1}{c_p N_A} e^{\frac{\psi_s}{kT}} \tag{5.39}$$

but, within the integral, we have to use the local value

$$\tau(\psi_s + \Delta\psi_s) = \tau_p\, e^{\frac{\Delta\psi_s}{kT}}. \tag{5.40}$$

Putting all this together, we obtain the final model of the frequency dependence of the semiconductor admittance of a MOS capacitor with interface traps, in depletion

$$\begin{aligned} Y_S = j\omega C_D + q^2 D_{it} \frac{1}{\omega\tau_p} \frac{1}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \mathrm{d}\eta e^{-\frac{\eta^2}{2\sigma_s^2}} e^{-\eta} \\ \left(\tfrac{\omega}{2} \ln\left(1 + (\omega\tau_p e^{\eta})^2\right) + j\omega \arctan\left(\omega\tau_p e^{\eta}\right)\right). \end{aligned} \tag{5.41}$$

The numerical evaluation of this integral, with $\sigma_s = 2$, is compared in Fig. 5.18 with the curves already shown in Fig. 5.16. The frequency response becomes broader when band bending fluctuations are included.

The final model Eq. (5.41), which describes the frequency dependence of the semiconductor admittance C_S at a fixed bias, has four parameters:

C_D the depletion layer capacitance, providing the origin, or offset, on the admittance axis,

D_{it} the interface trap level density, setting the amplitude on the admittance axis,

τ_p the interface trap response time, fixing the origin on the frequency scale, and

σ_s the width of the band bending fluctuations distribution, for the amplitude on the frequency axis.

In the following sections I will try to obtain these parameters from measured data.

5.4.2 Methods to extract interface trap properties from the conductance

The model that was derived in the previous section can be used to estimate interface trap properties from measured admittance of a MOS capacitor. A method, described in [19], uses the real part of the admittance, the parallel conductance.

The interface trap properties can be extracted from only two data points, if a neat conductance peak can be measured. All what is needed is

- the location of the maximum of the peak ω_p,
- the peak conductance G_p,
- and the value of the conductance at, for instance, five times the peak frequency $G(5\omega_p)$.

The analysis is done with three graphs or tables. The ratio between the two conductance values gives the width of the band bending fluctuations distribution from the first graph, which shows σ_s as a function of $G_p/G(5\omega_p)$.

The other two graphs give two factors $A(\sigma_s)$ and $B(\sigma_s)$, to get the interface trap density, which is proportional to the peak conductance $D_{it} = A(\sigma_s)G_p$, and the interface trap response time τ_p, which is proportional to the inverse of the peak position $\tau_p = B(\sigma_s)/\omega_p$.

This method is simple and no computer is needed to analyze the data, but a lot of high resolution data is necessary to figure out where the peak is and, eventually, only two conductance measurements are used while the rest is discarded.

I could not use this method with the data obtained from my samples, because the resolution of the conductance measurement was not sufficient. Fig. 5.17 includes a typical example of my conductance peaks, which exhibits distortions at some points, where the instrument switches the measurement range. Switching the range is necessary, because the signal amplitude is proportional to the oscillator frequency, which sweeps over several decades.

The capacitance data does not offer a similarly easy procedure but, when the model curve is fitted to a complete frequency characteristic, it makes no difference to use the capacitance or the conductance, as long as the measurement offers the same absolute resolution, for both the real and imaginary part of the admittance.

The case is different, if the capacitance and the conductance are measured with comparable relative resolution, since the capacitance signature is a small difference between two large numbers, whereas the conductance enters directly.

The HP 4192A impedance analyzer seems to give the same absolute magnitudes of noise and range switch distortions for the capacitance and the conductance. I suspect that the instrument measures the amplitude and the phase of the signal. In that case a systematic error of the phase measurement results in a large offset error of the conductance.

I decided to use the measured capacitance–frequency characteristics to obtain the interface trap properties, by fitting the parameters of the model to the data.

5.4.3 Interface trap capacitance model fit

The model for the frequency dependence of the semiconductor capacitance from Eq. (5.41),

$$C_S = C_D + q^2 D_{it} \frac{1}{\omega\tau_p} \frac{1}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \mathrm{d}\eta\, e^{-\frac{\eta^2}{2\sigma_s^2}}\, e^{-\eta} \arctan\left(\omega\tau_p e^{\eta}\right). \qquad (5.42)$$

is limited to bias conditions in depletion, not too near to flatbands or midgap. Therefore, the appropriate bias voltage range must be selected for the fit to the data, according to the method introduced in section 5.2. The data is corrected for series resistance and the silicon capacitance is calculated. The results are stored in a file for input to the interface trap fit program.

The fit program

The fit program employs a simple least square algorithm to find those values for the fit parameters for which the function

$$\chi^2 = \sum_i \left(C_S^{(i)} - C(\omega^{(i)}) \right)^2 \qquad (5.43)$$

is minimal, where $C_S^{(i)}$ is the capacitance measured at the frequency $\omega^{(i)}$ and $C(\omega)$ is the capacitance calculated from the model Eq. (5.42). The sum runs over all data points in the selected frequency range $f = 0.5$ to 500 kHz, for any given bias voltage. The parameters to be fitted are: the depletion layer capacitance C_D, the interface trap level density D_{it}, the interface trap response time constant τ_p, and the width of the band bending fluctuations distribution σ_s.

The procedure is to iterate the minimization function, as long as the result improves or a maximum number of iterations were done. To start with, the parameters must be initialized to reasonable values. These can have three different origins:

1. Initial values for σ_s and τ_p may be set on invocation of the program by commandline options. The setting of τ_p may depend exponentially on the bias voltage, whereas σ_s is a constant.

2. All parameters except σ_s can be initialized from the capacitance data, using minimum and maximum capacitance values and the approximate transition frequency.

3. Instead of starting all over, the results from a previous run of the fit program can be used as starting points for another one, possibly with different constraints on the parameters to change.

Very often, attempts to fit all four parameters do not converge, sometimes even three parameters are too much. To handle these cases, one fit iteration consists of up to six invocations of the fit algorithm, one after the other, with each of them keeping a different set of parameters constant. Any step,

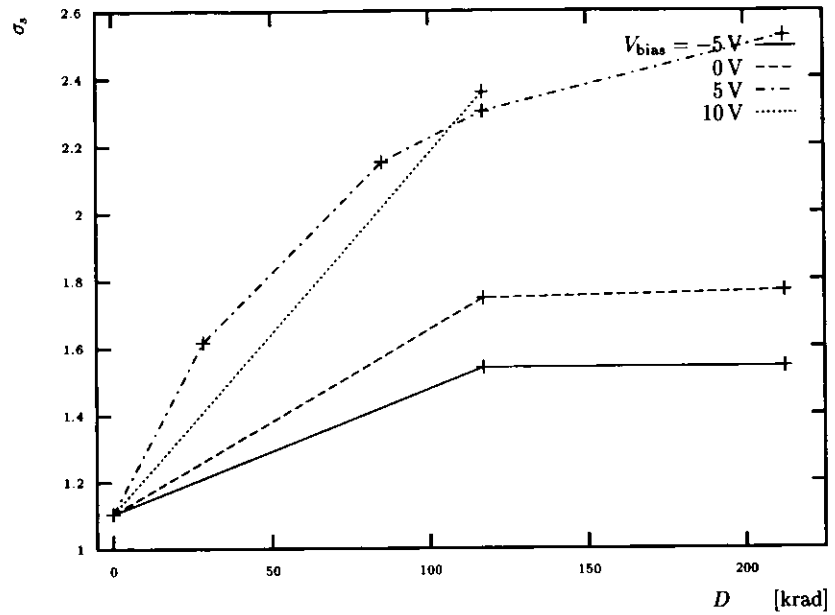


Figure 5.19: Width of the band bending fluctuations distribution σ_s vs irradiation dose.

that does not improve the result will be discarded. Which parameters are to be fitted, in the individual steps, is specified by a commandline option. If a parameter is not to be changed in any of the steps, it keeps its value throughout the fit.

The band bending fluctuations distribution

It turns out that fitting all four parameters C_D, D_{it}, σ_s, and τ_p, simultaneously, often fails, and if it succeeds introduces unnecessary errors. For instance, the parameter σ_s is expected to be almost independent of bias. Improved results are obtained by choosing a proper value for σ_s and to keep it constant during the fit.

The proper value of σ_s is obtained by fitting the data, allowing all four parameters to change. Afterwards, the average σ_s is computed of the results, for a range of bias conditions, where the fit is stable. This was done for every irradiated sample separately but, for the pre–rad condition, I used the average of five measurements. The results are plotted in Fig. 5.19 versus

irradiation dose.

Band bending fluctuations were introduced, assuming that they are caused by inhomogeneities in the distribution of interface charges. The width of the distribution of the band bending fluctuations σ_s is expected to scale, somehow, with the total interface charge density. Fig. 5.19 strongly supports this, comparing to the shape of threshold voltage shift curves in Fig. 4.2, which is, basically, the total amount of additional interface charge, generated during irradiation.

Interface traps introduce a bias dependence of σ_s. Measuring this dependence enables to distinguish the acceptor/donor nature of the interface traps. However, the noise level of my data discourages from following this idea.

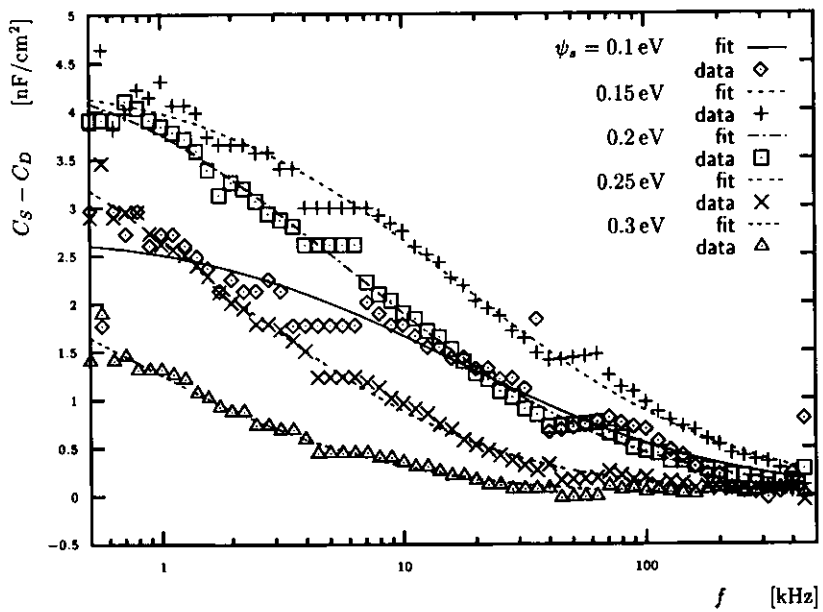


Figure 5.20: Raw data points and the fitted interface trap model curves for sample No. 07, at five different surface potentials ψ_s. The data is the silicon capacitance, offset by the depletion layer capacitance C_D, obtained from the fit.

An example fit

To give an idea how the data looks like, and how it fits to the model, Fig. 5.20 shows examples of data points, together with the fitted model curves. The

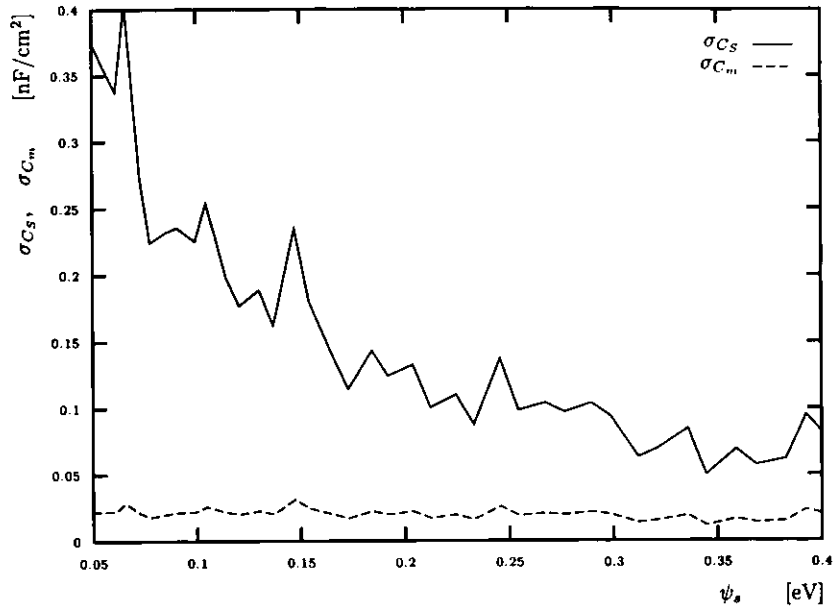


Figure 5.21: Standard deviations of the measured capacitance obtained from the fit. The solid line is the standard deviation σ_{C_S} of the semiconductor capacitance as seen by the fit, from Eq. (5.45). The dashed line is the standard deviation of the measured MOS capacitance σ_{C_m}, computed by solving Eq. (5.47). The data is from sample N° 05, after irradiation up to 117 krad.

extreme cases $\psi_s = 0.3\,\text{eV}$ and $\psi_s = 0.1\,\text{eV}$ are on the limit within which a reasonable fit can be done in this frequency range.

The capacitance noise

The fit procedure attempts to find a global minimum of the function

$$\chi^2 = \sum_i \left(C_S^{(i)} - C(\omega^{(i)})\right)^2 . \tag{5.44}$$

This is not a true χ^2, because the width of the distribution of the errors on the data points is unknown, and, therefore, not accounted for. However, the fit gives an estimate of these errors, which is, essentially, the noise of the

silicon capacitance measurement

$$\sigma^2_{C_S} = \frac{\chi^2}{N-4} \tag{5.45}$$

where N is the number of data points fitted. The silicon capacitance C_S is computed from the oxide capacitance C_{ox} and the MOS capacitance C_m

$$C_S = \frac{C_{ox}C_m}{C_{ox}-C_m}. \tag{5.46}$$

When C_S increases and C_m approaches C_{ox}, the errors on the silicon capacitance increase drastically

$$\sigma^2_{C_S} = \left(\frac{\partial C_S}{\partial C_m}\right)^2 \sigma^2_{C_m} = \left(1+\frac{C_S}{C_{ox}}\right)^4 \sigma^2_{C_m} \tag{5.47}$$

The noise observed from the fit as well as the corresponding noise of the MOS capacitance, obtained by solving Eq. (5.47), is plotted in Fig. 5.21. The graph confirms that the MOS capacitance was measured with a constant precision of $\sigma_{C_m} = 0.025\,\mathrm{nF/cm^2}$, averaged over the frequency range, independently from the bias. Considering the capacitors area $A = 0.01\,\mathrm{cm^2}$, the noise amounts to 0.25 pF or about 0.03 % of the oxide capacitance.

5.4.4 Results on interface trap properties in depletion

The interface traps are characterized by the level density D_{it} and the hole capture probability c_p. Both may depend on the surface potential, although the model relies on the assumption that they do not vary substantially within a few kT. However, there is no known reason that the hole capture probability should not be constant.

Hole capture probability

The hole capture probability c_p and the hole density at the surface p_S determine the interface trap response time, as stated in equation Eq. (5.39). The hole density is an exponential function of ψ_s.

Fig. 5.22 shows the results for the interface trap response time τ_p, obtained from samples which were irradiated at $V_{\mathrm{bias}} = 5\,\mathrm{V}$. In the center of the graph, where τ_p well matches the used frequency range, an exponential behavior is observed. Furthermore, the results are independent of the radiation dose.

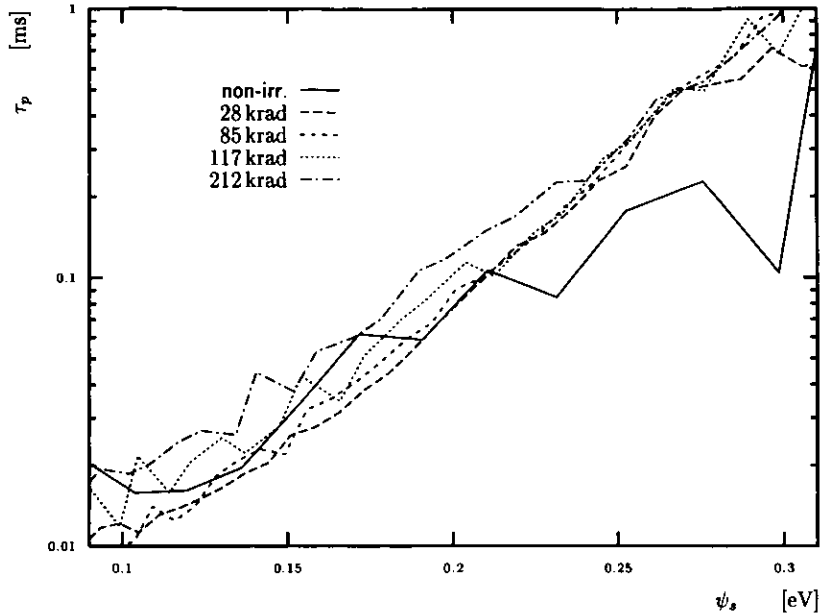


Figure 5.22: Interface trap response time vs surface potential for different irradiation doses, fitted for samples that were irradiated at $V_{\mathrm{bias}} = 5\,\mathrm{V}$.

That is no surprise, since the time constant is a characteristic of the nature of the traps, not of their amount.

Performing a linear regression on data, from all irradiated samples, for ψ_s between 0.1 eV and 0.28 eV, yields

$$c_p = 3.14{\cdot}10^{14}\,\mathrm{kHz\,cm^3} \tag{5.48}$$
$$kT = 0.045\,\mathrm{eV} \tag{5.49}$$

The measured temperature is off by a factor of about 2. Possible explanations are

- The model is wrong. From Fig. 5.20 we see that the formulas describe the data well.
- The calculation of the surface potential is wrong. Since two independent methods yield the same result, this is rather improbable.
- Equation Eq. (5.39) is wrong. There may be another effect how τ_p depends on ψ_s.

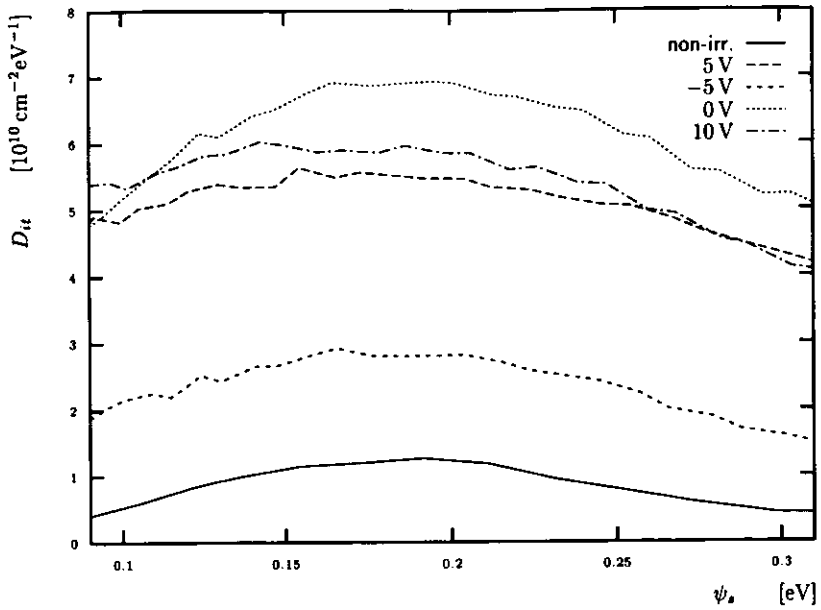


Figure 5.23: Interface trap level density profiles for different bias conditions during irradiation, fitted with a fixed hole capture probability. The radiation dose was 117 krad.

- The hole capture cross section varies within the silicon band gap.

These results are useless, as long as the temperature error is not understood.

Interface trap level density profiles

Asserting the assumption that the hole capture cross section is constant, there is no need to keep the noise introduced by fitting τ_p for each bias point. Instead, the fitted time constants in the data sets were replaced by those calculated from the parameters of the regression, and another fit was performed, this time keeping τ_p as well as σ_s constant.

Fig. 5.23 gives the result of this fit for all samples irradiated to 117 krad. The general shape of the profiles has a peak in the center of the accessible bias range. This is, most probably, a consequence of the limited frequency range of the measurement. The characteristic response time constant of the interface

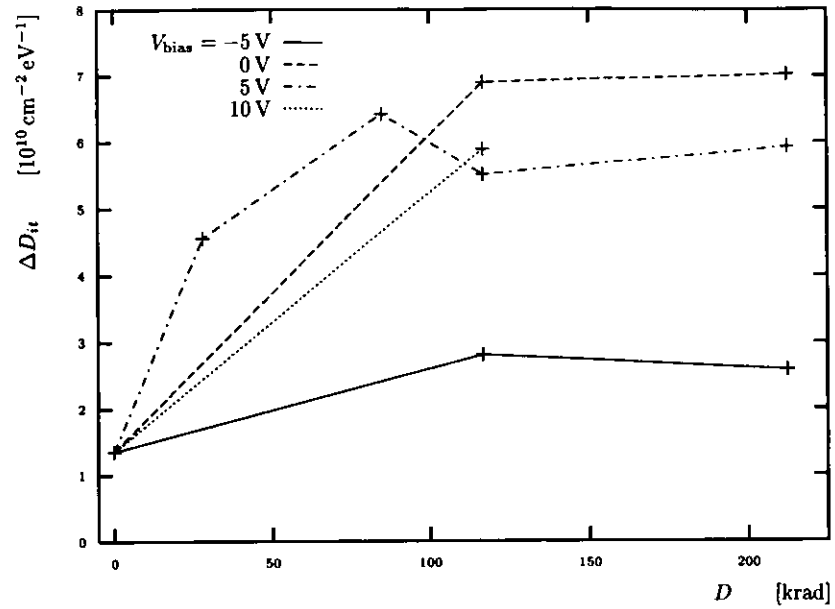


Figure 5.24: Interface trap level density vs total radiation dose, averaged from the fit results between $\psi_s = 0.17$ eV and 0.20 eV for various bias conditions.

traps τ_p changes exponentially with the surface potential. Only a very limited bias range falls into the frequency range, where reliable measurements could be done. It can hardly be a coincidence that D_{it} has a maximum in the center of this range, as suggested by Fig. 5.23, especially since interface trap density peaks in the lower half of the bandgap were not reported anywhere in the literature.

Therefore, the original goal, to measure interface trap density profiles, fails. Instead, we will trust the obtained interface trap level density, in the center of the fitted range. Fig. 5.24 shows the average of D_{it} over the range $\psi_s = 0.17 \ldots 0.20$ eV, versus total dose, for all irradiated samples. The dose and bias voltage dependence of the interface trap level density D_{it} is similar to the interface trap surface density N_{it}, estimated from the transistor static transconductance degradation in Fig. 4.6. The largest interface trap densities are observed on samples that were irradiated with zero bias. No significant increase is observed between 117 and 212 krad, for any bias condition.

5.4.5 Interface trap density summary

Interface trap densities were obtained by three different methods from capacitor measurements, and, with two methods, from transistor data. Fig. 5.25 shows the results for devices irradiated at three different bias conditions ($V_{\text{bias}} = -5, 0, 5\,\text{V}$) and with two total doses ($D = 117$ and $212\,\text{krad}$). Each data point is represented as a box with the interface trap level density value corresponding to the center of the box at the ordinate, while the extension on the abscissa marks the range of the surface potential, where the method was applied. The different methods are:

C_{it}-fit: (solid lines) The interface trap admittance fit results (Section 5.4.4). This is the only methods that gives the absolute value of the interface trap density. The data points in Fig. 5.25 are the difference of the post-irradiation and the pre-irradiation values.

Q_{if}-slope: (long dashes) The interface charge slope method (Section 5.3.1). There is no data point available for $D = 212\,\text{krad}$, $V_{\text{bias}} = 0\,\text{V}$, because this capacitor sample was not measured before irradiation.

V_{fb}, V_{mg}, V_{in}-shift: (short dashes) Interface surface density N_{it}, obtained from the difference of the flatbands, midgap, and inversion voltage shifts. (Section 5.3.1). This is transformed to a level density D_{it}, by dividing through the bulk potential $\varphi_B = 0.38\,\text{eV}$. Both data, from flatbands to midgap, and from midgap to inversion, are shown.

g_m-degrad.: (dots) This is the surface density of charged interface traps in inversion, obtained from the degradation of the static transconductance g_m of the transistors (Section 4.2.2). In the inversion regime only acceptor traps are charged, which are commonly assumed to be all located above midgap, while all donor traps are below midgap (see Section 2.2.2). Therefore, I assigned the obtained interface trap density to the region between midgap and inversion, and divided by φ_B to obtain the level density. The data measured with the annealed samples were used.

sub-thr. swing: (dash-dots) The Interface trap level density from the subthreshold swing method (Section 4.2.1). The used sub-threshold current range corresponds to the surface potential $\psi_s = 0.6 \ldots 0.78\,\text{eV}$. Both the immediate measurements and the annealed sample data is shown. The annealed samples show a larger interface trap density (drawn with slightly shorter dashes).

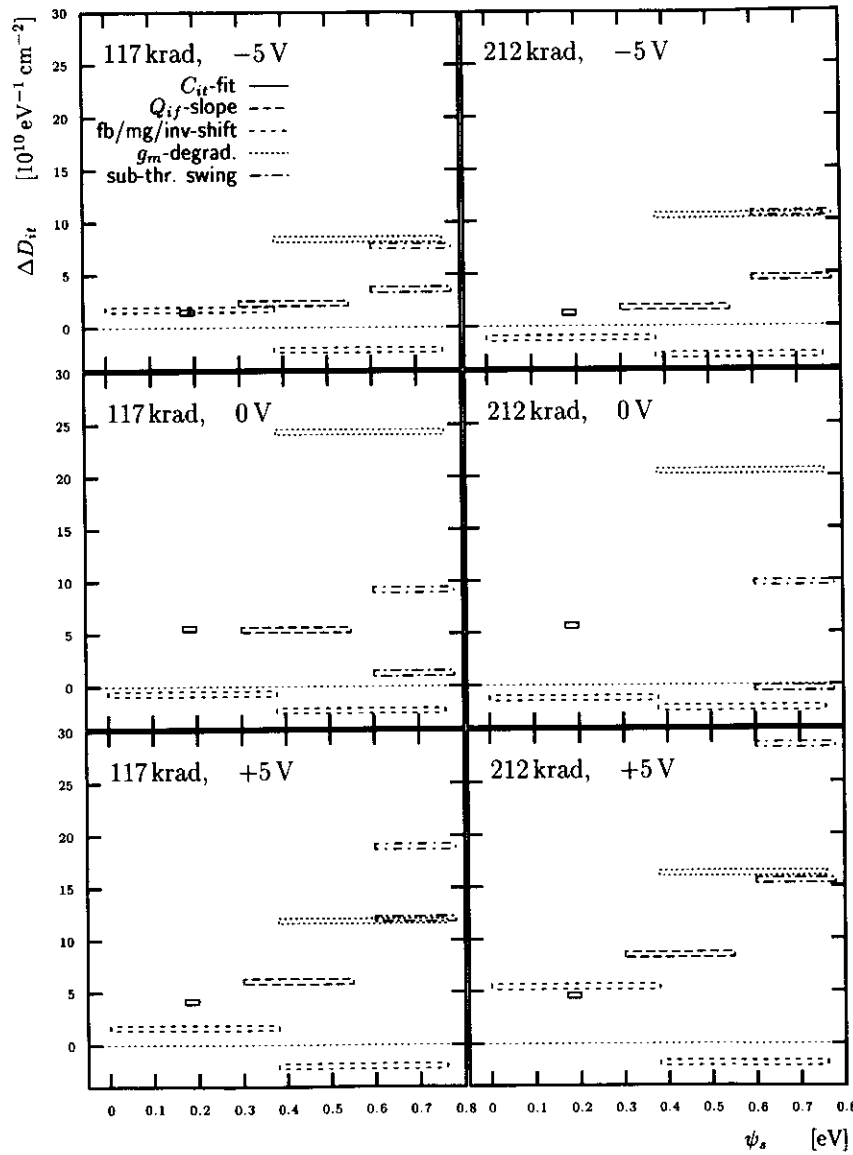


Figure 5.25: Interface trap level density versus surface potential for three bias voltage settings, −5, 0, and 5 V, and two total doses, 117 and 212 krad, obtained by five different methods (see text).

The results are inconclusive, except that all methods show that the interface trap level density is around or below $D_{it} \leq 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$, and in most cases below the limit for a precise measurement. The results of the sub-threshold swing method indicate that there may be some conversion of oxide traps to interface traps on the time scale of months after irradiation.

Chapter 6

Radiation effects in the ZEUS pipeline

Several changes in the circuits operation parameters were observed during irradiation:

- The reference current for the operational amplifiers I_{REF} decreases.
- The analog and digital supply currents I_{DDA} and I_{DDD} decrease up to a total dose of 100 krad. Higher doses cause increasing digital supply currents, while I_{DDA} continues to decrease.
- The speed of the readout amplifier decreases.
- The pedestal of the pipeline cell response changes, although the offset error of the readout amplifier keeps constant.
- The gain of the pipeline cells decreases.
- Leakage currents in the storage cells appear.

These parameters and how they are affected are explained in the following sections.

6.1 Supply currents

The supply current of a non-irradiated digital CMOS circuit is proportional to the operation frequency, and vanishes when the circuit is idle. After irradiation, sub-threshold leakage current, and threshold voltage shift approaching 0 V, in the NMOS transistors, will eventually lead to nonzero static supply current.

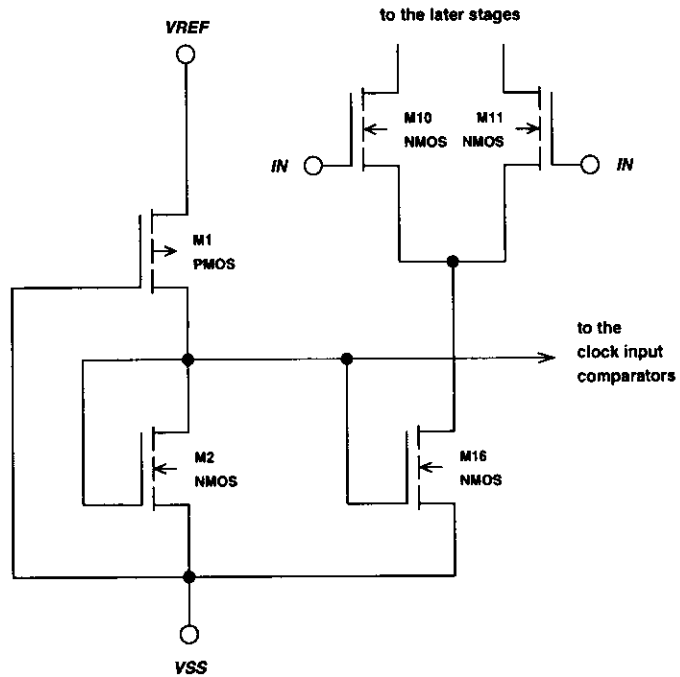


Figure 6.1: Input stage of the readout amplifier, with the current mirror circuit which provides the bias current. The current mirror, built of the transistors M2 and M16, provides a constant bias current to the differential amplifier M10/M11, which is proportional to the current applied at the VREF input. The PMOS transistor M1 acts as a resistor, to be able to control the bias current by the applied voltage, eliminating the need for an external current source. The current mirrors are built separately for each pipeline channel, although one M1/M2 branch could serve them all. They are connected to the same VREF input. However, the bias current reference for the differential input comparators is derived from the current mirror of one of the readout amplifiers.

However, there are two types of analog differential amplifiers present in the pipeline circuit, which draw a static supply current: Four readout amplifiers of the pipeline memory channels and three input comparators for the control clocks (see Fig. 1.4).

The input stage of the readout amplifier, with the current mirror circuit is shown in Fig. 6.1. The bias current, of both types of amplifiers, is set

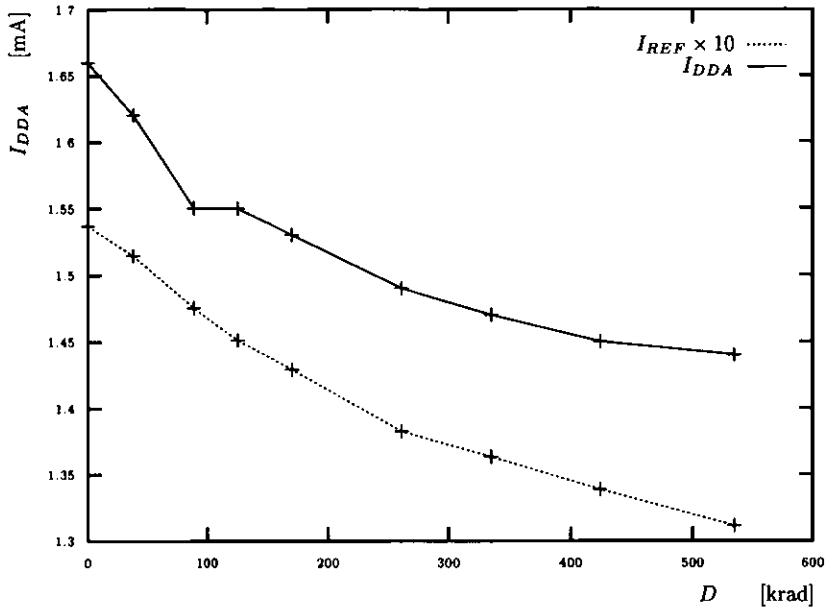


Figure 6.2: Pipeline analog supply current vs γ-dose. The solid line is the analog supply current I_{DDA} of the readout amplifiers, the dotted line is the bias reference current $I_{REF} \times 10$.

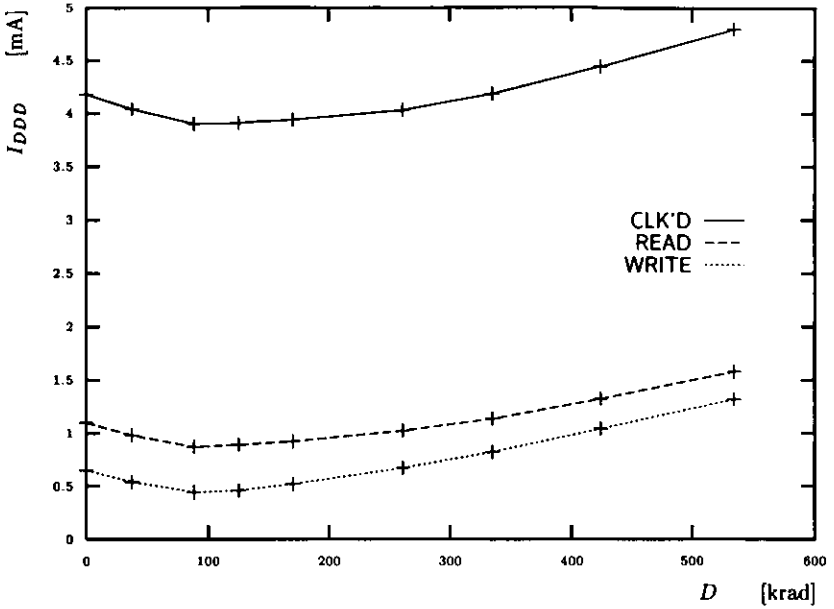


Figure 6.3: Pipeline digital supply current vs γ-dose. The current is measured with the clock pattern as applied during irradiation (solid line) and with the clocks stopped in READ/WRITE mode (dashed/dotted line).

by a common reference input V_{REF}, which feeds current mirror circuits via internal 'resistors' R_{REF}. These resistors are in fact PMOS transistors M1.

The readout amplifiers are supplied by a separate positive supply input V_{DDA}, while the input comparators are fed by the digital power supply V_{DDD}, which also serves the digital parts of the circuit.

The supply currents were measured with the control clocks stopped both in READ- and in WRITE-mode, and with the clock pattern applied as during irradiation. The analog supply current I_{DDA} does not depend on the state or frequency of the clocks. The digital supply current I_{DDD} is expected to be proportional to the frequency of the clocks, plus the bias current of the comparators. The difference of the static digital supply currents in READ and WRITE mode is caused by asymmetries of the output stage of the comparator. V_{REF} was connected through an external resistor $R_{\mathrm{EXT}} = 24\,\mathrm{k}\Omega$ to the positive power supply. The reference current I_{REF} was measured in terms of the voltage across this external resistor.

During irradiation the bias reference current I_{REF} decreases. The reason is the threshold voltage shift in the PMOS transistors M1, which makes R_{REF} more resistive. The analog and static digital supply currents decrease proportionally (Figs. 6.2 and 6.3).

After receiving a dose of about 100 krad, the digital supply current rises again (Fig. 6.3). At any given time, about half of the several thousand CMOS gates are in the logic HIGH output state. That is: the PMOS transistor is *on* and the NMOS transistor is *off*, with gate, source and bulk at zero and the drain at +10 V. An NMOS transistor in this state shows substantial sub-threshold leakage currents after irradiation. Fig. 6.4 shows the sub-threshold leakage of the NMOS transistor on the test insert, in the *off*-state, although with the reduced drain voltage $V_{ds} = 3\,\mathrm{V}$.

Surprisingly, compared to the exponential rise of the sub-threshold leakage current with the total dose, the increase of the digital supply current is rather moderate. One reason is, that those CMOS gates that are in the

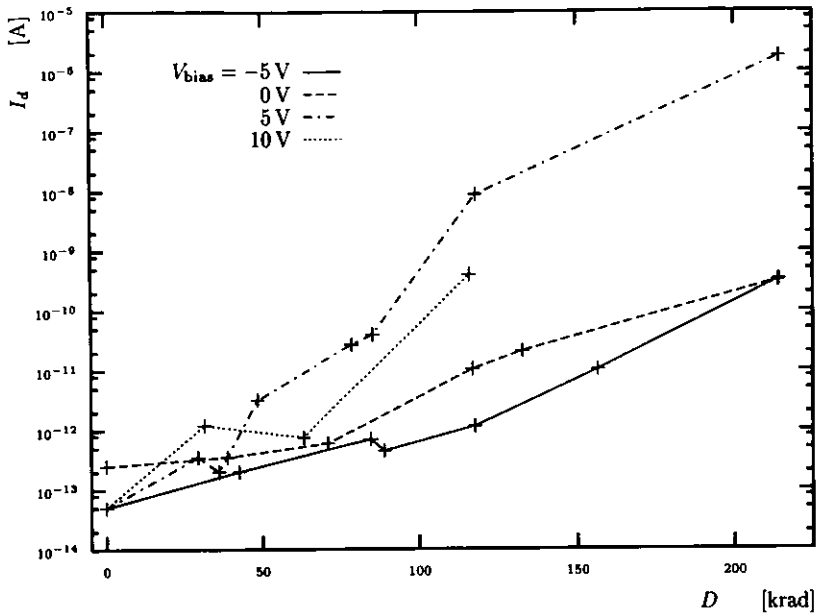


Figure 6.4: "Off state" leakage current of the NMOS transistor vs irradiation dose. $V_{ds} = 3\,V$, $V_{gs} = 0\,V$.

HIGH output state most of the time during supply current measurements are in the same state also during irradiation. The NMOS transistor is therefore irradiated with zero (negative) gate bias to the source (drain), causing comparatively low threshold voltage shift.

6.2 Pipeline gain and pedestal

The analog data path of the pipeline is designed to reproduce exactly the same voltage at the output as was sampled on the input

$$V_{OUT} = V_{IN}, \tag{6.1}$$

however, the true behavior deviates from the ideal case. For the nominal input voltage range the response is in fact linear within the requirements of the ZEUS experiment, and the deviations from Eq. (6.1) are specified by two

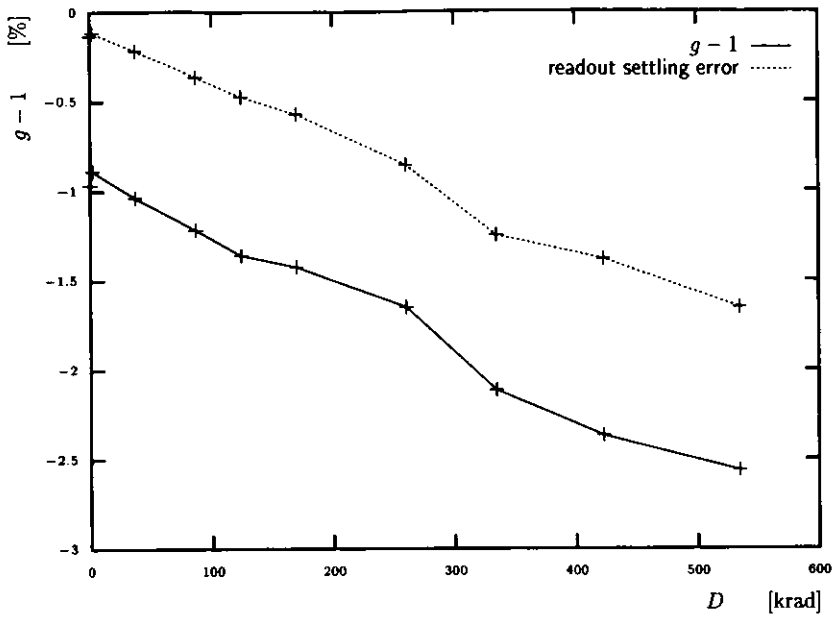


Figure 6.5: Pipeline gain vs γ-dose. The solid line is the deviation of the cell gain g from the nominal value 1, the dotted curve shows the amplifier error at the nominal readout time of 900 ns after the active CLK edge, referred to a settling time of 3 μs.

parameters: the cell gain

$$g = \frac{V_{OUT}(-2\,V) - V_{OUT}(0\,V)}{-2\,V} \tag{6.2}$$

and the offset or pedestal

$$p = V_{OUT}(0\,V), \tag{6.3}$$

thus replacing Eq. (6.1) by

$$V_{OUT} = gV_{IN} + p. \tag{6.4}$$

The gain g and pedestal p were measured for every individual storage cell.

6.2.1 Cell gain

In Fig. 6.5 the solid line shows how the average pipeline cell gain g decreases during irradiation. The apparent reason is drawn in the same figure: The

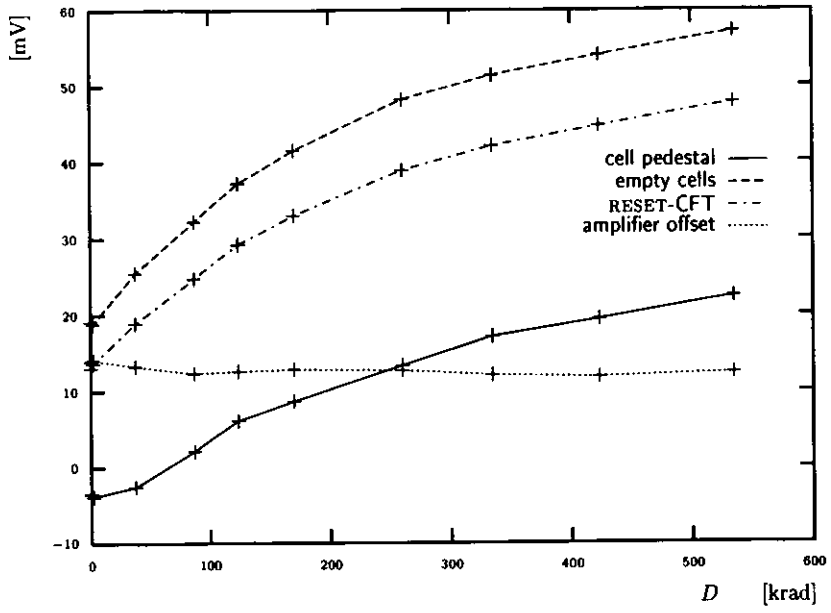


Figure 6.6: Pipeline pedestal, and related offset voltages vs γ-dose (see text).

gain was measured at the nominal output sample time about 900 ns after the CLK-edge which selected the storage cell. Comparing this to the output voltage sampled 3 μs after the CLK-edge, reveals that the readout amplifier did not reach the final state at the nominal readout sample time, and the error grows after irradiation. The readout amplifiers become slower, because of the reduced bias current.

The calorimeter readout calibration will account for gain reductions on the percent level. Larger deviations will be flagged as errors, to ensure that the resolution of the digitization does not deteriorate.

6.2.2 Cell pedestal

The transmission gates used as cell and RESET switches, were carefully optimized to compensate the *clock-feed-through* (CFT) via PMOS and NMOS gate-source capacitors. This compensation fails when threshold voltage shift occurs, and the switching time of the PMOS and NMOS transistors shift in opposite directions.

Fig. 6.6 shows various 'offset voltages' versus irradiation dose:

- The dotted line is the offset error of the readout amplifier, measured by sampling the output voltage after closing the RESET-switch. The input stages of the readout amplifier are built symmetrically, that is why we neither expect nor see any shift after irradiation. The case may be different when a pipeline is irradiated with the clocks stopped and the RESET-switch open, when one input may float to an arbitrary voltage. This kind of asymmetric bias may cause a shift of the offset error.

- The solid line is the average of the pedestal p of all cells in one pipeline channel. The pedestal shifts by about 25 mV at 500 krad.

- The dash-dotted line is the *clock-feed-through* of the RESET-switch, measured by applying the normal readout pattern except keeping the pipeline in WRITE-mode. The readout amplifier is disconnected from the rest of the pipeline channel. The output voltage is a measure for the amount of charge deposited on the readout capacitor C_R while opening the RESET-switch. Before irradiation the output voltage in this mode was almost the same as the amplifier offset voltage, confirming that the CFT was in fact well compensated.

  The RESET-CFT is running almost parallel to the cell pedestal, indicating that this is the major contribution to the pedestal shift.

- The dashed line is the *empty cell* readout, that is, cells read out during a second turn around the pipeline. Again, this curve runs parallel to the RESET-CFT. The CFT from closing and opening the cell switches should in fact compensate for the non-irradiated case, because the whole system is practically isolated from any current sources except the RESET-switch, which is (almost) open during these transitions.

The pedestal of the pipeline increases after irradiation, because the compensation of the clock-feed-through in the RESET-switch transmission gate fails due to threshold voltage shift. However, the pedestal stays well within the limits for proper operation in the ZEUS experiment.

The absolute value of the combined pedestal of the pipeline memories and the buffer memories in the buffer/multiplexer circuit are required to stay within 100 mV. If the pedestal becomes too large, the output voltage range does not fit into the input range of the analog to digital converters (ADC) used for the readout.

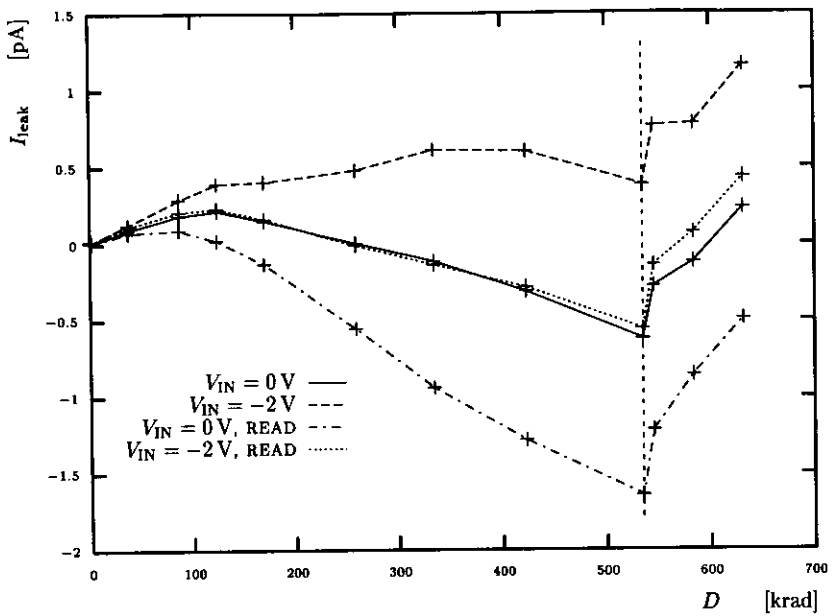


Figure 6.7: Pipeline cell leakage current vs γ-dose. The data is from channel N° 2 which had the input connected to $-2\,V$ during irradiation. The solid (dashed) lines refer to cells which were not read out during irradiation, while the dash-dotted (dotted) lines represent two cells that were discharged during half of the clock cycles, the leakage current was measured with input voltages of $V_{IN} = 0\,V$ ($-2\,V$) while the pipeline was stopped for one second in READ mode.
The plot includes data measured during annealing. The point where irradiation was stopped at 535 krad is marked by the dotted line. The abscissa continues measured in hours, with 1 krad $\equiv$ 0.56 h, to show the effect of annealing.

6.3 Storage cell leakage current

The information which is stored in a pipeline cell is represented as a charge on the storage capacitor $C_S = 1\,pF$, a MOS capacitor built on an n-well, employing gate-oxide as dielectricum and polysilicon for the upper plate (Fig. 1.6). The *hot end*, which is isolated during the storage time, is the upper plate, since it offers better isolation than the n-well. The *hot end* is further connected to the cell switch, a transmission gate built of two small transistors, one NMOS and one PMOS transistor. This is the point where some charge may be lost. The capacitor C_S is connected with, let us call it the drains of

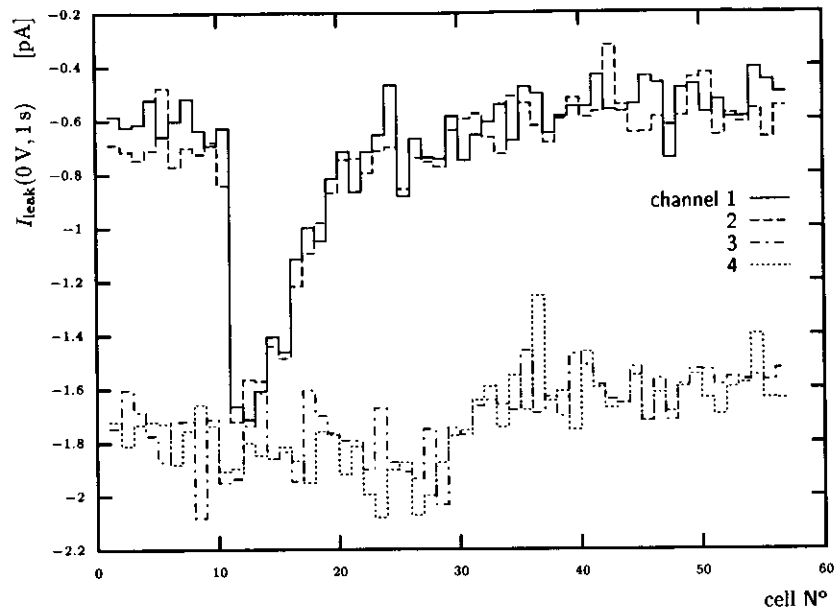


Figure 6.8: Pipeline cell leakage after irradiation vs cell number. The leakage current was measured with $V_{IN} = 0\,V$ and $\Delta t_s = 1\,s$. All four pipeline channels are shown. Channels 3 and 4 were keep floating during irradiation, while channels 1 and 2 were charged with $V_{IN} = -2\,V$.

the two transistors, while the sources are biased at the analog ground level, which is 5 V apart from each of the transistors bulk and gate voltage. In this state both transistors are well turned off. Any leakage that may occur goes from the drain to the bulk.

To obtain the leakage current, the output voltage of the pipeline cells was measured twice. Once, with the normal clock pattern yielding storage times $t_s \approx 100\,\mu s$, and again with the same clock pattern except for an extra delay after the input voltage was sampled into the cells, and the pipeline was switched back to READ mode. Comparing the output voltages of both runs gives the amount of charge that was lost during the extra delay.

$$I_{leak} = \Delta V_{OUT} \frac{C_S}{\Delta t_s} \tag{6.5}$$

I followed this procedure with different delay times $\Delta t_s = 10\,ms$ and 1 s, and with two different input voltages $V_{IN} = 0\,V$ and $-2\,V$.

The results for $t_s = 1\,\mathrm{s}$ are drawn in Fig. 6.7, including measurements during annealing. The data is from channel N° 2 which was charged with $V_{\mathrm{IN}} = -2\,\mathrm{V}$ during irradiation. The average leakage current of cells, that were not read out during the irradiation cycle and the first two cells that were discharged by READ clocks, are shown.

Non-irradiated pipeline cells exhibit negligible leakage, measurable but well below $I_{\mathrm{leak}} < 50\,\mathrm{fA}$ or $50\,\mathrm{mV/s}$. The net leakage current out of the cell is positive and typically larger with full scale input $V_{\mathrm{IN}} = -2\,\mathrm{V}$ than with zero input voltage. The conclusion is that the leakage of the NMOS transistor dominates.

Ionizing irradiation creates leakage current paths, both in the NMOS and the PMOS transistor, as there are currents of both polarities in Fig. 6.7. Low doses up to 100 krad lead to increasing positive leakage of the NMOS transistor. While continuing the irradiation eventually the negative leakage of the PMOS transistor dominates, except for full scale charged cells. The PMOS leakage shows rapid annealing, causing further net increase of the leakage, after the irradiation is stopped.

To understand what exactly this means, we need to establish the voltage level on the *hot node* of the storage cell, during storage in READ mode. With zero input, both plates of the capacitor, in fact the whole analog signal path, stay at the analog ground level all the time, or at +5 V measured from the p-substrate. When the storage capacitor was charged with $V_{\mathrm{IN}} = -2\,\mathrm{V}$ on the n-well side and the polysilicon plate at ground potential during WRITE, after switching to READ mode, the n-well is at analog ground potential, and the polysilicon plate is at +7 V referred to the p-substrate.

6.3.1 Dependence on the cell status during irradiation

Fig. 6.8 shows the cell leakage for every single cell in the pipeline after irradiation with 535 krad. Most cells in channel 1 and 2 were charged with full scale input all the time during irradiation. These cells all show almost the same leakage current.

Nine cells were discharged during READ access, cell number 11 and following. The first of these remained discharged for about half of the total cycle time, until the pipeline was switched back to WRITE mode. The following cells were discharged on successive READ clocks, resulting in shorter times in the discharged state. The steps in the curves for channels 1 and 2 in Fig. 6.8 reflect the decreasing fraction of the cycle with discharged cells.

Channels 3 and 4 had their inputs floating. The cells which were hit by

the READ clocks were discharged during that process, the charge state of the other cells were unknown. The fact that the leakage current does not differ significantly from the discharged cells may be a hint that they were discharged too. A mechanism to achieve this could be pumping charges from cell to cell via the input contact capacitance during WRITE mode.

The homogeneity and systematics of the leakage current development exclude localized defects as a source of the current.

There were in fact some problems with early batches of the redesigned pipeline, where arbitrary cells showed very large leakage currents up to several hundred pA in non-irradiated samples. These problems were traced down to the edge of the NMOS drain along the gate, and were solved by technological changes to reduce lattice distortions and the electric field in this region. This problem first indicated the sensitivity of the cell leakage to phenomena on the drain edge along the gate.

The sensitivity is confirmed by the development of the leakage current during irradiation and subsequent anneal, depending on the charge state of the cells. This was the only irradiation effect that was observed to depend on the analog input voltage during irradiation.

Leakage currents up to $I_{\mathrm{leak}} = 3\,\mathrm{pA}$ are acceptable for the application in the ZEUS experiment, as long as it appears in a limited number of cells with arbitrarily distributed cell numbers. A global limit for the cell leakage was not specified. In the ZEUS front-end electronics the storage time in the pipeline is about $t_s = 10\,\mu\mathrm{s}$ for most event triggers, but it may reach up to $200\,\mu\mathrm{s}$ when two triggers arrive in a short interval. Leakage during a constant storage time is caught by the regular electronics calibration. But, for events with extended storage times $\Delta t_s = 200\,\mu\mathrm{s}$, a leakage of the order of $I_{\mathrm{leak}} \approx 1\,\mathrm{pA}$ causes an error

$$\Delta V_{\mathrm{OUT}} = \frac{I_{\mathrm{leak}}\,\Delta t_s}{C_S} \approx 0.2\,\mathrm{mV}. \tag{6.6}$$

This looks negligible, compared to the resolution of the subsequent digitization of 1 LSB = 0.5 mV, but in the whole experiment, with 12 thousand channels, the accumulation of these small errors may fake a substantial energy deposition in the calorimeter.

Chapter 7

Conclusions

The ZEUS calorimeter readout chain uses analog pipeline memories made with a standard 2 μm CMOS technology to store detector signals during the first level trigger latency. Close to 6000 of these devices are mounted within the detector, where they are exposed to background radiation of up to 50 krad (500 Gy). A radiation tolerant NMOS transistor layout, with thin oxide extensions and guard bands was employed.

Measurements of radiation effects were carried out on the analog pipeline circuit, discrete NMOS transistors (width/length = 50/50 μm), and MOS capacitors (area = $1 \times 1\,\mathrm{mm}^2$).

γ-Radiation from a Cs^{137} source was used to irradiate a pipeline memory circuit with a total dose $D = 500$ krad (5 kGy), and a set of discrete devices with total doses up to 212 krad.

7.1 Discrete devices

Discrete NMOS transistors and MOS capacitors were irradiated under gate bias conditions of $V_{bias} = -5$, 0, +5, and +10 V. From I_d-V_{gs} characteristics in the linear region, measured before and after irradiation, I obtained

- the threshold voltage V_{th} (Section 4.1),
- interface trap level densities with the sub-threshold slope method (Section 4.2.1), and
- interface trap densities, estimated from the static transconductance degradation (Section 4.2.2).

The admittance of the MOS capacitors was measured from flatbands to the onset of inversion in the frequency range $f = 100$ Hz to 10 MHz. From this data I obtained

- the interface trap level density in weak inversion, from the slope of the radiation induced interface charge versus surface potential (Section 5.3.1),
- the flatbands, midgap, and inversion voltage shift,
- interface trap densities from the different shift of the flatbands, midgap and inversion voltage (Section 5.3.1), and
- the interface trap level density in depletion by fitting to a capacitance model (Section 5.4).

7.1.1 Threshold voltage shift

The threshold voltage of the NMOS transistors decrease linearly with the total radiation dose. The largest shift of $\Delta V_{th}/D = -6$ mV/krad was observed on samples, irradiated with a gate bias $V_{gs} = +5$ V (Fig. 4.2). After six months of shelf annealing at room temperature, the threshold voltage shift was reduced by 10 %.

The MOS structures of the capacitors is identical to the NMOS transistors. The shifts of the flatbands, midgap, and inversion voltage measured on the capacitors, agree well with the threshold voltage shift of the transistors (Fig. 5.12).

7.1.2 Interface traps

Five methods were used to obtain interface trap densities (Section 5.4.5). One method, using capacitor C-f curves, gives the absolute interface trap level density in the lower part of the bandgap (Section 5.4.4), while the remaining methods give the increase of the interface density by irradiation. These methods are:

- Using the slope of the additional interface charge after irradiation versus surface potential in the capacitors, to obtain the interface level density around midgap (Section 5.3.1).

- Using the difference of the flatbands, midgap and inversion voltage shifts of the capacitors, to obtain the integral interface density N_{it}, in the lower and upper part of the bandgap (Section 5.3.1).

- Comparing the sub-threshold current slope of the transistor characteristics, before and after irradiation, which gives the interface trap level density close to the onset of strong inversion (Section 4.2.1).

- Estimating the total interface trap density N_{it} from the degradation of the transistor static transconductance (Section 4.2.2).

The results of the different methods do not agree well. In most cases the interface trap density is too low to obtain reliable results.

The interface trap level density, in the samples before irradiation, is about $D_{it} = 1.5{\cdot}10^{10}\,\mathrm{cm^{-2}eV^{-1}}$. Interface densities measured after irradiation with 117 krad, were of the order of $D_{it} \approx 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$, with minor further increases at 212 krad.

Two methods show the largest interface trap buildup at zero bias (Figs. 5.23 and 4.6), while the others show the largest effect at $V_{\mathrm{bias}} = +5\,\mathrm{V}$ (Figs. 5.11 and 4.4).

Transistor measurements, after six months of shelf annealing at room temperature, revealed a significant increase of the interface trap densities, compared to data measured immediately after irradiation (Figs. 4.4 and 4.5). Therefore, the process of interface trap buildup occurs on a time scale which is larger than the duration of irradiation of one week. The capacitor measurements were performed one month after irradiation.

The observed transistor threshold voltage shift, in the order of 1 V, is caused by an interface charge density of $5.3{\cdot}10^{11}$ elementary charge units per square centimeter, which is one order of magnitude larger than the observed interface trap charge. Therefore, the threshold voltage shift is dominated by trapped oxide charges.

7.2 Radiation effects in the pipeline memory circuit

The following changes of performance parameters of the pipeline memory were observed after irradiation, with a total dose of $D = 500\,\mathrm{krad}$:

- A static digital supply current of about 0.75 mA appears (Fig. 6.3).

- The bias currents of the analog amplifiers in the circuit decrease by 12 % (Fig. 6.2).

  Consequently, the readout amplifiers become slower, and the gain g of the pipeline output response, measured at the nominal output settling time, decreases by 1.5 % (Fig. 6.5).

- The pedestal p of the pipeline output changes by 25 mV (Fig. 6.6).

- Storage cell leakage currents of the order of 1 pA appear, corresponding to a drift of the stored voltage by 1 V/s. Currents of both positive and negative sign occur, flowing to the negative and the positive power supply nodes, respectively (Fig. 6.7).

7.2.1 Static digital supply current

The static digital supply current is caused by leakage of NMOS transistors in the off-state, when the threshold voltage approaches 0 V

The rise of the static digital supply current is rather moderate, compared to the exponential increase of the leakage current of the off-state NMOS transistor, with the radiation dose (Fig. 6.4).

During operation of the pipeline memory circuit only a few CMOS gates, in the control logic and the selected memory cells, change their state. Most gates remain in their idle state most of the time. Those transistors that are predominantly in the off-state during operation of the circuit are in the same state during irradiation. This state, with zero gate voltage $V_{gs} = 0\,\mathrm{V}$ is less vulnerable to threshold voltage shift.

The static supply current at $D = 500\,\mathrm{krad}$ amounts to less than 10 % of the total supply current at the operation frequency of 10 MHz and is thus acceptable.

7.2.2 Analog amplifier bias currents, pipeline gain

There are two types of analog amplifiers in the pipeline memory circuit, the readout amplifier and the clock input comparators. The working point, or bias current, of these amplifiers is controlled by a bias reference input, via current mirror circuits. A critical PMOS transistor in the current mirror (M1 in Fig. 6.1) becomes more resistive due to threshold voltage shift. The result is an overall decrease of the analog supply current, and the degradation of the speed of the readout amplifiers. The pipeline output voltage does not

reach its final value after the nominal readout settling time of 900 ns, which causes the observed decrease of the pipeline gain g by 1.5 %.

In the application in the ZEUS calorimeter, the gain, as well as the pedestal (see below), are frequently calibrated for each individual storage cell. Gain deviations of several percent are tolerated by the calibration procedure. A major decrease of the pipeline gain would harm the resolution of the subsequent digitization of the signal.

7.2.3 Pipeline pedestal

A nonzero pipeline output pedestal voltage is caused by clock-feed-through (CFT) in transmission gate switches in the analog signal path of the pipeline memory. Threshold voltage shifts, in the NMOS and PMOS transistors of a transmission gate, cause changes in the CFT. The analysis of the pipeline response revealed that the observed pedestal shift $\Delta p = 25\,\mathrm{mV}$ at $D = 500\,\mathrm{krad}$ is predominantly related to the CFT of the RESET switch in the return path of the readout amplifiers (Section 6.2.2).

Pedestal values up to $\pm 100\,\mathrm{mV}$ are accepted by the readout calibration of the ZEUS calorimeter. Larger pedestals may cause the output voltage range to fall out of the acceptance of the subsequent digitization.

7.2.4 Cell leakage current

The voltage, stored in a non-irradiated pipeline memory cell, looses about 10 mV/s during the storage time, which corresponds to a leakage current of $I_{\mathrm{leak}} = 10\,\mathrm{fA}$. This is negligible, considering the typical storage time of 10 μs.

During irradiation, for doses of up to 100 krad, positive leakage currents appear, while, at higher dose, the negative leakage dominates, which reaches $I_{\mathrm{leak}} = -1.5\,\mathrm{pA}$ at 500 krad (Fig. 6.7). The leakage depends on the charge state of the cell during the measurements and during irradiation. The leakage current is uniform for cells measured and irradiated with the same charge state (Fig. 6.8).

Several days after irradiation, the negative component of the leakage current annealed, while the positive component did not.

The observed leakage current exceeds the specifications for the application in the ZEUS calorimeter. However, the effect of uniform leakage of the observed magnitude cancels in the reconstruction algorithm applied to the data.

7.3 Summary

The ZEUS analog pipeline memory circuit should work after exposure to ionizing radiation of up to 500 krad (5 kGy). This is one order of magnitude more than the radiation level expected, during the anticipated lifetime of the experiment.

The circuit suffers from minor parameter changes, caused by threshold voltage shift, in critical transistors. These changes stay within the specifications.

The most critical effect is the development of cell leakage currents. The systematics of this effect reduce the harm caused to the data, and the reliability of the calorimeter readout should not be affected.

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