Silicon Detectors for Particle Tracking at Future High-Energy Physics Experiments

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Abstract

Silicon tracking detectors are a central component of all present and planned high-energy physics experiments. For example, all experiments at the Large Hadron Collider (LHC) are equipped with silicon pixel and strip detectors. In future colliders, silicon detectors are planned to be used as tracking devices also at the ten times higher luminosity upgrade of the LHC (the so-called SuperLHC or SLHC), and at the foreseen International Linear Collider (ILC). The related R&D challenges come on one side from the harsh radiation environment close to the interaction point, on the other side from the need for a fast and precise vertex detector of unprecedented performance with minimum material. In both cases, the common trend is the use of thin detectors: a thinner detector needs a lower operating voltage and has less dark current, hence being intrinsically more radiation tolerant; in high-multiplicity environments, where an excellent two track separation is essential, a thinner detector is also superior. This thesis presents several contributions to the R&D program on silicon detectors for future particle tracking applications.

Radiation hardness studies on different silicon materials have been performed after irradiation with highly energetic electrons, which are effective in creating bulk damage in silicon and thus deteriorate the detector performance. Charge collection in irradiated silicon pixel detectors has also been simulated, in order to estimate the signals after the expected radiation levels at the SLHC, as a function of the geometrical design of the detector.

Monolithic Active Pixel Sensors (MAPS) have been proposed in recent years as a candidate technology for the vertex detector at the ILC. In this technology, sensor and readout electronics are on the same substrate, which is achievable with modern CMOS technology. It has been shown that they have an excellent performance for charged particle tracking; moreover, they can eventually be thinned down to a thickness of a few tens of μm. In this work, an experimental setup has been built for the test of a large size prototype, featuring 1 million pixels distributed on an area of 3.5 cm^2. Tests have been performed both with a radioactive source, for the calibration of the detector charge-to-voltage conversion gain, and with electron beams in order to study the detector tracking capabilities. The results from experimental tests are also compared with simulations performed with advanced simulation packages.

Kurzfassung

Siliziumspurdetektoren stellen eine zentrale Komponente aller gegenwärtigen und geplanten Hochenergiephysikexperimente (HEP) dar. Beispielsweise werden alle Experimente am Large Hadron Collider (LHC) mit Silizium-Pixel- und Streifendetektoren ausgerüstet. In zukünftigen Beschleunigerexperimenten, wie dem aufgerüsteten LHC, dem so genannten SuperLHC oder SLHC, mit seiner zehnfach höheren Luminosität oder dem geplanten International Linear Collider (ILC), sollen auch Siliziumdetektoren als Spurendetektoren eingesetzt werden. Die hier zugehörenden Herausforderungen in Bezug auf Forschung und Entwicklung kommen einerseits vom extremen Strahlungsuntergrund in der Nähe des Wechselwirkungspunktes, andererseits von der Notwendigkeit der Verwendung eines schnellen und präzisen Vertexdetektors verbunden mit einem Minimum an Masse. Für beide Herausforderungen geht die Entwicklung hin zu dünnen Detektoren, die eine geringere Betriebsspannung benötigen und einen geringeren Dunkelstrom aufweisen und daher an sich strahlungstoleranter sind. Nahe des Wechselwirkungspunktes, wo eine exzellente Trennung zweier Spuren notwendig ist, erweist sich ein dünner Detektor ebenfalls als die beste Lösung. Diese Arbeit präsentiert mehrere Beiträge zum Forschungs- und Entwicklungsprogramm für Siliziumdetektoren in zukünftigen Anwendungen zur Teilchenspurbestimmung.

Studien zur Strahlungshärte verschiedener Siliziummaterialien wurden mittels Bestrahlung mit hochenergetischer Elektronen, die zu einer Schädigung des Siliziumsubstratmaterials und dadurch zu einer Verschlechterung der Detektoreigenschaften führen, durchgeführt. Die Ladungssammlung in bestrahlten Siliziumpixeldetektoren wurde außerdem simuliert, um das Signal nach der im SLHC erwarteten Bestrahlungstärke als Funktion des geometrischen Design abschätzen zu können.

In den letzten Jahren wurden Monolithic Active Pixel Sensors (MAPS) als mögliche Technologie für den Vertexdetektor am ILC vorgeschlagen. In dieser Technologie sind Sensor- und Ausleseelektronik auf dem gleichen Substrat realisiert. Dies ist dank der CMOS Technologie möglich. Es hat sich gezeigt, dass diese Sensoren zur Spurbestimmung geladener Teilchen sehr gut geeignet sind. Außerdem können sie bis zu einer Dicke von einigen zehn μm abgedünnt werden. Im Rahmen dieser Arbeit wurde ein experimenteller Aufbau für den Test eines Prototyps, mit einer Million Pixel auf einer Fläche von 3.5 cm^2 angefertigt. Zum einen wurden zur Kalibration des Detektors in Bezug auf Verstärkung und Ladungssammlung Tests mit radioaktiven Quellen durchgeführt und zum anderen mittels eines Elektronenstrahls die Meßgenauigkeit und Nachweiswahrscheinlichkeit des Detektors untersucht. Die experimentellen Resultate wurden darüber hinaus mit Simulationen verglichen.

Contents

Chapter 1

Introduction

The goal of High-Energy Physics (HEP) is to understand the fundamental constituents of matter and the forces between them. Pursuing this goal experimentally requires the acceleration and subsequent collision of elementary particles at the highest energy possible at particle colliders. The products of these collisions are studied by large detectors which are built around the interaction point. While in general the measurement of the particle energy is provided by calorimeters, the momenta of charged particles are measured by precise tracking detectors in a magnetic field. Moreover, since particles containing heavy quarks (charm, bottom, top) have lifetimes of the order of picoseconds, they can be recognized by tracks originating from secondary decay vertices which are displaced from the collision point. Hence, high precision vertex detectors are positioned very close (order of several cm) to the interaction point, in regions with a very high particle density and correspondingly a hostile radiation environment.

Tracking detectors are usually arranged in several layers which measure the coordinates of a number of space points for track reconstruction, exploiting the ionization induced in a solid or gaseous medium by a charged particle. In most cases, a one-dimensional projection is measured in each layer by means of longitudinal detecting elements, e.g. strips or wires, and the points are reconstructed in 3 dimensions by combining layers with different orientations and arrangements. Nevertheless, very close to the interaction point the track density is so high that assignments of projections to tracks result in many ambiguities, hence a higher segmentation is required for vertex detectors.

Position-sensitive semiconductor detectors play a prominent role as tracking detectors in modern HEP experiments. Silicon microstrip and pixel detectors, for example, are being extensively used in experiments at the Large Hadron Collider (LHC). The advantage of using semiconductor detectors is due to the combination of material properties which ensure excellent detection capabilities, e.g. high efficiency and fast charge collection, and the availability of a developed technology for the fabrication of complex and very granular sensors. High charge signals can be obtained by moderate thicknesses of the sensitive volume, due to the relatively small energy required for ionization, while thanks to the advances of the planar and CMOS technologies, segmented structures for the collection of the charge signals can be implemented on the top of the detector, together with the electronics for signal amplification and readout.

An introduction to the basic properties of semiconductor detectors, with particular reference to silicon detectors, will be given in **Chapter 2**.

The future applications of silicon detectors, in particular at the planned luminosity upgrade of the LHC (the so-called SuperLHC) or at the International Linear Collider (ILC), will be highly demanding on the detector performances. While the harsh radiation environment close to the interaction point at LHC experiments is expected to be tolerated by present day silicon detectors[1], based on high-resistivity substrates, new efforts in material investigation and detector optimization are needed in order to provide resistance to the much larger radiation fluences expected at the SuperLHC. On the other side, the ILC vertex detector will require a technology with an unprecedented combination of very high segmentation, minimum amount of material, adequate readout speed and radiation tolerance, thus representing a major challenge for detector development. In this work, several contributions to the related research and development programs will be presented.

1.1 The LHC and its luminosity upgrade

The Standard Model (SM) of particle physics provides an extensive and experimentally verified theory of the interaction of fundamental particles, which includes the strong and the electroweak interactions between quarks and gluons. The mechanism of mass generation of the SM, the so-called Higgs mechanism, has not yet been verified. This is one of the main goals of general purpose experiments like ATLAS [ATL94] and CMS [CMS94] at the LHC, which is expected to start operation in 2007. Beside the search for the Higgs boson, physics at the LHC will address other fundamental questions, in particular how the SM, which in its present form is known to fail at the TeV scale, has to be extended, and other issues like the predominance of dark matter over ordinary matter, or the exploration of possible new scenarios beyond the SM that could be opened by the discovery of super-symmetric particles.

The LHC is expected to operate for at least 10 years and will collide protons at a center of mass energy of 14 TeV, with luminosities up to 10^{34} cm^{-2}s^{-1}. Bunches of 10^9 particles will collide every 25 ns, and the correspondingly high interaction rate will result in high particle fluxes and ultimately in a very harsh radiation background, especially at small distances from the beam. For example, at the position of the first pixel layer in the ATLAS silicon tracker, an annual 1 MeV neutron equivalent fluence up to $3{\cdot}10^{14}$ cm^{-2} is expected, the main contribution coming from charged hadrons (Fig. 1.1). The corresponding deterioration in the performance of silicon detectors has been studied in detail by the CERN-RD48 Collaboration, which has shown that oxygen enrichment of silicon substrates leads to a substantial improvement in the sensor radiation tolerance, thus allowing to withstand such fluence levels [RD48].

An upgrade to a factor 10 higher luminosity, up to 10^{35} cm^{-2}s^{-1}, is already discussed for the LHC, the so-called SuperLHC or SLHC [Gia02]. The SuperLHC will extend the LHC mass reach for the discovery of particles by up to 30% and achieve a much higher integrated luminosity. The higher luminosity, combined with a shorter bunch spacing of 12.5 ns, will

[1] The need to replace the inner pixel trackers after a few years of operation is nevertheless foreseen [CMSTr].

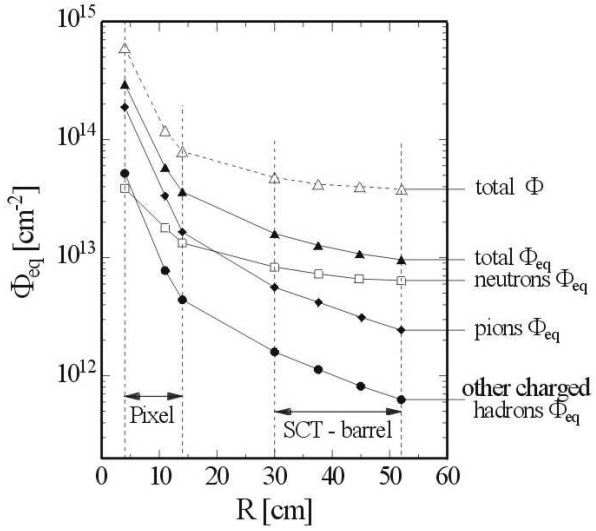

Figure 1.1: Expected particle fluences in the inner tracker of the ATLAS detector within one LHC operational year at a luminosity of 10^{34} cm^{-2}s^{-1} (from [MolTh]).

result in a higher occupancy in the tracking detectors, and above all in much higher radiation fluences: in 5 years of operation, an equivalent fluence of $1.5{\cdot}10^{16}$ cm^{-2} is expected at the position of the innermost tracking layers. Present silicon detector technologies cannot withstand such radiation levels, mainly because of the change in resistivity and the trapping of the drifting charge due to radiation-induced defects in the silicon bulk. They could possibly be used after the luminosity upgrade only if moved away from the interaction point, at radii a factor of $\sim$3 higher. Nevertheless, in order to preserve the measurement precision, tracking detectors will be also needed at smaller radii, therefore facing extreme radiation levels in a very high multiplicity environment. In 2002, the CERN-RD50 Collaboration was formed in order to concentrate the R&D efforts towards a more radiation hard detector material which could operate in these conditions [RD50]. Part of this work has been performed in the frame of this collaboration, whose research strategies concentrate both on material characterization and device engineering. **Chapter 3** will present the experimental results from radiation hardness studies performed on test-structures (diodes) manufactured from different silicon substrates, after irradiation with 900 MeV electrons. In particular, standard and oxygenated float-zone detectors will be compared with devices manufactured on thin epitaxial layers and on Czochralski substrates, materials of relatively low resistivity compared to float-zone silicon, which have been recently reconsidered for application in particle detectors. Together with the decrease in resistivity, another trend in more radiation hard detectors is the reduction of the thickness, resulting in a better control of the radiation-induced variations of the operational conditions (e.g. depletion voltage and leakage current). The first part of **Chapter 4** will show, starting from a general simulation of the induced current and of the charge collection properties in segmented silicon detectors, the simulation of trapping in irradiated thin pixel detectors up to very high particle fluences and for different sensor thicknesses, in order to predict the applicability of this detector concept at

the SuperLHC.

1.2 A vertex detector for the International Linear Collider

The next large collider facility planned by the HEP community is the International Linear Collider (ILC), an electron-positron accelerator which will initially produce collisions at a center of mass energy of 500 GeV, to be upgraded to ∼1 TeV in the second phase of operation, with a luminosity of $2{\cdot}10^{34}$ $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. A significant step towards the design of this machine has been taken in 2004, when the International Technology Recommendation Panel (ITRP) has recommended the acceleration technology based on superconducting RF cavities, developed by the TESLA collaboration [ITR04]. Since then, an international effort by laboratories and institutes from Asia, Europe and US is under way with the goal of realizing this collider and its detectors by about 2015. The physics motivation of the ILC resides indeed in its complementarity with the LHC: while the latter can achieve a larger mass reach due to the higher collision energy, it does not allow the same measurement precision the ILC can provide. In addition, the ILC has the possibility of tuning precisely the collision energy and the beams polarization. The ILC is therefore intended as a precision machine which should refine the discoveries of the LHC and make new discoveries.

An important step in the precise reconstruction of the physics processes at the ILC is the identification of the flavour of the particles containing heavy (b and c) quarks which originate from the electron-positron collisions, and decay very close to the interaction point. Hence, a precise vertex detector is needed in order to measure the tracks of the products originating from these decays, without disturbing the particle path, demanding as little material as possible in the detector volume. The major requirement for such a vertex detector is therefore a very high position resolution and an excellent two-track separation, especially in the core of high-energy jets, also for low (∼GeV/c) momentum particles: this translates in a very granular detector (e.g. a pixel detector) with a spatial resolution <5 μm and with a material budget as low as 0.1% X_0 per detecting layer [TES01].

In the proposed layout[2] (Fig. 1.2), the vertex detector consists of silicon pixel ladders arranged in 5 cylindrical concentric layers at radii ranging from 15 to 60 mm, with a polar angle coverage of $|\cos\theta|$ <0.96 for the inner layers and 0.90 for the two outer layers. The innermost layer, essential for the reconstruction of track impact parameters, is placed as close as possible to the interaction point, just outside the beam-pipe. A spatial resolution below 5 μm can be achieved with a pixel size of 20×20 $\mu\mathrm{m}^2$, while the thickness of each ladder should be ∼50 μm or smaller, in order to maintain the material budget at the desired low level, also taking into account the presence of the mechanical structures needed for support and for cooling.

Stringent requirements on the detector operation also come from the high machine background, especially due to $\mathrm{e}^+\mathrm{e}^-$ pairs originating from the so-called beamstrahlung: due to the

[2]The detector layout illustrated here is based on the one proposed in the TESLA Technical Design Report [TES01]. Other detector designs, proposing different values of the magnetic field and different arrangements of the detector layers, are also under study.

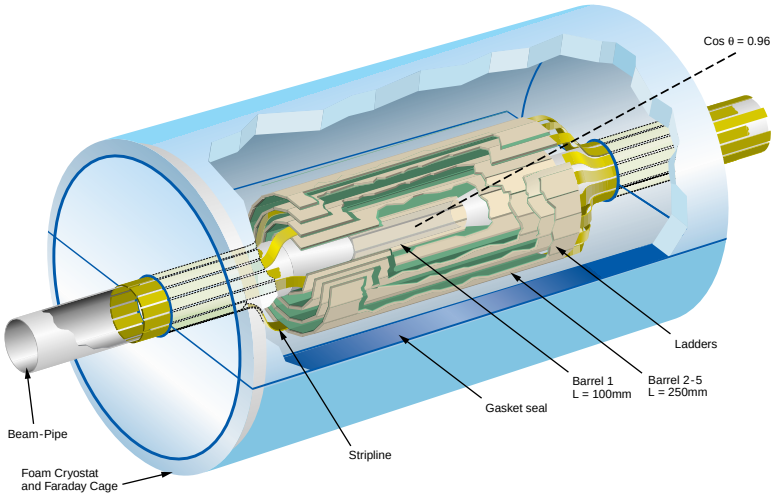

Figure 1.2: View of the proposed layout for the vertex detector at the Linear Collider (from [TES01]).

intense electromagnetic fields associated with the colliding electron and positron bunches, photons radiated from the particles in one bunch produce e^+e^- pairs in the field of the other. These pairs spiral in the magnetic field of the detector solenoid, and can possibly hit the detector layers several times. It has been estimated that in a 4 T magnetic field the number of hits per bunch crossing (BX)[3] caused by beamstrahlung pairs in the innermost layer can be as high as 5 hits/cm^2·BX, the main contribution coming from ∼10 MeV electrons, which are confined to small radii by the magnetic field [Win05b]. This results in a high detector occupancy, and therefore in a high readout speed needed to read out the vertex detector several times during one bunch train, e.g. 20 times every 50 μs for the innermost layer. The low-energy electron background has also an impact on the radiation tolerance requirements, resulting yearly in an ionizing dose of 50 krad and in a 1 MeV neutron equivalent fluence of $2{\cdot}10^{10}$ cm^{-2}yr^{-1} for non-ionizing damage at the position of the first layer. Another, less severe requirement on the radiation tolerance comes from low-energy neutrons inside the detector, expected to yield an integrated fluence of the order of 10^{10} cm^{-2}yr^{-1}.

Several pixel detector technologies are being investigated for their possible use in the vertex detector at the ILC. Present day pixel detectors based on high-resistivity float-zone silicon like the ones developed for the LHC (the so-called hybrid pixels since a separate readout chip is mounted directly on their top) do not seem to be applicable at the ILC; despite being fast and radiation hard, the presence of the readout electronics at the same time limits the position resolution and increases the material budget. Indeed, the development is oriented towards thin pixel detectors, capable of providing a low-noise performance so that also small signals from

[3]According to the proposed parameters for the ILC at the starting energy of 500 GeV, bunch trains of approximately 1 ms length will collide with a 5 Hz frequency, therefore with a duty cycle of 0.5%. Every bunch train will be composed of 2820 bunch crossings (BX), separated of 337 ns in time.

reduced thicknesses of the sensitive volume can be detected. Among other technologies, Charge-Coupled Devices (CCDs), which have been successfully used in the vertex detector of the SLD experiment [SLD97], can reach a very good granularity and be thin; nevertheless, their typical readout speed is not high enough to satisfy the ILC requirements and their radiation tolerance suffers from the fact that small charge signals are clocked through the detector bulk during readout. A promising technology is provided by DEPFET pixels [Fis02], which use a totally depleted substrate and sense the charge signals as a modulation in the current of a transistor implanted in each pixel, thus giving the first signal amplification at the pixel level.

A good trade-off between granularity, readout speed, radiation tolerance and material budget is offered by Monolithic Active Pixel Sensors (MAPS), also known as CMOS sensors, since they are fabricated in commercially available CMOS technologies. They use as sensitive volume the thin ($\sim$10 μm) epitaxial layers featured by these processes; the charges generated by the traversing particles diffuse in the epitaxial layer and are collected by small diodes implanted on the detector surface [Tur01]. One of the major advantages presented by these devices, enhanced by the trend of CMOS technology towards a very small feature size, is the integration of sensor, readout and signal processing electronics on the same substrate, thus allowing the realization of compact and highly functional detectors with a minimum material budget and at a relatively low cost.

In this work, device simulations and experimental tests of a MAPS prototype are presented. The second part of **Chapter 4** will present the simulation of the functioning of the sensor: the focus will be first on the charge collection properties as a function of the technological parameters, especially the thickness of the sensitive volume, then on the feasibility of these detectors in a deep-submicron technology, which introduces very thin epitaxial layers possibly resulting in small collected signals. **Chapter 5** will then show the experimental results obtained from the tests of a real-size (area of 3.5 cm^2) prototype, performed both with a radioactive source and in a series of beam-test experiments with a 6 GeV electron beam and a high-resolution silicon reference telescope in order to study the sensor detection performance.

The work will be concluded by a brief outlook on the current status and future perspectives of the above mentioned projects (**Chapter 6**), followed by a summary[4] of the main results presented in **Chapter 7**.

[4]More detailed summaries of the experimental results presented in Chapter 3, 4 and 5 can be found at the end of each of these chapters.

Chapter 2

Silicon Detectors

2.1 Electrical properties of semiconductors

2.1.1 Intrinsic semiconductors

Solid state materials for electrical applications are usually classified according to their resistivity. Materials with resistivity smaller than 10^{-2} Ω·cm are called conductors, materials with resistivity bigger than 10^5 Ω·cm are called insulators. In between, there are materials whose resistivity can vary over several orders of magnitude, and are called *semiconductors*. Semiconductors are called *intrinsic* when free electrons and holes can be created only by electronic excitations from the valence band to the conduction band. In practice, intrinsic semiconductors contain a negligible amount of impurities compared with the number of thermally generated electrons and holes. The occupation probability for an electronic state is given by the *Fermi distribution*

$$F(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} \tag{2.1}$$

where E_F is the Fermi energy, that is the energy at which the occupation probability of a possible state is 0.5, k_B is the Boltzmann constant and T is the absolute temperature. The density of free electrons and holes (n and p respectively) can be calculated by integrating the density of states per unity of energy times the occupation probability, yielding [Sze81]

$$n = N_C \exp\left(-\frac{E_C - E_F}{k_B T}\right) \quad \text{and} \quad p = N_V \exp\left(-\frac{E_F - E_V}{k_B T}\right) \tag{2.2}$$

where N_C, N_V are the effective densities of states in the conduction and valence band, respectively, given by

$$N_C = 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{3/2} \quad \text{and} \quad N_V = 2\left(\frac{2\pi m_h^* k_B T}{h^2}\right)^{3/2} \tag{2.3}$$

where m_e^* and m_h^* are the effective masses of electrons and holes, respectively, and h is Planck's constant. The product

$$np = n_i^2 \tag{2.4}$$

is constant at a certain temperature and equal to the square of the *intrinsic concentration* n_i. For silicon, n_i is of the order of 10^{10} cm^{-3} at room temperature. Equation 2.4 is also called *mass action law*.

The resistivity of the semiconductor bulk is given by

$$\rho = \frac{1}{q\left(\mu_e n + \mu_h p\right)} \tag{2.5}$$

where q=1.602·10^{-19} C is the elementary charge and μ_e, μ_h are the mobility of electrons and holes. For silicon, μ_e=1430 cm^2/Vs, μ_h=480 cm^2/Vs at T=300 K. A summary of fundamental constants and important properties of silicon can be found in App. A.

2.1.2 Extrinsic semiconductors

The electrical conductivity of semiconductor materials can be altered by several orders of magnitude by adding small quantities of other substances which are called *impurities*. This is the basic property on which the entire field of solid state electronics relies.

The process of replacing some atoms in the semiconductor lattice with impurities is called *doping*, and results in the creation of additional energy levels in the energy gap. The semiconductor is then called *extrinsic*. If the semiconductor atoms are replaced with atoms (for example P) with an additional valence electron, with respect to the 4 electrons needed to form the covalent bond, the impurity is called a *donor* since the additional electron can be donated to the conduction band, leaving the donor atom positively charged. If the impurity is instead missing one electron to form the covalent bond (for example B, with 3 valence electrons), it is called *acceptor* since it accepts an electron from the valence band, and leaves an hole there, thus becoming negatively charged.

If only shallow levels are considered, that is donor levels close to the conduction band and acceptor levels close to the valence band, the energies needed for the electron transitions are comparable with $k_B T$ at room temperature (26 meV), and almost all dopant atoms are ionized. For example, phosphorus introduces in silicon a donor level at $E_d = E_C - 0.044$ eV, and boron an acceptor level at $E_a = E_V + 0.046$ eV, where E_C and E_V are the energies of the bottom of the conduction band and of the top of the valence band, respectively.

If the concentration of donors N_D exceeds the concentration of acceptors N_A the material is called n-type, vice versa it is called p-type. The mass action law $n_i^2 = np$ is valid also in extrinsic semiconductors, but now $n > p$ in n-type and $p > n$ in p-type material.

2.1.3 Carrier transport in semiconductors

The movement of free carriers in the semiconductor bulk can occur either through the application of an external electric field (*drift*) or because of an inhomogeneous distribution of charge carriers (*diffusion*).

Movable charge carriers (electrons in the conduction band an holes in the valence band) are essentially free carriers, not associated with a particular lattice site. Their mean velocity at

room temperature is of the order of $\sim 10^7$ cm/s, and they scatter on imperfections within the lattice (due to thermal vibrations, impurity atoms and defects), with a typical mean free path of ~ 10 μm and a mean free time between collisions of the order of picoseconds.

In the absence of an electric field, the average displacement of free carriers due to random motion is zero. If an electric field is present, charge carriers are accelerated in between random collisions along a direction determined by the electric field, with a net average drift velocity proportional to the electric field

$$\vec{v}_{\mathrm{dr}_e} = -\mu_e \vec{E} \quad \text{and} \quad \vec{v}_{\mathrm{dr}_h} = \mu_h \vec{E} \tag{2.6}$$

for electrons and holes respectively. The proportionality between drift velocity and electric field actually holds only for fields small enough that the velocity change due to the acceleration by the electric field is small with respect to the thermal velocity, and the mean collision time is independent of the electric field. If the field is so high that the electron and hole energies become larger than the thermal energies, then strong deviations from linearity are observed and the drift velocities become independent of the electric field and reach a saturation value [Sze81].

In the case of an inhomogeneous distribution of free charge carriers in a semiconductor, even if the net average displacement of an individual charge carrier is zero in the absence of forces due to an electric field, the probability of carriers moving from a region of higher concentration to a region of lower concentration is larger than the probability of movement in the opposite direction. This effect is called *diffusion* and results in diffusion currents for electrons and holes that can be written

$$\vec{J}_{n,\mathrm{diff}} = q\, D_e \nabla n \quad \text{and} \quad \vec{J}_{p,\mathrm{diff}} = -q\, D_h \nabla p \tag{2.7}$$

where D_e, D_h are the diffusion constants and ∇n, ∇p are the gradients of the carrier concentrations.

Combining the effect of drift and diffusion, the current densities for electrons and holes can be written

$$\vec{J}_n = q\mu_e n\vec{E} + q\, D_e \nabla n \quad \text{and} \quad \vec{J}_p = q\mu_h p\vec{E} - q\, D_h \nabla p \tag{2.8}$$

where the mobility and the diffusion constants are related by the *Einstein equations*

$$D_{e,h} = \frac{k_B T}{q} \mu_{e,h}. \tag{2.9}$$

2.1.4 Carrier generation and recombination

Free electrons and holes can be generated in the semiconductor bulk by supplying the necessary energy for electrons to be lifted from the valence band to the conduction band. Common mechanisms to accomplish this are thermal generation, particularly important in semiconductors with a small band gap, excitation by electromagnetic radiation, if the energy of the absorbed photons is bigger than the band gap, and generation by charged particles losing part of their

energy while traversing the material. Every electron passing to the conduction band leaves a hole in the valence band, therefore equal numbers of electrons and holes are created simultaneously, with a *generation rate* G describing the number of electron-hole pairs generated per unit of volume and unit of time.

After the excitation, the return of the system to thermal equilibrium is due to the recombination of the excess minority charge carriers (e.g. electrons in p-type material) with the majority carriers (e.g. holes in p-type material), occurring at a *recombination rate* R. Direct band-to-band recombination processes are predominant in semiconductors with direct[1] band gap (e.g. GaAs). In semiconductors with indirect band gap (e.g. Si), where a direct band-to-band transition would require a large momentum transfer to the crystal lattice, recombination is most likely to occur in steps involving the capture and emission of electrons and holes by inter-gap generation/recombination centers.

In the assumption of low injection levels (and of recombination centers with energy levels close to midgap in the case of indirect recombination), the net recombination rate $U = R - G$ is found to be proportional to the density of excess minority carriers, the inverse of the proportionality constant giving the *charge-carrier lifetime*. Charge-carrier lifetime is an important parameter of detector-grade semiconductors, since it describes the transient behavior from a non-equilibrium charge distribution, obtained either by injection of additional carriers or by their removal, back to an equilibrium condition.

2.2 The $p - n$ junction

A $p - n$ junction is obtained when an interface between p-type and n-type semiconductor is realized on the same silicon bulk. The dopant concentration across the bulk varies from a surplus of acceptors N_A on the p side to a surplus of donors N_D on the n side. The gradient of the electron and hole densities results in the diffusion of electrons from the n region into the p region and of holes from the p into the n region. Electrons and holes recombine in the vicinity of the junction, thus creating a surplus of negative charge in the p region and of positive charge in the n region, coming from unneutralized acceptor and donor ions, respectively (Fig. 2.1). An electric field builds up, counteracting the diffusion of charge carriers and sweeping away mobile carriers in the region around the junction, creating a *space-charge region* (SCR) or *depletion region* and bringing the system into equilibrium.

2.2.1 The non-biased $p - n$ junction

The electrical properties of the $p - n$ junction can be calculated from the Poisson equation, which relates the electrostatic potential V to the charge density ϱ. In 1-dimension it is written

$$-\frac{d^2V}{dx^2} = \frac{\varrho(x)}{\epsilon_{\mathrm{Si}}\epsilon_0} \tag{2.10}$$

[1] A semiconductor is classified as *direct* if the momentum of holes at the top of the valence band and the momentum of electrons at the bottom of the conduction band are the same, as *indirect* otherwise.

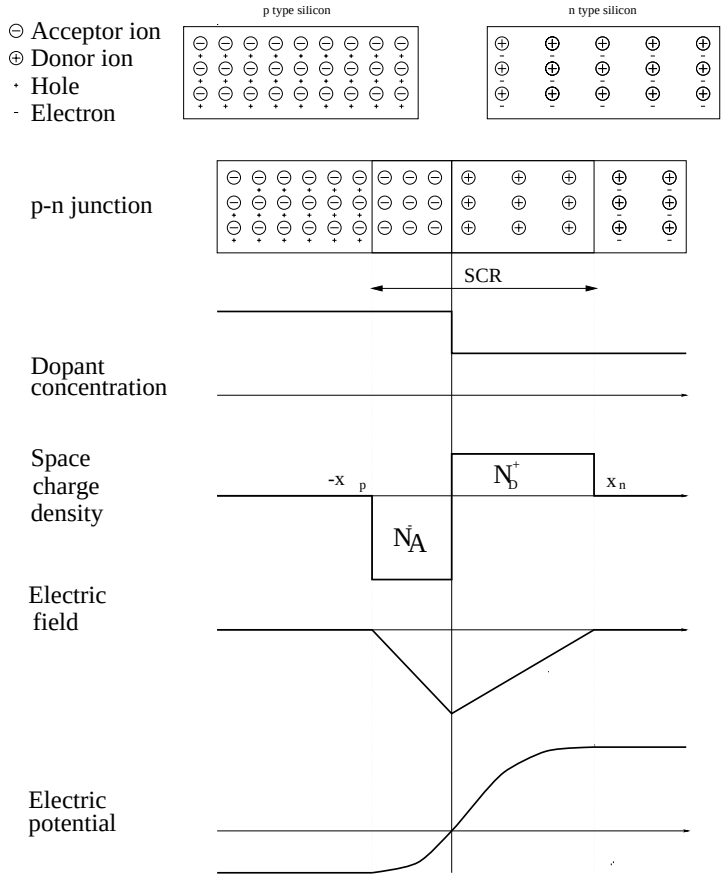

Figure 2.1: Dopant concentration, space-charge density, electric field strength and electrostatic potential of the $p-n$ junction in the abrupt junction approximation.

where ϵ_{Si} and ϵ_0 are the dielectric constant of silicon and the permittivity of vacuum, respectively. In the 1-dimensional case illustrated in Fig. 2.1 the Poisson equation is easily solved in the abrupt junction approximation, which assumes the absence of free carriers in the depletion region, and therefore $\varrho(x) = -qN_A$ for $-x_p < x < 0$ and $\varrho(x) = qN_D$ for $0 < x < x_n$. The potential difference across the depletion region in the absence of an external applied bias is called the *built-in potential*

$$V_{\mathrm{bi}} = \frac{q}{2\epsilon_{\mathrm{Si}}\epsilon_0}(N_D x_n^2 + N_A x_p^2). \tag{2.11}$$

The condition of electrical neutrality of the system requires the net charge in the depletion region to be zero. This gives

$$N_D x_n = N_A x_p \tag{2.12}$$

which shows that the depth of the depletion region on each side of the $p-n$ junction is inversely proportional to the doping concentration.

In tracking detectors the doping is usually much larger on one side of the junction than on the other. For example, in $p^+ - n$ detectors (where the plus indicates a high dopant concentration, typically $> 10^{18}$ cm^{-3}), the depth of the depletion region in the p^+ side is small compared with the one on the more weakly doped n side. Therefore, for the full depth w of the depletion region, using Eq. 2.12 and $N_A \gg N_D$, one obtains

$$w = x_p + x_n = \frac{N_D}{N_A} x_n + x_n \approx x_n \tag{2.13}$$

that is w can be approximated with the depth of the weakly doped side. Using Eq. 2.11 the depth of the depletion region can then be written

$$w = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0 V_{\mathrm{bi}}}{qN_D}}. \tag{2.14}$$

2.2.2 The biased $p - n$ junction

The depth of the depletion region can be increased by applying an external voltage V with the same polarity as the built-in potential. In Eq. 2.14, V_{bi} is then replaced by $V_{\mathrm{bi}} + V$, and considering that usually $V \gg V_{\mathrm{bi}}$ one can write the dependence of the depletion region depth on the applied bias as

$$w(V) = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0}{qN_D} V}. \tag{2.15}$$

The bias needed to deplete the full thickness D of the detector is the *full depletion voltage* V_{dep}, which is calculated from Eq. 2.15 as

$$V_{\mathrm{dep}} = \frac{qN_D D^2}{2\epsilon_{\mathrm{Si}}\epsilon_0} \tag{2.16}$$

that is the full depletion voltage depends quadratically on the detector thickness.

Low-doped detector-grade silicon substrates are usually obtained by donor compensation: the donor and acceptor concentrations are of the same order of magnitude, and the material doping is then referred to as *effective dopant concentration* N_{eff}

$$N_{\mathrm{eff}} = |N_D - N_A| \tag{2.17}$$

which replaces N_D in Eqs. 2.15 and 2.16. The effective dopant concentration N_{eff} is related to the ohmic resistivity of the silicon material. In the presence of only shallow dopants, for n-type (p-type) material $n \approx N_{\mathrm{eff}}$ ($p \approx N_{\mathrm{eff}}$) and $p \gg n$ ($n \gg p$), and Eq. 2.5 becomes

$$\rho = \frac{1}{q\,\mu_{e(h)} N_{\mathrm{eff}}}. \tag{2.18}$$

2.2.3 Capacitance of the $p-n$ junction

The capacitance of the depletion layer at a given voltage V_0 is defined as:

$$C(V_0) = \left.\frac{dQ}{dV}\right|_{V=V_0}. \tag{2.19}$$

In the abrupt junction approximation the space charge Q is given by the effective doping N_{eff} and the volume $v(V) = A \cdot w(V)$ of the depleted zone, where A is the area of the depleted zone; hence, using Eq. 2.15

$$C(V) = \frac{d}{dV}(qN_{\text{eff}}Aw(V)) = \frac{d}{dV}\left(qN_{\text{eff}}A\sqrt{\frac{2\epsilon_{\text{Si}}\epsilon_0}{qN_{\text{eff}}}V}\right) = A\sqrt{\frac{qN_{\text{eff}}\epsilon_{\text{Si}}\epsilon_0}{2V}} \tag{2.20}$$

which is valid for $w < D$ and shows that the detector capacitance decreases with $V^{-1/2}$. If the volume of the detector is completely depleted $w = D$ and the capacitance reaches its final value at

$$C_{\text{end}} = \frac{\epsilon_{\text{Si}}\epsilon_0 A}{D} \tag{2.21}$$

which is called the geometrical capacitance.

2.3 The MOS structure

The importance of silicon as a semiconductor material is also related to the possibility of obtaining, with a compatible technology, an insulator (SiO_2) with excellent electrical and mechanical properties. The properties of the oxide-silicon system are fundamental for the operation of microelectronics devices, and have also allowed the development of the planar technology (Sect. 2.4.3) and the large scale fabrication of integrated devices [Mul86].

The Metal-Oxide-Semiconductor (MOS) structure is obtained by depositing a metal layer (the *gate*) on the top of the oxide. The MOS structure forms the basis of most Charge-Coupled Devices (see Sect. 2.6.2), commonly used for optical imaging, and above all forms the essential part of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the building block of present-day integrated circuits [Tsi99].

2.3.1 Band diagram

Figure 2.2 shows the different configurations of the band diagram of an ideal MOS structure, corresponding to different applied voltages. The assumption of an ideal MOS structure implies the absence of charge in the oxide and at the silicon/oxide interface.

At the thermal equilibrium (i.e. without the application of an external voltage) the Fermi level is the same in all three materials. The application of an external voltage modifies the system thermodynamical equilibrium conditions and its charge, enriching or depleting the silicon surface of the majority carriers. Depending on the polarity and strength of the applied voltage, one can distinguish between the following operational conditions:

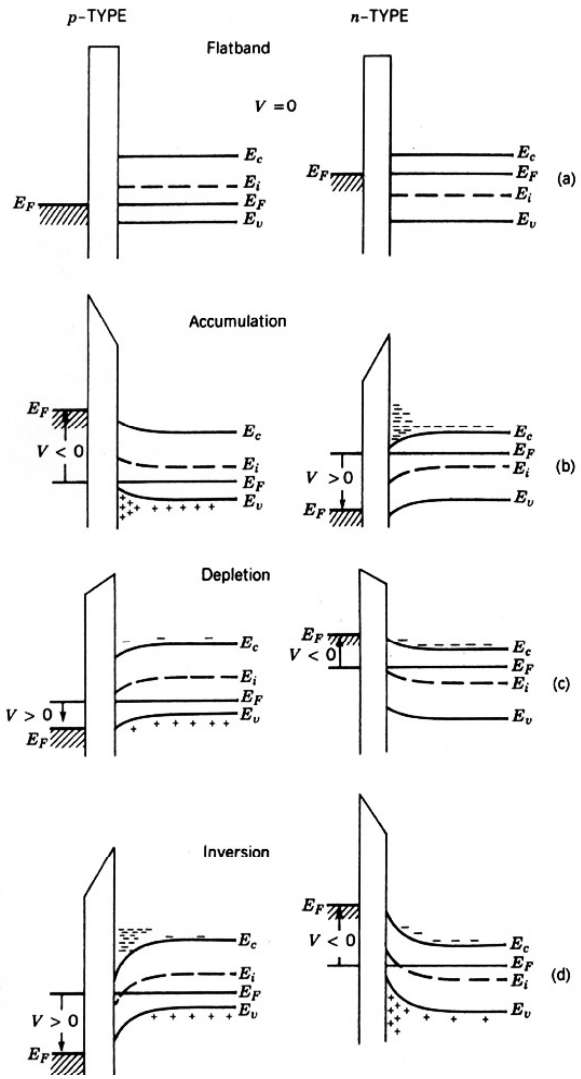

Figure 2.2: Band diagram of a MOS structure.

- **Flat-Band condition**, in which the charge carrier concentration in the semiconductor is uniform up to the boundary with the oxide and the electric field strength throughout the semiconductor is zero. Also the oxide, which is free of charge, is field-free. This condition is equivalent to an applied voltage that exactly compensates the difference between the work functions of the metal Φ_m and of the semiconductor Φ_s, the *flat-band voltage*

$$V_{FB} = \Phi_m - \Phi_s. \tag{2.22}$$

- **Accumulation**: if a voltage more negative (positive) than V_{FB} is applied to a p-type (n-type) MOS structure, the potential at the semiconductor-oxide interface will also move in

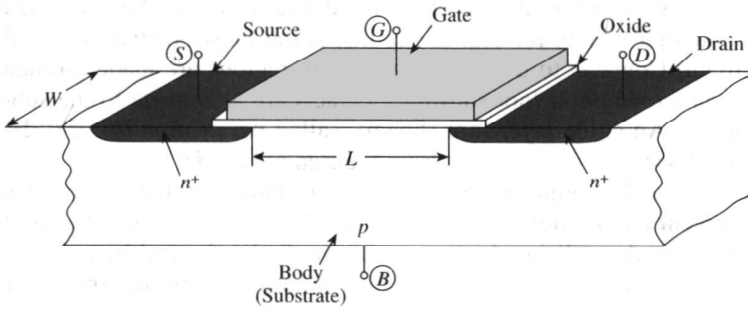

Figure 2.3: Cross-section of an n-channel MOSFET.

the negative (positive) direction, so that the energy bands will bend upwards (downwards) in the boundary region. As the Fermi level gets closer to the valence (conduction) band edge, the majority carriers are attracted towards the insulator-semiconductor interface, building a very thin conducting layer of the same type as the semiconductor.

- **Depletion**: if a voltage more positive (negative) than V_{FB} is applied to a p-type (n-type) MOS structure, the energy bands will bend downwards (upwards) in the boundary region. The majority charge carriers are then repelled from the insulator-semiconductor interface, and an insulating depleted layer, whose thickness depends on the applied voltage, forms in the surface region of the semiconductor.

- **Inversion**, which is reached when the applied voltage magnitude is further increased and the intrinsic level at the interface reaches, and eventually crosses, the Fermi level. This happens for an applied voltage defined as the *threshold voltage* V_T. At the threshold voltage, a thin conducting layer of minority carriers forms close to the insulator-semiconductor interface, followed by an insulating space-charge layer whose thickness is independent on the applied voltage.

2.3.2 The MOSFET transistor

An n-channel MOSFET device (Fig. 2.3) consists of two very asymmetrically doped $n^+ - p$ junctions (the *source* and the *drain*) joined by a MOS structure. At negative or zero gate voltage source and drain are insulated from each other. At sufficiently positive gate voltage, i.e. above the threshold voltage V_T, an inversion layer (the *channel*) will form below the gate at the semiconductor-insulator interface. Therefore drain and source will be connected by a conductive layer, whose conductivity can be controlled by the gate voltage.

Symmetrically, a p-channel MOSFET is obtained from $p^+ - n$ drain and source junctions on a n-type substrate, and the application of negative voltages is needed for operation in inversion condition.

2.3.3 Charge in the oxide and at the interface

An essential impact on the properties of real MOS structures is due to the presence of oxide charges in the SiO_2 bulk and at the Si-SiO_2 interface. Charges in the oxide bulk are due to holes trapped at defects in the oxide. These positive charges are fixed in space, and the density of sites at which they can be trapped is higher close to the Si-SiO_2 interface, where strong lattice distortions are present in the transition region from oxide to silicon. Interface defects can assume several charge states, since they can capture electrons or holes from the semiconductor.

The consequence of the presence of oxide charges on the static behavior of the MOS structure can be described in terms of the corresponding change in the flat-band voltage, which depends on the amount and distribution of the charge inside the oxide. In general, a sheet of positive charge with surface charge density σ at a distance x from the metal will cause a flat-band voltage change of $\Delta V_{FB} = -\sigma x/\epsilon_{\mathrm{ox}}\epsilon_0$, where ϵ_{ox} is the dielectric constant of the oxide. Hence, the combined effect of a surface charge density σ_{int} at the interface and a volume charge density $\varrho(x)$ in the oxide bulk will be given by

$$\Delta V_{FB} = -\frac{1}{\epsilon_{\mathrm{ox}}\epsilon_0}\left[\sigma_{\mathrm{int}} d_{\mathrm{ox}} + \int_{x=0}^{d_{\mathrm{ox}}} \varrho(x) x \mathrm{d}x\right] \tag{2.23}$$

where d_{ox} is the oxide thickness. The flat-band voltage variation ΔV_{FB} has to be added to the workfunction difference between metal and semiconductor, and will cause a corresponding variation of the threshold voltage V_T [Lut99].

An increase of the oxide charge and a modification of the interface states, with a corresponding variation of the threshold voltage, are the main consequences of the exposure of MOS structures to ionizing radiation [MaD89]. Radiation increases the number of defect states both in the oxide bulk and at the interface. Electrons and holes are generated by ionization inside the oxide: while electrons have a very high-mobility in SiO_2, and are thus rapidly collected at the interfaces (either with the metal or with silicon depending on the polarity of the gate voltage), holes diffuse slowly through the oxide and can be trapped at radiation-induced defects, leading to an increase of the positive charge in the oxide. Moreover, the holes that can reach the interface with the silicon bulk, can be trapped by interface states and thus also contribute to the increase of the positive charge. The charge state of interface states can be either positive or negative, and depends on the position of the Fermi level at the interface and therefore on the device type: in general, the charge at the interface is mainly negative in an n-MOSFET and positive in a p-MOSFET [MaD89].

On the whole, the variation of the threshold voltage due to charges in the oxide and at the interface is different for n-channel and p-channel devices: in a p-MOSFET the two contributions in Eq. 2.23 are both positive and tend to shift V_T to more negative voltages; in an n-MOSFET, the variation of the (positive) threshold voltage is in general a combination of the effect of the positive charge in the oxide bulk, which tends to decrease V_T, and the negative charge at the interface, which tends to increase it.

2.4 Silicon technology

2.4.1 Why silicon as a detector material?

Silicon presents several features which make its use favorable for particle detection. The energy band gap (1.12 eV at room temperature) is small enough to produce a large number of charge carriers per unit energy loss of the ionizing particles to be detected. In connection with this, the high material density (2.33 g/cm^3) leads to a large energy loss per traversed length of the ionizing particle (3.8 MeV/cm for a minimum ionizing particle). It is then possible to build thin detectors that still produce large enough signals to be measured. The mobility of electrons and holes is high at room temperature, and only moderately influenced by doping. The charge can thus be rapidly collected, with collection times in the order of ns, and detectors can be used in high-rate environments. The silicon band gap is on the other side large enough to have a sufficient low leakage current due to electron-hole pair generation.

As far as detector fabrication is concerned, the major advantage of silicon resides in the availability of a developed technology, which also allows the integration of detector and electronics on the same substrate. Moreover, its excellent mechanical rigidity allows the construction of self-supporting structures.

In recent years a strong effort has been also put into research of other semiconductor materials for detector application. Research has been focused especially on diamond [RD42] and silicon carbide (SiC) [RD50].

Diamond has a very large band gap (5.5 eV), and very high mobility for electrons and holes, hence diamond detectors show very fast collection times. Beside that, an excellent radiation hardness has been shown by them. The main limitation for diamond comes from the high energy of 13.1 eV needed for the creation of an electron-hole pair, which results in relatively small signals and consequently in a reduced signal-to-noise ratio. Additionally, diamond cannot rely on a developed technology like in the case of silicon, and is therefore available only at high cost.

Silicon carbide has a band gap of 3.3 eV, which would allow operation also well above room temperature. Nevertheless, the electron-hole pair creation energy is relatively high (8 eV) and the mobility of electrons and holes is significantly smaller than in silicon. Therefore, thick and low doping layers are needed in order to gain high signals, and this represents a technological challenge for detector applications.

2.4.2 Silicon growth techniques

Czochralski silicon

Most of the silicon which is nowadays used in microelectronics fabrication is grown via the Czochralski method. The starting material is polysilicon, which is melted in a rotating quartz crucible via a radio frequency field. The dopants are added into the crucible. A single seed crystal is placed from above on the surface of the liquid silicon. The crystal is slowly drawn

upwards while being rotated and the silicon solidifies in a single crystal. With this method crystals of diameter up to 50 cm can be obtained. Standard diameters used in microelectronics fabrication are 6 inches (15 cm) and 8 inches (20 cm).

The main source of impurities in the Czochralski process is the quartz crucible. The impurity with the highest concentration is usually oxygen with values up to 10^{18} cm^{-3}. The high oxygen concentration can lead to the formation of small oxygen clusters, which can be electrically active and change the electrical properties of the material. Moreover, impurities caused by the contact with the quartz crucible limit the maximum resistivity achievable with this method to about 100 Ωcm, up to 1 kΩcm with newer technologies.

The needed amount of dopants for the desired electrical properties of the material is added to the molten silicon in the crucible. The most common dopants are group III element boron (B) to obtain p-type silicon and group V element phosphorus (P) to obtain n-type silicon.

Float-zone silicon

Another possibility to grow silicon is the float-zone method. The material produced with this method has usually less contaminations than material produced with the Czochralski method, and it is also possible to grow higher resistivity material.

The starting material is again polysilicon, which is already formed in a rod. This is put into a vertical holder and a radio frequency field is used to partly melt the silicon. The molten silicon is touched from below with a seed crystal. Both the silicon rod and the seed crystal are rotating. The molten zone is then moved slowly along the rod and the silicon solidifies in a single crystal. By repeating the process many times it is possible to obtain very pure material. The process is also done under a vacuum or in an inert gaseous atmosphere, therefore the amount of impurities in the final crystal is very low. Typical concentrations of oxygen in float-zone silicon are $<10^{16}$ cm^{-3}.

Epitaxial silicon

Epitaxial layers are grown as thin films on a single crystal substrate. The crystal structure of the epitaxial silicon is defined by the lattice structure and by the surface orientation of the substrate. If the layers and the substrate are identical the process is called homoepitaxy, otherwise the process is called heteroepitaxy.

Different methods exist to grow epitaxial layers, most common ones are the Molecular Beam Epitaxy (MBE) and the Chemical Vapor Deposition (CVD). Epitaxial layers used in this work were manufactured with the CVD method, which is shortly described here in the following.

One of the basic substances employed in the growth of epitaxial layers is silicon tetrachloride ($SiCl_4$), but also other chlorosilanes or silane can be used. After removal of the native oxide layer on the top of the Czochralski substrate, the wafer undergoes a high temperature (1150°C) etching process with HCl in order to remove the top layers of silicon. Afterwards, chlorosilane,

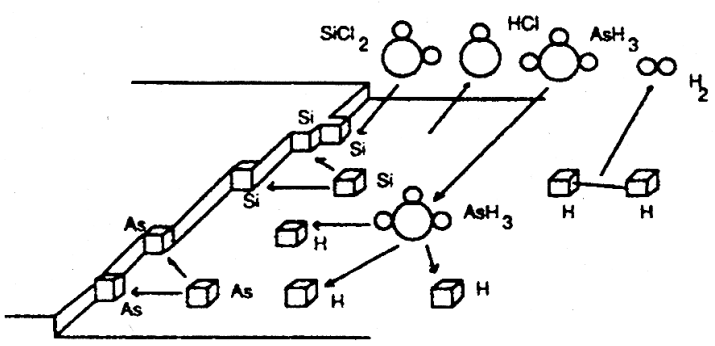

Figure 2.4: Growth of an epitaxial layer by extension of a single crystal. The silicon atoms and the dopants join the crystal structure, while the hydrogen and the chlorine atoms form hydrogen gas and hydrogen chlorine (from [Dez00]).

hydrogen and the dopants are added to the reactor at 1130°C and the following reaction occurs

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl. \tag{2.24}$$

At this temperature the silicon atoms can arrange and attach themselves to the crystal lattice of the substrate. The basic growth process is illustrated in Fig. 2.4.

There are two possibilities for doping the epitaxial layers. The first one is autodoping, which is caused by dopant atoms evaporated from the substrate. Besides the dopants, also other impurities will diffuse from the substrate into the epitaxial layers (e.g. oxygen, carbon, hydrogen and nitrogen). Even though the epitaxial process is much "cleaner" than the Czochralski one, these impurities will be present inside the final material, especially oxygen, since the Czochralski substrate is very oxygen rich. The other possibility for doping is intentional doping, which can be accomplished by introducing dopant gas into the reactor (commonly used are phosphine, PH_3 or diborane, B_2H_6). Doping of the layers is due to the same mechanism as growth: the dopants are built in the layer instead of silicon atoms.

2.4.3 Silicon processing

The planar process

The use of the planar processing technology for detector fabrication was first demonstrated in [Kem80]. After the crystal growth the ingots are cut into thin wafers, whose surfaces are polished on one or both sides. These polished wafers are the starting material for the detector processing. The following steps are the most commonly used in planar technology:

- **Oxidation**: silicon dioxide (SiO_2) is used to passivate open bonds at the silicon surface. This is done either by heating silicon in dry oxygen at ∼1000°C or in a wet H_2O atmosphere, since the rate of oxide growth is enhanced by hydrogen. In both cases oxygen

diffuses through the layer of oxide already grown at the Si/SiO_2 interface, creating an oxygen profile inside the silicon bulk.

- **Photolithography** is used to transfer structures on the silicon wafer. The surface of the wafer is covered with a thin layer of a photosensitive resin, which is illuminated through a mask after drying. Afterwards the photoresist is developed and, if for example the photoresist is positive, the illuminated resist dissolves leaving the wafer surface in the corresponding regions unprotected and exposed to the subsequent processing steps.
- **Chemical etching** is used to remove the oxide in the regions which are not protected by the photoresist. Etching can be either wet etching or dry ion etching, the latter having the disadvantage of introducing radiation damage in the oxide.
- **Doping** is then aimed at changing the doping concentration in specific regions of the silicon wafer (e.g. to create a $p-n$ junction), with respect to the uniform doping which is present after crystal growth. This is done either by *diffusion* or *implantation*. In diffusion doping a defined amount of dopants is deposited on the wafer surface and allowed to move into the semiconductor volume, usually by heating at elevated temperatures during the process. Implantation is done by bombarding the wafer with a defocused ion beam of defined energy. The ions will be stopped in the semiconductor in the regions that have been opened in the preceding photolithographic and etching steps.
- **Thermal treatments** are then necessary to move the dopants, for example if introduced by ion implantation, from interstitial positions into regular lattice sites, and also to repair the damage which has occurred during the implantation process.
- **Metal deposition**: the contacts of the semiconductor structures are covered with thin metal layers to achieve a low resistivity connection to the outside. The most commonly used metal is Al, which can be deposited either by evaporation or by sputtering (a target of the material is bombarded with excited ions that knock atoms from the target; these atoms are then deposited on the target).
- **Final passivation** is the last processing step, in which the wafer is covered, except for the electrical connections, with an electrically insulating layer to protect the structures against chemical poisoning and environmental changes. Silicon oxide and silicon nitride (Si_3N_4) are most commonly used for this purpose.

The CMOS technology

The most common integrated circuit technologies are based on MOS transistors (see Sect. 2.3). Besides the relative simplicity in fabrication, low power consumption in digital applications is a strong point for the use of MOSFETs. Mostly used is the *CMOS* (Complementary Metal-Oxide-Semiconductor) technology, which uses in its simplest form only n- and p-channel transistors as active devices. These complementary transistors are insulated from each other by putting one of them into a well with opposite doping with respect to the original bulk material (this is the so-called bulk CMOS process, see Fig. 2.5a).

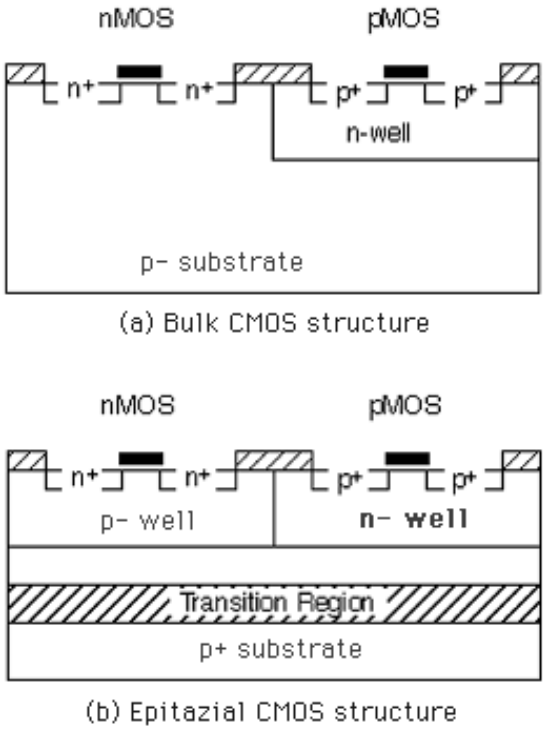

Figure 2.5: Cross sections of bulk (a) and epitaxial (b) CMOS processes.

A special problem with CMOS electronics is *latchup*, an effect observed when the $p-n$ junctions in CMOS devices produce parasitic transistors, which can unintentionally turn on the device. An alternative approach in CMOS fabrication is the *twin well* or *twin tube*, in which the active regions of n-MOS and p-MOS transistors are defined by a p-well and a n-well implanted on an epitaxial layer, grown on a highly-doped p^+ substrate (see Fig. 2.5b). The high doping reduces the substrate resistance, making latchup less likely compared to standard bulk processes.

2.5 Position sensitive silicon detectors

2.5.1 Principle of operation

The basic element of a silicon detector is a $p^+ - n$ diode on a high ohmic n-type substrate[2] operated under reverse bias, usually at voltages above the full depletion voltage in order to use the whole volume for charge collection. A simple model of such an element is sketched in Fig. 2.6. On the bottom side of the detector, the ohmic contact between the detector bulk and

[2]In the following we will refer always to detectors manufactured on n-type substrates. The fabrication of detectors on p-substrate is also possible.

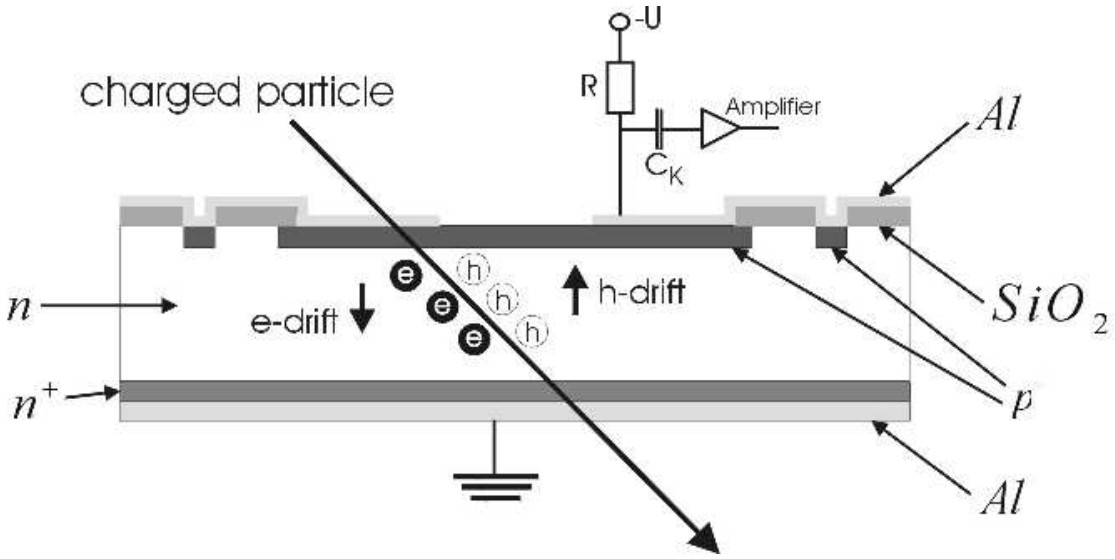

Figure 2.6: Schematic illustration of the detection principle in a silicon detector. A charged particle is traversing the depleted detector volume creating electron-hole pairs by ionization.

the back-side metallization is usually provided with a layer of n^+ silicon.

If an ionizing particle is traversing the detector sensitive volume, electron-hole pairs are created along its path. The electric field in the depleted volume separates electrons and holes, which drift to the positive, respectively negative electrode inducing a current in the readout circuit. This current is amplified and integrated by a charge sensitive amplifier resulting in an output voltage which is proportional to the collected charge.

If the particle is stopped inside the detector, the measured charge is proportional to the energy of the particle, otherwise the particle will traverse the detector and the measured signal will be proportional to the energy loss of the particle. The energy loss is due to Coulomb interaction, Bremsstrahlung and scattering with the electrons and the core of the silicon atoms. The mean energy needed for the creation of an electron-hole pair in silicon is of 3.6 eV.

In a silicon detector with a thickness of 300 μm the most probable value of electron-hole pairs generated by a minimum ionizing particle (mip) is of 24000. For these particles the energy loss is almost proportional to the path length through the detector.

2.5.2 Segmented detectors

A position-sensitive silicon detector is in general an array of $p-n$ junctions produced on the same wafer. Usually the p^+ side is segmented[3], and the segmentation determines how the position is read out.

[3]Also n^+ implants on a n-type substrate can be segmented ($n^+ - n$ detectors).

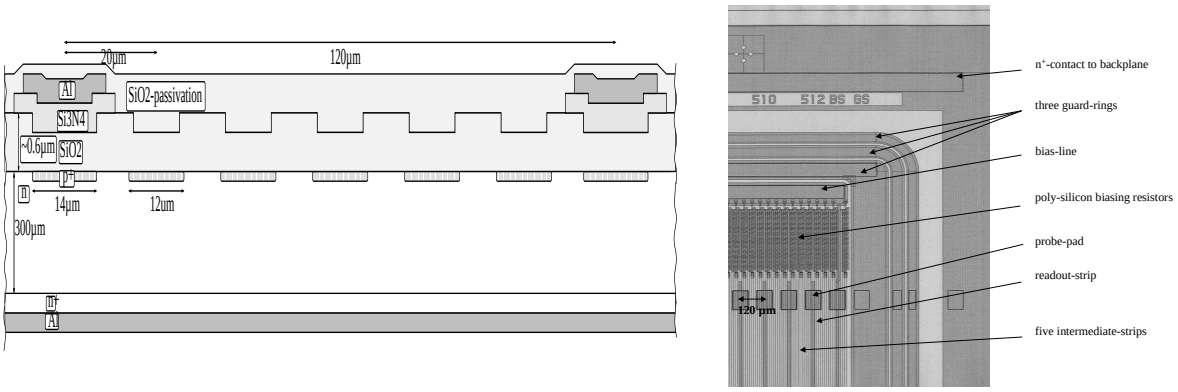

Figure 2.7: Cross section of the silicon microstrip sensors of the ZEUS micro-vertex detector (left) in the region between two readout strips, with a pitch of 120 μm. Five intermediate strips can be seen between the two readout strips. The picture on the right shows a detail of the corner of one module (from [MilTh]).

Silicon microstrip detectors

Silicon microstrip detectors are produced by segmenting the p^+ side into strips over the full length of the detector. The strips are usually from few tens to few hundreds of μm apart, with the detector position resolution increasing with the decreasing strip pitch. The segmented side is usually covered by a few μm layers of SiO_2 or Si_3N_4, which protect the wafer during fabrication (Sect. 2.4.3) but also the detector itself. Aluminum strips allowing a good ohmic contact with the electronics can be placed directly on the p^+ strips (DC coupled detectors) or on a thin oxide or nitride layer, in which case the p^+ strips are capacitively connected to the electronics (AC coupled detectors). The latter solution is more expensive, due to the additional steps needed in the production, however capacitive coupling prevents leakage currents to flow through the electronics. The electrical connection between the strips and the readout electronics is usually realized via thin wires (wire-bonding).

The strip potential is defined by the electronics in the case of DC coupling, while for AC coupled detectors the implant strips need to be grounded separately. This is usually done by means of polysilicon resistors (from few 10 kΩ to a few 100 MΩ). In addition, silicon microstrip detectors usually have guard-rings surrounding the sensitive area which act as sinks for the surface currents from the edges of the detector. As an example, Fig. 2.7 shows on the left side the cross-section of the silicon microstrip sensors of the micro-vertex detector of the ZEUS experiment at HERA, and on the right side a mask detail of the corner of one module.

A second coordinate determination can be provided by the segmentation of the n^+ layer on the detector bottom side into strips under some angle with respect to the p^+ strips on the top side, giving a *double-sided* detector. In this case the bottom detector surface has also to be passivated with oxide, and additional isolation structures are required between the n^+ strips in order to prevent that accumulation layers at the oxide interface form conductive paths between

the strips that can short-circuit them. Most commonly used isolation techniques are inserting p^+ strips (called p-stop) between the n^+ strips, or inserting a so-called p-spray layer of lowly doped p-type silicon. Manufacturing of double-sided detectors requires however more steps in the fabrication process and therefore a higher cost, comparable with the production cost of two single-sided detectors glued back-to-back.

Silicon pixel detectors

The planar process allows also the segmentation of one of the detector sides into a two-dimensional array of pixels. In this case an unambiguous 2-dimensional information about the position of the hit is achieved. The lateral size of pixels usually ranges between a few tens of μm and a few mm. The number of pixels and by that the number of readout channels increases linearly with the active area of the detector, while for silicon strip detectors the number of readout channels increases with the square root of the active detector area. A higher cost of pixel detectors results from the complexity of the readout electronics and of the mounting techniques, especially when the pixel dimensions are small.

The use of pixel detectors is nevertheless inevitable in environments in which the detector occupancy is high, i.e. the sensor is traversed by many close-by particles. The use of strip detectors is in this case impossible due to ambiguities in the determination of the hit positions. Consequently, and also because of their high position resolution, pixel detectors are most often used very close to the interaction point. Section 2.6 will present a short review of pixel detector technologies on which research is on-going for particle tracking applications.

2.5.3 Signal formation in silicon detectors

The mobile charges generated by a traversing ionizing particle in a silicon detector drift in the electric field and induce a current pulse on the detector electrodes, if these are connected to low impedance. The induced current can be derived from the Reciprocity Theorem of the induced charge, which defines the relation of the potential and charges on a multi-electrode system for two different states [KraTh]. If V_n, Q_n and V_n', Q_n' denote the potential of one electrode before and after the change of state, respectively, then the reciprocity theorem can be written:

$$\sum_{electrodes} Q_n' V_n = \sum_{electrodes} Q_n V_n'. \tag{2.25}$$

A drifting charge q can also be seen as a small electrode at the point m in the detector, with potential V_m. By applying the Reciprocity theorem, it can be shown (App. B) that the induced current I_s flowing in the sensing electrode s at the potential V_s can be calculated as

$$I_s = -q \nabla U_w \cdot \vec{v}_{\mathrm{dr}} \tag{2.26}$$

where $\vec{v}_{\mathrm{dr}}$ is the drift velocity of the charge q in the electric field, and $U_w = V_m/V_s$ is the so-called *weighting potential*. As the charge q moves, it sees different U_w with time. The gradient of the

weighting potential, needed for evaluation of equation 2.26, is commonly called the *weighting field* or *Ramo's field*

$$\vec{E}_w = -\nabla U_w \tag{2.27}$$

and is a measure of the electrostatic coupling between point m and the sensing electrode s. U_w is obtained by solving the Laplace equation with the boundary conditions following from its definition

- $U_w = V_m/V_s = 1$ at the surface of the sensing electrode (electrodes m and s are connected);
- $U_w = V_m/V_s = 0$ at the surface of any other electrode n connected to low impedance (electrodes m and n are connected).

Since the weighting field is a measure of the electrostatic coupling between the moving charge and the sensing electrode, it is calculated as if there were a vacuum between the electrodes [Rad88]. Dielectric properties of the material between the electrodes or even the presence of fixed space charge, as in the case of a reversely biased $p-n$ junction, do not enter in the calculation. Therefore, the weighting field depends only on the geometry of the electrodes, and is in general quite different from the real electric field.

If all the electrodes are connected to low impedance, the induced current flowing in the sensing electrode is finally written according to the Ramo's theorem [Ram39]

$$I_s(t) = q\vec{E}_w(\vec{r}(t))\vec{v}_{\mathrm{dr}}(\vec{r}(t)) \tag{2.28}$$

where $\vec{r}(t)$ indicates the drifting charge trajectory, which is a solution of the equation of motion in the electric field $\vec{E}(\vec{r})$

$$\frac{d\vec{r}}{dt} = \mu\vec{E}(\vec{r}). \tag{2.29}$$

The mobility μ in general depends on the electric field strength, on the temperature and on the effective dopant concentration [Sel90].

2.6 Pixel technologies for particle detectors

2.6.1 Hybrid Pixel Detectors

Hybrid pixel detectors use high-resistivity silicon substrates like in the case of microstrip detectors. The pixel array sensor and the corresponding readout chip are processed independently and are interconnected only at a later production stage. This approach makes it possible to combine sensor radiation hardness and high readout speed, for example in order to meet the requirements for detectors close to the interaction point at the LHC.

The readout electronics is usually built in standard CMOS technology, and has an architecture which is similar to the one of a classical microstrip detector readout. Detector and readout electronics are usually connected by the *bump bonding* technique: small balls of solder, indium or gold establish the electrical and mechanical connection between the single pixel and its readout

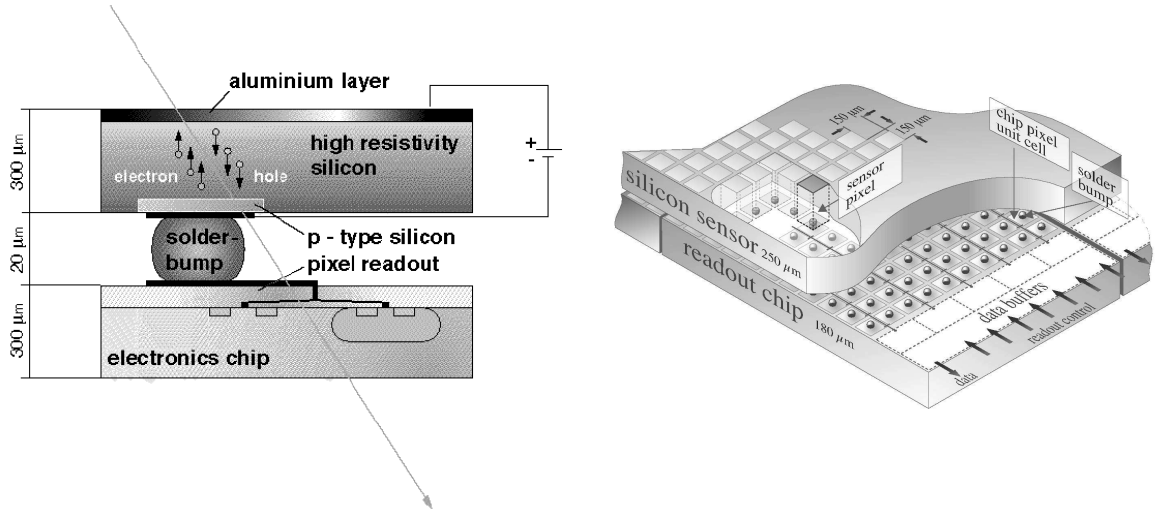

Figure 2.8: Principle of hybrid pixels detectors (left), in which the readout electronics is mounted on top of the silicon sensor by means of the bump-bonding technique, and simplified sketch of the CMS pixel detectors (right, from [CMSTr]).

circuit which is placed on top of it (left part of Fig. 2.8). The size of the pixel is therefore essentially determined, and limited, by the size of the readout chip. Example of pixel sizes employed in present-day hybrid pixel detectors are of 150×150 μm^2 for the CMS and 50×400 μm^2 for the ATLAS pixel detectors. As an example, a sketch of the CMS pixel detector is shown in the right part of Fig. 2.8.

Other disadvantages of hybrid pixel detectors, besides the limited granularity and the complexity of the interconnections, come from the amount of material introduced and the relatively high power dissipation, which make their utilization not favorable in terms of material budget.

2.6.2 Charge-Coupled Devices

The charge-coupling principle was first presented by Boyle and Smith in 1970 [Boy70], while the first Charge-Coupled Device (CCD) was demonstrated by Amelio, Tompsett and Smith [Ame70]. CCDs are extensively used as imaging devices, but have also been successfully used as tracking detectors, for example in the vertex detector of the SLD experiment [SLD97], thanks to the possibility of fabricating very thin devices with a very high spatial resolution (e.g. pixels of 20×20 μm^2 were used at SLD).

In its simplest form a CCD is an array of closely spaced MOS capacitors on a continuous oxide layer that covers the same semiconductor substrate [Sze81]. The spacing between the capacitors is small enough to let the free charge stored in the inversion layer of one of them to be transferred in the channel of the adjacent device. Under the application of a proper sequence of clock voltages to the MOS gates, a CCD can store and transfer charge packets in a controlled

way across the substrate (Fig. 2.9).

The most common types of CCDs are the surface-channel (SCCD) and buried-channel (BCCD). In the first, charge is stored and transferred at the semiconductor surface, whereas in the latter the doping of the semiconductor substrate is modified so that the charge packets are stored and transferred more deeply into the bulk of the semiconductor. Different types of electrode configurations and clocking techniques can be used in making a practical CCD.

A limitation in the operation of CCD as particle detectors is their intrinsically low read-out speed, due to the fact that the charge has to be transferred for long distances across the detector bulk before reaching the readout line. Another limitation of CCDs, with respect to their application as tracking detectors, is their sensitivity to radiation damage, which results in the degradation of the charge transfer efficiency due to trapping of the signal charges at radiation-induced defects in the detector bulk.

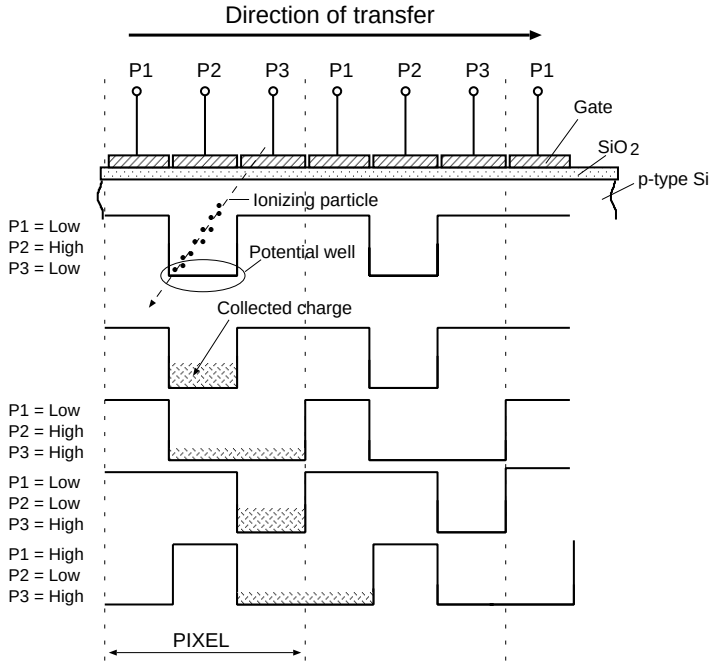

Figure 2.9: Principle of CCD operation. The charge generated by an ionizing particle is collected in a potential well below one MOS gate, and is then clocked across the substrate by means of a proper sequence of clock voltages applied to the MOS gates.

2.6.3 Monolithic Active Pixel Sensors

Monolithic pixel sensors were first proposed in the early 90's as an alternative to CCDs in visible light imaging [Die97, Koz99], which required simple, low-power, low-cost imaging devices. Their development rapidly found applications in a variety of fields, ranging from space devices, medical

imaging and consumer electronics [Fos97]. They are currently referred to also as CMOS imagers, since they are usually fabricated in a standard CMOS VLSI technology. Two main types of sensors exist: the Passive Pixel Sensor (PPS), in which a photodiode is integrated in the pixel together with selection switches, which connect the photodiode directly to the output line for readout; the Active Pixel Sensor (APS), in which an amplifier is integrated in each pixel and directly buffers the charge signal. Today most CMOS imagers have an APS structure because of its better performance. Their basic cell architecture is shown in Fig. 2.10. A photodiode is integrated on an individual pixel together with the first signal processing electronics, constituted by three transistors: a reset switch M1, which resets the photodiode to reverse bias, the input M2 of a source follower and a row selection switch M3; the source follower current source, common to an entire row, and the column selection switch are located outside the pixel.

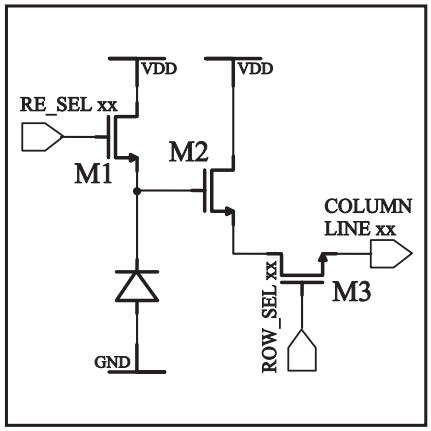

Figure 2.10: Baseline pixel architecture of a CMOS imager.

The main advantages featured by CMOS sensors with respect to the more used CCDs are [Tur01]:

- they are fabricated in a fully standard VLSI technology, so their cost is low;
- several functionalities can be integrated on the same sensor substrate;
- the circuitry in each pixel is active only during the readout, therefore the power consumption may be also considerably reduced.

Common CMOS sensors are not suitable for particle tracking applications. In fact, the detector part is made of low resistivity silicon, the depletion region is shallow and consequently the charge collection efficiency is poor. In addition, because of the presence of the transistors, the *fill factor*, that is the fraction of the pixel area that is sensitive to light, can be relatively low (order of 30%). Moreover, issues like radiation tolerance, fast readout and integration of data sparsification functionalities are not crucial for most visible light sensors. Therefore,

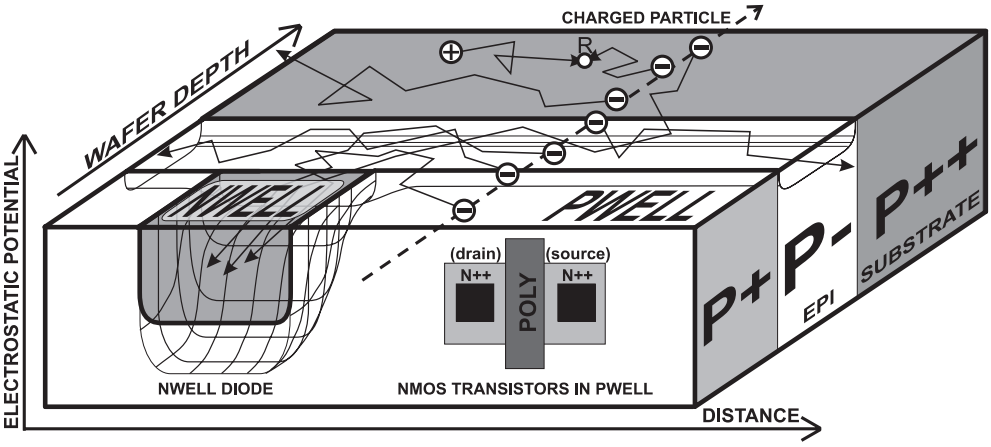

Figure 2.11: Illustration of the principle of operation of Monolithic Active Pixel Sensors (MAPS), from [Tur01].

commercially available sensors are not adapted to charged particle tracking and a dedicated design and fabrication is necessary.

In order to achieve a 100% fill factor for ionizing particle detection, it was first proposed in [Tur01] to integrate a sensor in a twin-well technology (see Sect. 2.4.3), with the charge collecting element formed by the n-well diode on the p-type epitaxial silicon, grown on a highly doped p^{++} substrate, and the three transistors of the pixel circuitry integrated in the p-well. A sketch of the proposed structure for Monolithic Active Pixel Sensors (MAPS) is shown in Fig. 2.11.

The passage of the incident charged particle produces excess carriers in the epitaxial layer, and the electrons diffuse towards the n-well diode in a time which is typically of a few tens of nanoseconds. The 3 orders of magnitude difference between the doping levels of the lightly doped p-type epilayer and the p^+ wells and p^{++} substrate leads to the creation of potential barriers at the boundaries, which act like mirrors for the excess electrons. The sensitive volume is thus the thin, partially depleted, epitaxial layer. The p^{++} substrate is made with "low quality" silicon, in which the recombination time is relatively short; therefore, only a small part of the charge created in the substrate is expected to be able to drift towards the epitaxial layer and then to be seen by the collecting electrodes.

The charge collected by the diode is directly converted into an electronic signal at the pixel level. This is a major difference with CCDs, where the charge produced by the particle detected is clocked out through the detector bulk. Equivalent noise charges as low as 10 electrons can be achieved at the single pixel level after design optimization [DepTh], resulting in a good signal-to-noise performance despite the relatively low signals available from the thin sensitive volume.

The pixel size is usually between 10 and 20 times the minimum feature size of the used technology; a 2-D pitch of 10 μm is then possible, giving the possibility of achieving a spatial resolution better than 3 μm even with a binary readout. The spatial resolution can be improved to 1.5 μm with analogue readout and exploiting the natural charge spreading between neighboring pixels [Gor02].

Other advantages of MAPS for tracking applications reside on one side on the improved radiation tolerance which is expected from the use of present-day submicron fabrication processes, on the other side from the possibility of thinning the substrate down to a few tens of μm, so that a very low multiple scattering is introduced.

The main disadvantage of the proposed approach comes from the fact that the circuitry which can be implemented in each pixel can only make use of n-MOS transistors, thus limiting the complexity of the functionalities which can be integrated at the pixel level. Moreover, the use of commercially available CMOS processes, despite being one of the major advantages of this detector technology in terms of cost, can potentially be a limitation in the sensor design due to the need to cope with the technological parameters available from a specific fabrication process.

Monolithic Active Pixel Sensors will be extensively considered in this work, with respect to their possible application in the vertex detector of the International Linear Collider, as introduced in Sect. 1.2. The simulation of the sensor charge collection properties will be presented in Sect. 4.2. In Chapter 5, after a review of the features and achievements of a series of MAPS prototypes fabricated in recent years for particle tracking applications, experimental tests of a real prototype chip will be extensively reported.

2.6.4 DEPFET detectors

Another approach in monolithic detectors is realized in the so-called DEPFET[4] pixel sensors, which were first proposed in [Kem87]. The DEPFET principle of operation is shown in Fig. 2.12. A MOSFET or a JFET[5] transistor is implanted on the detector substrate. By means of sidewards depletion and of an additional n-implant below the transistor, the so-called *internal gate*, a potential minimum for electrons is created underneath the transistor channel. An ionizing particle traversing the detector creates electron-hole pairs in the fully depleted silicon substrate, but while the holes drift to the detector rear contact, the generated electrons are collected and stored in the internal gate. The signal charge leads to a change in the potential of the internal gate, resulting in a modulation of the transistor channel current. After every readout cycle, the electrons collected by the internal gate are removed by a positive voltage pulse which is applied to a clear contact.

One of the main advantages of this technology comes from the use of a fully depleted bulk which gives large signals; at the same time, low noise operation is guaranteed by the very small capacitance of the internal gate, of the order of 10 fF. The combination of both these advantages leads to the possibility of fabricating thin devices which retain good detection performance and

[4]DEPFET stands for Depleted Field Effect Transistor.
[5]Junction Field Effect Transistor.

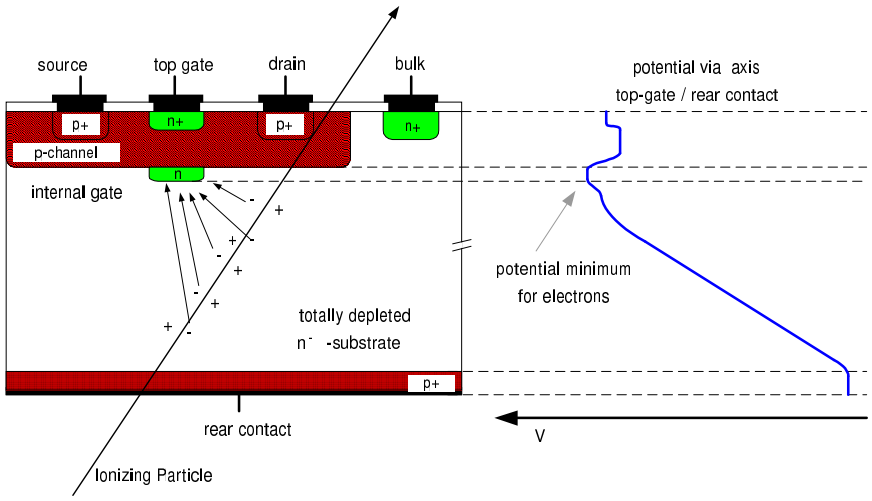

Figure 2.12: Principle of operation of a DEPFET pixel structure. Cross-section (left) of half a pixel and potential profile (right).

show very low power consumption [Fis02].

Chapter 3

Radiation Hardness of Silicon Detectors

Radiation-induced bulk damage is one of the main limiting factors for the use of silicon detectors in the intense radiation fields near the interaction point at high-energy physics experiments. In recent years much effort has been devoted to the study of the radiation hardness of silicon detectors against different particle types, and to the study of the improvements possibly achievable by using different silicon substrate materials. This research has been mainly driven by the requirements of the silicon central trackers of LHC experiments like ATLAS or CMS, which will have to face a harsh radiation environment mainly due to hadronic particles (Sect. 1.1).

Extensive investigations have been performed by the CERN-RD48 collaboration [RD48] in particular by irradiating detectors, test structures and raw materials with charged hadrons (pions and protons) and neutrons. Several studies have also been conducted with γ-ray photons [Dez00][Fre03]. Results from the RD48 collaboration have shown that the oxygen enrichment of the silicon substrate leads to a substantially improved radiation hardness against charged hadrons and γ-irradiation, and that oxygen-enriched silicon detectors can sustain the fluences expected over the lifetime of 10 operational years for LHC, up to $3{\cdot}10^{15}$ e/cm^2 1 MeV neutron equivalent at the position of the innermost tracking detector. Nevertheless, the planned upgrade of the LHC to a ten times higher luminosity, the so-called SuperLHC, foreseen in 2012, will push the requirement up to a fluence of $1.5{\cdot}10^{16}$ e/cm^2 1 MeV neutron equivalent [Gia02], which present-day oxygen-enriched silicon detectors cannot withstand. The new CERN-RD50 collaboration was founded in 2002 in order to search for a more radiation-hard material that could meet this new requirement [RD50].

In contrast to the huge number of studies of radiation hardness against hadrons and photons, very few contributions have been devoted to the study of the damage produced by high-energy (GeV) electrons in silicon. Earlier results, obtained with 500 and 900 MeV electron irradiation of silicon devices fabricated on high-resistivity float-zone material, have shown that high-energy electrons, like neutrons and protons, are very effective in creating bulk damage in silicon [Lau97, Bos03, Rac02]. In a recent work [Dit03], extending the study to oxygen-enriched

silicon substrates, no significant effect of the oxygen has been observed up to an electron fluence of $4.5 \cdot 10^{14}$ e/cm^2.

This chapter shows the results of extended investigations, which have been performed by irradiating with 900 MeV electrons a wider range of substrate materials, reaching fluence levels up to $6.1 \cdot 10^{15}$ e/cm^2, higher than the ones considered in previous works. After a review of the basic mechanisms of radiation damage in silicon, and of the corresponding degradation in the detector macroscopic properties, the experimental techniques used for detector characterization will be presented. The different irradiated devices and the experimental conditions will then be described before devoting the remaining part of the chapter to the presentation and discussion of the experimental results.

3.1 Radiation damage in silicon

3.1.1 Basic mechanisms

The basic radiation damage mechanism is initiated by the interaction of high energetic particles (hadrons, leptons, photons) with the silicon crystal, resulting in the formation of *point defects* and *clusters* of defects. The impinging particle displaces a *primary knock-on atom* (PKA) out of his lattice site resulting in a silicon interstitial and a vacancy left by the displaced atom (the interstitial-vacancy pair is also referred to as *Frenkel pair*). Both the interstitial and the vacancy can migrate through the lattice and combine with impurities of the silicon bulk, thus forming point defects. The threshold energy for the primary recoil atom to be displaced is E_d=25 eV [Lin80]. The energy of the PKA can nevertheless be much higher, and the recoil atom can lose energy across its path through the silicon bulk in ionization and further displacements. While the ionization losses usually do not lead to relevant changes in the silicon lattice, at the end of an heavy recoil range the non-ionizing interactions prevail, and dense agglomerates (*clusters*) of defects are formed. The threshold energy for the production of clusters is of about 5 keV [Lin80].

The maximal energy $E_{R,\max}$ that can be transferred by a particle of mass m_P and kinetic energy E_P to the recoil silicon atom can be calculated in the non-relativistic approach by elastic scattering:

$$E_{R,\max} = 4E_P \frac{m_P m_{\mathrm{Si}}}{(m_P + m_{\mathrm{Si}})^2}. \tag{3.1}$$

For example, electrons need a kinetic energy of about 255 keV to produce a Frenkel pair and more than 8 MeV to produce a cluster.

Point defects and defect clusters represent the real damage of the silicon bulk material, causing the deterioration of the detectors macroscopic properties (Sect. 3.1.3) .

3.1.2 The NIEL scaling hypothesis

The radiation damage produced by different particles with different energies can be scaled under the assumption of the so-called *Non-Ionizing Energy Loss (NIEL) hypothesis*. The basic

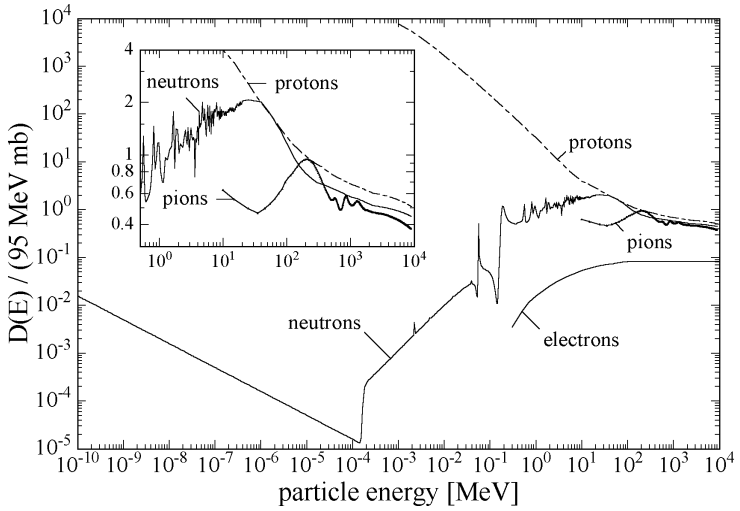

Figure 3.1: Displacement damage functions $D(E)$ normalized to 95 MeVmb (thus representing the damage equivalent to 1 MeV neutrons) for neutrons, protons, pions and electrons (from [MolTh], compiled after [Gri93, Kon92, Huh93, Sum93]).

assumption behind it is that any change in the material induced by displacement damage scales linearly with the amount of energy imparted in displacing collisions, irrespective of the spatial distribution of the introduced displacement defects in one PKA cascade, and of the various annealing sequences taking place after the initial damage event. The radiation damage in the silicon bulk then depends only on the non-ionizing energy loss.

In each interaction leading to displacement damage a PKA with a specific recoil energy E_R is produced. The portion of the recoil energy that is deposited in form of displacement damage depends on the recoil energy itself and can be calculated with the *Lindhard partition function* $P(E_R)$. Considering all the possible ν interactions between the incoming particle of energy E, if σ_ν is the cross-section corresponding to the ν-th reaction and $f_\nu(E, E_R)$ the probability of generation of a PKA with recoil energy E_R by a particle of energy E undergoing the ν-th reaction, the NIEL can be calculated by the *displacement damage cross section*

$$D(E) := \sum_\nu \sigma_\nu(E) \cdot \int_0^{E_{R,\max}} f_\nu(E, E_R) P(E_R) dE_R. \tag{3.2}$$

The integration is done over all possible recoil energies E_R above the displacement threshold. Figure 3.1 shows the displacement damage cross sections for neutrons, protons, pions and electrons compiled from [Gri93, Kon92, Huh93, Sum93].

With the help of the displacement damage cross section $D(E)$ it is possible to define a *hardness factor* κ that allows to compare the damage efficiency of different radiation sources with different particles and individual energy spectra $\phi(E)$. The hardness factor is usually defined as the ratio of the damage produced by a specific irradiation to the damage that would

be produced by 1 MeV neutrons and the same fluence:

$$\kappa = \frac{\int D(E)\phi(E)dE}{D(E_n = 1\,\mathrm{MeV}) \cdot \int \phi(E)dE}. \tag{3.3}$$

The damage caused by different particles is then usually compared to the damage caused by neutrons, taking the NIEL of 1 MeV neutrons as the reference point. The standard value for the NIEL of 1 MeV neutrons is 95 MeVmb. The equivalent 1 MeV neutron fluence Φ_{eq} can be calculated as

$$\Phi_{\mathrm{eq}} = \kappa\Phi = \kappa \int \phi(E)dE \tag{3.4}$$

The NIEL scaling hypothesis has been experimentally demonstrated after irradiation of standard float-zone silicon with protons, neutrons and pions [RD48]. Numerous violations of this hypothesis have been nevertheless observed. Despite that, the NIEL calculation is still used as the reference for the normalization of fluences of different particles and different energies.

3.1.3 Change of detector properties

The most important radiation-induced changes in the detector macroscopic properties due to bulk damage are a change in the effective dopant concentration, an increase of the leakage current and the degradation of the charge collection efficiency due to the trapping of the drifting charge by defect levels introduced by radiation in the band gap. In particular, the effect on the effective dopant concentration corresponds to a change in the detector full depletion voltage and has the highest impact in the degradation of the detector operability, together with the charge losses due to trapping, which can be significant especially at high fluences. The increased leakage current can in fact be suppressed by cooling the detector.

Effective dopant concentration

Radiation induces donor- and acceptor-like defects which influence the detector effective dopant concentration N_{eff} and consequently the full depletion voltage. The starting material is usually n-type due to the doping with phosphorus donors. After irradiation the donors are deactivated due to the creation of the so-called *E-centers*, given by the combination of a vacancy with a phosphorus dopant atom. This process is also called *donor removal*, and results in the reduction of the positive space charge. In parallel, deep acceptor levels are introduced by irradiation, resulting in an increase of the negative space charge. The continuous generation of negative space charge leads to a space charge sign inversion, followed by a rapid increase of the depletion voltage (Fig. 3.2).

Measurements of the RD48 collaboration have shown that oxygen-rich silicon material is radiation harder after charged hadron and γ irradiation, while no significant effect of the oxygenation has been observed after neutron irradiation (see for example Fig. 3.3 which refers to hadron irradiation) [RD48]. Defect models attribute this effect to a deep acceptor which is suppressed in oxygen rich material, since the presence of a high oxygen concentration favors the production of electrically inactive complexes. The oxygen effect depends on the ratio of the

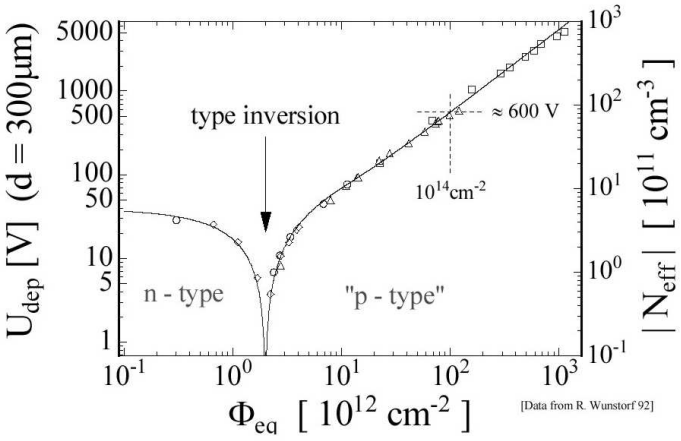

Figure 3.2: Change of the depletion voltage (left scale) and of the corresponding absolute dopant concentration (right scale) as a function of the neutron fluence (from [Wun92]).

damage between clusters and point defects. The strongest effect is observed after γ irradiation, when only point defects are created, while no effect is visible for neutrons, when mostly clusters are generated.

Figure 3.4 shows the typical time development of the radiation induced change in the effective dopant concentration with respect to its initial value $N_{\text{eff},0}$ before irradiation

$$\Delta N_{\text{eff}}(\Phi_{\text{eq}}, t) = N_{\text{eff},0} - N_{\text{eff}}(\Phi_{\text{eq}}, t) \tag{3.5}$$

where $t = t(T_a)$ indicates the annealing time at a certain temperature T_a. As a function of time and fluence ΔN_{eff} can be described as

$$\Delta N_{\text{eff}}(\Phi_{\text{eq}}, t) = N_A(\Phi_{\text{eq}}, t) + N_C(\Phi_{\text{eq}}, t) + N_Y(\Phi_{\text{eq}}, t) \tag{3.6}$$

where ΔN_{eff} has been divided into the three components:

- N_A is the so-called *short term annealing* component. A variation in the detector full depletion voltage V_{dep} is indeed observed soon after irradiation. Since for type-inverted detectors the depletion voltage decreases (i.e. the negative N_{eff} becomes more negative), this annealing component is also called *beneficial annealing*. For non type-inverted detectors the depletion voltage usually increases (i.e. the positive N_{eff} becomes more positive), resulting in any case in a reduction of ΔN_{eff} which is attributed to the annealing of acceptors. This reduction as a function of the annealing time is described by an exponential decay whose amplitude is proportional to the irradiation fluence.

- N_C has experimentally turned out not to depend on annealing and is therefore called *stable damage* component. It is due to incomplete donor removal from the non-irradiated substrate, which depends exponentially on the irradiation fluence, combined with a fluence proportional introduction of stable acceptors. This is the most important damage

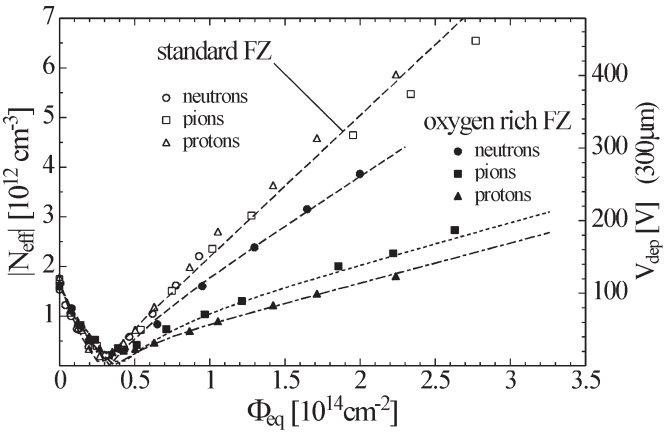

Figure 3.3: Comparison in the change of the absolute dopant concentration for standard and oxygenated float-zone material after different particle irradiations (from [MolTh]).

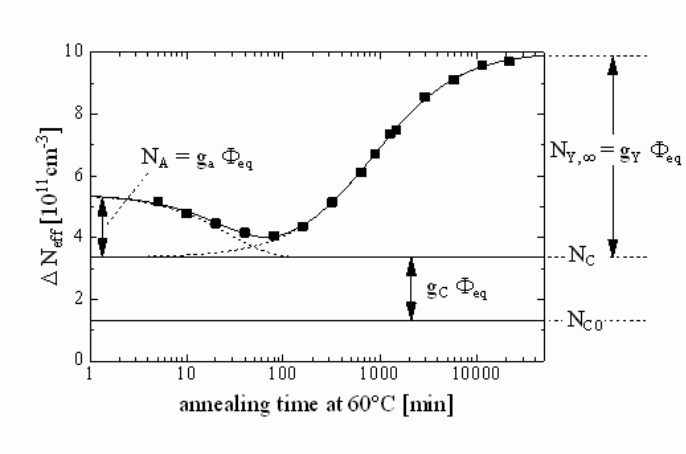

Figure 3.4: Example of annealing behavior of the radiation-induced change in the effective dopant concentration ΔN_{eff} after thermal annealing at 60°C (from [MolTh]).

component with respect to the application and operability of silicon detectors in intense radiation fields.

- N_Y is the so-called *reverse annealing* component, since its behavior is opposite to beneficial annealing and leads to an increase of ΔN_{eff} for longer annealing times. In the long term, in fact, the space charge becomes more negative due to the build-up of acceptor states, and ΔN_{eff} increases up to a saturation value, reached for very long annealing times, which is proportional to the irradiation fluence.

A further discussion and a quantitative parameterization of these components will be pre-

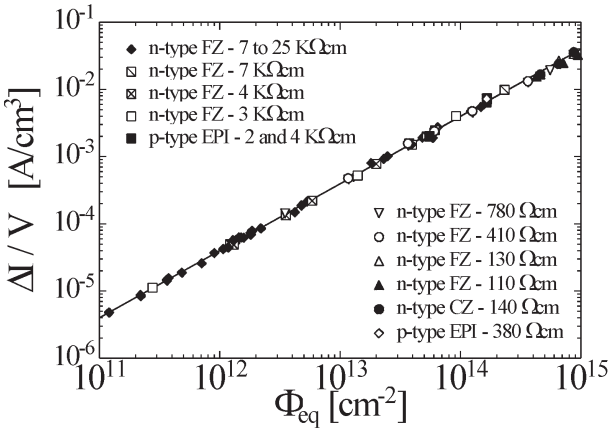

Figure 3.5: Fluence dependence of the leakage current density for silicon detectors manufactured from different substrate materials. The experimental values were measured after 80 min of thermal annealing at 60°C (from [MolTh]).

sented in Sect. 3.3.2 together with experimental results.

Leakage current

Another effect of radiation damage in silicon detectors is the increase of the reverse leakage current. The main contribution to the latter comes from generation of carriers in the depleted region. The generation current after irradiation is enhanced by the emission of electrons and holes from defect levels, and has been shown to increase proportionally to the irradiation fluence and independently of the substrate material [MolTh]. The increase of the leakage current ΔI is the reverse current after irradiation minus the current measured before irradiation. For a standard detector thickness of around 300 μm the current before irradiation is usually in the order of a few hundred pA and is neglectable compared to the current generated by radiation-induced defects, which is orders of magnitude higher. Figure 3.5 shows the variation of the leakage current normalized to the detector volume after neutron irradiation (from [MolTh]).

The increase can be described by

$$\Delta I = \alpha \Phi_{\mathrm{eq}} V \tag{3.7}$$

where α is called the *leakage current damage constant* and V is the detector volume. If all irradiated detectors go through the same heat treatment, Eq. 3.7 can be used to evaluate the irradiation fluence after the irradiation experiment. The α value depends on the annealing time and on the annealing temperature. For the same experimental conditions, a universal annealing behavior of the leakage current has been observed [Mol99], as will be further discussed in Sect. 3.3.2.

Trapping of the drifting charge

The defect levels generated by radiation in the silicon band gap act as traps for the drifting charge. Each level can trap electrons and/or holes, thus changing the charge state of the defect. For example a donor can trap holes if it is occupied and electrons if it is empty, and an analogue situation stands for an acceptor. In the space-charge region both donors and acceptors above the intrinsic level are predominantly empty, so they are mainly electron traps. Correspondingly, acceptors and donors below the intrinsic level are mainly hole traps. The defect trapping probability is defined as the inverse of the trapping time $\tau^t_{\mathrm{tr}_{e,h}}$, that represents the mean time that an electron or a hole spends in the space-charge region before being trapped by the trap t. The *effective trapping probability* $1/\tau_{\mathrm{eff}_{e,h}}$ for electrons and holes is obtained by summing over the trapping probabilities of all defects. At a given temperature and time after irradiation it is found [KraTh] to be proportional to the irradiation fluence:

$$\frac{1}{\tau_{\mathrm{eff}_{e,h}}} = \sum_t \frac{1}{\tau^t_{\mathrm{tr}_{e,h}}} = \beta_{e,h}(t,T) \cdot \Phi_{\mathrm{eq}} \tag{3.8}$$

where $\beta_{e,h}$ represents the effective electron or hole trapping damage constant.

3.2 Experimental techniques

3.2.1 Test structures

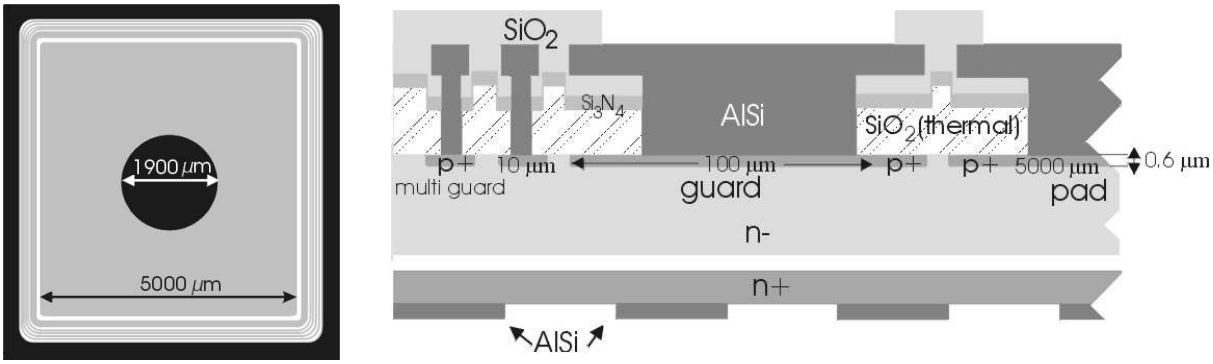

Figure 3.6: Top view (left) and cross section (right) of the test structures (pad diodes) used in this work for radiation hardness studies.

Figure 3.6 shows a sketch of the typical silicon test structure (pad diode) used in this work for radiation hardness studies. The diode active area is of 5×5 mm^2 and is defined by a first guard-ring of 100 μm width, which is 10 μm distant from the central pad. Besides the first guard-ring, the pad is surrounded by a multiguard-ring structure. Nevertheless, during measurements, only the first guard-ring is contacted to the instruments or grounded, in order to sink leakage

currents generated outside the pad area. The outer rings are operated floating in order to lower the potential difference between the central pad and the edges of the detector.

The detector bulk is doped with phosphorus (n-type). The devices used in this work present a doping of the bulk which varies between $5{\cdot}10^{11}$ cm^{-3} and $7{\cdot}10^{13}$ cm^{-3}. The p^+ layers on the top of the diode have a thickness of 0.6 μm and are doped with a boron concentration of about $1{\cdot}10^{19}$ cm^{-3}. On the bottom of the bulk is a highly-doped n^+ layer with a thickness of 1 μm and a doping of $1{\cdot}10^{19}$ cm^{-3}.

The metallization of the contacts is done with aluminum. In order to perform optical injection both from the top and from the bottom of the detector, a 1.9 mm diameter hole is left on the top side, while the metallization on the back contact is deposited with a mesh-like structure. The parts of the detector which are not metallized are covered with silicon oxide and silicon nitride.

3.2.2 C/V-I/V measurements

The diode macroscopic parameters of main interest are the depletion voltage V_{dep} and the reverse current I_{leak}. In order to extract these parameters, the diode capacitance-voltage (C/V) and current-voltage (I/V) characteristics are measured.

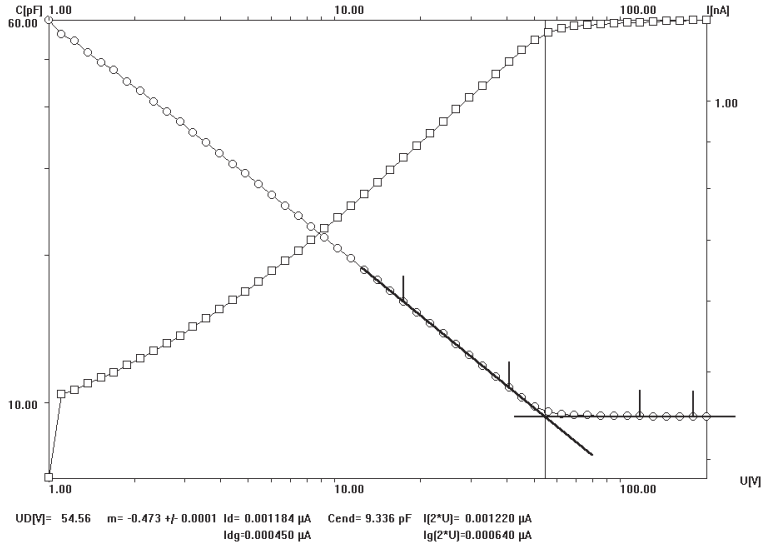

Figure 3.7: Example of C/V-I/V characteristics. The C/V curve is fitted with straight lines to extract the detector depletion voltage.

As shown in Fig. 3.7, the depletion voltage is extracted from the C/V characteristics by fitting two lines on the experimental curve plotted in a log-log scale: one on the slope of the curve, where the capacitance is decreasing, the other on the final, horizontal part of the curve where the capacitance is constant and equal to the geometrical capacitance (Eq. 2.21). The depletion voltage is estimated as the abscissa of the intersection point between these two lines.

An estimation of the leakage current is then extracted from the I/V characteristics by considering the reverse current I_{dep} at the depletion voltage.

The C/V measurements are performed with a HP 4263 LCR Meter, with which the admittance Y of the diode is measured. A schematic description of the used experimental setup can be found in [FeiTh, MolTh]. For a circuit with a capacitor and a resistor in parallel the admittance is given by

$$Y = \frac{1}{R_p} + j\omega C_p. \tag{3.9}$$

The admittance is measured by adding a small AC voltage with an amplitude of 0.5 V and a frequency ω to the DC voltage of the reverse bias. The frequency can be chosen out of 1 kHz, 10 kHz and 100 kHz. The experimental results presented in this work refer to measurements performed at the 10 kHz frequency.

The I/V characteristics is measured with a Keithley 6517A Electrometer. Since the value of the measured current depends strongly on the temperature, the latter is also recorded with a Keithley 195A Multimeter. The experimental I/V curve is then normalized during data analysis to the reference temperature of T_R=20°C by multiplying the measured values $I(T)$ with a factor $F(T)$ according to the formula [Sze81]

$$I(T_R) = I(T) \cdot F(T) \quad \text{with} \quad F(T) = \left(\frac{T_R}{T}\right)^2 \exp\left(-\frac{E_g}{2k_B}\left[\frac{1}{T_R} - \frac{1}{T}\right]\right). \tag{3.10}$$

3.2.3 Transient Current Technique (TCT) measurements

Basics of TCT measurements

The Transient Current Technique (TCT) is based on the measurement of the induced current pulse arising from the drift of free carriers generated in the detector by a short laser pulse. Current pulse signals measured at the terminals of a detector follow in time the electric field distribution which is seen by the moving charge.

If N electron-hole pairs are created in the direct vicinity of the front or rear contact of the fully depleted detector, either only electrons or holes will travel across the whole detector. The complementary carriers are collected immediately by the adjacent electrode. These two situations are referred to as electron and hole injection respectively (Fig. 3.8). The generated free carriers have an exponential spatial distribution starting from the electrode and decreasing exponentially towards the detector bulk, with a decay constant given by the absorption length of light in silicon. The absorption length of light in silicon depends on temperature and wavelength. For the red laser with 670 nm wavelength used in this work, one obtains at room temperature $\alpha_{\text{abs}}(293\ K)$=3.3 μm. Hence, while in general the total induced current is the sum of both electron and hole contributions $I(t) = I_e(t) + I_h(t)$, for a penetration depth of a few microns the contribution of carriers drifting to the adjacent electrode is negligible.

In the case of electron injection (front contact), the electron drift velocity is large at the beginning of the drift and decreases towards the end of the drift, indicating a higher electric

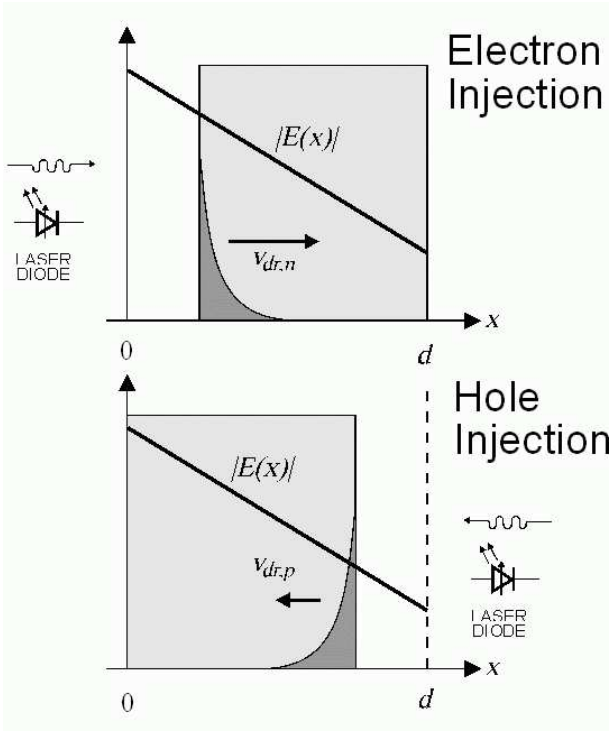

Figure 3.8: Schematic illustration of the origin the current pulse shapes in the case of laser illumination.

field at the front contact and a lower electric field at the back contact. On the other side, for hole injection (back contact), holes are generated in the low electric field region, and their velocity increases during their passage through the detector bulk. Such an electric field profile is in agreement with the electric field in a non-irradiated detector with a positive effective space charge. Therefore, a benefit of the current pulse measurement is the direct evidence of the sign of the space charge.

An increased reverse bias voltage results in a higher electric field and accordingly in a larger induced current, until the drift velocity starts to saturate for high electric field strengths. In general, the drift time of holes is around three times longer than for electrons, in agreement with the ratio of mobilities. If the reverse bias is smaller than the depletion voltage and the space charge sign is positive, electrons injected at the front contact travel towards the low field region with a reduced velocity, so that a long tail in the current emerges. On the contrary, holes are injected at the back and have to diffuse through the undepleted bulk region before reaching the depleted region, where they are then swept by the electric field. Since diffusion is a relatively slow process, the peak of the induced current appears at later times.

If the space charge is negative the above described picture is inverted: the current induced by electron injection has qualitatively the same shape of the current induced by holes in the case of positive space charge and vice versa.

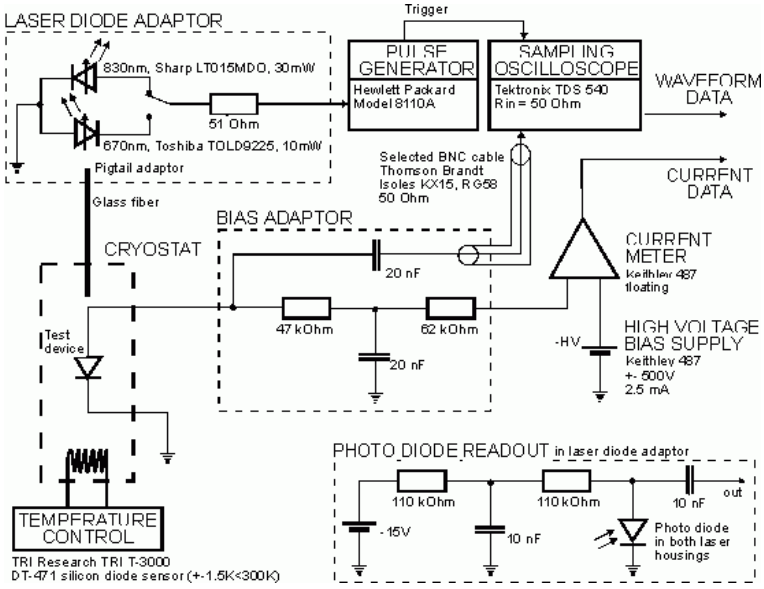

Figure 3.9: Electrical setup for TCT measurements, as constructed by V. Eremin [Ere95]. In this work, a red laser with 670 nm wavelength was used.

Experimental setup

The electrical scheme of the experimental setup used for TCT measurements is displayed in Fig. 3.9. The key element is a Tektronix TDS 540 sampling oscilloscope which provides a maximum of 1 Gigasamples per second and an analog bandwidth of 500 MHz. The detector current signal is transmitted via a coupling capacitor from the front contact electrode to the oscilloscope input connector, which is terminated by a 50 Ω resistor. Accordingly, the voltage measured by the oscilloscope is related to the current signal by $V(t) = 50\ \Omega \cdot I(t)$. The free carriers are generated underneath the sample electrodes by illumination with a short (<1 ns) light pulse emitted from a low power semiconductor laser diode. A pulse generator HP 8110A is used to drive the laser electronically and also provides an accurate trigger signal which initiates the recording of a waveform into the oscilloscope. Typically up to a hundred of current pulse shapes need to be averaged in order to improve the signal-to-noise ratio. The leading and trailing edges of the pulse are affected by the total system rise-time, which is determined on one side by the analog bandwidth of the oscilloscope and, on the other side, by the sample capacitance (of around 10 pF) and the oscilloscope input impedance of 50 Ω, resulting in around 1 ns.

Alternatively from laser illumination for charge carrier trapping measurements, with the same experimental setup tested devices can also be illuminated with α-particles emitted by a ^{244}Cm source in order to perform charge collection efficiency measurements. In our setup this is possible only from the detector front side. The α-particles are emitted with an energy of 5.8 MeV, but before reaching the silicon bulk lose part of their energy through a 3.7 mm air gap and a 3 μm layer due to Al, SiO_2 and Si (the p^+ implant) on top of the bulk. Using values

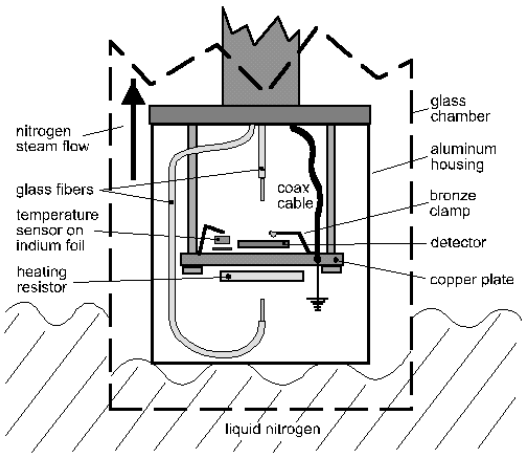

Figure 3.10: Side view of the mechanical setup used for the study of laser-induced current pulses.

taken from [Zie78], the final energy deposited in the silicon can be calculated as 4.8 MeV. The penetration depth of α-particles in silicon is of the order of 23 μm [Das55], therefore charge generation occurs not only in the vicinity of the contact like in the case of laser illumination, but also deeper inside in the detector bulk.

The mechanical setup used for laser illumination on the detector front and rear sides is illustrated in Fig. 3.10. The detector is mounted directly on a circular copper plate which is grounded. A bronze clamp is used to establish the front contact and to put pressure on the sample in order to improve the thermal contact. A temperature sensor is placed in the direct vicinity of the sample. All electrical connectors and also the two glass fibers for front and rear illumination are led into the aluminum housing through a glass tube from the top. The whole apparatus is placed into a bottle-like glass chamber, in which cooling can be provided by means of liquid nitrogen. Heating power can eventually be supplied by a heating resistor glued to the bottom side of the copper plate. Nevertheless, measurements presented in this work have been performed at the laboratory room temperature. In the case of α-illumination, the emitting source is simply placed on top of the detector inside the aluminum housing.

Data analysis

The transient current technique is a useful tool to study effective trapping times. In this work the *charge correction method*, based on the correction of time-resolved current pulse shapes due to trapping, is used. The method was proposed independently in [Bro00, Kra02].

In the case of a diode (two parallel electrodes with lateral dimensions much larger than the detector thickness), the induced current due to the drift of electrons and holes is given by Ramo's theorem (see Eq. 2.28) as:

$$I_{e,h}(t) = -\frac{qN_{e,h}(t)}{D} \cdot v_{\mathrm{dr}_{e,h}}(t) \tag{3.11}$$

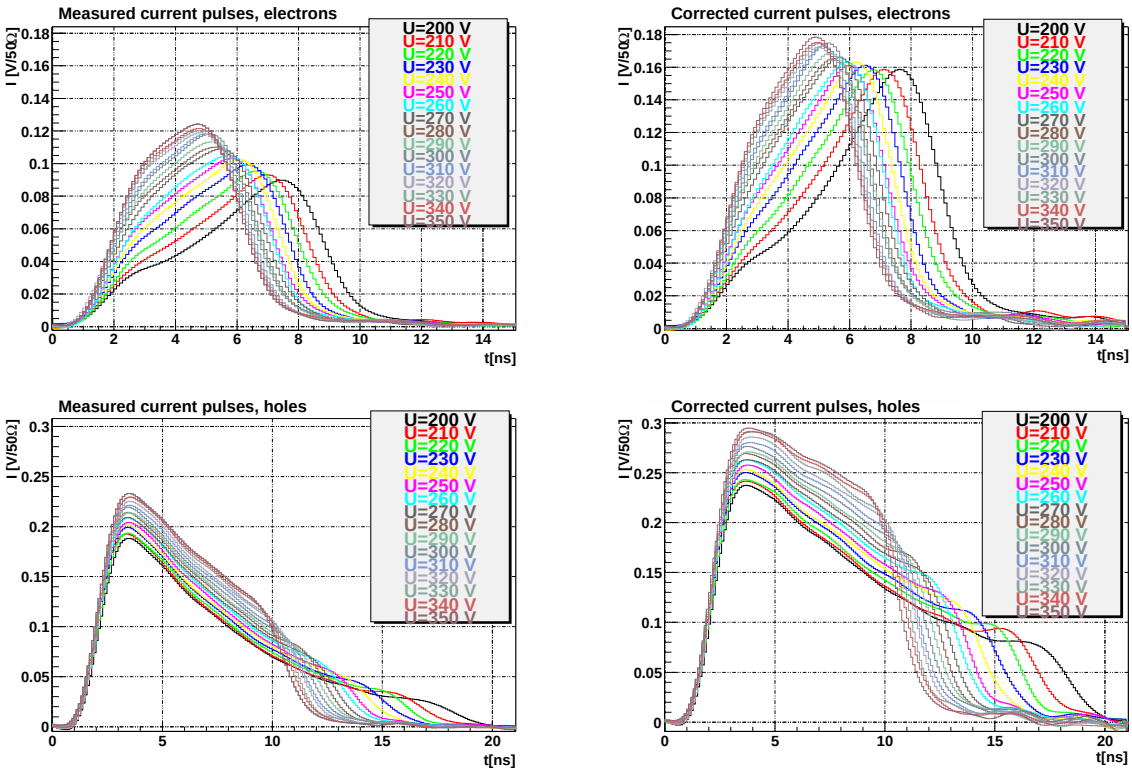

Figure 3.11: Example of measured and corrected induced current shapes, for a standard float-zone sample irradiated with Φ_{el}=6.1·10^{15} e/cm^2 (see Sect. 3.3.1). The top plots refer to front (electron) injection, the bottom to back (hole) injection.

where $N_{e,h}(t)$ is the number of drifting electrons and holes, respectively, D is the detector thickness and $v_{\mathrm{dr}_{e,h}}(t)$ the carrier drift velocity. The amount of the drifting charge $N_{e,h}(t)$ decreases with time due to trapping as:

$$N_{e,h}(t) = N_{e,h}(0) \cdot \exp\left(-\frac{t}{\tau_{\mathrm{eff}_{e,h}}}\right) \tag{3.12}$$

where $N_{e,h}(0)$ is the number of generated electron-hole pairs and $1/\tau_{\mathrm{eff}_{e,h}}$ the effective trapping probability.

The effective trapping time can be determined from the behavior of the current integral at voltages above V_{dep}, where the measured charge becomes independent of the applied bias voltage, provided that the current integration time is longer than the drift time of electrons and holes. If the laser pulse is short compared to the drift time, it can be seen from Eqs. 3.12 and 3.11 that correcting the measured pulse current $I_m(t)$ with a single exponential can compensate for trapping:

$$I_c(t) = I_m(t) \cdot \exp\left(\frac{t - t_0}{\tau_{\mathrm{tr}}}\right) \tag{3.13}$$

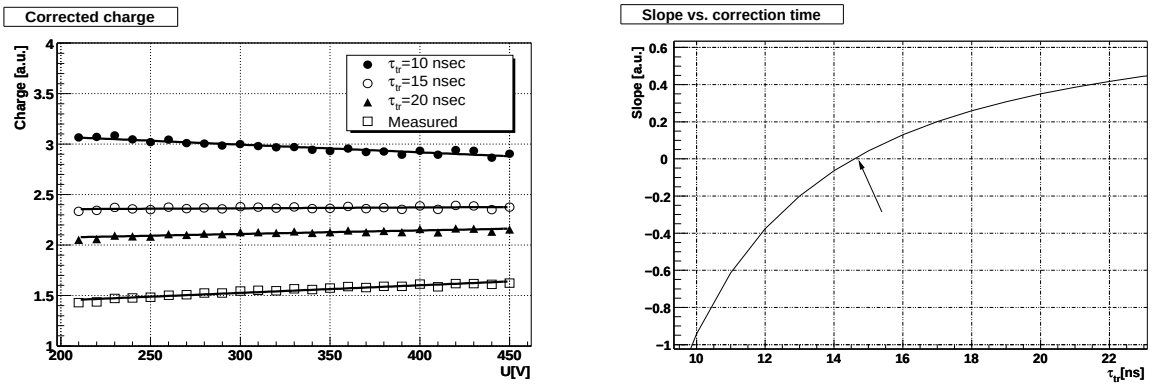

Figure 3.12: Illustration of the charge correction method used to determine effective trapping times from TCT measurements. Measured charge and corrected charge for different values of the effective trapping time $\tau_{\rm tr}$ (left), and slope of the linear fit to the corrected charge as a function of $\tau_{\rm tr}$ (right). The effective trapping time is determined from the zero intersection point. The plots refer to hole injection in a standard float-zone sample irradiated with $\Phi_{\rm el}$=6.1·10^{15} e/cm^2 and type-inverted after irradiation (see Sect. 3.3.1).

where t_0 is the carrier injection time, set to the start of the laser pulse. Figure 3.11 shows an example of measured and corrected induced current pulses, both for electron and hole injection, in the case of a type-inverted device after irradiation.

If $\tau_{\rm tr}$ in Eq. 3.13 represents the correct effective trapping time, then the integral over time is equal for all voltages above $V_{\rm dep}$. The method is applied only for voltages above $V_{\rm dep}$, since for voltages below $V_{\rm dep}$ the correction can not be applied in a simple way. It is also evident how the ratio $I_m(t)/I_c(t)$ represents the charge collection efficiency.

If $1/\tau_{\rm tr} > 1/\tau_{{\rm eff}_{e,h}}$ the corrected charge is too high at low voltages, where the charge drift is long, and vice versa for $1/\tau_{\rm tr} < 1/\tau_{{\rm eff}_{e,h}}$. The corrected charge does not depend on the applied voltage anymore if $1/\tau_{\rm tr} = 1/\tau_{{\rm eff}_{e,h}}$, which therefore corresponds to the sign inversion of the slope of the linear fit to the corrected charge as a function of the applied voltage.

In practice, the measured current pulse $I_m(t)$ is recorded for different voltages, and the curves corresponding to $V > V_{\rm dep}$ are corrected for trapping for several values of $\tau_{\rm tr}$. Then the distribution of the corrected charge, i.e. the integral over time of the corrected current $I_c(t)$, as a function of the applied voltage is fitted with a linear trend and the slope of the fit is plotted against the applied voltage (see Fig. 3.12). The effective trapping probability is finally determined from the zero intersection point of such a curve.

The uncertainty of the method comes mainly from the variation of the slope of the linear fit, which is related to the number of points included in the fit, and has been estimated to be of the order of 10% [Kra02].

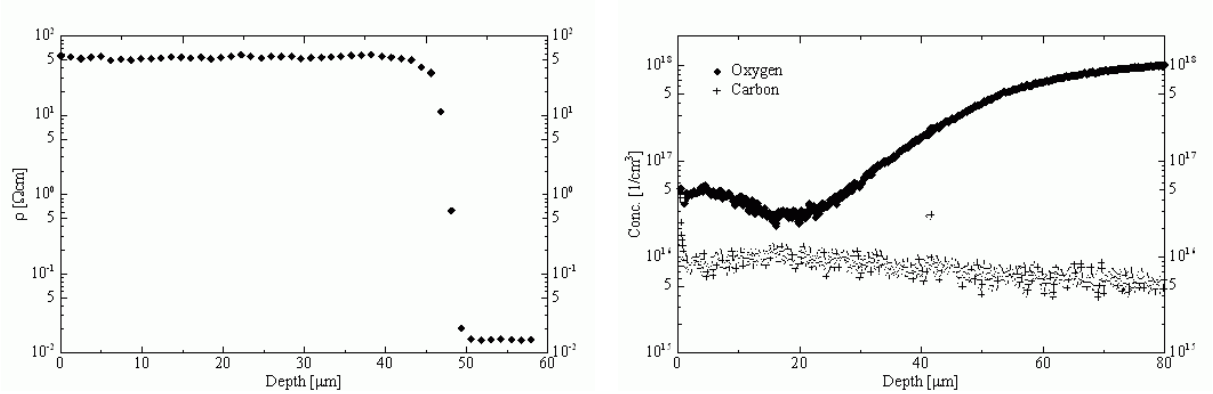

Figure 3.13: Resistivity profile (left) and SIMS measurements (right) performed on epitaxial devices.

3.3 High-energy electron irradiation of different silicon substrates

3.3.1 Devices and experimental conditions

Tested devices are $p^+/n^-/n^+$ pad detectors (see Sect. 3.2.1) fabricated on different silicon substrates, namely standard and diffusion-oxygenated float-zone (which in the following we will address as StFZ and DOFZ, respectively), Czochralski (CZ) and epitaxial (EPI) silicon[1].

A set of standard and oxygenated float-zone devices has been manufactured by CiS (Erfurt, Germany) on Wacker (111) substrates of typical resistivity of 3-4 kΩcm. Oxygen diffusion for DOFZ devices has been performed in an N_2 environment for 72 hours at 1150°C. A second set of StFZ diodes has been fabricated by ITC-irst (Trento, Italy) on high purity wafers from Topsil, with a resistivity of 10-20 kΩcm. Some of the substrates had been previously converted to DOFZ by a 12 hour oxidation at 1150°C followed by a 36 hour diffusion in N_2 at the same temperature, resulting in an oxygen concentration of $1\text{-}3 \cdot 10^{17}$ cm^{-3} across the substrate.

Czochralski and epitaxial devices have also been processed by CiS. CZ diodes are manufactured on (100) wafers of resistivity 1.2 kΩcm from Sumitomo; EPI diodes are processed on a 50 μm thick epitaxial layer (of resistivity 50 Ωcm) grown by ITME (Warsaw, Poland) on a 300 μm thick low-resistivity (0.01 Ωcm) Czochralski (111) substrate. The resistivity profile for EPI devices can be seen in Fig. 3.13 (left), in which the transition between the epitaxial layer and the Czochralski substrate is clearly visible.

The active area of all CiS diodes is of 0.5×0.5 cm^2, while devices fabricated by ITC-irst have an area of 0.35×0.35 cm^2. The substrate thickness for all devices is of about 300 μm.

Table 3.1 summarizes the values of resistivity and oxygen concentration of the different materials. The values for the oxygen concentrations of CiS devices come from SIMS measurements performed by ITME. It should be noted that while in CZ devices the oxygen concentration is very homogeneous over the complete detector thickness, for EPI diodes a strong oxygen profile

[1] A review of the different silicon growth techniques can be found in Sect. 2.4.2.

is observed, as shown if Fig. 3.13 (right). The concentration in the Czochralski substrate is of about $9{\cdot}10^{17}$ cm^{-3}, that is in the same range as for CZ diodes. Inside the epitaxial layer a minimum is reached at about 17 μm from the surface, and the concentration grows on both sides, towards the surface and towards the interface with the Czochralski substrate. Such a profile is the result of diffusion of oxygen into the epilayer on one side from the oxygen-rich Czochralski substrate, on the other side from the detector surface, most likely during the passivation process. The value of $9{\cdot}10^{16}$ cm^{-3} given in table 3.1 is the average oxygen concentration inside the epitaxial layer.

material	manufacturer	resistivity	oxygen concentration
StFZ(111)&(100)	ITC-irst	10-20 kΩcm	$<1{\cdot}10^{16}$ cm^{-3}
DOFZ(111)	ITC-irst	10-20 kΩcm	$1\text{-}3{\cdot}10^{17}$ cm^{-3}
StFZ(111)	CiS	3-4 kΩcm	$<5{\cdot}10^{16}$ cm^{-3}
DOFZ(111)	CiS	3-4 kΩcm	$1.2{\cdot}10^{17}$ cm^{-3}
CZ(100)	CiS	1.2 kΩcm	$8{\cdot}10^{17}$ cm^{-3}
EPI(111)	CiS	50 Ωcm	$9{\cdot}10^{16}$ cm^{-3}

Table 3.1: Irradiated substrate materials and values of the corresponding resistivity and oxygen concentration.

Irradiations have been performed with the electron beam of the LINAC injector at the synchrotron light facility Elettra in Trieste (Italy). Devices have been kept unbiased during irradiation, at the room temperature of the LINAC (25°C). To ensure a uniform irradiation of the whole area covered by the devices, these were moved along a serpentine path in a plane perpendicular to the beam, by means of a remotely controlled translation stage. The electron fluence was measured by means of a toroidal coil coaxial with the beam, allowing the electric charge of the individual beam pulses to be monitored.

A first irradiation run was performed in 2003 on all devices, up to an electron fluence of $2.1 \cdot 10^{15}$ e/cm^2 [Dit04, Dit04b]. A second irradiation run was performed in 2004 on CiS devices only, extending the fluence reach of 3 times up to $6.1 \cdot 10^{15}$ e/cm^2 [Dit05].[2] The fluences of each irradiation step are reported in Table 3.2 and 3.3 for the two subsequent runs, respectively. The first error associated with these values takes into account the fluctuations of the beam intensity observed during the irradiation, while the second one accounts for the systematic uncertainty on the calibration of the toroidal coil.

Irradiated devices have been electrically characterized by reverse bias C/V-I/V measurements as described in Sect. 3.2.2, performed first about one day after irradiation and then after thermal annealing cycles at 80°C. Between irradiation and the first measurements the samples have been kept at room temperature. After the first series of measurements devices have been stored at about -7°C. All C/V-I/V measurements have been performed at 10 kHz frequency. The temperature in the laboratory during the measurements varied between 22 and 24°C. All

[2] In the 2004 irradiation run, described in [Dit05], devices from CiS were compared also to devices manufactured on different Czochralski substrates by Helsinki Institute of Physics (Finland). In the following, the discussion is nevertheless limited to results obtained on CiS devices.

step	fluence (e/cm^2)
1	$(1.74 \pm 0.06 \pm 0.07) \cdot 10^{12}$
2	$(2.31 \pm 0.01 \pm 0.09) \cdot 10^{13}$
3	$(7.24 \pm 0.04 \pm 0.29) \cdot 10^{13}$
4	$(1.25 \pm 0.01 \pm 0.05) \cdot 10^{14}$
5	$(4.04 \pm 0.01 \pm 0.16) \cdot 10^{14}$
6	$(7.82 \pm 0.03 \pm 0.31) \cdot 10^{14}$
7	$(1.37 \pm 0.01 \pm 0.06) \cdot 10^{15}$
8	$(2.09 \pm 0.004 \pm 0.08) \cdot 10^{15}$

Table 3.2: Cumulative electron beam fluences after each irradiation step for the 2003 irradiation run.

step	fluence (e/cm^2)
1	$(1.06 \pm 0.01 \pm 0.04) \cdot 10^{15}$
2	$(1.97 \pm 0.01 \pm 0.08) \cdot 10^{15}$
3	$(4.16 \pm 0.05 \pm 0.17) \cdot 10^{15}$
4	$(4.97 \pm 0.05 \pm 0.20) \cdot 10^{15}$
5	$(6.11 \pm 0.02 \pm 0.25) \cdot 10^{15}$

Table 3.3: Cumulative electron beam fluences after each irradiation step for the 2004 irradiation run.

measured currents have been normalized to 20°C by using Eq. 3.10.

3.3.2 Experimental results: effective dopant concentration and leakage current

Effective dopant concentration

The values of the substrate effective dopant concentration $N_{\text{eff}} = |N_D - N_A|$, defined as the difference between the concentration of positively charged donors and the concentration of negatively charged acceptors, is calculated from the measured values of the full depletion voltage V_{dep}. By inserting Eq. 2.17 in Eq. 2.16, one obtains

$$|N_{\text{eff}}| = \frac{2\epsilon_{\text{Si}}\epsilon_0}{qD^2} \cdot V_{\text{dep}} \tag{3.14}$$

where the substrate thickness D is evaluated for each device from the saturation value of the diode capacitance above full depletion voltage, according to Eq. 2.21.

We report here the results of the measurements performed after thermal annealing for 8 minutes at 80°C. According to [MolTh], an annealing state of 8 minutes at 80°C, which are roughly equivalent to ∼15 days at room temperature, corresponds to a minimum in the radiation-induced change of the substrate effective dopant concentration, after the irradiated silicon material has undergone initial short-term beneficial annealing (see Sect. 3.1.3). Even if this is not true for all considered materials (indeed we will see that it is only verified in type-inverted StFZ

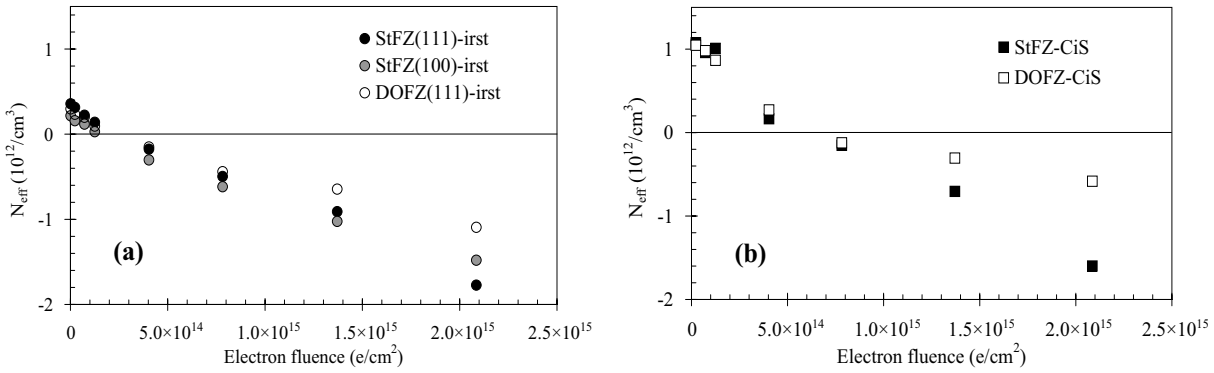

Figure 3.14: Effective dopant concentration for StFZ and DOFZ devices from (a) ITC-irst and (b) CiS measured after 8 minutes of thermal annealing at 80°C. Data refer to the 2003 irradiation run.

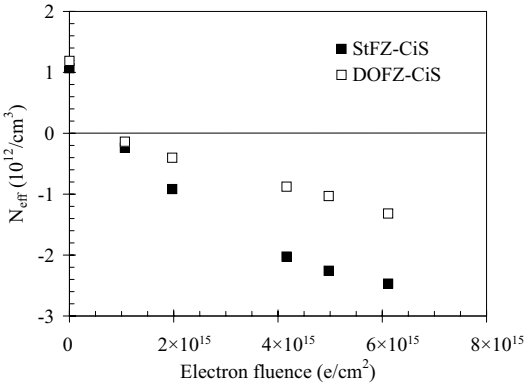

Figure 3.15: Effective dopant concentration for StFZ and DOFZ devices from CiS measured after 8 minutes of thermal annealing at 80°C. Data refer to the 2004 irradiation run.

and DOFZ devices), it is nevertheless taken as a general criterion for comparison between the different devices. In this way, the comparison should on one side be independent from the particular thermal history that every single device has undergone (e.g. duration of the irradiation itself, time elapsed between the end of the irradiation and the first measurements), on the other side take into account that in a real operational scenario (e.g. the collider operation with its beam on/off periods) the immediate radiation-induced effect is always followed by annealing effects.

Figures 3.14(a) and (b) show the values of N_{eff} as a function of the electron fluence for the StFZ and DOFZ devices manufactured respectively by ITC-irst and CiS, as measured after the 2003 irradiation run. The corresponding measurements performed on CiS devices after the 2004 run are shown in Fig. 3.15. A negative sign has been assigned to those values of N_{eff} that are considered likely to correspond to an inverted (p-type) substrate, based on the criterion of obtaining a smooth curve. Substrate type inversion is observed for all devices, confirming

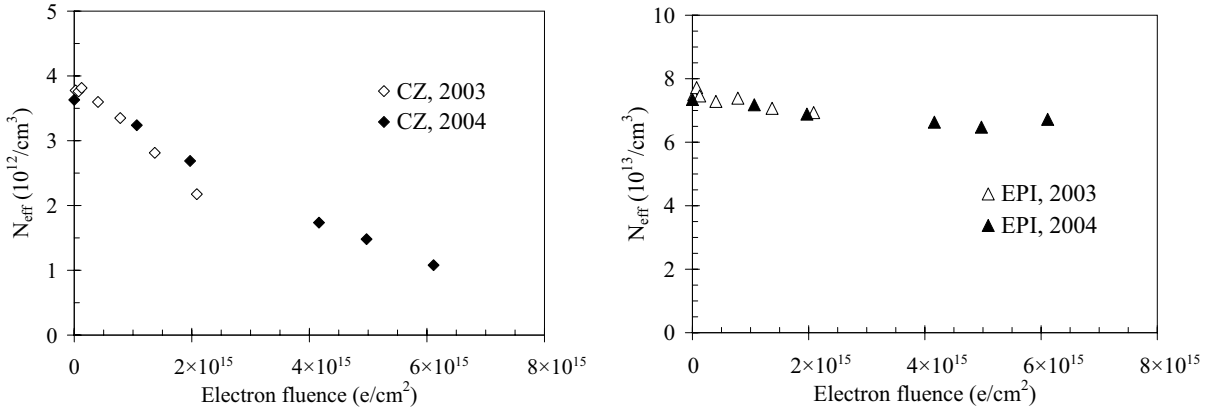

Figure 3.16: Effective dopant concentration for CZ (left) and EPI (right) devices measured after 8 minutes of thermal annealing at 80°C. The values reported have been equalized according to the procedure described in the text.

that high-energy electrons are quite effective in creating bulk damage in silicon. Type inversion appears around $2.5{\cdot}10^{14}$ e/cm^2 for the ITC-irst devices (fabricated on higher resistivity material), and at about $5 \cdot 10^{14}$ e/cm^2 for the CiS devices. After type inversion, the experimental curves follow an approximately linear trend which reflects the introduction rate of negative space charge; in all cases, a lower slope is clearly associated with DOFZ substrates, suggesting an oxygen effect (Sect. 3.1.3) similar to the one observed after charged hadron irradiation [RD48]. Differences between diodes fabricated by ITC-irst and by CiS are to be attributed to the different starting materials and oxygen diffusion treatments.

In Fig. 3.16 the N_{eff} values obtained for the CZ and EPI substrates as a function of the electron fluence and after annealing for 8 minutes at 80°C are reported. Due to the fact that the samples used for the various irradiations had non negligibly differing values of initial resistivity, the following equalization procedure has been applied: for each device, the variation in N_{eff} due to irradiation $N_{\text{eff,after}} - N_{\text{eff,before}}$ has been added to the average value of the initial effective dopant concentration, calculated taking all devices into account.

Substrate type inversion is not observed both in CZ and EPI devices. Nevertheless, a decreasing trend of N_{eff} is observed for CZ devices, with an approximately linear trend that with a simple extrapolation would eventually lead to type inversion at a fluence of about $8 \cdot 10^{15}$ e/cm^2. Irradiations of the same type of devices with charged hadrons (24 GeV/c protons and 190 MeV/c pions) have nevertheless shown no type inversion even at equivalent fluences up to 10^{15} cm^{-2} [HoeTh, Mol05], one order of magnitude higher than the fluences considered here.

For EPI devices, the relative changes in N_{eff} are quite small and comparable with the uncertainty in the evaluation of the depletion voltage. Although a decrease of the effective dopant concentration with increasing fluence is apparent from the plot, substrate type inversion is not even approached at the fluences considered, in agreement with what already observed after irradiation with 24 GeV/c protons [Kra03b], where an initial decrease in N_{eff} is followed by a

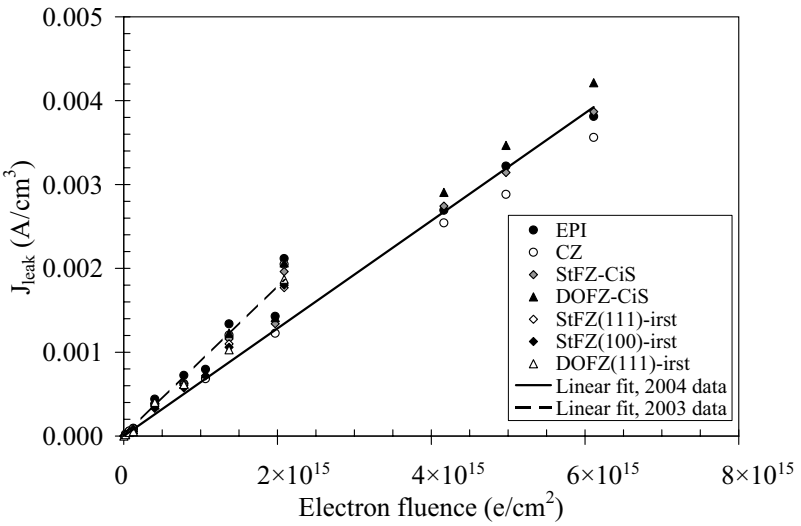

Figure 3.17: Leakage current density measured for all devices after thermal annealing for 8 minutes at 80°C. Two different linear fits are shown for the data from the 2003 and 2004 runs.

moderate increase at higher fluences (order of 10^{15} cm^{-2} 1 MeV neutron equivalent, see Sect. 3.4 for further discussion).

Leakage current and damage constant α

In Fig. 3.17 we report the fluence dependence of the reverse leakage current per unit volume $J_{\rm leak}$, as measured for all devices after thermal annealing for 8 minutes at 80°C (the choice of the annealing state is consistent with what discussed in Sect. 3.3.2). A good uniformity is obtained between all devices, indicating that the leakage current increase does not depend on the substrate material, as expected from extensive results obtained after hadron irradiation [Mol99]. Two slightly different linear trends can be seen for the two different irradiation runs: this can be related, besides to errors in the determination of the electron fluences, to the particular conditions and irradiation history of each run. Indeed, especially for the highest fluences, i.e. for the 2004 run, several days were needed to achieve the desired fluences, with the devices kept at the room temperature of the LINAC during the corresponding nights. A linear fit of the experimental data gives a slope of $9.0 \cdot 10^{-19}$ A/cm for the 2003 data and $6.4 \cdot 10^{-19}$ A/cm for the 2004 data; according to Eq. 3.7, this can be considered an experimental estimation of the leakage current damage constant α, referred to the actual electron fluence (in Eq. 3.7 the radiation-induced variation ΔI of the leakage current density is replaced by the current density after irradiation, which is orders of magnitude higher than the pre-irradiation one).

According to Eq. 3.4, the hardness factor of 900 MeV electrons with respect to 1 MeV neutrons can be estimated from the ratio of the damage constant α thus measured and the value reported in the literature for 1 MeV neutrons after the same annealing cycle, namely

$4.0 \cdot 10^{-17}$ A/cm [Mol99]. This yields a value of $\kappa = 2.3 \cdot 10^{-2}$ and $\kappa = 1.6 \cdot 10^{-2}$ for the 2003 and 2004 data, respectively. Using the NIEL calculation relative to 200 MeV (the highest available energy in the literature) electrons in [Sum93], and extrapolating it to higher energies thanks to the saturating trend of the displacement damage function as a function of the electron energy (see Fig. 3.1), the ratio of the NIEL values for high-energy electrons and for 1 MeV neutrons is $8.1 \cdot 10^{-2}$. The experimental values are on average $\sim$4 times smaller than this, and the NIEL scaling hypothesis seems therefore not adequate when comparing electron with hadron irradiation, even in the GeV electron energy range.

The discrepancy could be explained by considering the different relative contribution of radiation-induced point defects and clusters to the degradation of the carrier generation lifetime. Clusters, which are predominant after neutron irradiation, are more effective in producing generation current since they have defect levels very close to the midgap. Point defects, on the contrary, may also have energy levels close to the band edges. Even at equal NIEL, high-energy electrons may then be less effective than neutrons in degrading the carrier generation lifetime of the substrate material since they produce a higher relative amount of point defects with respect to clusters.

Annealing studies

Long-term annealing studies were performed after the 2003 irradiation run, on diodes irradiated at the two highest fluences ($1.4{\cdot}10^{15}$ and $2.1{\cdot}10^{15}$ e/cm^2, see Table 3.2). The annealing behavior at 80°C of N_{eff} and of the damage constant α has been monitored over a period of $\sim$800 hours. In the following experimental results obtained on CiS samples are reported. For high annealing times (>120 minutes), the measurements performed after each annealing step have been repeated after storing the samples for 24 hours in the dark at room temperature, in order to investigate the possible occurrence of transient effects in the depletion voltage appearing after the heat treatment, as first observed in [Mol95].

The annealing curves for the N_{eff} of StFZ and DOFZ samples from CiS are reported in Fig. 3.18. For these devices, which have undergone type inversion after irradiation, an initial beneficial annealing can be observed, leading to a minimum of N_{eff} after about 8 minutes, followed by an increase (reverse annealing), consistently with the well-known picture introduced in Sect. 3.1.3. A different behavior is observed between StFZ and DOFZ diodes after the additional heat treatment at room temperature: while the effective dopant concentration N_{eff} of StFZ devices decreases reaching an equilibrium value, no significant differences are observed in the case of DOFZ devices.

Following the parameterization introduced in [FeiTh] for the 3 components of the radiation-induced change in the effective dopant concentration ΔN_{eff} with respect to the pre-irradiation value $N_{\text{eff},0}$ (see Eqs. 3.5 and 3.6), the experimental points for StFZ devices can be fitted by the function:

$$|N_{\text{eff}}(t)| = N_0 + N_s e^{-t/\tau_s} + N_l(t) \tag{3.15}$$

where $N_0 = N_C - N_{\text{eff},0}$ represents the difference between the stable damage component N_C (independent from the annealing time) and the pre-irradiation effective dopant concentration

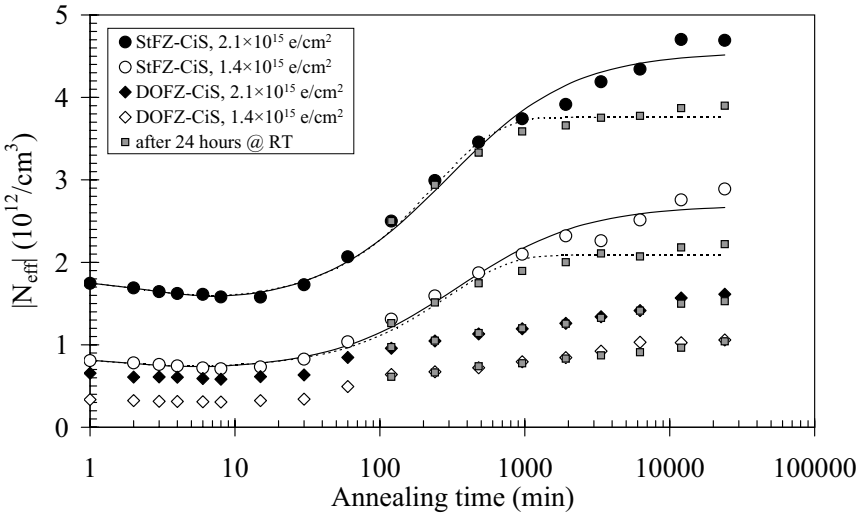

Figure 3.18: Effective dopant concentration for StFZ and DOFZ devices from CiS, as a function of the annealing time at 80°C. The data refer to devices irradiated at the two highest fluences of the 2003 run.

	$\Phi = 1.4 \cdot 10^{15}$ e/cm^2		$\Phi = 2.1 \cdot 10^{15}$ e/cm^2	
N_0	0.71 ± 0.05	0.69 ± 0.07	1.51 ± 0.06	1.49 ± 0.10
N_s	0.18 ± 0.27	0.19 ± 0.33	0.34 ± 0.18	0.35 ± 0.24
τ_s	1.6 ± 3.1	1.9 ± 4.5	2.7 ± 2.4	2.9 ± 3.7
N_1	1.38 ± 0.05		2.25 ± 0.07	
τ_1	293 ± 37		241 ± 22	
N_2		1.99 ± 0.08		3.07 ± 0.11
τ_2		342 ± 67		282 ± 43

Table 3.4: Values of the fit parameters for the experimental curves of the N_{eff} of StFZ devices from CiS as a function of the annealing time at 80°C, reported in Fig. 3.18. For each fluence, the two columns report the fit parameters for a first and second order process, respectively (see text). τ_s and $\tau_{1,2}$ are expressed in minutes, N_s and $N_{0,1,2}$ in 10^{12} cm^{-3}.

$N_{\text{eff},0}$. The second term, with amplitude N_s, accounts for the exponential behavior of the short-term annealing (the N_A component in Eq. 3.6).

As for the long-term component $N_l(t)$, representing the reverse annealing component in Eq. 3.6, the experimental points obtained after the additional tempering for 24 hours at room temperature are best fitted by a function $N_{l,1}(t) = N_1(1-e^{-t/\tau_1})$, describing a first order process in the defect kinetics, while the measurements obtained immediately after the 80°C annealing steps are better described by a function $N_{l,2}(t) = N_2\left(1-\frac{1}{1+t/\tau_2}\right)$, describing a second order process. According to [Mol95], this difference in the annealing behavior is attributed to the generation of bistable defects, whose activation and annihilation depend on the particular heat treatment used. The values of the parameters coming from fitting the experimental curves are reported in Table 3.4.

For DOFZ devices, a similar parameterization of the annealing curves is not straightforward, since it is not possible to clearly separate the two different components of the reverse annealing; on the other side, a fit taking into account both components would not be reliable because of the high number of free parameters (7) when compared to the number of experimental points (18).

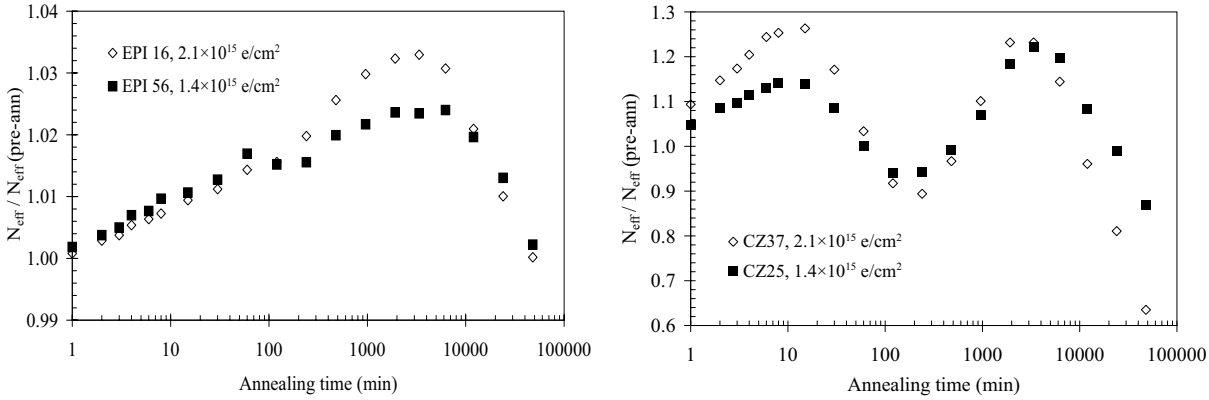

Figure 3.19: Effective dopant concentration for EPI (left) and CZ (right) devices from CiS, normalized to the pre-annealing values, as a function of the annealing time at 80°C. The data refer to devices irradiated at the two highest fluences of the 2003 run.

The annealing behavior of N_{eff} for EPI and CZ devices, which have not undergone type inversion, is reported in Fig. 3.19, where N_{eff} measured after each annealing step is divided by the pre-annealing value, in order to highlight the relative variations occurring during the tempering process. In the case of EPI samples, an initial increase of N_{eff} with time is observed, then a decreasing trend starts at very long annealing times. The observed variations are very small, in the order of a few percent. On the other side, CZ devices show an atypical behavior, with significant variations (order of 20-30%). The reasons for this peculiar time-dependence, which is similar to the one observed after hadron irradiation [HoeTh], are at present still not understood and under investigation. It is nevertheless interesting to notice that the behavior is reproduced on the same time scale (i.e. the series of maximum and minimum values are reached

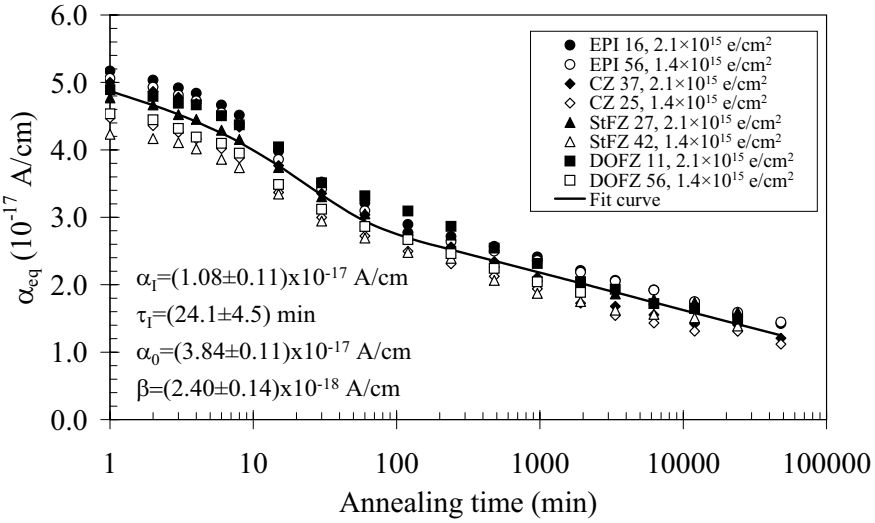

Figure 3.20: Leakage current damage constant α for all CiS devices as a function of the annealing time at 80°C. The data refer to devices irradiated at the two highest fluences of the 2003 run.

at equal times) for diodes irradiated at different fluences, and that the maximal variation of N_{eff} with respect to the pre-annealing value is much more contained than in the case of StFZ and DOFZ devices.

Figure 3.20 reports the annealing behavior of the damage constant α_{eq}

$$\alpha_{\text{eq}}(t) = \frac{J_{\text{leak}}(t)}{\Phi_{\text{eq}}} \tag{3.16}$$

related to the equivalent 1 MeV neutron fluence $\Phi_{\text{eq}} = \kappa \cdot \Phi_{\text{el}}$, where $\kappa = 2.3 \cdot 10^{-2}$ is the hardness factor, as estimated after the 2003 irradiation run, J_{leak} the leakage current volume density and Φ_{el} the actual electron fluence. The same functional dependence on the annealing time is observed for all devices, independently of the substrate material. All the experimental points have been fitted by means of the following parameterization [Mol99]:

$$\alpha_{\text{eq}}(t) = \alpha_I \cdot \exp\left(-\frac{t}{\tau_I}\right) + \alpha_0 - \beta \cdot \ln\left(\frac{t}{t_0}\right) \tag{3.17}$$

where the exponential component describes the initial short-term annealing, and the logarithmic one accounts for the long-term annealing; α_I, τ_I, α_0 and β are the free parameters of the fit, while t_0 is set to 1 minute (the parameterization is valid for $t \geq 1$ minute). The values of the free parameters calculated from the fit are reported in Fig. 3.20; they show a significant agreement with results obtained after hadron irradiation [MolTh, Mol99], providing further confirmation of the universal behavior of the damage constant α (i.e. of the leakage current density) with respect to thermal annealing.

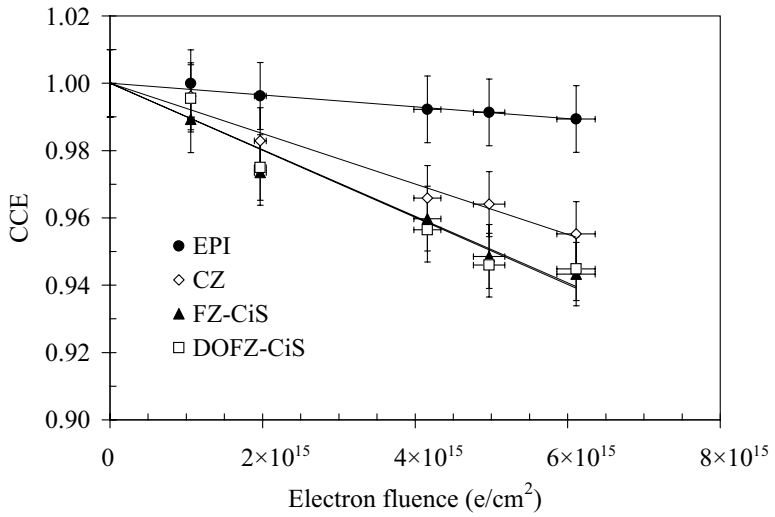

Figure 3.21: Charge collection efficiency measured on CiS devices, after thermal annealing for 8 minutes at 80°C, after the 2004 irradiation run.

3.3.3 Charge collection efficiency measurements

The charge collection efficiency (CCE) has been measured by means of the Transient Current Technique (TCT) on CiS samples annealed for 8 minutes at 80°C. The charge injection has been performed by making use of a collimated beam of α particles from a ^{244}Cm source hitting the diodes on the junction side (front illumination), as explained in Sect. 3.2.3. The CCE has been calculated as the ratio between the charge collected in irradiated and non-irradiated devices. During the measurements, the bias voltage was adjusted for every device in order to ensure an overdepletion condition.

The results obtained after the 2004 irradiation run are reported in Fig. 3.21, for measurements performed at the laboratory room temperature, typically varying between 20 and 22°C. The single points represent averages done over measurements performed for several bias voltages above the full depletion voltage. A slight decrease of the CCE, qualitatively described by a linear trend, can be observed for all devices as a function of the increasing electron fluence. The relative variations, despite being quite small and comparable with the experimental error, are nevertheless different for the different materials considered: the decrease at the highest fluence is within 1% for EPI devices, and of about 4% for CZ devices; a slightly more pronounced decrease, of between 5 and 6% is associated with StFZ and DOFZ samples, which show a rather uniform behavior, therefore not hinting, at least in the fluence range considered, at improvements due to oxygenation of the substrate.

The better performance of EPI devices was expected considering their reduced thickness (50 μm), which results in a shorter collection time compared to all other devices, of 300 μm thickness, and therefore in a reduced effect of trapping of the drifting charge.

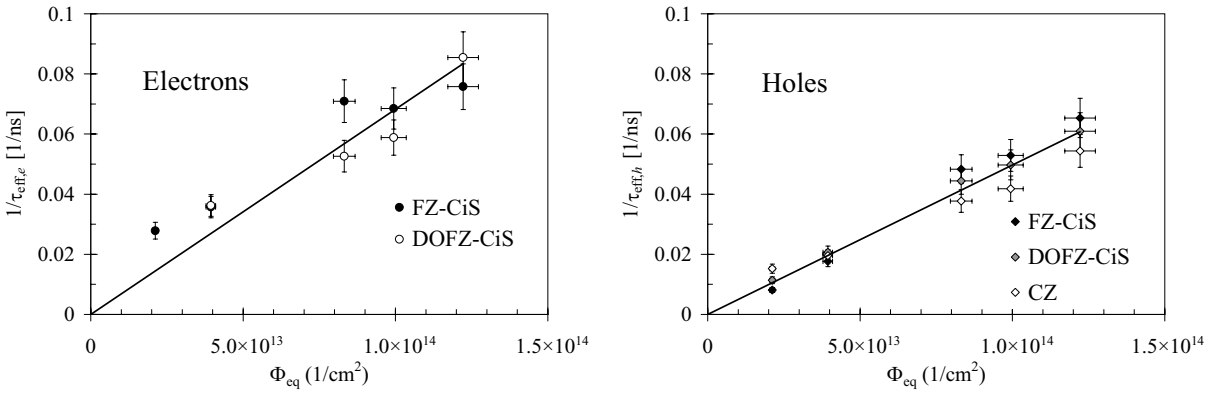

Figure 3.22: Fluence dependence of the effective trapping probability for electrons (left) and holes (right) determined from TCT measurements. Measurements were performed at room temperature on devices annealed for 8 minutes at 80°C, after the 2004 irradiation run.

3.3.4 TCT measurements of trapping probability

The effective trapping probability for holes and electrons has been measured by means of the TCT technique on StFZ, DOFZ and CZ samples from CiS irradiated in the 2004 irradiation run, after an annealing cycle of 8 minutes at 80°C. The charge correction method was applied in the analysis of the experimental data as described in Sect. 3.2.3. Such measurements were not possible on EPI devices, since in the used experimental setup the time constant $\tau_{\mathrm{RC}} \approx$2.8 ns of the signal amplifier is much higher than the charge collection time in the detector (e.g. for electrons ∼250 ps for an applied voltage of 100 V), due to the high capacitance ($C \approx$56 pF) of the latter with respect to 300 μm thick, higher resistivity devices. Moreover, the data measured with front injection on CZ devices could not be analyzed properly: the measured trapping probability was not showing a clear dependence on the irradiation fluence, and yielded always values close to those that could be detected on pre-irradiated devices. A similar difficulty with CZ devices from CiS has been reported by other users of the same experimental setup [Hoe05]. This is probably related to process-induced defects, or to the presence of a dead layer on the detector top side, as proposed in [HoeTh].

Figure 3.22 reports the fluence dependence of the effective trapping probability for electrons and holes as measured at room temperature (i.e. 20-21°C)[3]. Within the experimental errors, a good uniformity between different materials is observed in the case of hole injection, while the data from electron injection show larger fluctuations. The effective trapping damage constants for electrons and holes (Eq. 3.8) can be estimated from the linear fit of the two distributions as β_e=(6.8±0.3)·10^{-16} cm^2/ns and β_h=(5.0±0.1)·10^{-16} cm^2/ns, respectively. The value for electrons is thus found larger than the one for holes, in contrast with measurements performed after hadron irradiation, namely 190 MeV/c pions and 24 GeV/c protons, which showed trapping

[3]The trapping probability depends on temperature (see Eq. 3.8), as systematically investigated for example in [KraTh, HoeTh, SchTh]. The variation due to different measurement temperatures within a few °C is nevertheless negligible.

probabilities systematically lower for electrons with respect to holes [KraTh, SchTh] or similar in both cases [HoeTh, Kra04]. The value measured here for β_h is in quite good agreement with the corresponding measurement reported for example in [SchTh, Kra04], but a predominance of electron trapping was so far not reported. Nevertheless, it should be mentioned that most of the measurements performed after hadron irradiation considered a much larger fluence range (up to an equivalent fluence of $\sim 10^{15}$ cm^{-2}) than the one considered here; indeed, the determination of $\beta_{e,h}$ would strongly depend on eventual experimental points at higher fluences. Further investigations are needed in order to understand if the observed difference is a result of the smaller fluence range considered, or should rather be attributed to a different microscopic behavior of electron-induced damage with respect to hadron damage.

3.4 Summary of radiation hardness studies

Irradiations with 900 MeV electrons have shown different behaviors in the electrical and annealing characteristics of silicon devices manufactured from different substrate materials. Substrate type-inversion is observed for diodes fabricated on float-zone detector-grade material, both standard (StFZ) and diffusion-oxygenated (DOFZ). A beneficial effect of oxygen diffusion is nevertheless evident in the lower acceptor introduction rate associated with DOFZ devices, which translates into a smaller stable damage component. A long-term annealing at high temperature enhances the more favorable behavior of DOFZ devices.

Devices manufactured on thin epitaxial layers (EPI) and on Czochralski (CZ) substrates, which are relatively new materials with regard to their possible application in particle detectors, show in comparison promising performances: type-inversion does not appear at the fluences considered, and a decrease of the detector depletion voltage, more pronounced for CZ devices, is instead observed as a function of the increasing electron fluence. The difference with respect to StFZ and DOFZ devices can be attributed on one side to the higher initial doping of these substrates (in particular for EPI devices), on the other side to the significant oxygen concentration in their bulk, of the same order as for DOFZ in the case of EPI samples, and almost one order of magnitude higher in the CZ case (see Table 3.1).

The advantage of using a thinner substrate with a higher initial doping concentration was first highlighted in [Kra03b] after irradiation with high-energy protons at much higher fluence levels. Figure 3.23 shows the depletion voltage variation measured on the same silicon devices from CiS considered in this work, after irradiation with 24 GeV/c protons up to an equivalent fluence of $1.3{\cdot}10^{15}$ cm^{-2}. The measurements refer to the so-called "CERN-scenario" experiment, in which consecutive irradiation steps are followed by annealing for 4 minutes at 80°C and a C/V-I/V characterization. It can be seen that while StFZ and DOFZ samples undergo type inversion at relatively low fluences, EPI devices exhibit only a moderate variation of the depletion voltage (i.e. of N_{eff}) over the whole fluence range. This could be explained by considering that the generation of oxygen-related donor centers during irradiation may lead to a compensation of the radiation-induced acceptor introduction, thus limiting the change in the effective dopant concentration. This result has been further extended after irradiation with high-energy protons and neutrons up to equivalent fluences of $\sim 10^{16}$ cm^{-2} [Fre05, Lin05], and shows that thin epitaxial detectors

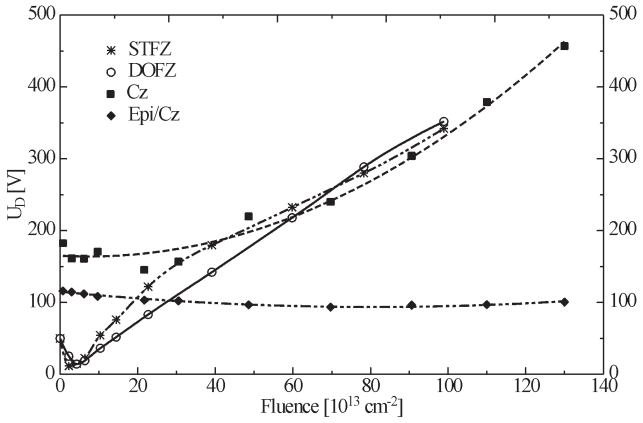

Figure 3.23: Change of depletion voltage after irradiation with 24 GeV/c protons of the same CiS diodes considered in this work (from [StaTh]).

are a viable option for the innermost layers of tracking detectors at the SuperLHC (see also Sect. 6.1).

The annealing curves of EPI and CZ samples measured in this work after electron irradiation do not follow a standard behavior as float-zone devices, but anyway show how even at very long annealing times a full depletion condition can be reached with bias voltages which do not exceed by more than 20-30% the pre-annealing value, which is lower than the pre-irradiation one. In particular, for EPI devices, the very small variations in the N_{eff} as a function of the annealing time show, in view of their eventual application in particle detectors, how a proper maintenance scenario can be found resulting only in moderate changes of N_{eff} during long operational times. This could be achieved even by keeping the detector at close to room temperature, as remarked in [Kra03b, Lin05].

The increase of the reverse leakage current after irradiation has shown for all devices a uniform linear trend as a function of the electron fluence, and has allowed the experimental estimation of $\kappa \approx 2 \cdot 10^{-2}$ for the hardness factor of 900 MeV electrons with respect to 1 MeV neutrons. This value is smaller than the one predicted by the NIEL scaling hypothesis, and the deviation can probably be explained by a more pronounced introduction of point defects with respect to cluster formation. The annealing of the leakage current density, described by the time evolution of the damage constant α, shows for all materials a universal behavior, in agreement with the standard parameterization proposed for hadron irradiation.

Only a slight degradation of the charge collection efficiency versus the electron fluence has been observed for all devices, a better performance being nevertheless evident in EPI samples, showing that all materials still retain good particle detection capabilities at the fluences considered. The measurement of the effective trapping probability for electrons and holes would suggest a predominance of electron trapping with respect to hole trapping, in contrast with results obtained after hadron irradiation at much larger particle fluences. Further investigations

are indeed needed, in order to understand if the effect is peculiar to electron irradiation or is rather a result of the limited fluence range considered.

On the whole, the results presented in this chapter confirm the effectiveness of high-energy electrons in creating bulk damage in silicon, and in deteriorating correspondingly the detector characteristics. Moreover, they also give a hint to the improvements in radiation hardness which are achievable by considering different materials and design approaches, e.g. thinner detectors with a higher initial resistivity. The issue of electron damage in silicon is particularly important for the application of silicon detectors at future lepton colliders, e.g. at the International Linear Collider, where the background in the first layers of the silicon vertex detector will be dominated by $\sim$10 MeV electrons (Sect. 1.2). Despite the higher energy considered in this study, and the different effects expected at lower energies (e.g. in the relative contributions from point defects and clusters, by approaching the threshold energy for formation of the latter), the results presented here can give an indication of the impact of such radiation on the operation of silicon detectors, also considering the unavailability of systematic studies performed at lower electron energies.

Chapter 4

Simulation of Thin Silicon Pixel Detectors

The use of position sensitive silicon detectors is foreseen in almost all high-energy physics experiments at future particle colliders. The requirements imposed on the detector technology are closely related to the conditions in which the sensors will have to operate.

For the application of pixel sensors in the innermost layers of tracking detectors at the LHC, and moreover at the SuperLHC, the challenge for the detector technology is to sustain the high radiation fluences, since detectors will be put very close to the interaction point and thus exposed to very large particle fluxes (Sect. 1.1). At the expected fluences, effective trapping times become comparable with charge collection times, resulting not only in the reduction of the charge collection efficiency, but also in other important phenomena depending strongly on the detector design. The first part of this chapter (Sect. 4.1) will present the simulation of charge collection in heavily irradiated, reverse-biased silicon pixel detectors, with the prediction of their performance at the fluence levels expected at the SuperLHC.

On the other side, in order to fulfill the physics reach of the International Linear Collider (ILC), the vertex detector technology needs to combine a high granularity with a fast readout and the smallest possible material budget (Sect. 1.2). Because of these requirements, present-day silicon hybrid pixel detectors are not considered as an option for such an application, mainly due to the considerable amount of material introduced by having a separate sensor and readout chip, besides the possible limitations in granularity arising from the use of the bump-bonding technology for the interconnections (see Sect. 2.6.1). The R&D focus is then concentrated on technologies which combine a thin detector with the possibility of placing the readout electronics outside the sensitive area. This can be achieved, for example, by making use of the thin, high quality epitaxial layers provided by the CMOS technology as the sensitive volume, like in the case of Charge-Coupled Devices (CCDs) or Monolithic Active Pixel Sensors (MAPS), and by implementing the readout circuitry and the signal processing electronics at the edges or at the ends of the detector ladders. Among the technologies presented in Sect. 2.6, MAPS are a good candidate for such an approach, thanks to the possibility of integrating readout functionalities

on the same sensor substrate. As described in Sect. 2.6.3, the physical principle governing such technology does not rely on the presence of an electric field in the detector volume, and is therefore determined by diffusion of the generated charge. The second part of this chapter (Sect. 4.2) will present an advanced device physics simulation of the charge collection properties of MAPS.

4.1 Simulation of heavily irradiated silicon pixel detectors

4.1.1 Simulation of the induced current in silicon detectors

The charge generated by an impinging ionizing particle in a reversely biased silicon detector drifts in the electric field and induces currents at the detector electrodes (Sect. 2.5.3). In the presence of trapping, the amount of the drifting charge, and consequently the induced current, decreases with time according to Eq. 3.12. The current $I_{e,h}$ induced in a sensing electrode by the drift of a point charge q is then obtained from Eqs. 2.28 and 2.29, and after correcting for trapping is given by

$$I_{e,h}(t) = q \exp\left(-\frac{t}{\tau_{\text{eff}_{e,h}}}\right) \vec{E}_w(\vec{r}_{e,h}(t)) \mu_{e,h} \vec{E}(\vec{r}_{e,h}(t)), \tag{4.1}$$

where $\vec{E}_w = -\nabla U_w$ is the weighting field with potential U_w, describing the electrostatic coupling between the drifting charge and the sensing electrode, $\tau_{\text{eff}_{e,h}}$ is the effective carrier trapping time, $\mu_{e,h}$ the carrier mobility and $\vec{r}_{e,h}(t)$ the trajectory obtained by solving the equation of motion in the electric field $\vec{E}$. The charge collected in the sensing electrode is then calculated by a straightforward integration of the induced current, and the charge collection efficiency (CCE) is estimated as the ratio between the induced and the generated charge.

In this work, the simulation of the drift and the calculation of the induced current for minimum ionizing particles in a reversely biased silicon detector has been performed by custom-made software, using the approach described in detail in [KraTh, Kra01, Kra02c]. Electric and weighting field calculations have been performed by using the ISE-TCAD commercial package [TCAD], which allows the description of complex 3-dimensional structures and the fast solution of the field equations.[1] The charge generated by a minimum ionizing particle traversing the detector has been simulated considering the most probable energy loss in silicon, i.e. 80 e-h pairs are generated per μm of the particle path.

All simulations have been performed considering an operational temperature of $T = 263$ K. The bulk of non-irradiated detectors was always assumed to be n-type silicon with initial dopant concentration $N_{\text{eff}} = 10^{12}$ cm^{-3}. After irradiation the effective dopant concentration is assumed to be spatially uniform and increasing linearly with fluence as $N_{\text{eff}} = -g \cdot \Phi_{\text{eq}}$. The parameter $g = 0.0071$ cm^{-1} corresponds roughly to the minimal $|N_{\text{eff}}|$ during annealing for an oxygenated

[1] The ISE-TCAD package will be described in more detail in Sect. 4.2, where it will be extensively employed in the simulation of Monolithic Active Pixel Sensors.

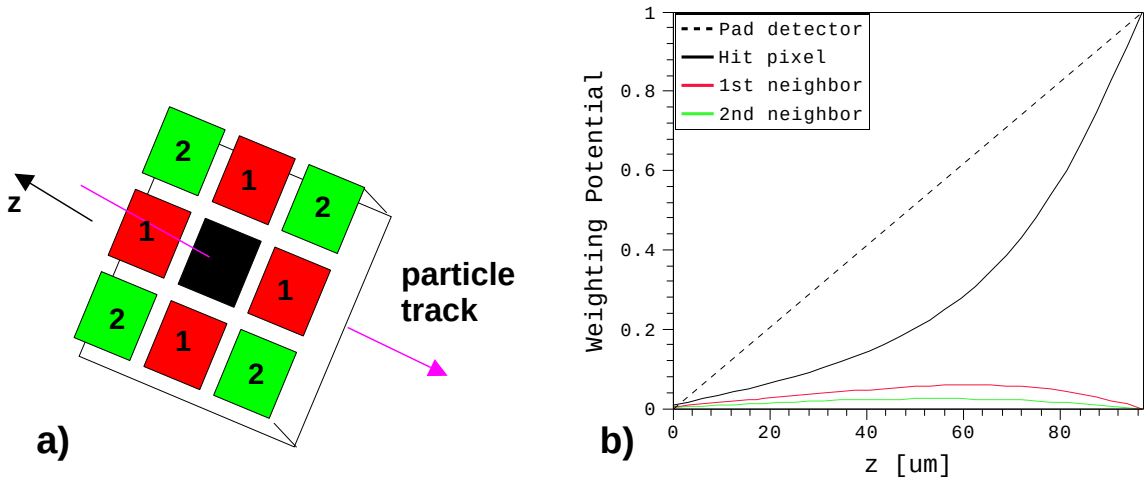

Figure 4.1: (a) Schematic picture of the simulated structure of 3×3 pixels. The pixel pitch is 70×70 μm^2, the implant width 50×50 μm^2 and the detector thickness 100 μm. The minimum ionizing particle track is simulated through the center of the central pixel (hit pixel). Neighboring pixels are denoted by the corresponding numbers. (b) Weighting potential along the axis through the center of the hit pixel and through the center of the two closest neighbors. For comparison U_w of a pad detector is also shown.

material irradiated with high-energy charged hadrons [RD48]. The corresponding trapping probabilities can be calculated as $1/\tau_{\mathrm{eff}_{e,h}} = \beta_{e,h}\Phi_{\mathrm{eq}}$, with proportionality factor $\beta_e = 5.7 \cdot 10^{-16}$ cm^2/ns and $\beta_h = 7.7 \cdot 10^{-16}$ cm^2/ns taken from [Kra02b].

In the following sections we will first review the general properties of charge collection in segmented devices, before and after irradiation, then the simulation of pixel detectors for application at the SuperLHC will be presented, with particular emphasis on the collected charge as a function of the sensor geometrical parameters like thickness, pixel pitch and implant width. It is indeed important to distinguish between the size of the pixel cell (i.e. the pixel pitch) and the actual size of the collecting electrode, i.e. the size of the metal contact on top of the implant, which determines the electrode capacitance and thus the weighting field distribution.

4.1.2 Charge collection in segmented detectors

The charge collection in segmented devices differs from the one in the simple pad detectors (diodes) which are widely used in radiation damage studies. The difference comes mainly from the $\vec{E}_w$ term in Eq. 4.1 as illustrated in Fig. 4.1. The charge generated by an ionizing particle traversing along the axis through the center of the pixel (Fig. 4.1a) drifts in an approximately linear electric field similar to the one in a diode. On the other side, the weighting field in such pixel detector differs substantially from that of the diode as can be seen in Fig. 4.1b. If z_1 and z_2 are two points along the drift path, the difference $U_w(z_2) - U_w(z_1)$ measures the fraction of the drifting charge induced in the sensing electrode when the charge drifts from z_1 to z_2.

In the case of a pad diode, due to the constant E_w, it follows that holes and electrons drifting

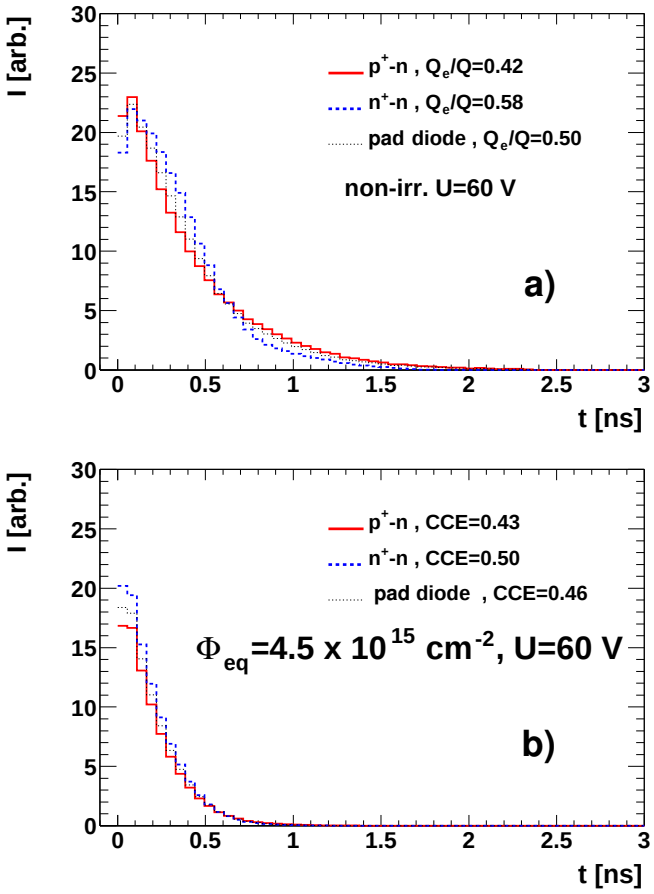

Figure 4.2: Simulated total induced current in central pixel (see Fig. 4.1a) of a 50 μm thick pixel detector with a pitch of 70×70 μm^2 and an implant width of 50×50 μm^2, for a track traversing the detector through the pixel center: (a) before irradiation; the contribution of the electrons drift to the induced charge is denoted by Q_e/Q; (b) after irradiation. Note that the sign of the induced current in the $n^+ - n$ detector is reversed for easier comparison.

to opposite directions contribute equally to the induced charge. On the other hand, in the case of the pixel detector, the carriers drifting to the segmented side contribute more to the charge induced in the hit pixel.

This is illustrated in Fig. 4.2a, which shows the currents induced in a non-irradiated diode and pixel detector collecting electrons (n^+ pixels) and holes (p^+ pixels)[2]. The simulation refers to a detector thickness of 50 μm. A clear difference can be seen between the induced currents in the two pixel types and in the diode, however their integral, i.e. the induced charge is the same for all three cases. This is not true anymore in an irradiated detector as can be seen in Fig. 4.2b.

[2]The initial rise in the simulated curves is a result of the discrete binning of the histograms. Indeed, the simulation is performed in discrete steps, and the initial time step of the carriers starting their drift in the low field region may be longer than the width of the first bin, thus filling the second bin instead of the first.

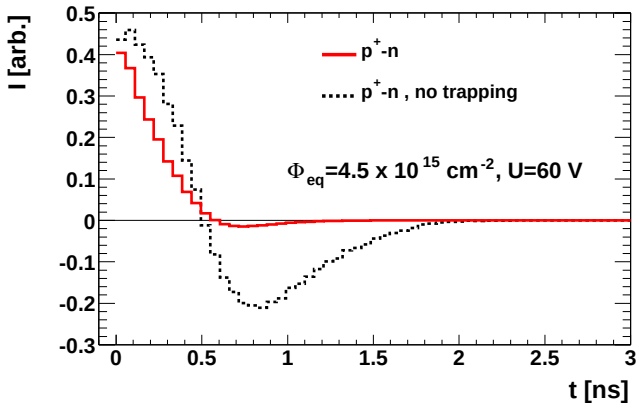

Figure 4.3: Current induced in the first neighboring pixels (p^+ pixel case), after irradiation and comparing the case in which trapping is and is not included in the simulation. The pixel detector geometry is the same as considered in Fig. 4.2.

Shorter trapping times of holes than of electrons and their slower drift have as a consequence a smaller CCE in a $p^+ - n$ detector compared to a $n^+ - n$ detector, with the CCE of the diode in between.

Trapping has important consequences also on the detector charge sharing mechanism. If all the pixels were connected to the same amplifier, such circuit would be equivalent to a diode. Therefore the sum of the charges induced in all the pixels should equal that of the diode $\sum_{\text{pixel}} Q_i = Q_{\text{diode}}$. Larger (smaller) charge induced in the hit pixel compared to the charge induced in the diode inevitably leads to charge of the opposite (same) sign induced in the neighboring pixels. This reasoning is confirmed by the simulation shown in Fig. 4.3. The integral of the bipolar current pulse induced in the first neighbors by the drift of charge to the hit pixel does not vanish in presence of trapping. This effect is far more pronounced in detectors with p^+ pixels, due to the larger hole trapping. Hence, incomplete charge collection due to trapping has as a consequence a charge sharing mechanism which can dominate over diffusion in heavily irradiated detectors.

The reduction of CCE represents a serious danger of loss of detection efficiency. The charge induced on the electrode can become comparable with the detection cuts applied to reduce the noise occupancy of the electrode. Therefore, $n^+ - n$ detectors seem more appropriate for operation in harsh radiation environments. An additional advantage of the negative signals induced on the neighbors, i.e. of the higher positive signal induced in the hit electrode, is the increase of the signal-to-noise ratio in the latter.

4.1.3 Simulation of thin pixel detectors

As already mentioned, the possible upgrade of the LHC will put higher demands on the silicon vertex detectors, whose innermost layers will have to sustain equivalent fluences of $\sim 10^{16}$ cm^{-2}

in the planned 5 years of operation. The physics requirements as well as the harsh radiation environment will require the use of thin pixel detectors. Thinner detectors have smaller leakage current ($I_{\text{leak}} \propto D$) and full depletion voltage ($V_{\text{dep}} \propto D^2$) compared to standard 300 μm thick detectors. The reduced thickness implies a shorter collection distance and therefore shorter collection times. In addition, the lower mass and consequently the smaller radiation length makes them favorable also in terms of material budget. The main disadvantage in the use of thinner detectors comes from the smaller signals obtainable compared to thicker detectors; this puts severe requirements on the readout electronics which, besides being radiation hard, has to assure a good low-noise performance. Another consequence of the reduced thickness is the increase of the detector capacitance, which can eventually be compensated by smaller cell sizes.

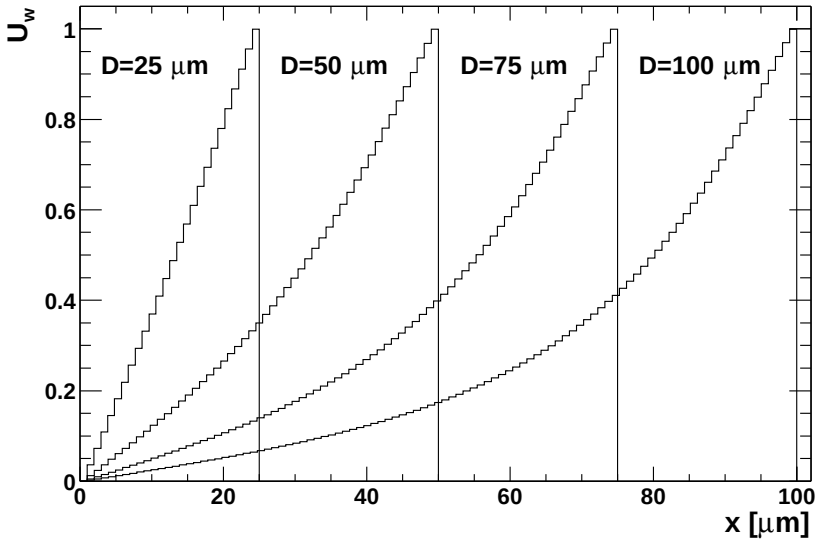

Figure 4.4: Weighting potential along the axis through the central pixel for thin pixel detectors. The detector back-plane is at x=0 in all cases.

In the following we present the simulation of 3×3 pixel arrays of pitch 70×70 μm^2 and implant width of 50×50 μm^2, with different thicknesses between 100 and 25 μm. Results will be shown only for particle tracks passing through the center of the central pixel as illustrated in Fig. 4.1a. The calculated weighting potential along the same axis is shown in Fig. 4.4 for the different thicknesses considered. It can be seen that by decreasing the thickness, the weighting potential approaches a linear distribution, i.e. like in a diode. This is consistent with the fact that the ratio between implant width (fixed at 50 μm) and detector thickness is increasing, the same ratio being $\gg$1 in common diodes. In such a case, after the considerations exposed in Sect. 4.1.2, no difference in charge collection is expected between n^+ and p^+ pixels.

The induced charge simulated at different fluences for thin detectors of different thicknesses is shown in Fig. 4.5. As expected, as the ratio between the electrode area and the sensor thickness increases, the difference between n^+ and p^+ pixel detectors decreases: for the D=25 μm case, the performance of the two pixel types is identical, while the better performance of n^+ pixels

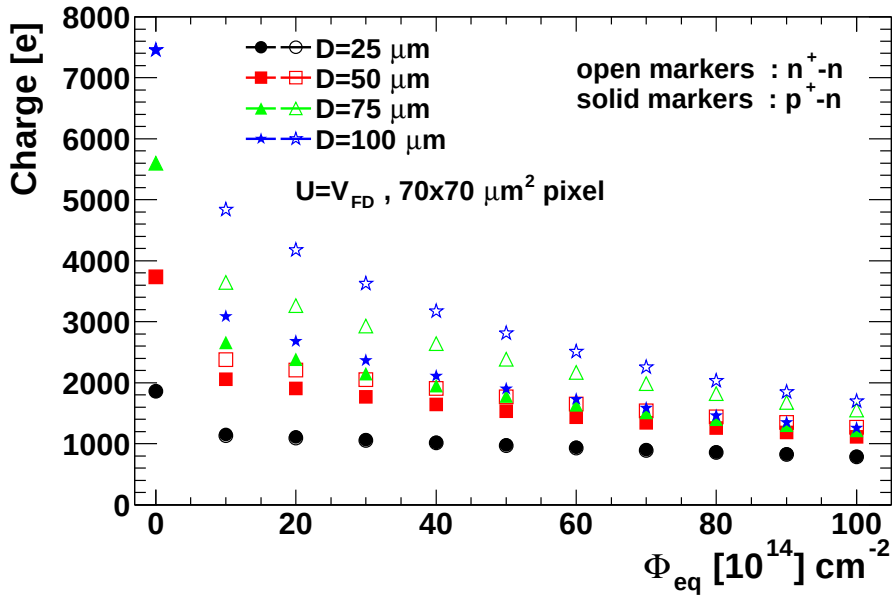

Figure 4.5: Induced charge as a function of fluence in thin pixel detectors of different thicknesses operated at V_{dep} [Kra03].

becomes visible at bigger thicknesses.

A significant decrease of the induced charge, more pronounced for a larger detector thickness, can be noticed after the first simulated fluence Φ_{eq}=10^{15} cm^{-2}: this is related to the operation of detectors at the full depletion voltage V_{dep}, which is quite low[3] (e.g. 54 V for 100 μm thick devices), resulting in large charge losses due to trapping.

At the highest fluences, the correspondingly short trapping times diminish the importance of thicker detectors: the ratio between the charge collected by a 100 μm thick detector and a 25 μm one is $\sim$2, which is smaller than the factor of 4 difference in the thicknesses. A signal of around 2000 e can be expected at the highest fluences for a detector with D=100 μm, decreasing to about 1200 e for D=50 μm. Such signals can be large enough for successful operation providing that the electronics survives the irradiation and introduces low noise.

Figure 4.6 shows the charge induced in the central pixel and in the neighboring pixels in the case of thickness D=100 μm, both for p^+ and n^+ pixels. It can be seen that the charge induced in the neighboring pixels can be significant: depending on the fluence, a charge of a few 100 e is induced in the four closest neighbors and also further in the second closest neighbors. This trapping-induced charge sharing can be used to improve the position resolution providing that the electronics is sensitive also to induced charge of the opposite polarity, such as the one induced in the case of n^+ pixels.

An obstacle for the operation of thin detectors could be the breakdown due to the high

[3]The full depletion voltage V_{dep} can be calculated from Eq. 3.14 with $|N_{\mathrm{eff}}|$=0.0071·Φ_{eq}, see Sect. 4.1.1.

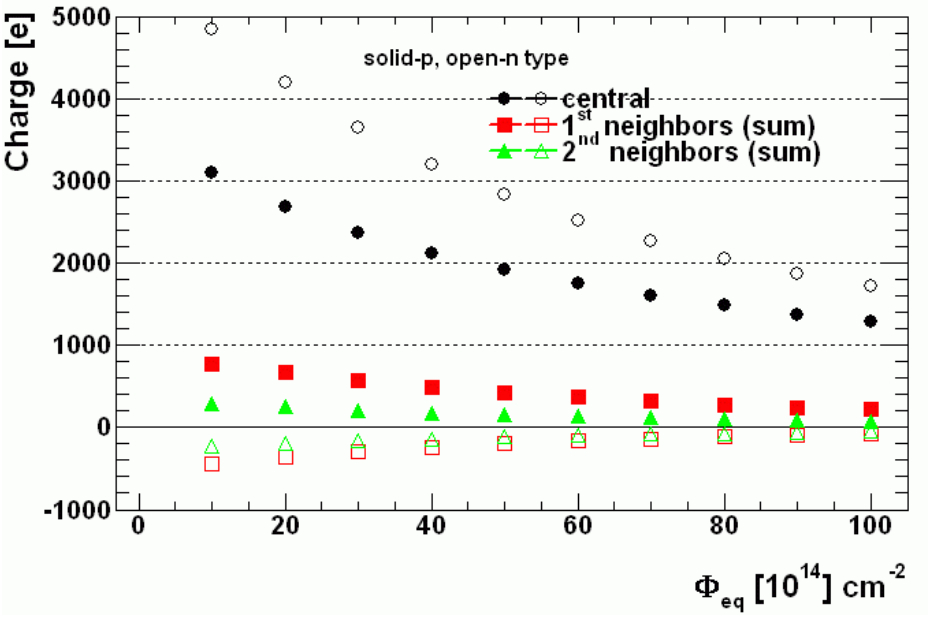

Figure 4.6: Induced charge in the hit (central) pixel and in the first closest neighbors for 100 μm thick $p^+ - n$ and $n^+ - n$ pixel detectors, operated at V_{dep} [Kra03].

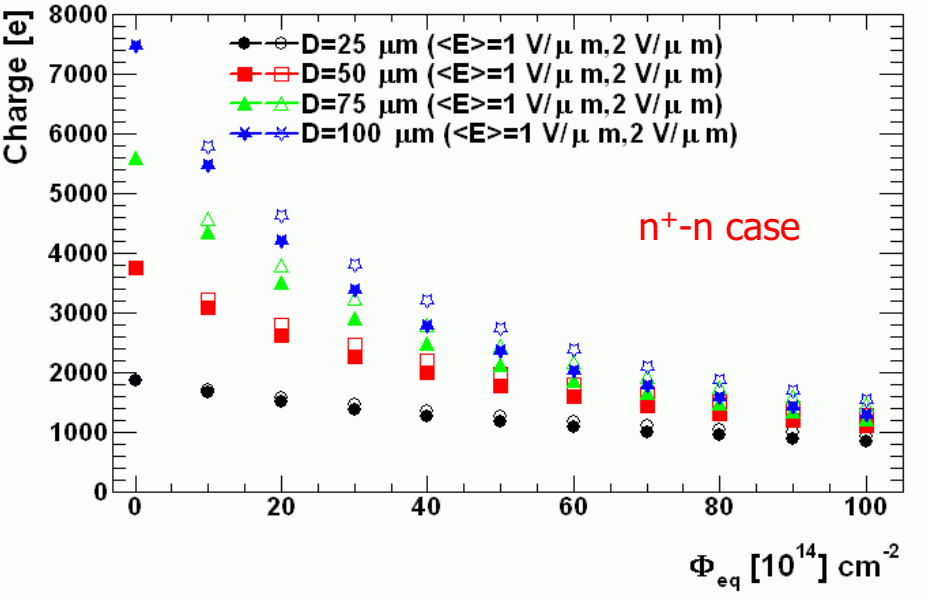

Figure 4.7: Induced charge as a function of fluence with $N_{\text{eff}} \sim 0$ - constant electric field - for $n^+ - n$ detectors of different thicknesses, with 70×70 μm^2 pixel pitch and 50×50 μm^2 implant width [Kra03].

electric field, coming from the increase of the operational voltage combined with a reduced thickness. For example, for D=100 μm an average electric field $< E >$=52 kV/cm is expected. As remarked in Sect. 3.4, detectors produced from epitaxial and Czochralski substrates are very promising in terms of $V_{\rm dep}$ change after irradiation. In the ideal case the silicon material would have $N_{\rm eff} \approx 0$, so that the electric field across the detector would be constant. Figure 4.7 shows the simulated induced charge in such a detector (with n^+ pixels) at electric fields of 10 kV/cm and 20 kV/cm, using the same geometrical parameters as before and for different thicknesses. From the comparison with Fig. 4.5, it can be seen that, at the same thickness, the induced charge does not differ much from the one in detectors with large $N_{\rm eff}$. In addition, a higher electric field does not improve the induced charge significantly, due to the saturation of the carrier drift velocity.

4.2 ISE-TCAD simulation of Monolithic Active Pixel Sensors

In order to study the charge collection mechanism and its time properties in Monolithic Active Pixel Sensors, and to give a quantitative estimation of the collected charge and of its spatial charge spreading onto neighboring pixels, device physics simulations have been performed by means of the ISE-TCAD commercial package [TCAD].

Most commercially available packages allow 2-dimensional modeling of the simulated device. This approach has nevertheless a limitation for the simulation of pixel detectors, which are intrinsically 3-dimensional devices. The ISE-TCAD package was therefore chosen for its capabilities of a 3-dimensional modeling of the simulated device. This software allows a detailed description of the detector geometry and physical parameters (e.g. doping profiles), complemented with advanced physical models for the description of carrier mobility, recombination and transport mechanisms. A great flexibility in the simulation is also given by the possibility of studying the simulation results as a function of the parameters by varying them within the same simulation session.

4.2.1 The simulation tool: the ISE-TCAD package

Electrical models

Charge collection simulation is based on the *drift-diffusion* transport model, whose variables are the electrostatic potential ψ and the electrons and hole concentrations n and p. The three basic equations governing the model are the Poisson equation, which relates the electrostatic potential to the local charge densities, and the continuity equations for the description of the evolution of the electron and hole densities as a result of the transient transport, generation and recombination processes. The Poisson equation is written as:

$$\nabla^2\psi = -\frac{q}{\epsilon_0\epsilon_{\rm Si}}(p - n + N_D^+ - N_A^-) \tag{4.2}$$

where ϵ_0 and ϵ_{Si} are the electrical permittivity of vacuum and the dielectric constant of silicon, and N_D^+, N_A^- are the concentrations of ionized donors and acceptors, respectively. Phosphorus and boron atoms are usually used as donors and acceptors in common CMOS processes. Their energy levels in the silicon band gap are sufficiently shallow to justify the assumption of complete ionization at room temperature.

The density of charge created in any part of the detector by an impinging minimum ionizing particle is negligible compared to the density of ionized dopants at room temperature. The potential distribution in the detector volume can then be calculated by taking into account only the distribution of thermally generated charges and ionized dopants, and the external voltages applied to the contact electrodes. Hence, a time independent electric field can be assumed for the charge transport. In non-equilibrium conditions the electron and hole densities cannot be referred anymore to the Fermi level like in Eqs. 2.2; two separate *quasi-Fermi levels*, with corresponding *quasi-Fermi potentials* ϕ_n, ϕ_p, are introduced for electrons and holes in order to relate the carrier densities to the electrostatic potential for non-equilibrium conditions, as

$$n = N_C \exp\left(\frac{q\phi_n - E_C}{k_B T}\right) \quad \text{and} \quad p = N_V \exp\left(\frac{E_V - q\phi_p}{k_B T}\right) \tag{4.3}$$

where E_C and E_V are the energies of the conduction and valence band edges, and N_C and N_V are the effective densities of states in the conduction and in the valence band (Sect. 2.1). The quasi-Fermi potentials are given by

$$\phi_n = \psi - \frac{k_B T}{q} \ln\left(\frac{n}{n_{i,\mathrm{eff}}}\right) \quad \text{and} \quad \phi_p = \psi + \frac{k_B T}{q} \ln\left(\frac{p}{n_{i,\mathrm{eff}}}\right), \tag{4.4}$$

where $n_{i,\mathrm{eff}}$ is the effective intrinsic carrier density accounting for the effect of *band-gap narrowing* in the case of high doping concentrations. Following [Gre90], $n_{i,\mathrm{eff}}$ is defined as

$$n_{i,\mathrm{eff}} = n_i \gamma_{BGN} \quad \text{with} \quad \gamma_{BGN} = \exp\left(-\frac{\Delta E_g}{2 k_B T}\right) \tag{4.5}$$

where ΔE_g accounts for the band gap narrowing effect (see below for the detailed description of the band gap value dependence on doping and temperature). From Eqs. 2.7, by taking the gradient of Eqs. 4.3 and using the Einstein relation (Eq. 2.9), the continuity equations for electrons and holes are written

$$\vec{J_n} = -qn\mu_e \nabla\phi_n \quad \text{and} \quad \vec{J_p} = -qp\mu_h \nabla\phi_p \tag{4.6}$$

where μ_e, μ_h are the electron and hole mobilities, respectively.

Mobility and recombination lifetime parameterization

In the simulation of charge transport by thermal diffusion and of charge collection at the n-well/p-epi diode, a set of physics models is chosen. The carrier mobility is parameterized according to the Masetti model [Mas83], which takes into account its doping dependence. According

to this model, the carrier mobility is written

$$\mu_{\mathrm{dop}}(N_i) = \mu_{\mathrm{min1}} \exp\left(-\frac{P_c}{N_i}\right) + \frac{\mu_{\mathrm{const}} - \mu_{\mathrm{min2}}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \tag{4.7}$$

where $N_i = N_D^+ + N_A^-$ is the total concentration of the ionized donor and acceptor impurities, μ_{min1}, μ_{min2} and μ_1 are reference mobilities and P_c, C_r, C_s are reference doping concentrations[4]. The exponents are typically $\alpha \sim 0.7$ and $\beta = 2$ both for electrons and holes. The low-doping reference mobility μ_{const} is determined from the Constant Mobility model [Lom88], which assumes that the carrier mobility is only affected by phonon scattering and is therefore dependent only on the lattice temperature according to

$$\mu_{\mathrm{const}} = \mu_L \left(\frac{T}{T_0}\right)^{-\zeta} \tag{4.8}$$

where μ_L is the intrinsic reference mobility (1417 and 470.5 $\mathrm{cm}^2/\mathrm{V{\cdot}s}$ for electrons and holes, respectively) accounting only for lattice vibrations, and $T_0 = 300$ K is the reference temperature. The exponent ζ is 2.5 for electrons and 2.2 for holes.

For the carrier net recombination rate, only the contribution due to recombination via deep levels in the band gap is taken into account. This is described by the Shockley-Read-Hall (SRH) mechanism [Sho52], and the recombination rate is expressed by the formula

$$R^{SRH} = \frac{np - n_{i,\mathrm{eff}}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{4.9}$$

with

$$n_1 = n_{i,\mathrm{eff}} \exp\left(\frac{E_{\mathrm{trap}}}{k_B T}\right) \quad \text{and} \quad p_1 = n_{i,\mathrm{eff}} \exp\left(-\frac{E_{\mathrm{trap}}}{k_B T}\right) \tag{4.10}$$

where E_{trap} is the difference between the defect energy level and the intrinsic level. Since a precise measurement of the defect levels is not possible, a default value of $E_{\mathrm{trap}} = 0$ was assumed in the simulation, possibly overestimating the values of carrier lifetimes.

The minority carriers lifetime τ_{dop} is also dependent on the doping concentration according to the Scharfetter relation

$$\tau_{\mathrm{dop}}(N_i) = \tau_{\mathrm{max}} \left[1 + \left(\frac{N_i}{N_{\mathrm{ref}}}\right)\right]^{-1} \tag{4.11}$$

where τ_{max} and N_{ref} are reference values for the carrier lifetimes and for the concentration of ionized impurities, respectively[5]. The carrier lifetime dependence on the temperature is also taken into account by means of a power law model with exponent -3/2, so that the combined dependence on the doping concentration and on temperature is given by

$$\tau(T, N_i) = \tau_{\mathrm{dop}}(N_i) \left(\frac{T}{T_0}\right)^{-\frac{3}{2}}. \tag{4.12}$$

[4] The actual values used in the simulations for these parameters are omitted for simplicity; they can be found in [TCAD].

[5] $\tau_{\mathrm{max}} = 1 \cdot 10^{-5}$ and $3 \cdot 10^{-6}$ s for electrons and holes, respectively, and $N_{\mathrm{ref}} = 1 \cdot 10^{16}$ cm^{-3} [TCAD].

The electron and hole diffusion lengths L_e and L_h, which determine the average distance at which a minority carrier with a specific lifetime can be found from the point where it was generated, are related to the carrier lifetimes $\tau_{e,h}$ and mobilities $\mu_{e,h}$ through the equations

$$L_e = \sqrt{\frac{k_B T}{q} \mu_e \tau_e} \quad \text{and} \quad L_h = \sqrt{\frac{k_B T}{q} \mu_h \tau_h}. \tag{4.13}$$

Band gap parameterization

As mentioned above, the value of the band gap depends on the concentration of impurities and on the lattice temperature. The dependence on the doping concentration is modeled with the Slotboom empirical formula [Kla92]

$$\Delta E_g(N_{A,D}) = \Delta E_{g0} + E_{BGN} \left[\ln \frac{N_{A,D}}{N_{\mathrm{ref},\Delta E_g}} + \sqrt{\left(\ln \frac{N_{A,D}}{N_{\mathrm{ref},\Delta E_g}} \right)^2 + 0.5} \right] \tag{4.14}$$

where $\Delta E_{g0} = -4.795 \cdot 10^{-3}$ eV, $E_{BGN} = 6.92 \cdot 10^{-3}$ eV and $N_{\mathrm{ref},\Delta E_g} = 1.3 \cdot 10^{17}$ cm^{-3}, and $N_{A,D}$ is the donor or acceptor concentration for n-type and p-type material, respectively. The value of the energy band gap combining both doping and temperature dependence is calculated according to

$$E_g = E_{g0} + \Delta E_g(N_{A,D}) + \Delta E_g(T) \quad \text{with} \quad \Delta E_g(T) \approx -\frac{\alpha_{E_g} T^2}{\beta_{E_g} + T} \tag{4.15}$$

where $\alpha_{E_g} = 4.73 \cdot 10^{-4}$ eV/K and $\beta_{E_g} = 6.36 \cdot 10^2$ K [TCAD].

Charge generation model

The interaction of a charged particle with the detector is simulated by an excess charge distribution in the sensitive volume, which is specified at the beginning of a transient simulation according to a predefined ionization rate. The particle impact position is defined as a point on the detector surface, and the distribution of the generated charge density is specified along the particle track. The *alpha particle model* [TCAD] was used to describe the excess charge due to the passage of a single minimum ionizing particle. A uniform charge distribution with a characteristic value of 80 e-h pairs per μm of particle path was assumed. A Gaussian radial distribution was assumed, with a constant width along the particle track of $\sim$1 μm.

The simulation flow

The simulation of charge collection with the ISE-TCAD package proceeds via three fundamental steps:

- the detector geometry is described by means of boundaries inside which the desired mesh granularity and doping profiles are specified. The design of the simulated structure can be accomplished in 2D with the graphical interface provided by the MDRAW-ISE package, while for 3D structures it has to be coded by the user in specific files. This is the input for the MESH-ISE package which generates the grid and discretizes accordingly the doping information;

- the generated grid and the corresponding doping information constitute the input for the DESSIS-ISE package, a multidimensional mixed-mode device and circuit simulator for semiconductor devices, which incorporates the physical models and parameters and the numerical methods used in the simulation. The package can perform both static and transient simulations;

- the simulation results can be visualized and analysed by means of various packages, among which the INSPECT-ISE package is used for the analysis of two-dimensional curves and the PICASSO-ISE for three-dimensional visualization.

The GENESIS-ISE package provides a user-friendly graphical interface and environment to control the simulation flow, to specify the desired values for the simulation parameters and their variations, and for scheduling the simulation jobs.

4.2.2 Simulation of charge collection

Design of the simulated structure

In the following simulation, the approach described in [Dep01, Dep01b, DepTh] for the simulation of MAPS is followed. The simulated pixel structure was designed as a 3D model of a 3×3 pixel cluster. The collecting diode for every pixel is placed at the center of the pixel itself. The pixel pitch, the lateral size of the collecting diode and the epilayer thickness could be varied as parameters of the simulation.

Inside these boundaries, the doping profiles and the desired mesh granularity were specified. The doping profiles used in this work refer to an existing twin-tub CMOS 0.6 μm process [Dep02], but can be considered typical for modern, twin-tub bulk CMOS processes [DepTh]. Fig. 4.8 shows the doping profiles used in the simulated structure for an epilayer thickness of 15 μm. The black, continuous line represents the profile along the axis passing through the center of the collecting n-well/p-epi diode, while the red, dotted line refers to the profile along an axis passing through the complementary p-well. It can be seen that there are four orders of magnitude difference between the doping of the epitaxial layer ($\sim 1 \cdot 10^{15}$ cm^{-3}) and the doping of the low-resistivity substrate ($1 \cdot 10^{19}$ cm^{-3}), and two orders of magnitude between the doping of the epilayer and of the p-well (up to $1 \cdot 10^{17}$ cm^{-3}). As illustrated in Sect. 2.6.3 when introducing the principle of operation of MAPS, these doping differences create potential barriers at the boundaries of the epilayer, acting like mirrors for the charge generated by an impinging ionizing particle, which then diffuses in the epilayer until it is collected by the n-well, in which a high-doping n^{++} implant is present under the pixel electrode.

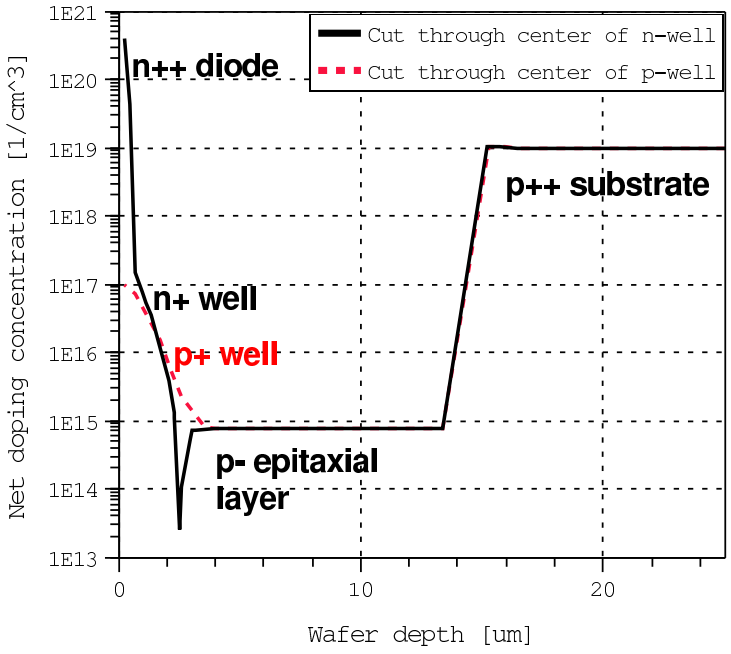

Figure 4.8: Doping profile of the simulated MAPS structure across the center of the collecting n-well/p-epi diode and across the center of the p-well.

A crucial parameter for the charge collection process is the carrier lifetime in the different parts of the detector. The carrier lifetime at a certain temperature depends on the doping concentration and on the material quality (e.g. bulk defects, traps): no assumptions were made about the latter in the simulations, and from the empirical Scharfetter relation 4.11, the electron lifetime can be estimated to be around 10 ns in the substrate, 10 μs in the epitaxial layer and between 1 and 10 μs in the p-well.

The detector substrate was simulated with a reduced thickness, typically a value of 10 μm, with respect to real ones, in order to reduce the number of grid points and therefore minimize the computing power needed for the simulations. This is justified by the fact that the high-doping substrate is expected to behave just as an ohmic contact, and that only the very first μm close to the epitaxial layer are expected to give a significant contribution to the collected charge. This is true since the transition region between the epilayer and the substrate has in reality a doping gradient not as sharp as the one depicted in Fig. 4.8, due to diffusion of dopant atoms into the epilayer during the growth process (see Sect. 2.4.2).

The mesh granularity was adjusted in different parts of the detector, especially in the regions with high gradients of doping concentration or carrier densities. A mesh size of $\sim$1 μm was used in the volume below the pixel hit by the particle track, i.e. the central pixel of the cluster, and was increased to 2-3 μm in the volume underneath the 8 neighboring pixels. A finer granularity down to $\sim$0.5 μm was used around the collecting diodes and along the path of the traversing

particle.

The size of the simulated structure, i.e. a 3×3 pixel cluster with pixel pitch of 20 μm, was mainly limited by the computing power of the workstation used for the simulations. In the real detector, charge carriers generated by the ionizing particle can diffuse far away from the interaction point and eventually be collected by pixels outside the 3×3 cluster or recombined in the detector volume. The boundaries of the simulated structure can be treated by DESSIS-ISE only with reflective (also called ideal Neumann) boundary conditions, which require the components of the electric field and of the diffusion current densities along the boundary surfaces to be equal to zero. The charge carriers who would reach the boundaries would then be reflected backwards and could lead to an overestimation of the collected charge. In order to simulate non-reflective boundary conditions, an additional region of silicon was added all around the cluster volume, and an artificially high recombination velocity was specified in a 1 μm thick belt surrounding its external boundary surfaces, as a way of removing the charge carriers which would eventually reach them.

Transient simulation of charge collection

The DESSIS-ISE package performs the simulations in the following steps:

- a static solution of the Poisson equation is calculated in order to obtain the distribution of the electrostatic potential and of the electric field inside the simulated structure;
- using this solution as a starting point, a static solution of the coupled Poisson and continuity equations is obtained;
- the real transient simulation is then started; the passing of a minimum ionizing particle through the detector structure is simulated and the relaxation process of the excess charge towards an equilibrium condition is followed in time; the current thus induced at the pixel electrodes is calculated and the collected charge is finally computed by integration.

During the transient simulation, only the solution of the electron continuity equation is updated, while the electrostatic potential distribution coming from the solution of the Poisson equation and the solution of the hole continuity equation are kept equal to the starting ones. This is motivated on one side by the fact that the amount of excess charge introduced in the detector is negligible compared to the concentration of ionized impurities, on the other side by the fact that holes do not contribute to the charge collection process.

Simulation results

Figure 4.9 shows an example of the calculated electrostatic field and potential in the simulated structure. The plots refer to a two-dimensional cut plane perpendicular to the detector surface and passing through the centers of the 3 pixels in a row. It can be seen that the electric field is close to zero in the whole detector volume, apart from the vicinity of the collecting diodes, in which a high gradient of doping concentration is present. Correspondingly, the electrostatic

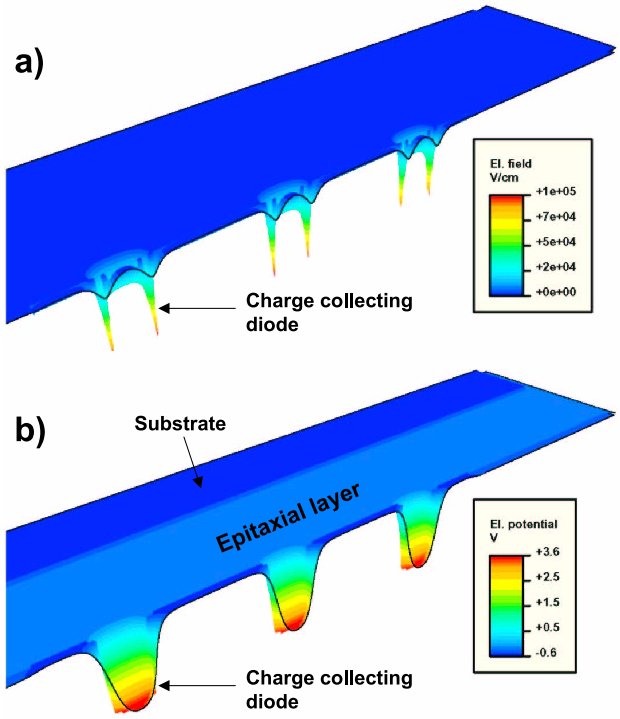

Figure 4.9: Two dimensional cut of the (a) electric field and (b) electrostatic potential in the simulated MAPS structure.

potential is constant in the substrate and in the epilayer, while potential wells for the collection of electrons are formed around the diodes. The detector volume is depleted only in a shallow region around the diodes whose extension can be calculated from Eq. 2.15, to be of about 2 μm for the typical applied reverse bias of 3 V and an epitaxial layer doping of $\sim 1 \cdot 10^{15}$ cm^{-3}. The potential barriers at the boundaries between the epitaxial layer and the substrate, and between the epilayer and the p-wells can be estimated from the

$$V_{\mathrm{bar,sub}} = \frac{k_B T}{q} \ln\left(\frac{N_{A,\mathrm{sub}}}{N_{A,\mathrm{epi}}}\right) \quad \text{and} \quad V_{\mathrm{bar,p-well}} = \frac{k_B T}{q} \ln\left(\frac{N_{A,\mathrm{p-well}}}{N_{A,\mathrm{epi}}}\right) \tag{4.16}$$

to be of 245 mV and 125 mV, respectively, using the doping profiles of Fig. 4.8. Both barriers are several times higher than the thermal potential $k_B T/q \approx 26$ mV at 300 K, justifying the assumption that they act as perfect mirrors for the electrons.

The passage of a minimum ionizing particle through the detector generates an excess of minority charge carriers (electrons). The electrons generated in the substrate undergo a much faster recombination than in the epilayer. This can be seen in Fig. 4.10, which shows an example 3-dimensional representation of the electron concentration on a plane cut across the simulated structure, as calculated 10 ns after the passage of the minimum ionizing particle through the

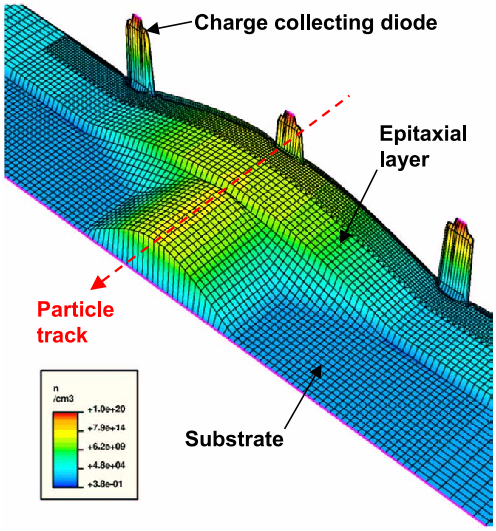

Figure 4.10: Electron concentration in the simulated MAPS structure (cut plane across the center of the pixel cluster) after the passage of a mip and 10 ns of transient simulation.

central pixel of the cluster. The charge spreading is larger in the epitaxial layer than in the substrate, where the electrons have a smaller mobility and are rapidly recombined due to the much higher doping. These electrons are mostly lost for the charge collection process. Nevertheless, the electrons generated in the field-free epitaxial layer can diffuse until they approach the electric field around the n-well/p-epi diodes and are collected by the junction capacitance. The collected charge is in general distributed between more than one diode (i.e. pixel), forming a signal cluster of several pixels, whose width depends on the pixel size and on the epitaxial layer thickness.

The charge collected in every pixel is calculated at the end of the transient simulation by integrating the current flowing through the electrode contacts. In Fig. 4.11 we report the results of the transient simulation performed on a structure with pixel pitch of 20 μm, a fixed diode size of 3×3 μm^2, and 3 different thicknesses of 5, 10 and 15 μm for the epitaxial layer. The minimum ionizing particle is always passing through the center of the central pixel (i.e. the hit pixel) and perpendicular to the detector surface[6]. The plots report the current pulse (left scale) and the collected charge (right scale) in the hit pixel, the charge of the 2×2 pixel cluster exhibiting the highest signal, and the total charge collected in the 9 pixels of the complete cluster.

As expected, the total collected charge increases by increasing the epilayer thickness, i.e. the thickness of the sensitive volume. A total signal of 850 electrons can be expected from a 15 μm epilayer, decreasing to about 640 electrons and 380 electrons for a 10 and 5 μm epilayer,

[6]The case here considered of central hits is an "ideal" one, since in reality the charge collected in the hit pixel will depend strongly on the hit position within the pixel itself. The simulation results presented here are intended as an illustration of the detector charge collection mechanism and as a rough estimation of the expected signals. A detailed simulation of the charge collection dependence on the hit position can be found in [DepTh].

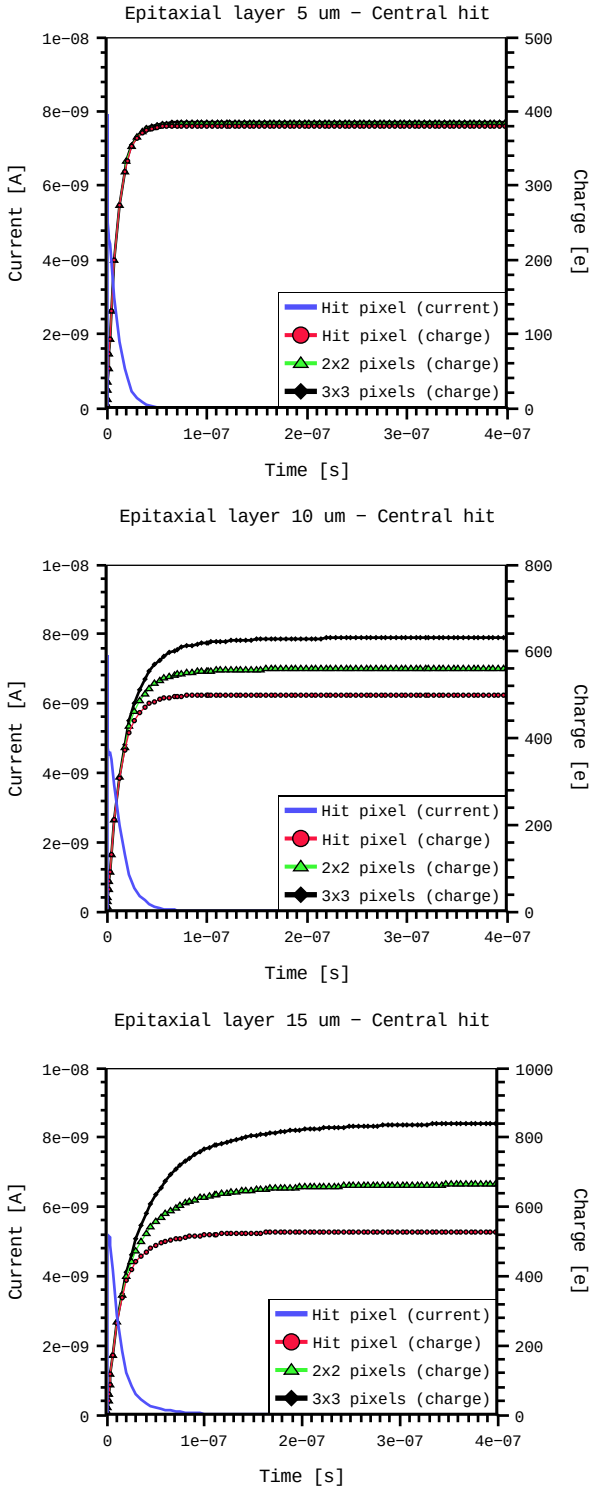

Figure 4.11: Simulation of charge collection in MAPS for 20 μm pixel pitch and for 5, 10 and 15 μm thin epitaxial layer, for a minimum ionizing particle passing through the center of the hit pixel. The size of the collecting diode in each pixel is of 3×3 μm^2.

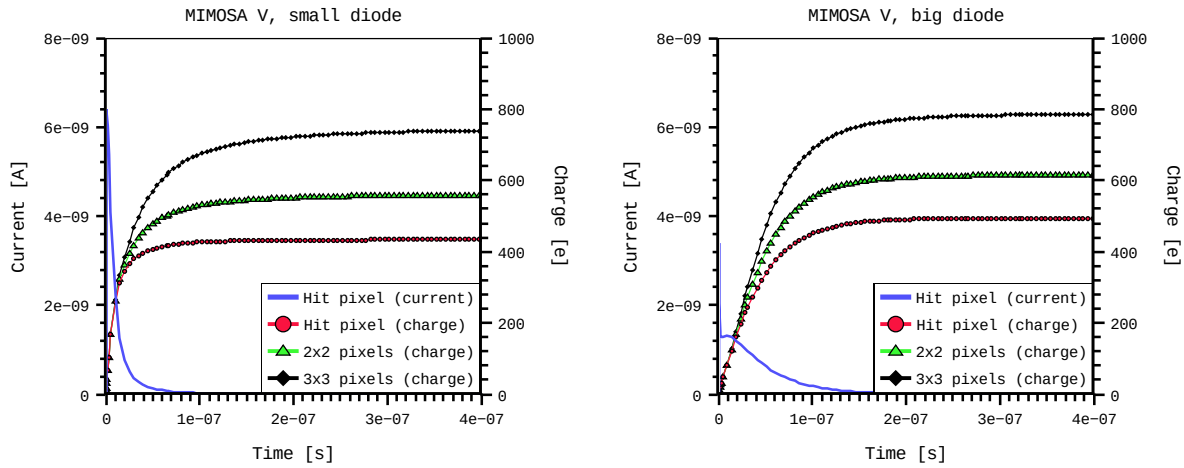

Figure 4.12: Simulation of charge collection using MIMOSA-5 technological parameters: pixel pitch 17 μm, epitaxial layer thickness 14 μm. The left plot refers to the "small" diode option, in which the area of the charge collecting diode in each pixel is of 3.1×3.1 μm^2, the right plot to the "big" diode option with a 4.9×4.9 μm^2 charge collecting diode.

respectively. Nevertheless, the charge spread among neighboring pixels also increases with the epilayer thickness. In the considered case of central hits, the charge collected in the hit pixel is almost 95% of the total charge for the 5 μm epilayer, while the ratio decreases to 80% and 60% for the 10 and 15 μm cases, respectively.

The charge collection time t_c can be estimated from the saturation of the curve representing the total cluster charge. It was here calculated as the time after which 90% of the total charge is collected. The total charge is estimated from the charge collected after 400 ns, which is considered a long enough time interval for the charge collection process to finish [DepTh]. Charge collection is faster for a thinner epilayer: t_c ∼20 ns for 5 μm and increases to about 70 and 100 ns for 10 and 15 μm epilayer, respectively.

In the next chapter, the test of the MIMOSA[7]-5 prototype chip will be presented. The detector is manufactured in a 0.6 μm CMOS technology from AMS, with a 14 μm thin epitaxial layer and a pixel pitch of 17×17 μm^2. The size of the charge collecting diode in each pixel can be either of 3.1×3.1 μm^2, in the so-called "small" diode option, or of 4.9×4.9 μm^2, in the "big" diode option. The simulation of a 3×3 pixel cluster with such parameters, using the same doping profiles as in Fig. 4.8, is presented in Fig. 4.12 for the two different diode sizes. A larger collected signal is associated with a larger area of the charge collecting diode, as expected from the correspondingly larger capacitance of the collecting node. A total cluster signal of 740 and 786 electrons is collected for the small and big diode case, respectively, in both cases with a collection time of ∼100 ns. The smaller signals compared to the 15 μm epilayer case presented in Fig. 4.11 is due to the (slightly) reduced epilayer thickness and to the smaller pixel pitch. The fraction of the total charge collected in the hit pixel is of 59% and 63% for small and big diodes,

[7]**MIMOSA** stands for **M**inimum **I**onizing particle **MOS** **A**ctive pixel sensor.

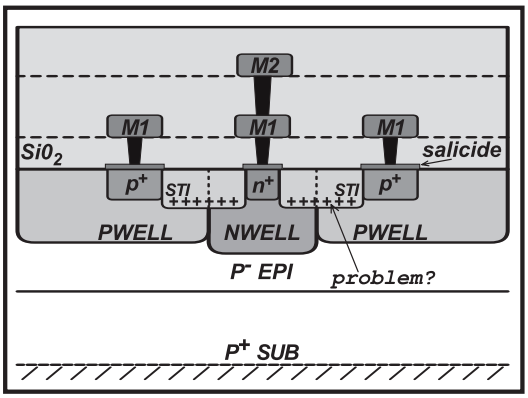

Figure 4.13: Configuration of the n-well/p-epi collecting diode with p-type guard-ring implemented in a deep-submicron fabrication process with Shallow Trench Isolation (STI), from [DepTh].

respectively, indicating a slightly larger charge sharing in the former case. These results will be compared with experimental results from beam-tests of the MIMOSA-5 chip in Sect. 5.5.3.

4.2.3 Simulation of MAPS in deep-submicron technology

A possible drawback in the use of MAPS for particle detectors is the dependence on the fabrication technologies. The technology roadmap in the VLSI industry proceeds at a steady pace, and the availability of a specific fabrication process cannot always be guaranteed over a long period of time. The iteration of detector prototypes has then to follow in time the evolution of commercial CMOS processes, whose trend is the scaling down of the minimum featuring size, towards the so-called *deep-submicron* (<0.25 μm) processes.

The main consequence of the use of a deep-submicron technology in the sensor fabrication is the reduction of the epilayer thickness, which is the key parameter in the performance of a MAPS detector, being the actual sensitive volume. With a thinner epilayer the expected charge signals decrease (Sect. 4.2.2), and the contribution to the collected charge coming from the substrate becomes more important, as already shown by simulations performed on this issue in [Man02].

Beside this, a typical feature of deep-submicron technologies is the presence of isolation structures like STI (Shallow Trench Isolation) or LOCOS (LOCal Oxidation of Silicon) around the implantations. In the case of MAPS, the configuration of the n-well/p-epi collecting diode with STI is shown in Fig. 4.13. These structures, and in particular their interfaces with the silicon bulk of the sensor, may play an important role as regards the sensor radiation hardness [Cla02] because of the build-up of radiation-induced interface states which can act as traps for the moving charge, resulting in a reduction of the charge collection efficiency, and as generation-recombination centers leading to an increase of the leakage current.

In this section we will present ISE-TCAD simulations of MAPS fabricated in deep-submicron technology. Besides the study on how the reduction of the epilayer thickness influences the charge

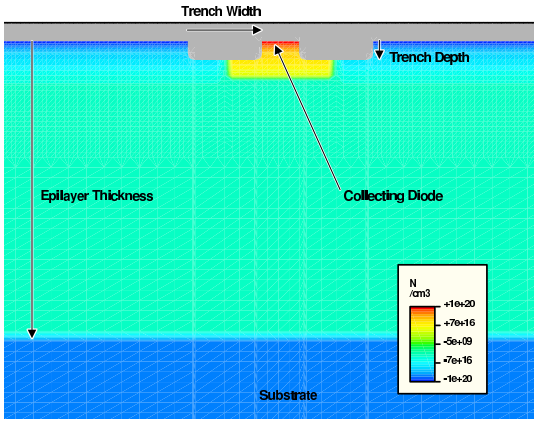

Figure 4.14: Simulated pixel structure for deep-submicron MAPS.

signal, an estimation of how radiation-induced interface states can influence the detector charge collection efficiency will be presented.

Design of the simulated structure

The simulations were performed in 2D, due to the complexity of the design in 3 dimensions of the isolation structures surrounding the collecting diodes. The trenches, in fact, had to be designed with a smooth profile, resembling the shape of real structures, in order to avoid the presence of a high electric field at the corners. Epilayer thickness, trench width and trench depth were varied as parameters of the simulations, while the pixel pitch was fixed to 20 μm and the collecting diode lateral size to 3 μm. The substrate thickness was fixed to 50 μm.

For the doping profiles, typical values resembling the ones of commercially available 0.25 μm processes were used [Man02], i.e. $1{\cdot}10^{19}$ cm^{-3} for the highly-doped substrate and for the n^+- and p^+-wells, $5{\cdot}10^{15}$ cm^{-3} for the p-type epitaxial layer and $1{\cdot}10^{20}$ cm^{-3} for the n^{++} implants of the collecting diodes. The simulated structure is displayed in Fig. 4.14. Of course, the values of the geometrical parameters and of the doping profiles represent an approximation of the real ones, since such information is usually not disclosed by manufacturers.

The radiation-induced damage at the interfaces between oxide and silicon has been simulated by the introduction of interface trap concentrations of 10^{11} and 10^{12} eV^{-1}cm^{-2}, the latter being roughly equivalent to a total ionizing dose of $\sim$5 kGy, according to a parameterization in [Wue01]. The DESSIS-ISE package allows to specify the traps type (donor, acceptor or neutral), their energy level in the silicon band gap, their concentration and their capture cross sections for electrons and hole. The Poisson equation is modified accordingly in order to take into account the variation of the charge due to trapping [TCAD]. The most common model for the charge nature of interface traps postulates that traps are acceptors in the upper part of the band gap and donors in the lower part of the band gap. Moreover, the typical distribution of the interface

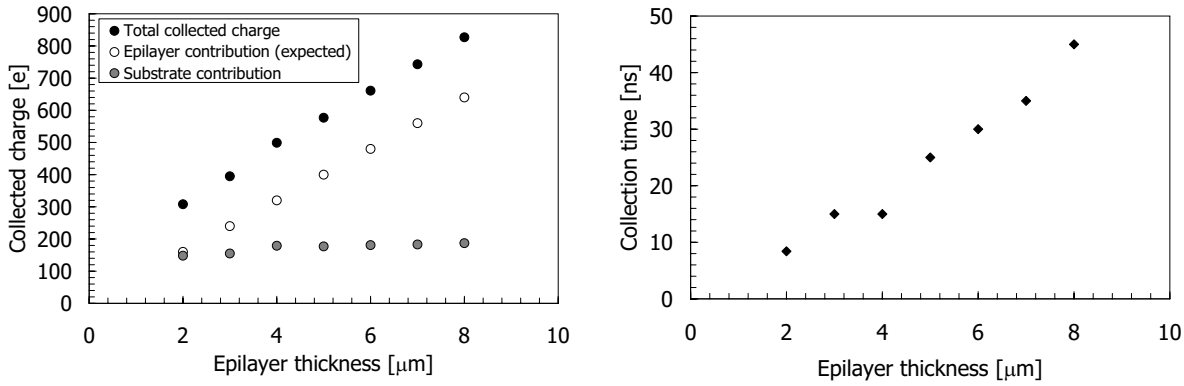

Figure 4.15: Total collected charge as a function of the epilayer thickness for deep-submicron MAPS (left), and corresponding charge collection times (right).

trap density across the silicon band gap has a minimum for energy levels close to the midgap, and then monotonically increases towards both band edges up to density values a couple of orders of magnitude higher than in the center [MaD89]. In the following simulation two discrete levels were used to approximate this situation: an acceptor level close to the conduction band, with typical capture cross-sections for electron and holes of 10^{-14} and 10^{-12} cm^2, respectively, and a donor level close to the valence band with capture cross-sections of 10^{-12} and 10^{-13} cm^2 for electrons and holes, respectively.

Simulation results

The simulated total charge in a 3-pixel cluster, in the case of central hits, as a function of the epilayer thickness is shown in the left part of Fig. 4.15, while the corresponding collection times are shown in the right part of the same figure. The epilayer thickness was varied between 2 and 8 μm, in steps of 1 μm.

An increasing, almost linear dependence of the collected charge as a function of the increasing epilayer thickness can be observed (the charge is anyway expected to saturate for large epilayer thicknesses [DepTh]). The signal amounts to only ∼300 electrons for the thinnest epilayer, and then increases up to ∼850 electrons for an 8 μm epilayer. Clearly, a thicker epilayer is more favorable in terms of signal and therefore signal-to-noise ratio. On the other side, a thinner epilayer results in shorter collection times and therefore in a faster collection: the charge collection time is of ∼10 ns for a 2 μm thin epilayer and increases up to ∼45 ns for an 8 μm one.

The substrate contribution to the total charge, also shown in the left part of Fig. 4.15, can be estimated from the difference between the simulated total charge and the charge expected from the thickness of the epilayer and the most probable value of charge deposited by the minimum ionizing particle per unit of length (80 e/μm). It can be seen that the substrate contribution is almost constant as a function of the epilayer thickness, and constitutes a significant relative

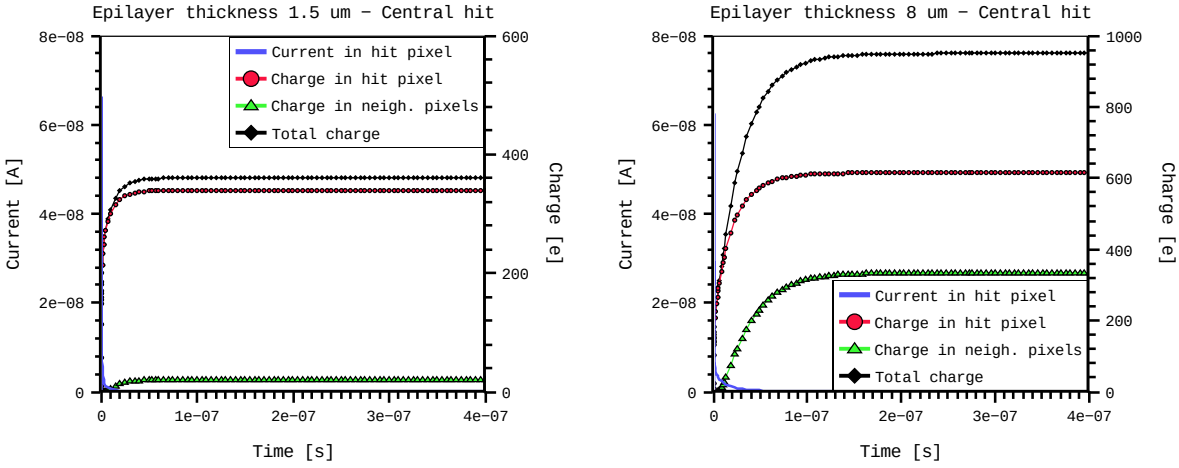

Figure 4.16: Transient simulation of charge collection in deep-submicron MAPS with 1.5 μm (left) and 8 μm (right) epilayer, for a pixel pitch of 20 μm.

part of the total charge, especially for thin epilayers (up to ∼50 % for a 2 μm thin epilayer). Its magnitude between 150 and 180 electrons can be related to the charge generated in the first ∼2 μm of the substrate.

Two-dimensional simulations of charge collection in deep-submicron MAPS have been addressed also in [Man02], by using technological parameters from two commercially available CMOS processes using 1.5 and 8 μm epilayers, with doping profiles very similar to the ones used here. The two epilayer thicknesses can be considered as extremes of the ones available by common deep-submicron processes. The corresponding results of transient simulations analogue to the ones performed in Sect. 4.2.2 are shown in Fig. 4.16. The different impact of the two thicknesses on the charge spreading between neighboring pixels, i.e. on the cluster size, is evident: while in the 1.5 μm epilayer case almost all the charge is collected by the central pixel, in the 8 μm case about 65% of the total charge is collected in the central pixel, and the remaining 35% in the two adjacent pixels. A thinner epilayer gives a very limited charge spreading, but at the price of a poorer signal; a thicker epilayer provides a larger signal, but with an increased charge spreading.

The detector charge collection efficiency (CCE) has been simulated for different values of the epilayer thickness also as a function of the radiation-induced interface trap concentration, as described above, in order to study the possible impact of shallow trench isolations on the device radiation tolerance. The CCE is here defined as the ratio between the total charge collected in the 3-pixel cluster after the introduction of interface traps and before, and is therefore fixed to 1 when the traps are excluded from the simulation. The results are shown in Fig. 4.17 for epilayer thicknesses of 2, 5 and 8 μm and for two difference trench depths (see Fig. 4.14) of 0.2 and 0.5 μm, while the trench lateral width is fixed to 2 μm.

While the collection times (not shown) were found not to be affected, a significant impact

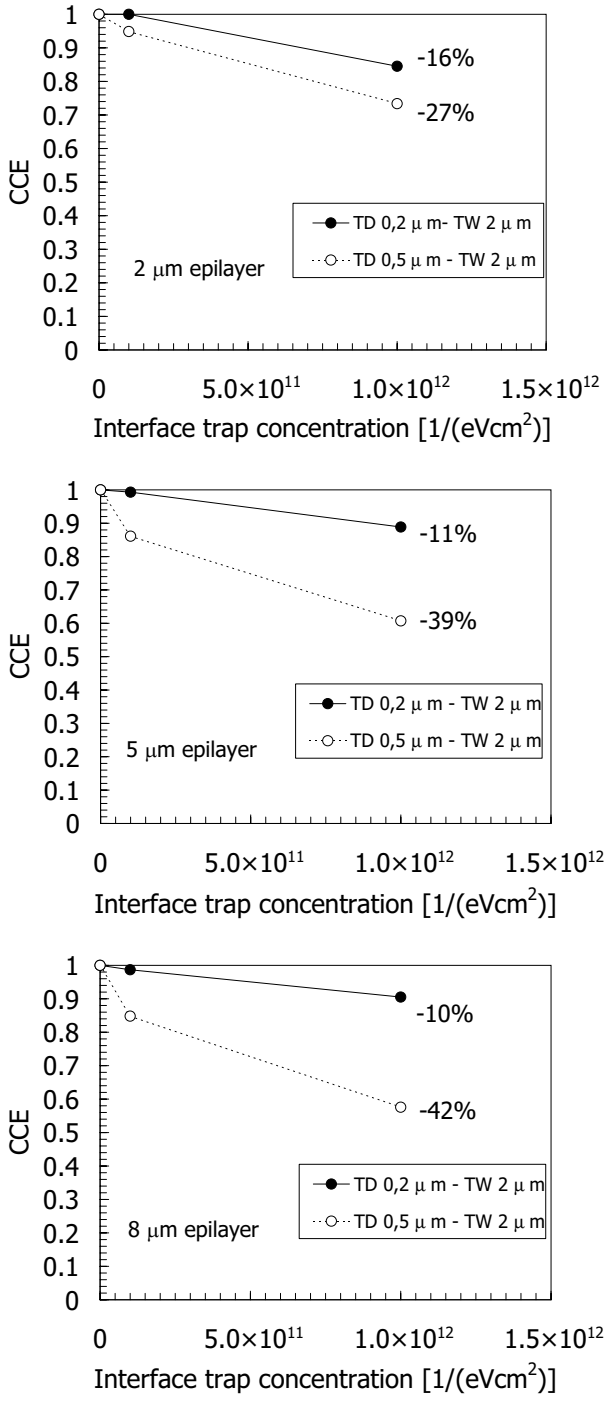

Figure 4.17: Simulated charge collection efficiency in deep-submicron MAPS as a function of the interface trap concentration for 2, 5 and 8 μm thin epitaxial layer, and for two different trench depths.

of the interface damage on the CCE can be observed, pointing at the potential danger of the isolation structures: a significant decrease of up to ∼40% is observed at the highest trap concentration considered, corresponding to ∼5 kGy of ionizing dose; the charge loss strongly depends on the geometry of the trench, especially on its depth, with respect to the n-well implant depth (here of 1 μm). No significant differences are observed between the 5 and 8 μm epilayer cases, the effect seeming more moderate for the thinnest epitaxial layer of 2 μm considered.

4.3 Summary of simulations

In the first part of this chapter (Sect. 4.1) a general simulation of the charge collection in irradiated silicon pixel detectors has been presented. The focus has been on reverse-biased silicon detectors, and on the impact of trapping of the drifting charge on their charge collection properties.

There is a difference in charge collection between irradiated detectors using p^+ or n^+ electrodes. The detectors using n^+ (p^+) electrodes exhibit larger (smaller) induced charge in the hit electrode when compared to a pad detector of the same thickness. Significant charge signals can be induced also in the neighboring electrodes, of the same sign as in the hit pixel in the case of a $p^+ - n$ detector, of the opposite sign in the case of a $n^+ - n$ detector. One can therefore expect wider clusters in a $p^+ - n$ detector, and a higher signal in the hit pixel of a $n^+ - n$ detector.

Thin pixel detectors are considered a viable option for use at the SuperLHC, where they will have to stand a very harsh radiation environment, up to equivalent fluences of $\sim 10^{16}$ cm^{-2}. Indeed, the reduced thickness translates into smaller leakage current and depletion voltage, besides being advantageous in terms of material budget. The signal from pixel detectors of different thicknesses $\leq$100 μm has been simulated as a function of the irradiation fluence: at most ∼2000 electrons can be expected from a 100 μm thick detector with n^+ readout at Φ_{eq}=10^{16} cm^{-2}, the signal decreasing with the detector thickness. Such signals can still be large enough for the sensor successful operation, if low-noise readout electronics can be provided. The charge induced on the neighboring pixels depends on the detector geometry, especially on the ratio between the size of the collecting electrode and the detector thickness, and can be significant especially for $n^+ - n$ detectors.

In the second part of the chapter, Sect. 4.2 has described a set of technology CAD simulations of the charge collection properties of Monolithic Active Pixel Sensors (MAPS) as a function of their design parameters, especially the thickness of the sensitive volume (the low-resistivity epitaxial layer), with particular reference to the typical parameters of commercially available deep-submicron CMOS technologies. The latter can introduce shallow trench isolation (STI) around the doping wells forming the charge collecting elements, and may possibly lead to a performance degradation due to radiation-induced damage at the silicon/oxide interfaces.

The results obtained from the performed simulations can be summarized as:

- a signal of ∼900 electrons can be collected in a 9-pixel cluster with a pixel pitch of 20 μm and a 15 μm thick epitaxial layer;

- an epilayer thickness of a few μm only results in a poor signal, but also in a limited charge spreading and in short collection times, i.e. in a faster charge collection process;
- a thicker epilayer results in a larger signal and in a larger charge spreading over neighboring pixels, i.e. in a larger cluster size. The use of a thicker epilayer is thus favorable in terms of signal-to-noise ratio, and the increase of the cluster size can be advantageous for tracking applications in the improvement of the position resolution by means of special position finding algorithms (e.g. center of gravity). The charge collection in a thicker epilayer is slower but still at an acceptable level;
- by decreasing the epilayer thickness, the relative contribution to the total collected charge coming from the highly-doped substrate increases. When the epilayer thickness is small, the highest substrate contribution is observed for the central pixel of the cluster, since the fast recombination in the substrate limits the charge spreading;
- in the presence of isolation structures (shallow trenches) around the collecting elements, radiation-induced shallow trapping states at the silicon/oxide interfaces lead to a significant decrease of the charge collection efficiency after an ionizing dose of a few kGy. The degradation is dependent on the geometry of the isolation structures, mainly on the depth.

In conclusion, the choice of a fabrication process for MAPS sensors should be driven by a thickness of the epitaxial layer which is large enough to provide a reasonable signal for a good signal-to-noise performance, but not too large in order to keep the charge spreading over neighboring pixels at a moderate level. The possible impact on the sensor radiation tolerance of technological features like additional isolation structures close to the charge collecting elements should be also taken into account.

Chapter 5

Test of Monolithic Active Pixel Sensors

The principle of operation of Monolithic Active Pixel Sensors (MAPS) has been introduced in Sect. 2.6.3. Since 1999, the design, fabrication and test of a series of prototypes has been pioneered by the IReS/LEPSI institutes in Strasbourg (France), exploring different design options for the sensing element and for the readout architecture, and using several manufacturing processes. Due to their features and promising performances, MAPS sensors are currently being developed as a candidate technology for the vertex detector of the future International Linear Collider (ILC). In this framework, a working group at DESY and Hamburg University is active in detector simulation and tests, physics studies, and mechanics and cooling engineering issues.

In this work, an experimental setup has been built in order to test one real-size prototype chip (area of $\sim$ cm^2) both with radioactive sources and with an electron beam at DESY. This chapter will start with a review of the fabricated prototypes and of their performance (Sect. 5.1), followed by the description of the experimental setup in Sect. 5.2. The data analysis procedure will be described in Sect. 5.3. Experimental results will then be presented both from tests with low-energy X-rays (Sect. 5.4) and from a series of beam-tests with the 6 GeV electron beam of the DESY-II synchrotron (Sect. 5.5). The emphasis will be on the experimental results achieved regarding the detector charge collection properties, signal-to-noise ratio and detection efficiency. Finally, Sect. 5.6 will present the preliminary results obtained after irradiation of one prototype chip with low-energy ($\sim$10 MeV) electrons.

5.1 The MIMOSA[1] prototypes

5.1.1 Features and performances of MIMOSA prototypes

The main features of the MIMOSA prototypes fabricated so far by IReS/LEPSI are summarized in Table 5.1, which reports the used manufacturing process, the two main design parameters,

[1] **MIMOSA** stands for **M**inimum **I**onizing particle **MOS A**ctive pixel sensor.

Prototype	Year	Manufacturing process [μm]	Epilayer thickness [μm]	Pixel pitch [μm]	Chip configuration (arrays/pixels)	Important features
MIMOSA-1	1999	AMS 0.6	14	20	4/64×64	Thick epitaxy
MIMOSA-2	2000	MIETEC 0.35	4.2	20	6/64×64	Thin epitaxy, rad-hard layout
MIMOSA-3	2001	IBM 0.25	2	8	2/128×128	Deep-submicron technology
MIMOSA-4	2001	AMS 0.35	none	20	4/64×64	No epitaxial layer (low-doping substrate)
MIMOSA-5	2001/03	AMS 0.6	14	17	4/510×512	Reticle-size prototype, 1M pixels
MIMOSA-6	2002	MIETEC 0.35	4.2	28	1/30×128	CP r.o., on-pixel CDS, integrated discrimination
MIMOSA-7	2003	AMS 0.35	none	25	1/16×64	CP r.o., on-pixel CDS, photoFET
MIMOSA-8	2003	TSMC 0.25	8	25	1/32×128	CP r.o., on-pixel CDS, integrated discrimination
MIMOSA-9	2004	AMS 0.35	20	20, 30,40	1/64×64 3/32×32	Opto technology, different pixel pitch
MIMOSA-10	2004	TSMC 0.25	8	30	2/64×128	CP r.o, prototype for STAR VXD upgrade
MIMOSA-11	2005	AMS 0.35	20	30	4/42×42	Radiation hardness test structures

Table 5.1: History of MIMOSA prototypes fabricated from 1999 to 2005. The different readout architectures are discussed in the text.

i.e. the thickness of the epitaxial layer and the pixel pitch, the number of arrays present in each chip and the corresponding arrangement of columns and rows. In the last column, important features of each prototype are presented.

The first four prototypes were focused on the technology demonstration and on the exploration of different manufacturing processes. MIMOSA-1 and 2 were fabricated in two different processes featuring correspondingly two different epilayer thicknesses, a "thick" option of 14 μm and a "thin" option of 4.2 μm, respectively. Moreover, rules for radiation tolerant layout design of the electronics were used in MIMOSA-2, which could be used as a test-bench for radiation hardness studies [Dev03]. The MIMOSA-3 prototype was the first attempt at the use of a deep-submicron fabrication technology, which allowed the design of a large number of small pitch pixels in a small area, but featured also a very thin epilayer thickness, resulting in a small signal. The MIMOSA-4 prototype was manufactured with a technology without epilayer, using a low-doping substrate[2], a common trend in several present-day CMOS processes. After the first series of small-scale prototypes (area of a few mm^2), the MIMOSA-5 chip was intended as a test of the reproducibility of the performances of the first, small scale prototypes in a large,

[2]Typical epitaxial layer doping levels for common CMOS processes are in the order of $\sim 10^{15}$ cm^{-3}. In the case of the MIMOSA IV prototype, "low-doping" means a concentration of $\sim 10^{14}$ cm^{-3}.

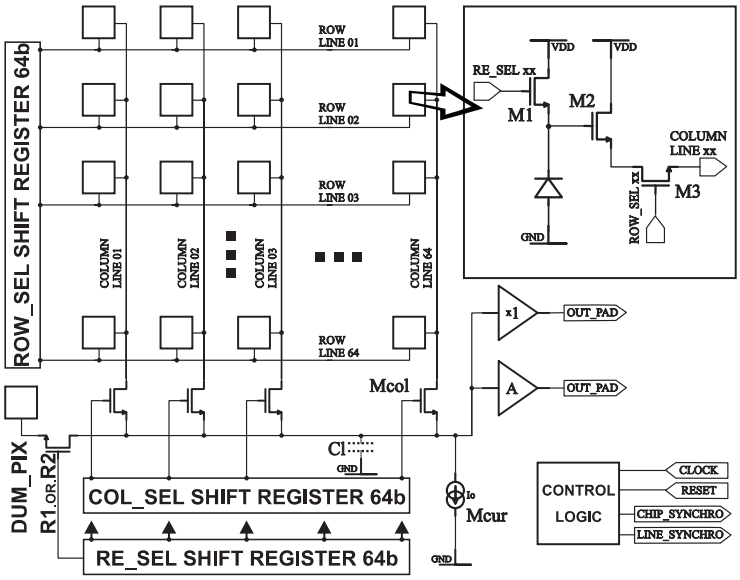

Figure 5.1: Schematic readout architecture of the MIMOSA-1 prototype (from [DepTh]).

reticle-size prototype of a surface of several cm^2.

Apart from the just mentioned MIMOSA-5 case, with which we will deal in detail in the following sections, the first prototypes were built with a moderate number of active elements arranged in small arrays. In its simplest form, a schematic diagram of the architecture of such an array can be seen in Fig. 5.1. The chip is equipped with a serial analog readout, requiring, apart from a few biasing lines, only two digital signals to operate, the *CLOCK* signal which is used to address pixels for readout and for selecting the columns to restore the reverse bias on the charge-sensing node during the reset phase, initiated by the *RESET* signal (a positive voltage pulse applied to the gate of the M1 transistor). Analog power supplies, bias signals and analog outputs are separated for the sub-arrays of each chip, and the corresponding lines are routed independently. The digital parts used for control and addressing are also independent for each array, but are powered from common digital power supplies and driven from the common control lines *CLOCK* and *RESET*.

The reset phase is needed in order to remove the charge collected by the charge collecting node capacitance and to avoid saturation of the diode leakage current, and therefore to prepare the node for the following readout cycle. This introduces in the pixel signal a kTC reset noise, which can nevertheless be effectively removed by means of the Correlated Double Sampling (CDS) technique [Hyn92], which also reduces the influence of low-frequency (i.e. $1/f$) noise and of the noise components deriving from non-uniformities in the array, the so-called Fixed Pattern Noise. As displayed in Fig. 5.2 and 5.3, the useful signal is obtained from the difference of two consecutive frames taken after the reset. The charge integration time is thus equal to

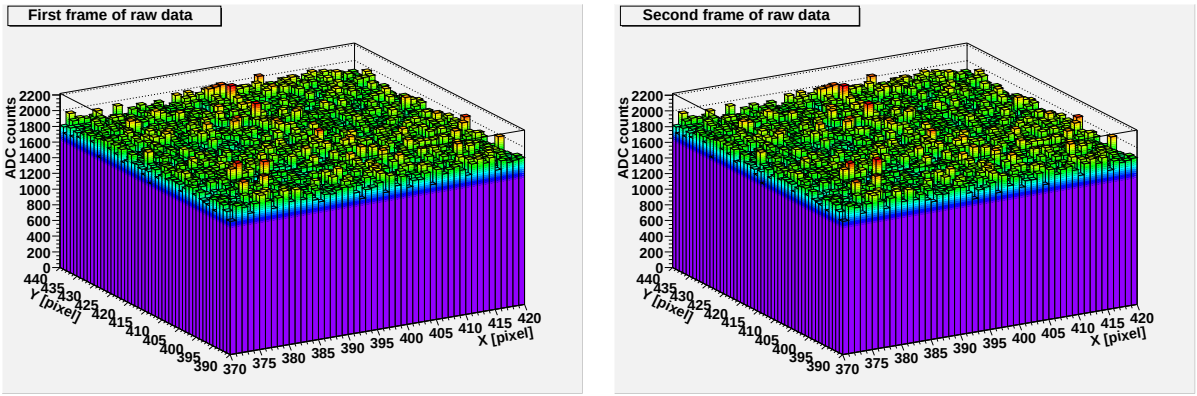

Figure 5.2: Example of raw data for two readout frames before Correlated Double Sampling (CDS). The plots refer to a subset of pixels of one matrix of a MIMOSA-5 prototype, exposed to a 6 GeV electron beam (see Sect. 5.1.2 and following).

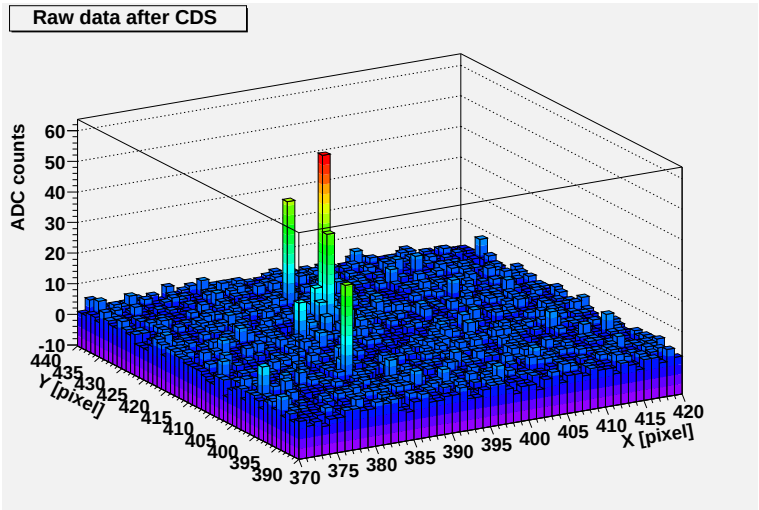

Figure 5.3: Example of raw data after Correlated Double Sampling (CDS). The image is the result of the subtraction of the two images in Fig. 5.2.

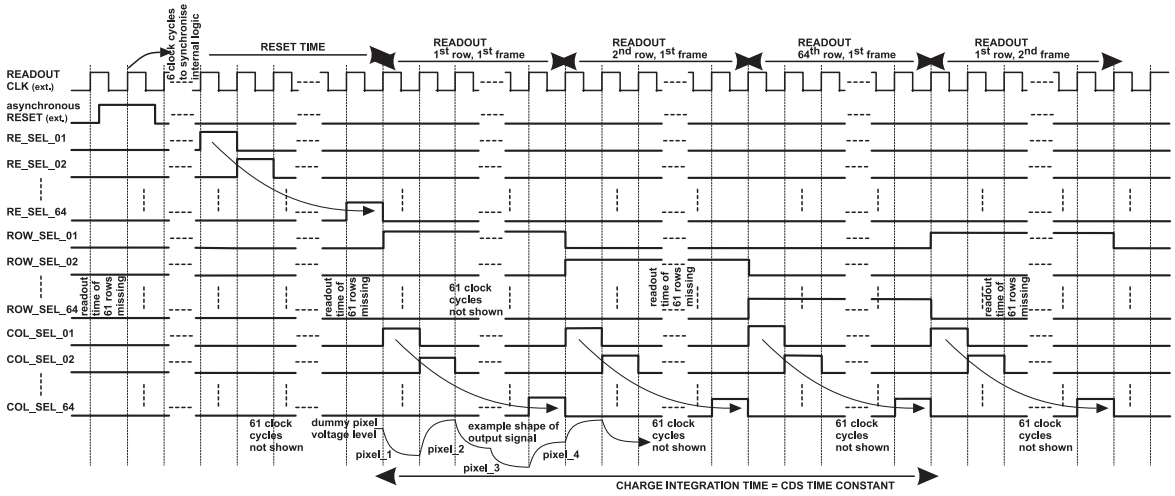

Figure 5.4: Timing diagram of MIMOSA-1 operation (from [DepTh]).

the readout time of one full frame, determined by the ratio between the number of pixels N_{pix} connected to the same serial output line and the readout clock frequency f_{clk}:

$$\tau_{\text{int}} = \frac{N_{\text{pix}}}{f_{\text{clk}}}. \tag{5.1}$$

The sequential pixel addressing during readout is done selecting rows and columns by means of two shift registers, whose lengths in bits depend on the number of pixels per row and per column (64 for both in the case of the MIMOSA-1 architecture displayed in Fig. 5.1). A further shift register is used for selecting rows (or columns) for reset. The length of the reset pulse varies according to the considered prototype, and has typically a length of one clock cycle or more. After the reset phase, consecutively addressed pixels are multiplexed onto the common output line. The sequential addressing of pixels for readout yields a charge integration time which is equal to the time needed for one full readout cycle of all pixels in the array, i.e. the *frame* readout time. An example timing diagram for the MIMOSA-1 chip is shown is Fig. 5.4.

In the case of the simple MIMOSA-1 architecture, every pixel is directly connected to the single readout-line. This nevertheless represents a limitation in the maximum readout speed achievable, in practice up to 10 MHz, since the voltage of each readout line has to settle at the level imposed by the source follower transistor currently driving the line [DepTh]. In the following prototypes, also featuring serial analog readout, several modifications were introduced in the readout architecture, including the re-arrangement of the reset operation from column-wise to row-wise and above all the use of more readout lines switched alternatively via a multiplexer to the output buffer, e.g. in the case of two readout lines, odd columns are linked to the first readout line and even columns to the second readout line. This approach, together with

an optimized design of the output operational amplifier[3] results in maximum achievable clock frequencies up to a few tens of MHz, without affecting the number of clock cycles required to perform the readout of one full frame, since the sequential addressing of pixels during readout is preserved.

After the first five prototypes, the focus of the technology development was directed towards the optimization of the readout architecture and on the integration of on-chip functionalities: the prototypes MIMOSA-6, 7 and 8 feature a column-parallel readout architecture, with the CDS operation performed on pixel (by means of the inclusion of capacitors and switches inside the pixels in order to store the two necessary signals), and a discriminator at the end of each column. The readout options explored with these prototypes will be reconsidered in Sect. 6.2, due to their importance in the development of a CMOS-based vertex detector suited for the International Linear Collider (ILC). In addition, MIMOSA-7 features a novel charge-sensing element, i.e. the photoFET, aiming at an increased sensitivity of the pixel response to the charge generated inside the detector active volume [Dep03].

The MIMOSA-9 prototype was fabricated in an Opto technology introduced by AMS in 2004, optimized for CMOS imaging applications. This process represents probably the current best choice for the fabrication of CMOS monolithic pixels, since it features a 20 μm thick epilayer and a good, controlled quality of the surfaces, i.e. a low surface leakage current (<45 pA/mm^2), besides a convenient number of metal layers (4), needed for the integration of the pixel circuitry. An important feature of this prototype is the presence of different pixel pitches in the different sub-arrays. The MIMOSA-11 prototype has been recently fabricated on the basis of MIMOSA-9, but with a modified layout of the charge collecting diode with minimum field oxide around the junction, in order to aim at a higher radiation tolerance. In-between, the MIMOSA-10 prototype had been fabricated in 2004 as the first prototype chip designed in view of the application of MAPS in the upgrade of the vertex detector of the STAR experiment at RHIC [Wie01].

The tracking capabilities of several prototypes (MIMOSA-1, 2, 4, 5 and 9) have been extensively tested by the IReS/LEPSI group with high-energy (∼100-120 GeV/c) pion beams at CERN and most recently with ∼6 GeV electrons at DESY (for the prototypes MIMOSA-5, 8, 9 and 11), with the help of a high precision (∼1 μm) silicon reference telescope. Experimental results have been presented in several publications [4] and are reviewed in [Win03, Win05]. The main achievements can be summarized as:

- all tested prototypes showed a very high detection efficiency >99%, which could be measured over a large range of operational temperatures (from -20°C to 40°C); on the MIMOSA-9 prototype it has proven to be very high even for a 40 μm pixel pitch (for a large pixel size, and moreover in the presence of a thick epitaxial layer, charge losses are expected due to the large free path of generated charge carriers before they are sensed by the collecting diodes);

[3] The output amplifiers are custom-designed, low-noise, and drive the input capacitance of an amplifier situated outside the chip. The input capacitance of the output amplifier on chip is small compared to the load introduced by the readout lines, and is therefore charged in a short time after the transfer gate connecting the selected readout line is activated.

[4] For example in [Cla01, Cla01b, DepTh, Gor02, Dev03, Dep03, Gor03].

- individual pixel noise levels from 10 to 20 electrons, with a corresponding average S/N ratio between 20 and 40 could be measured in all prototypes, the lower S/N values referring to the MIMOSA-5 prototype due to the ∼2 times higher noise, mainly coming from the presence of a second buffering stage between the pixels and the output amplifier (Sect. 5.1.2);

- a single point resolution between 1.5 and 2.5 μm, and a double hit resolution of ∼30 μm have been measured for a pixel pitch of 20×20 μm^2; the spatial resolution is still as good as ∼5 μm for a 40 μm pixel pitch in MIMOSA-9. The single point resolution has also been studied as a function of the number of ADC bits, showing that resolutions of 2-3 μm are still possible even with a 3 bit encoding;

- promising performances have been obtained from the MIMOSA-4 prototype, without epilayer, showing excellent charge collection and detection efficiency, despite the poorer spatial resolution (4 μm) due to the larger charge spreading in the substrate;

- the sensor radiation tolerance has been assured in tests performed mainly with neutrons and low-energy (10 keV) X-rays: no significant charge losses have been observed up to an equivalent neutron fluence of $\sim 10^{12}$ cm^{-2}, with a corresponding marginal decrease in the detection efficiency, and also the tolerance to ionizing doses up to several kGy has been assessed. More recently, tests with ∼10 MeV electrons (see Sect. 5.6) have been performed on MIMOSA-9, up to a fluence of $1 \cdot 10^{13}$ e/cm^2: a good S/N and a correspondingly high detection efficiency were still obtained after irradiation, by cooling the detector to -20°C.

5.1.2 MIMOSA-5: the large-scale prototype

The first real-scale prototype MIMOSA-5 was first fabricated in 2001. A second iteration was fabricated in 2003 with an improved fabrication process aimed at the reduction of the dead columns rate and at the improvement of the chip yield[5], which had been found to be only of 20-30% in the first iteration. The sensors from the 2003 batch are sometimes referred to as MIMOSA-5B.

As already mentioned, the main motivation for the fabrication of a real size detector, with an active area of a few cm^2, was the test of the reproducibility of the performance demonstrated on the first small scale prototypes. Moreover, it was also the first attempt at the production of silicon modules which could be assembled to a prototype detector ladder, and at the same time a test of the yield with which consecutive working modules could be obtained on the same wafer.

The detector is built in a AMS 0.6 μm technology (5 V maximum voltage) which features a 14 μm thick epitaxial layer. A single chip consists of 4 matrices of 510×512 pixels each of 17 μm pitch, for a total of ∼1 million pixels distributed over the active area. The only design difference between different sub-arrays comes from the different size of the collecting diode with which

[5]The wafer *yield* is defined as the percent of good/working parts produced out of the total number of parts in which a wafer is separated, i.e. the percentage of die that are acceptable after functional test.

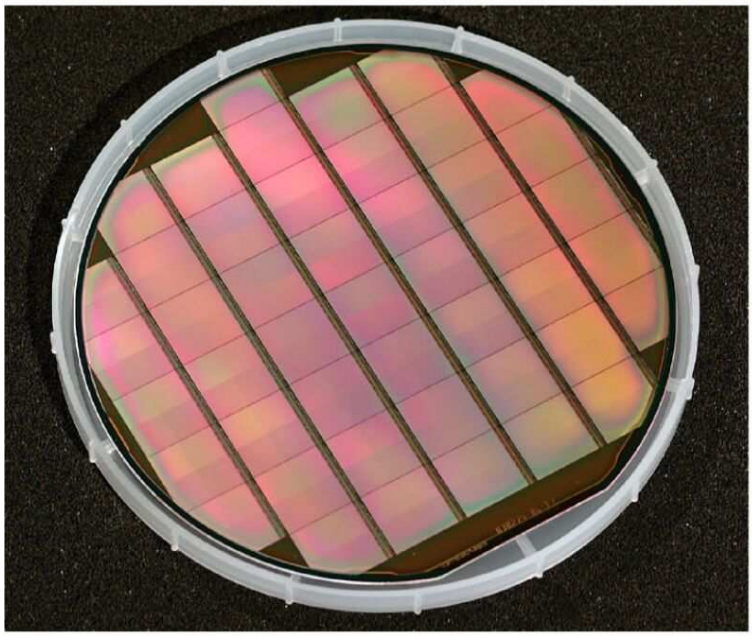

Figure 5.5: View of a MIMOSA-5 wafer (from IReS, Strasbourg).

they are equipped in each pixel. Looking at the chip from the top, the two left sub-matrices (labeled in the following as TOP2 and BOT2) implement a "big" diode option with a size of 4.9×4.9 μm^2, while the two right sub-matrices (TOP1 and BOT1) implement a "small" square diode of 3.1 μm lateral dimensions.

The reticle size is 17350×19400 μm^2. Each chip is equipped with four independent parallel outputs, i.e. one output per array. The readout electronics chain and the noise performance have been optimized to achieve a maximum readout clock frequency of 40 MHz.[6] As can be seen in Fig. 5.5, the modules are aligned along one direction in a 6" wafer in groups of 5 or 7, with a dead area in-between modules of 200 μm. The readout electronics is placed in a 2 mm wide band at the bottom of each module, including input/output pads. No rules for radiation tolerant layout were applied in the detector design [DepTh].

A schematic layout of a detector ladder built using MIMOSA-5 prototypes is shown in Fig. 5.6, which illustrates also the capability of reading the sub-arrays of each detector module in parallel along the shortest side of the ladder, a possibility which is provided by the fact that the readout electronics is placed on one edge of the modules. Nevertheless, since as mentioned above the detector was mainly meant for feasibility demonstration, its architecture was not optimized in terms of readout timing and data transfer, in order to keep the fabrication costs acceptable. Instead, a simple 3-transistor pixel architecture (Fig. 2.10) was maintained and a serial analog readout was implemented.

[6] In practice tests have been performed almost exclusively at 10 MHz clock frequency.

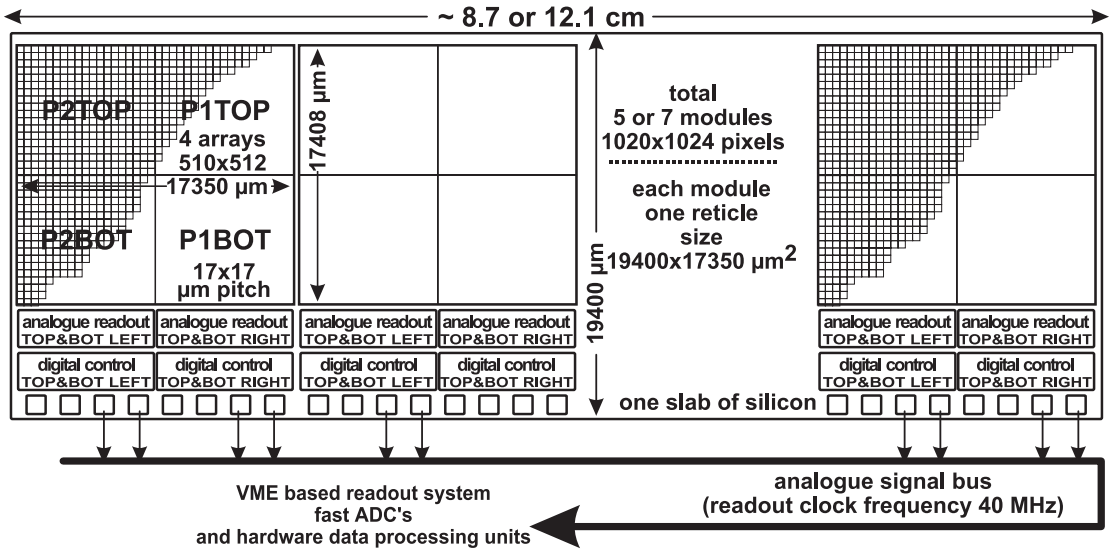

Figure 5.6: Ladder concept in MIMOSA-5 fabrication (from [DepTh]).

In order to cope with the much larger number of pixels, the readout architecture in MIMOSA-5 is different from the simple one shown in Fig. 5.1. The pixels are still addressed sequentially by means of an appropriate row and column selection, but the output of each pixel is sent alternately to 6 horizontal readout lines through a p-MOS source follower which is added at the bottom of every column. Each readout line is terminated with a voltage amplifier with a gain of 5, whose output is multiplexed to the common output buffer (Fig. 5.7). The columns are selected in groups of three (this feature is connected to the various possibilities for readout mode mentioned below) by 170 COL_SEL signals, which are also used to switch on currents in column readout lines, thus biasing the source followers of pixels being selected for readout. When a chosen group of 3 columns is being read out, the following group of 3 columns is being "prepared" by switching on the bias current passing through the source follower transistors of the corresponding pixels, thus charging the capacitive load of the line to the level corresponding to the voltage of the source followers. At the end of every row (selected by the ROW_SEL register), two additional clock cycles are necessary in order to provide enough time for preparation of the first pixel of the next one. The last two pixels in each row (i.e. pixels 509 and 510) are thus readout twice, resulting in acquired images of 512×512 pixels [Dep05].

In the basic operation mode, the standard one in which all pixels are sequentially addressed and read out serially, only one switching signal is active, and therefore only one column is multiplexed at once onto the output buffer. Other readout possibilities (which where nevertheless not used in this work) are provided, for example a fast scan of the array is possible by reading out only every third pixel, or the signal from three consecutive pixels can be summed in the row direction, thus increasing the effective readout pitch in one direction to three times the pixel pitch [DepTh].

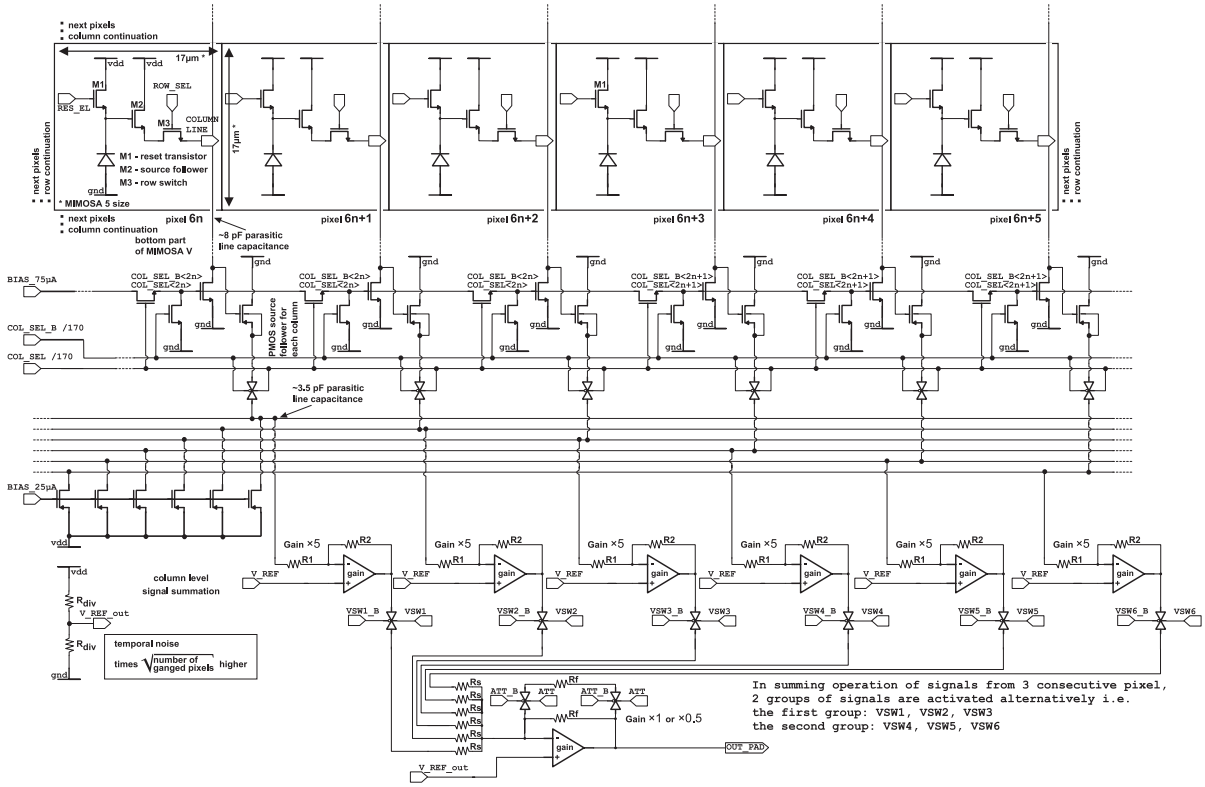

Figure 5.7: Schematic of MIMOSA-5 readout architecture (from [DepTh]).

5.2 Experimental setup for prototype tests

A dedicated test-stand for prototype chip measurements was built in order to perform tests of the MIMOSA-5 prototype. The initial goal of the tests was the calibration of the sensor charge-to-voltage conversion gain and the estimation of the leakage current and noise performance. This was mainly accomplished by illuminating the chip with a low-energy X-ray source. The test-stand was then ported to a beam-test area and combined with a silicon reference telescope in order to study the detector performance for charged particle tracking.

5.2.1 Test-stand for measurements with radioactive sources

A schematic representation of the test-stand built for prototype measurements is shown in the left part of Fig. 5.8, while the right part of the same figure displays actual pictures of the experimental setup. The hardware and the software for the readout of the MAPS prototypes have been provided by IReS/LEPSI [Cla04].

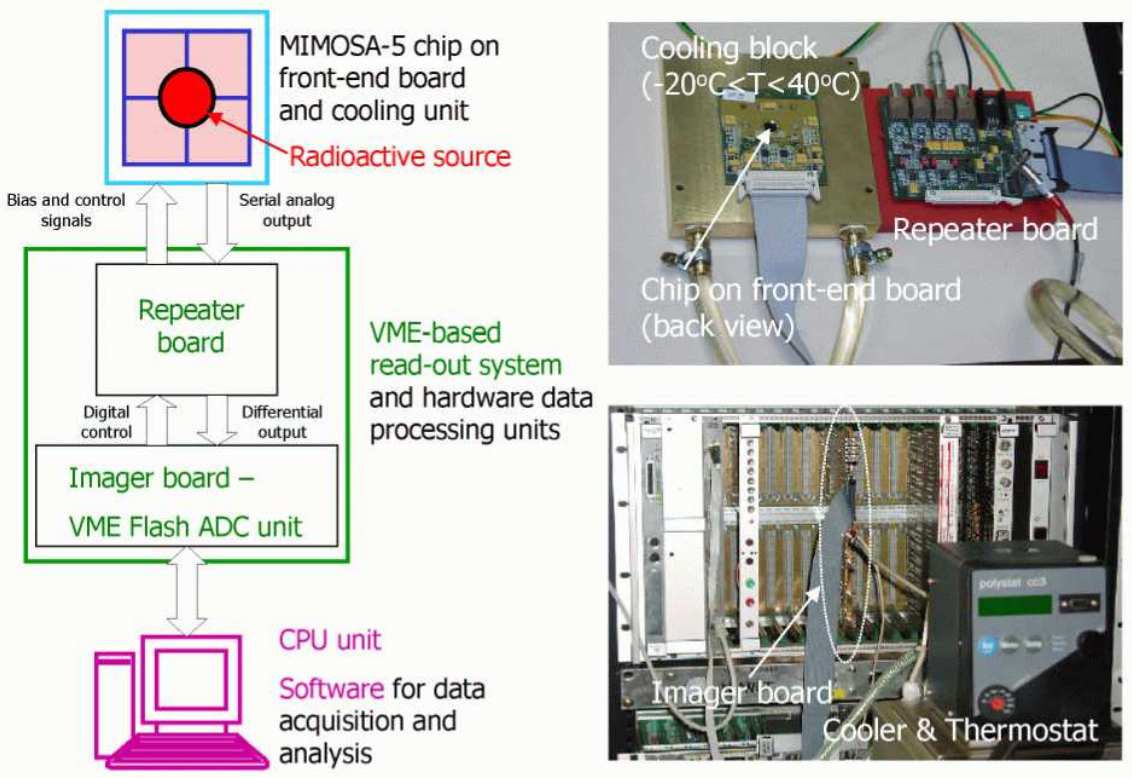

Figure 5.8: Schematic of the data acquisition setup for the test of MIMOSA-5 prototypes.

The MIMOSA-5 chip is mounted and wire-bonded on a PCB board (*front-end board*) with the first stage of external amplifiers and current sources needed for the detector operation. The front-end board is connected to an auxiliary board (*repeater board*), which is connected to an external power supply and is used to provide the chip with analog and digital power, and to generate reference voltage levels for the on-chip and external amplifiers. The repeater board is also used for the two-directional transmission of digital control signals between the chip and the VME *imager board*, and for the transmission of the analog output data for digitization, performed on the imager board by 4 independent Flash ADC Units with 12 bit resolution. The imager board generates the needed digital signals, i.e. the readout clock and the reset signals, which are then transmitted to the front-end board via the repeater board. The digital control of the data acquisition is handled by a Xilinx FPGA logic unit, consisting in one controller and two processor chips (see schematic in Fig. 5.9), installed on the imager board. The latter also provides SRAM memory for the storage of two consecutive images (frames) of the full detector, and the possibility of being programmed in order to realize algorithms for on-line data processing, e.g. the CDS operation of subtracting the two consecutive frames of one event can be performed on the board and the result stored on disk together with the information from the single frames. The imager board is housed in a VME crate, controlled by a Motorola PowerPC CPU running the LynxOS real-time operative system. An ethernet link connects the VME CPU

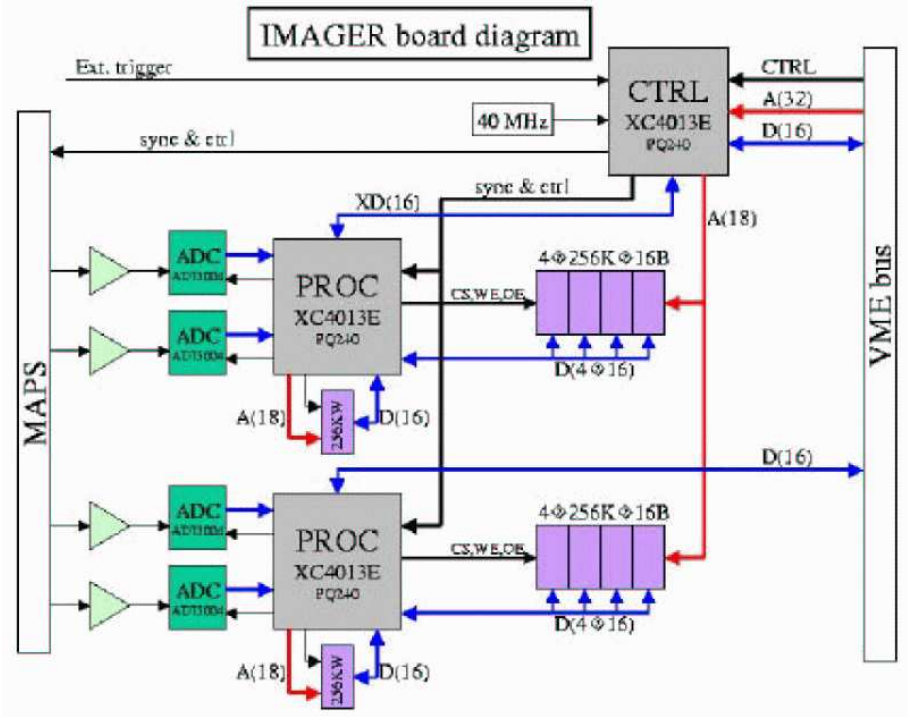

Figure 5.9: Schematic of the VME imager board (from IReS, Strasbourg).

to a remote Linux PC: the data acquisition software running on the PowerPC CPU reads the data in the memory of the imager board and sends it through the ethernet link to the hard disk of the Linux PC, where it is stored. The Linux PC is also used for data quality control and off-line analysis, by means of custom-made software based on the Root object-oriented, C++ based framework [Root].

Considering the rather large charge integration time (26 ms), the leakage current of the pixel diodes, which modifies the voltage of the charge collecting node, can lead to output voltage levels outside the dynamic range of the ADC, thus leading to saturation of the latter. For the same reason, the rate at which a reset is applied to the detector is very important for proper operation. Stable test conditions, with moderate increase of the leakage current (see Sect. 5.4.1), are reached by cooling the detector to temperatures close to or lower than 0°C.

The PCB board is housed in a brass block used in order to cool down the detector. A circular opening on one half of the brass block allows to place a ^{55}Fe radioactive source on top of the detector. Light is prevented to pass through the opening by a thin aluminum foil. Thin plastic absorbers can be placed between the radioactive source and the aluminum foil in order to decrease the rate of photons reaching the detector. The brass block is connected to a cooling unit, which can operate in a temperature range between -20°C and 40°C, controlled by a thermostat. The cooling liquid, a 50% mixture of water and glycol, flows from a storage tank into a circular path, part of which is inside the walls of the brass block, which then cools

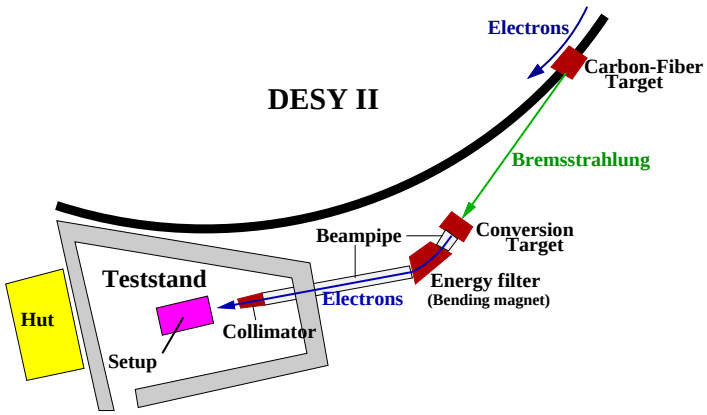

Figure 5.10: Schematic of the DESY-II test-beam area.

down the detector by thermal conduction and convection. Part of the cooling pipes and the brass block are housed inside an insulating polystyrene box. Nitrogen inside the cooling box maintains the environment dry and therefore avoids condensation on the detector surface and on the electronics.

In the case of illumination with a radioactive source, no trigger information is available and consecutive events from the pixel sensor are acquired by reading two frames and transferring the data to disk immediately after the second frame. Two frames are then available for each event for the extraction of the useful signal information from the CDS difference. The measured signals from photons coming from the radioactive source will be the ones integrated during the acquisition time between the first and the second frame.

In the case of beam-tests, which will be described in the following, a trigger is provided to the data acquisition system, and is handled by the imager board. After a reset is issued, the sensor is being read out continuously. The imager board can store in its memory only two frames therefore, as long as no trigger signal is received, the two memory locations are being overwritten with consecutive frames. Upon reception of a trigger, the data acquisition is stopped after a number of clock cycles equal to the ones needed to acquire a complete frame, and the CDS difference is calculated between the frame thus acquired and the frame previously stored on the board memory. The signal from the particle triggering the setup will then be available from the CDS difference. After the data is sent to disk, the imager board is re-initialized, a reset is issued and the data acquisition system is ready to accept the next triggered event.

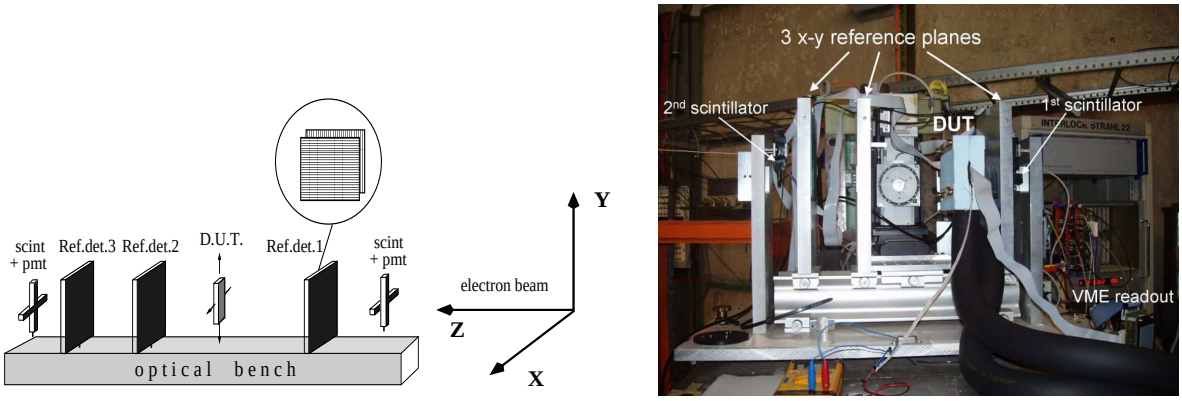

Figure 5.11: Schematic layout of the optical bench (left) and actual picture of the complete test-beam setup (right). The pixel prototype, here labeled as DUT (Device Under Test), is placed in a polystyrene foam box for thermal insulation.

5.2.2 Setup for tests with electron beam

The beam-test facility at the DESY-II synchrotron

The DESY-II test-beam area, schematically depicted in Fig. 5.10, provides a parasitic electron beam after two conversions of the beam of the electron/positron synchrotron DESY-II . A bremsstrahlung beam is produced by a 10 μm thick carbon fiber target which intercepts the electron beam. The generated photons are converted by a target into electron-positron pairs. Targets of aluminum or copper of various thicknesses can be selected. A bending magnet together with a collimator slit, used to select the particle momentum, delivers the beam into the experimental hall. The beam momentum can be chosen by setting the magnet current. Depending on the operation of DESY-II, the maximal momentum achievable for electrons or positrons is around 7 GeV. In this work, energies from 3 to 6 GeV were used. The choice of an electron energy which is slightly smaller than the maximum is a-priori justified by the correspondingly higher rate achievable, in principle up to several 100 Hz depending on beam energy, converter target and collimator opening. The actual event rate in the test of MAPS prototypes is nevertheless limited by the data acquisition system of the pixel detector, and is between 0.5 and 1 Hz, the main limitation coming from the dead-time needed for transferring the data over the ethernet connection and writing it to disk, and from the internal settling time of the imager board.

A silicon reference telescope was used for the reconstruction of the particle tracks. It consists of three planes which are mounted on an optical bench (Fig. 5.11) and can be moved at different positions along the direction Z of the beam axis. Each plane can provide a 2-dimensional measurement of the particle impact position in the X and Y directions perpendicular to the beam axis (see below for a description of the telescope sensors). The MAPS prototype is mounted between two telescope planes on an aluminum support that can be clamped to the optical bench, and is covered by an insulating polystyrene box. Part of the circuit in which the cooling fluid

flows is inside the aluminum frame and thus serves the purpose to cool down the detector. The detector surface was mounted parallel to the surface of the telescope planes. The sensor could be moved along the beam direction and in the X and Y directions, for centering on the beam spot, but always with the surface perpendicular to the beam direction, i.e. only the case of tracks with normal incidence was considered.

The data acquisition system for the telescope readout is located in the same VME crate together with the MAPS imager board, and is controlled by custom-made, C/C++ based readout software running on the VME PowerPC. The readout software controls the initialization and operation of a sequencer Caen V551B for pattern generation, and of two ADC modules Caen V550 [CAEN] for digitization of the analog output from the telescope sensors.

The trigger is provided by the coincidence signals of two small plastic scintillators located at each end of the telescope and defining a trigger area of roughly 7×9 mm^2 in the (X, Y) plane. The trigger is sent to an input available on the MAPS imager board, which, upon reception and acceptance of the trigger, can deliver a secondary trigger to the input of the V551B sequencer, in a master-slave mode. This ensures a one-to-one correspondence between the events acquired for the pixel detector and for the telescope detector.

The silicon reference telescope

The telescope modules are a version of a CERN development [Col96], and were originally assembled in the DESY-II area for the test of the silicon strip detectors for the Micro-Vertex Detector (MVD) of the ZEUS experiment at HERA [MilTh]. Each telescope plane consists of two high-resolution single-sided, AC-coupled silicon microstrip detectors, mounted in an electrically shielded metal box with perpendicular strip orientation, for the measurement of two orthogonal coordinates, X and Y, at a distance of ∼2 mm. Each sensor is ∼300 μm thick, and has an area of 32×32 mm^2; the strip pitch is of 25 μm, and the readout pitch of 50 μm, i.e. every second strip is connected to the readout electronics and every sensor has 640 readout channels. The intrinsic position resolution of these silicon sensors has been measured to be of ∼3 μm in [MorTh].

The sensors are operated fully depleted at a bias voltage of 50 V. The 640 readout strips in each sensor are read out by five VA2 chips [IDEAS], which are built in a 1.2 μm technology and contain each 128 channels. Each channel has a charge-sensitive pre-amplifier followed by a CR-RC shaper, with 2 μs peaking time, and a sample-and-hold circuitry. The data from each channel is serially sent through a multiplexer to an output buffer, and the analog signals are finally digitized by the V550 ADCs (with 10 bit resolution and a maximum conversion rate of 5 MHz), controlled by the V551B sequencer.

Figure 5.12 shows the signal distributions for the 6 telescope modules. The plots represent, for each module, the cluster signal (in ADC counts, since no charge-to-voltage conversion is available) as calculated after cluster reconstruction as the sum of the highest strip signal and the signals in the neighboring strips which are above a signal-to-noise threshold of 2. The telescope sensors achieve a high signal-to-noise ratio, with values varying from ∼50 to ∼90, which results in a very high (>99%) detection efficiency. The data analysis procedure for the

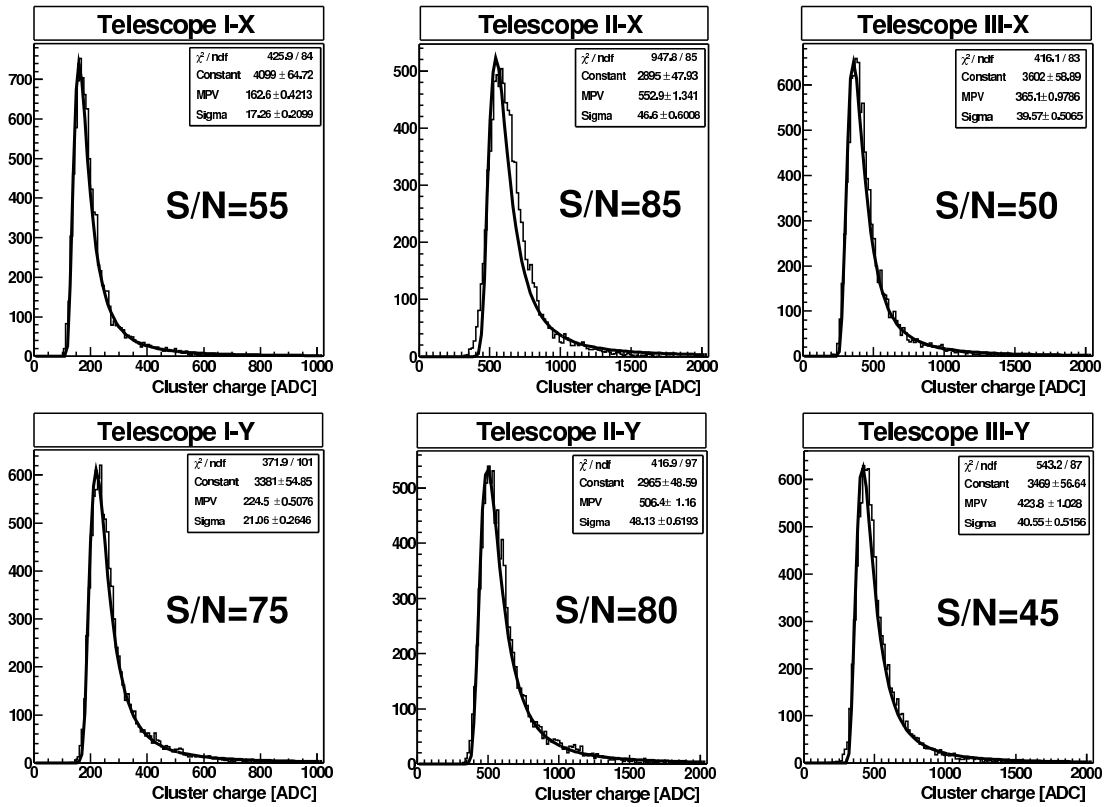

Figure 5.12: Pulse height distributions for the telescope detectors and corresponding Landau fits.

telescope data is similar, apart from the pedestal correction, to the one used for the pixel sensor data, and will be described in detail in next section.

5.3 Data analysis procedure

In this section the procedures applied in the analysis of the detector data is presented. Two different approaches were used for the analysis of the telescope data and of the pixel sensor data. In the first case, a set of thresholds for the detector channels were initially defined from a calibration run. For each channel, the threshold value was set equal to the average pedestal for the specific channel, plus one deviation standard of the measured noise signals. The threshold values were stored in the memory of the ADC modules, allowing on-line zero-suppression during data taking. The analysis of the experimental data is then done starting from the cluster search described in Sect. 5.3.2. In the case of the pixel detector, the pedestal and noise contributions are estimated from the initial part (100 or 200 events) of every run, and the corresponding corrections are then applied in the analysis of the remaining events of the same run.

5.3.1 Pedestal, noise and signal calculation

The *raw signal* r_k^i of the detector channel k in the event i is given by the sum of the signal s_k^i (which is the convolution of the physical charge signal and of the random noise), the pedestal p_k^i and the common mode shift c^i:

$$r_k^i = s_k^i + p_k^i + c^i \tag{5.2}$$

where the common mode shift c^i is the same for a specific group of channels, defined according to the readout architecture (e.g. the 128 channels read out by every VA2 chip on each module of the reference telescope or a 512 pixel line in the case of the pixel sensor).

In order to determine the pedestal for each channel, an initial estimate is extracted from the first N events of a run, typically a value N=100 has been used in this work. The *true* initial pedestal is defined as

$$p_{k,N} = \frac{1}{N}\sum_{i=1}^{N}(r_k^i - s_k^i) = \frac{1}{N}\sum_{i=1}^{N}\tilde{r}_k^i \tag{5.3}$$

that is the sum runs over the *signal suppressed raw values* $\tilde{r}_k^i$. In order to extract signal suppressed raw values from the experimental data, a *pedestal estimator* has to be defined. The chosen approach was to divide, for each channel, the raw values from the N events into smaller buffers of M=5 raw values from M consecutive events. Any value inside the buffer smaller than the maximum is considered an estimator of a signal suppressed raw value, and is included in the calculation of the pedestal estimator after N events as

$$p_{k,N}^{\mathrm{est}} = \frac{1}{N'}\sum_{j=1}^{N'}\tilde{r}_k^j \tag{5.4}$$

where the sum runs over the $N' = N - E$ considered events, with E the number of values excluded from the N events (i.e. the maxima of the buffer of M events). The efficiency of such a pedestal estimation method depends on the probability of finding two physical signals in the buffer of M events, and ultimately on the pixel occupancy. In the typical test conditions described in this work the latter is always at the per mill level.

The initial noise for each channel after the first N events is then calculated as the standard deviation of the pedestal estimator

$$n_{k,N} = \sqrt{\frac{N'}{N'-1}}\sqrt{\left(\frac{1}{N'}\sum_{j=1}^{N'}(\tilde{r}_k^j)^2\right) - (p_{k,N}^{\mathrm{est}})^2} \tag{5.5}$$

where the sum runs over signal suppressed raw values $\tilde{r}_k^j$. It is clear that if raw values with signal would not be suppressed, the noise of channels which are actually illuminated would be overestimated.

Pixels whose pedestal or noise is found to be very high (or very low, in the case of negative fluctuations in the pedestal) with respect to the average value calculated for the whole matrix

can be masked as *bad pixels* and excluded from the analysis. The typical number of such pixels is found to be in the order of a few hundred, i.e. ∼1 per mill of the total number of pixels.

For events $i > N$ the signal charge for every channel is estimated from Eq. 5.2 as

$$s_k^i = r_k^i - p_k^i - c^i \tag{5.6}$$

that is the correction of the raw signal in every channel for pedestal and common mode shift. The common mode shift is calculated row-wise[7] as

$$c^i = \frac{1}{K} \sum_{k=1}^{K} (r_k^i - p_k^i) \tag{5.7}$$

and the pedestal is found by using the *recursive pedestal-follower method*

$$p_k^i|_{i>N} = \frac{1}{A} \left[(A-1) \cdot p_k^{i-1} + \tilde{r}_k^i - c^i \right] \tag{5.8}$$

where p_k^{i-1} is the pedestal for the same channel from the previous event and $\tilde{r}_k^i$ is a signal suppressed raw value, i.e. the pedestal is updated only for channels where the absolute value of the difference $|r_k^i - p_k^i|$ is within three times the estimated channel noise, otherwise the value from the previous event is kept. The common mode shift in the corresponding row is calculated including only channels which satisfy the same condition, so in general $K \leq 512$ in the sum of Eq. 5.7.

The weight A in the pedestal calculation is used in order to minimize the impact of strong fluctuations in the pedestal value coming from the contribution of noisy or bad events. The pedestal variation in such a case is smoothed by the amplitude $1/A$, and then decays with a constant A. The value for the weight has been chosen in order to be at the same time robust against fluctuations and sensitive enough to follow small changes in the pedestal. A value of $A = 100$ has been experimentally chosen in this work.

The noise for events $i > N$ can be calculated from the noise in the previous event and the signal fluctuation in the actual event as

$$n_k^i|_{i>N} = \sqrt{\frac{1}{B} \left[(B-1) \cdot (n_k^{i-1})^2 + (\tilde{r}_k^i - p_k^i - c^i)^2 \right]} \tag{5.9}$$

and again the noise is updated only with signal suppressed raw values $\tilde{r}_k^i$, otherwise the value from the previous event is kept. A recursive method is applied here in the same way as for the pedestal in Eq. 5.8. A value $B = 100$ has been experimentally chosen also for the weight B, which in general can be different than the one of the weight A.

The procedure of correcting the raw signal data from the ADC for pedestal and common mode shift is illustrated in Fig.5.13 for one pixel. The raw data assume discrete values and distribute around a non-zero mean value (top-left part of the figure). This is corrected for the pedestal

[7] In the case of the telescope modules, the common mode shift is calculated for groups of 128 readout strips connected to same VA2 chip.

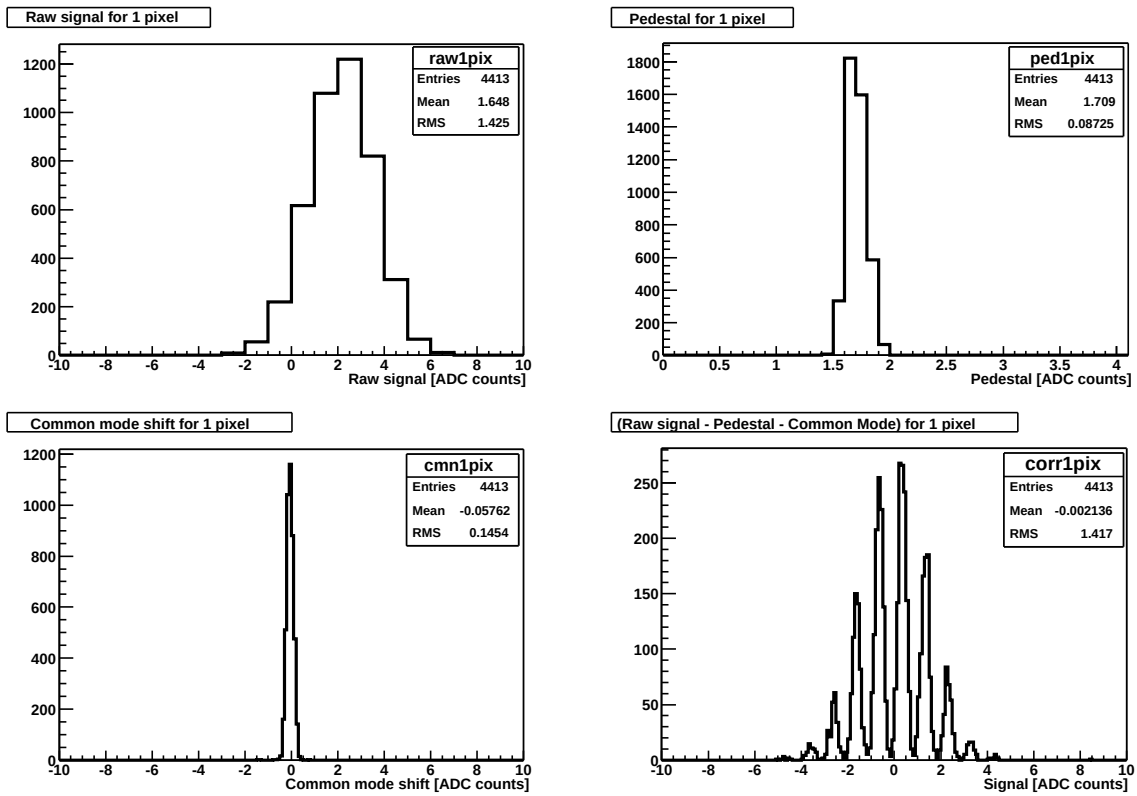

Figure 5.13: Illustration of the correction of the raw ADC data after CDS for pedestal and common mode shift for 1 pixel.

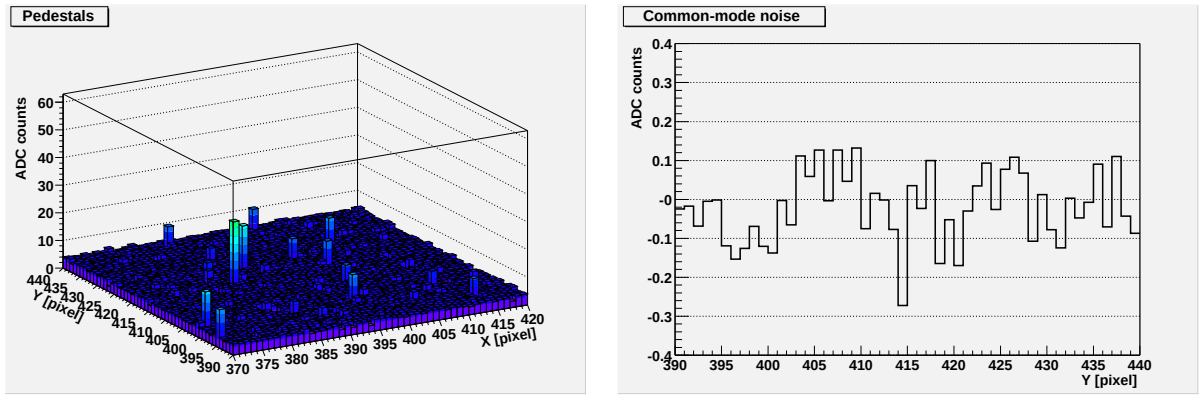

Figure 5.14: Example of MAPS data analysis: pedestal and common mode calculation, for the same raw data after CDS displayed in Fig. 5.3. The common mode values are shown as a function of the row number.

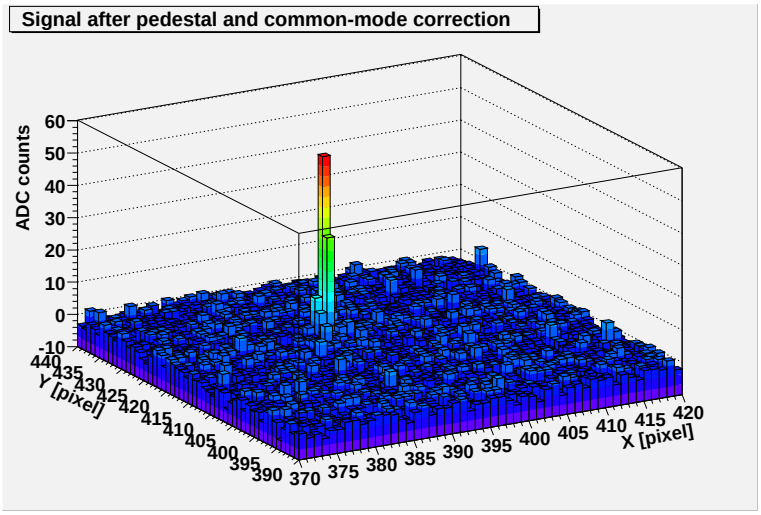

Figure 5.15: Example of MAPS data analysis: signal after pedestal and common mode correction. The plot shows the signals extracted from the raw data after CDS displayed in Fig. 5.3, after correcting for pedestals and common mode shifts (Fig. 5.14) and after masking of bad pixels.

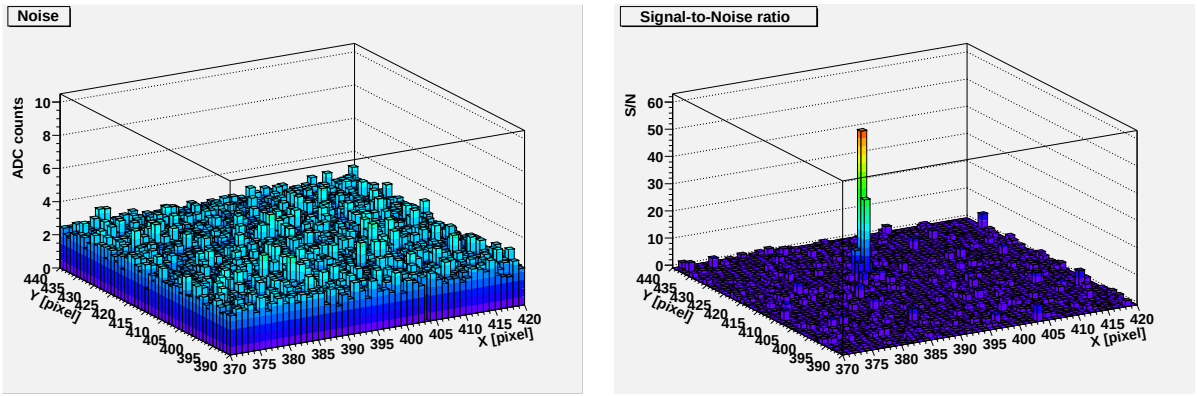

Figure 5.16: Example of MAPS data analysis: noise and signal-to-noise calculation, from the same data of Fig. 5.3 and Fig. 5.15.

calculated for every event according to Eq. 5.8 and for the common mode shift calculated from Eq. 5.7 (top-right and bottom-left part of the figure, respectively). The resulting distribution of pedestal subtracted and common mode corrected signals is shown in the bottom-right part of the figure. The mean of the distribution is close to 0 and the root mean square gives an estimation of the pixel noise. The distribution is structured in peaks due to the quantization by the ADC: indeed, the raw ADC integer values are corrected by floating values (i.e. pedestal and common mode shift values) whose dispersion is smaller than 1.

Figure 5.14 shows an example of the calculated pedestals and common mode shifts in a 50×50 pixel subset of one MIMOSA-5 sub-matrix, for the same raw data displayed in Fig. 5.3.

The resulting signals after pedestal and common mode correction are shown in Fig. 5.15. From the comparison with Fig. 5.3, it can be seen that two pixels, which have been found noisy during the analysis, are masked, and only one hit cluster is clearly visible. Figure 5.16 shows the noise and the corresponding signal-to-noise ratio calculated from the same data.

5.3.2 Cluster selection

After the first part of the analysis described in the previous section, the values of the signal charge and of the noise are known for every channel. In order to determine the candidate *hits* on the sensor due to a photon emitted by the ^{55}Fe source or to the charged particle from the beam, a search of *seed pixels*[8] is performed by selecting the channels whose signal-to-noise ratio is above a certain threshold, i.e.

$$\frac{s_{\text{seed}}}{n_{\text{seed}}} \geq t_{\text{seed}}. \tag{5.10}$$

The seed pixel can be defined as the pixel with the highest S/N ratio of the cluster, or the pixel with the highest charge. The two definitions are in general not equivalent, but are expected to yield equivalent results, considering the rather good uniformity in the pixel noise for the whole matrix (see Sect. 5.4.1).

In the analysis, a first loop is performed over all the pixels of the matrix for the selection of those which satisfy the requested cut. This is followed by a check that two pixels of the same cluster are not recognized as two different seed pixels, and at the same time that the cluster is defined around the pixel with the highest S/N ratio, according to its definition. This is done by sorting all the potential seed pixels according to decreasing signal-to-noise ratio, and then, starting from the pixel with the highest S/N, the distance between it and all the other pixels in the list is controlled. If other pixels of the list are found in the 3×3 pixel region around the first seed, they are eliminated from the list of potential seeds. The same procedure is then repeated for the second potential seed and so on for all the pixels of the potential seeds list.

The efficiency of such a method can of course be affected by the presence of the so-called "hot pixels", that is pixels which very often show a large signal even in the absence of a physical signal, e.g. due to a high leakage current. In general, these pixels can pass the masking of bad pixels mentioned above, but can be recognized later in the analysis as those pixels who are reconstructed too often as potential hits compared to the average occupancy.

After the selection of seed pixels, a cluster is reconstructed around them, by applying a further cut on the 8 neighboring pixels in the 3×3 cluster. This can be done in two ways:

- the signal-to-noise ratio of the neighbors is required to be above a certain threshold, i.e.

$$\frac{s_{\text{neigh}}}{n_{\text{neigh}}} = \frac{\sum_{i=1}^{8} s_i}{\sqrt{\sum_{i=1}^{8} n_i^2}} \geq t_{\text{neigh}}^{stn} \tag{5.11}$$

[8]The procedure for cluster selection is here explained with reference to the pixel sensor data. The application of the same procedure to the 1-dimensional case of the telescope strip detectors is straightforward.

- the total charge on the 8 neighboring pixels is required to satisfy a certain cut, i.e.

$$s_{\text{neigh}} = \sum_{i=1}^{8} s_i \geq t^q_{\text{neigh}} \tag{5.12}$$

All clusters which are reconstructed from seed pixels satisfying condition 5.10 and neighboring pixels satisfying condition 5.11 or 5.12 are stored in an ntuple to be used in further analysis. For each reconstructed hit, the information from a 5×5 pixel cluster around the seed pixel is stored.

The *cluster size* for each reconstructed cluster is defined by counting, apart from the seed pixel, the number of pixels around it which satisfy a certain cut on their individual signal-to-noise ratio. In the reconstruction, the application of cuts only to the 3×3 pixel cluster around the seed pixel is justified a posteriori from the knowledge of the typical hit cluster size, as measured from experimental tests (Sect. 5.5).

5.3.3 Position reconstruction

The hit position, i.e. the impact point of the particle in the detector plane, can be reconstructed from the charge collected on the detector channels in the hit region. In the following, the most common algorithms used for position reconstruction are shortly reviewed.

Digital hit position

The simplest determination of the hit position is given by the *digital hit position*, defined as the center of the seed strip (pixel). The measurement precision depends on the strip (pixel) pitch and on the readout method. As long as only digital information is used, and effects arising from track inclination and charge diffusion during collection are neglected, the measurement precision (root mean square deviation from the true coordinate) is estimated from the pitch P as

$$\sigma_p^{\text{dig}} = \sqrt{\langle \Delta x^2 \rangle} = \sqrt{\frac{1}{P}\int_{-P/2}^{P/2} x^2 dx} = \frac{P}{\sqrt{12}}. \tag{5.13}$$

The measurement precision can be significantly improved if the signal charge is collected on more than one strip (pixel) and the coordinate is found by interpolation, i.e. with the center of gravity of the signals or with more refined algorithms.

The center of gravity algorithm

The center of gravity method gives the hit position x_h^{cog} in terms of the charge fraction in each i^{th} strip (pixel) of the cluster. In one dimension, if Q_i is the charge collected by the i^{th} channel and Q_{tot} is the total cluster charge:

$$x_h^{\text{cog}} = \frac{\sum_i Q_i \cdot x_i}{\sum_i Q_i} = \frac{\sum_i Q_i \cdot x_i}{Q_{\text{tot}}} = \sum_i \eta_i \cdot x_i \tag{5.14}$$

with

$$Q_{\rm tot} = \sum_i Q_i \quad \text{and} \quad \eta_i = \frac{Q_i}{Q_{\rm tot}}. \tag{5.15}$$

The sum is usually done over channels whose signal-to-noise ratio exceeds a certain threshold, or can be applied to a default geometrical arrangement of pixels, e.g. a 3×3 pixel cluster in the case of MAPS sensors.

The center of gravity algorithm can be refined by means of the so-called *Double Centroid (DC)* algorithm, which reconstructs the impact position using the strip (pixel) with the highest collected charge and its two (four) closest neighboring strips (pixels). In one dimension, after having computed the center of gravity $C_{\rm left}$, $C_{\rm right}$ between the central strip (pixel) and the left and right neighboring strip (pixel), respectively, the hit position is given by

$$x_h^{\rm DC} = \frac{C_{\rm left}/dr + C_{\rm right}/dl}{dl + dr} \tag{5.16}$$

with

$$dl = \frac{Q_{\rm left}}{Q_{\rm right}} \quad \text{and} \quad dr = \frac{Q_{\rm right}}{Q_{\rm left}}. \tag{5.17}$$

The $\eta-$algorithm

The $\eta-$algorithm is a standard method widely applied in the case of small incidence angles, and consists in a non-linear interpolation between the two neighboring strips (pixels in one direction) of the cluster which have collected the highest signals (indicated in the following as $S_{\rm left}$ and $S_{\rm right}$), among the ones whose signal-to-noise ratio is above a certain threshold. The quantity

$$\eta = \frac{S_{\rm right}}{S_{\rm right} + S_{\rm left}} \tag{5.18}$$

is calculated for each event. A probability density function

$$f(\eta_0) = \frac{1}{N_0} \cdot \int_0^{\eta_0} \frac{dN}{d\eta} d\eta \tag{5.19}$$

is then introduced, where N_0 is the total number of entries in the $dN/d\eta$ distribution, and η_0 is the η value for the considered event. The corrected hit position is then given by

$$x_h^{\rm eta} = P \cdot f(\eta_0) + x_{\rm left} \tag{5.20}$$

where P is the readout pitch and $x_{\rm left}$ denotes the position of the left strip (pixel). Figure 5.17 shows an example of η distribution obtained from one microstrip module of the reference telescope. The non-uniformity of the distribution over the detector area indicates that the capacitive charge division mechanism does not depend linearly on the hit position between readout strips, and the peak which is visible in the middle of the distribution is related to the presence of one interpolating strip between the two readout strips. On the right part of the same figure the corresponding probability density function is shown; a straight line is also drawn in the same figure to illustrate the deviation from linearity.

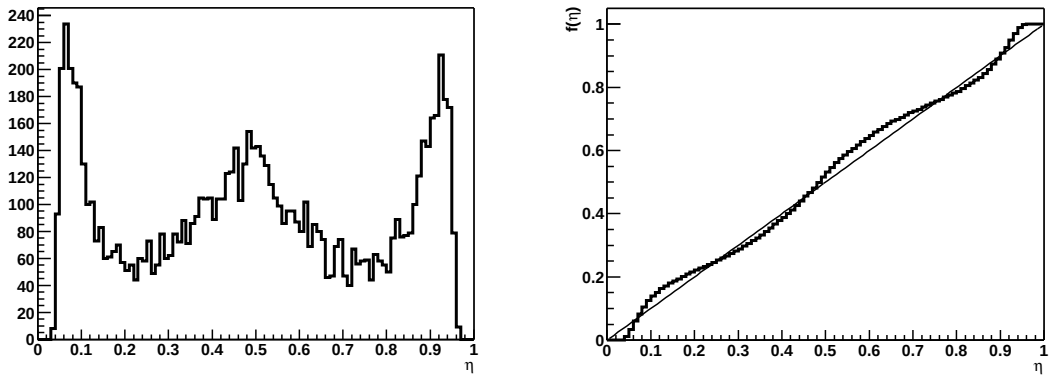

Figure 5.17: Example of η distribution (left) and corresponding probability density function $f(\eta)$ (right) for one telescope module.

5.3.4 Alignment with reference tracks

In order to reconstruct the particle trajectories with the reference telescope and interpolate the particle impact positions on the pixel sensor, the telescope and the pixel sensors need to be aligned with respect to each other in a common reference system. The chosen reference system is defined by the center of the first telescope plane and by the X and Y directions defined by the strips of the corresponding silicon sensors. A parallel mounting, perpendicular to the beam (Z) direction, and orthogonal strip directions are assumed for these sensors.

In general, the free parameters of the alignment procedure are three offsets off_x, off_y and off_z along the X, Y and Z axes and three rotations θ_x, θ_y and θ_z around the same three axes. The offsets along the Z axis (i.e. the beam direction) are estimated from mechanical measurements, while the remaining parameters are determined from a χ^2 square fit which minimizes, in each plane, the distance between the measured and the predicted hit positions:

$$\chi^2 = \frac{(x - x_{\text{pred}})^2 + (y - y_{\text{pred}})^2}{\sigma_{\text{tot}}^2} \tag{5.21}$$

where the predicted coordinates (x_{pred}, y_{pred}) are defined by the straight line extrapolation, parallel to the beam direction, of the position reconstructed in the reference plane(s) and the coordinates (x, y) are obtained from the transformation of the measured coordinates (x_{meas}, y_{meas}) into the reference system by means of the:

$$x = (\cos\theta_y \cdot \cos\theta_z) \cdot x_{\text{meas}} + (-\sin\theta_x \cdot \sin\theta_y \cdot \cos\theta_z + \cos\theta_x \cdot \sin\theta_z) \cdot y_{\text{meas}} + \text{off}_x \tag{5.22}$$

$$y = (-\cos\theta_y \cdot \cos\theta_z) \cdot x_{\text{meas}} + (\sin\theta_x \cdot \sin\theta_y \cdot \sin\theta_z + \cos\theta_x \cdot \cos\theta_z) \cdot y_{\text{meas}} + \text{off}_y. \tag{5.23}$$

The error σ_{tot} on the reconstructed positions is given by the quadratic sum of the intrinsic resolution of the telescope modules $\sigma_{\text{intr,TEL}}$ and of the extrapolation error σ_{ms} due to the effect of multiple Coulomb scattering, i.e.

$$\sigma_{\text{tot}} = \sqrt{\sigma_{\text{intr,TEL}}^2 + \sigma_{\text{ms}}^2}. \tag{5.24}$$

The influence of multiple scattering on the hit position measurement will be discussed in Sect. 5.5.5. The typical alignment procedure consists first in aligning the second telescope plane with respect to the first one. The third telescope plane is then aligned on the extrapolated positions determined with the first two planes. Finally, the MIMOSA sensor is aligned with respect to the tracks obtained from a linear fit between the three telescope planes. Both the alignment procedure and the correlation between the hit positions predicted by the reference tracks and the ones measured on the MIMOSA sensor are performed by selecting events in which the reconstructed particle tracks satisfy a specific quality cut, typically a $\chi^2 < 4$ is required in the analysis. Figure 5.18 (left part) shows an example of correlation plot, for one coordinate, between the position predicted by the track from the reference telescope and the hit position reconstructed on the pixel sensor, after alignment. The corresponding *residual* distribution, i.e. the distribution of the differences between measured and predicted positions, is shown in the right part of the same figure.

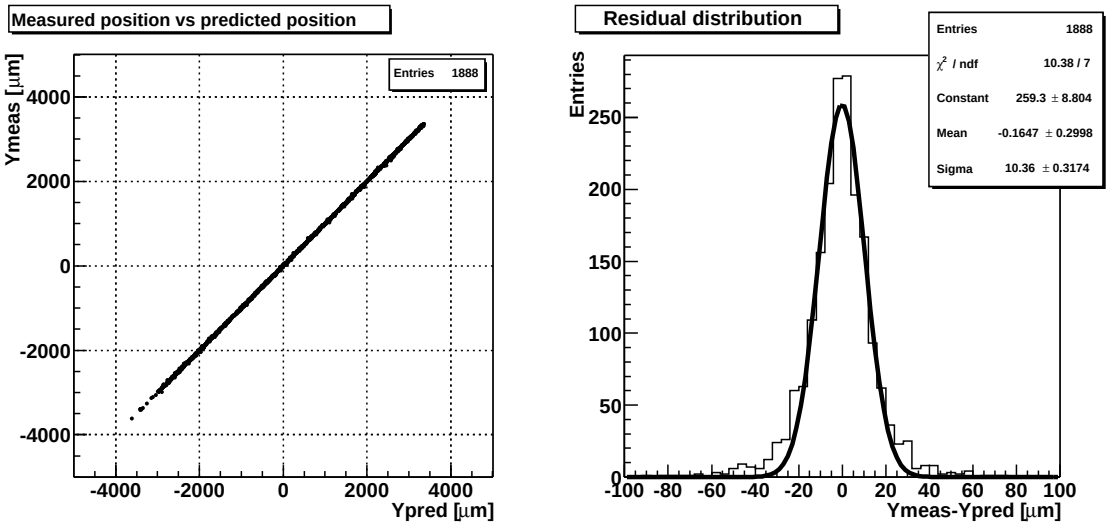

Figure 5.18: Example of correlation plot (left) between position predicted by the reference telescope and reconstructed on the pixel sensor, and corresponding residual distribution (right), for one coordinate.

5.4 Experimental results: calibration measurements

5.4.1 Pedestals and noise

An important step in the characterization of MAPS sensors is the determination of the temporal noise, that is the variation in the pixel output which occurs even in the absence of changes in the input. Low-noise operation and therefore good signal-to-noise ratio performance is in fact essential in order to provide good detection capabilities.

A detailed analysis of noise in MAPS devices is performed in [DepTh]. The three main noise

contributions are related to the three phases of detector operation, i.e. reset, integration and readout. They can be summarized as

- **noise during reset**: reset is needed in order to remove, after readout, the charge collected by the sensing element, and to compensate the diode leakage current. During the reset operation, the row and column selection transistors are switched off and a voltage pulse is applied to the M1 transistor (see Fig. 5.1) in every pixel. The reset pulse should be long enough for the drain current of the reset transistor M1 to equal the level of the diode leakage current. The average reset noise power is related to the total node capacitance C_d which is seen at the input of the source follower transistor M2, and can be estimated by the formula:
$$\overline{V_{\mathrm{n,res}}^2} = \frac{1}{2}\frac{kT}{C_d}; \tag{5.25}$$

- **noise during integration**: it is dominated by the shot noise due to the diode leakage current i_{leak}. It is proportional to the integration time t_{int}, and thus becomes more important with increasing integration time. The mean square value of the noise sampled at the end of the integration can be expressed as
$$\overline{V_{\mathrm{n,int}}^2(t_{\mathrm{int}})} = \frac{q i_{\mathrm{leak}}}{C_d^2} t_{\mathrm{int}}; \tag{5.26}$$

- **noise during the readout**: the main noise sources during the readout are the source follower transistor M2, the transistors for row and column switching (M3 inside the pixel and a transistor common to a whole column outside the pixel), and the current sources used to bias the source follower transistors. A detailed analysis [DepTh] shows that the dominating contributions come from the source follower and from the current source transistors, and that the overall noise performance can be optimized at the design level by choosing the dimensions of these transistors and the load capacitance of the readout lines.

Reset noise is usually the predominant component of temporal noise in MAPS devices, but is effectively removed by the CDS operation, which is also very efficient in removing the influence of low-frequency ($1/f$) noise and of all noise components deriving from non-uniformities in the pixel array, the so-called Fixed Pattern Noise, as shown in [DepTh]. The noise contributions which are not suppressed by CDS, and effectively enter in the measurement, are the noise during integration and the noise during readout.

The pedestal levels and the noise at a particular operational temperature can be determined by means of simple pedestal runs, i.e. runs in which no physical signals coming from a radioactive source or a particle beam are present. Consecutive events are acquired in order to achieve a reasonable statistics for the computation of the mean pedestal and the noise for every pixel. An example of typical pedestal and noise distributions measured on one MIMOSA-5 prototype is shown in Fig. 5.19. The data refer to experimental values calculated after CDS on one sensor submatrix at 0°C. As expected, the pedestal distribution has a non-zero average, which represents the base level of the acquired image after CDS. The pedestal level in every pixel is mainly due

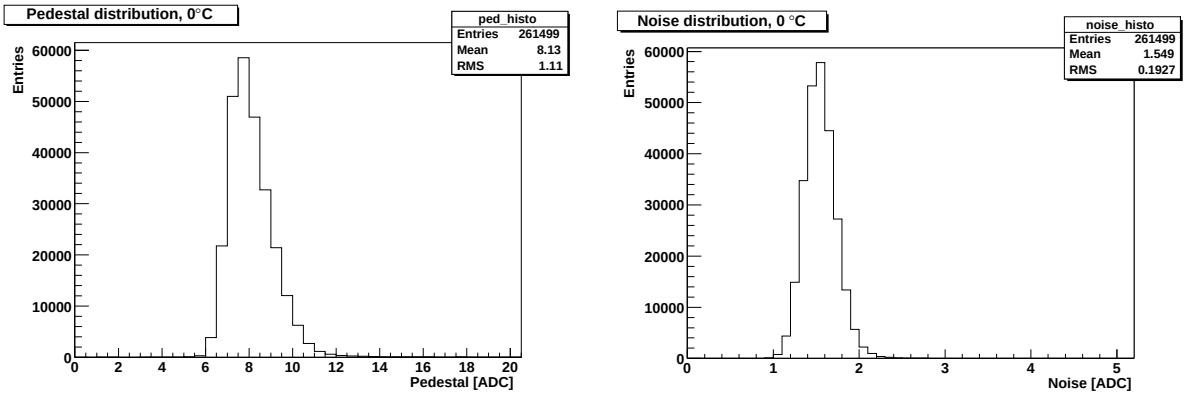

Figure 5.19: Pedestal and noise distributions measured on one MIMOSA-5 sub-matrix at 0°C.

to the leakage current of the charge collecting diode, which can be estimated[9] to be of the order of fA, and is a sensitive function of the operational temperature (see below). The distributions have a non-Gaussian shape; in particular, the tail of the pedestal distribution is related to pixels exhibiting high leakage current, the so-called "hot pixels". The pixel-to-pixel dispersion is in general significant, as a consequence of non-uniformities in the pixel characteristics, mainly coming from the wide spread of the transistor parameters.

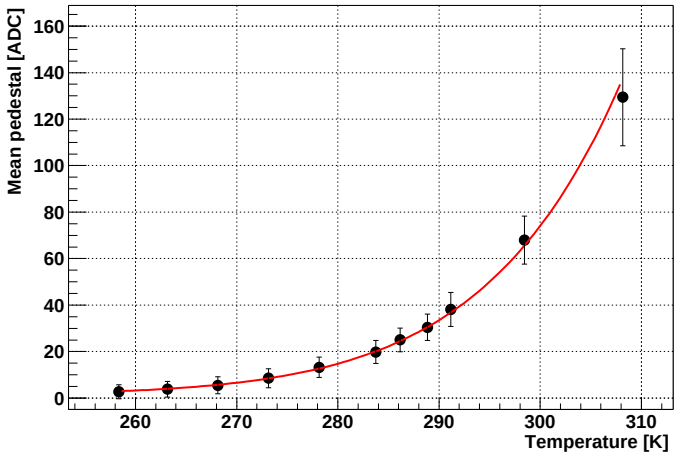

Figure 5.20: Mean pedestal variation as a function of the operational temperature. The error bar associated with each experimental point represents the r.m.s. of the corresponding pedestal distribution, not the error of the mean.

[9]The leakage current can be estimated quantitatively, if the sensor charge-to-voltage conversion gain is known (see Sect. 5.4.2), from the ratio between between the amplitude of the signal in the absence of illumination, i.e. the pedestal, and the frame readout time of 26 ms.

Figure 5.20 shows the mean pedestal measured as a function of the cooling temperature. The error associated with every point is given by the r.m.s. of the corresponding pedestal distribution, representing the pixel-to-pixel dispersion over the whole matrix. The experimental points clearly follow an exponential trend which, consistently with a dependence on the leakage current, can be qualitatively fitted with a function

$$p = c_0 + c_1 T^2 \exp\left(-\frac{E_g}{2k_B T}\right) \tag{5.27}$$

where E_g is the silicon band gap and k_B is the Boltzmann constant. The need to keep the leakage current low, in order to avoid saturation of the pixel output, is the main motivation for the operation of the detector at temperatures lower than room temperature. It should be noted that in this work most of the experimental tests have been performed in a temperature range between -10°C and +10°C. In this temperature range, the measured noise in ADC units is close to the resolution limit of the ADC (i.e. between 1 and 2 ADC counts). In order to extract the noise of the pixel sensor, the values measured experimentally have to be corrected quadratically by the noise introduced by the ADC. This can be estimated from a run in which the chip (i.e. the front-end board) is disconnected from the rest of the readout chain. The noise introduced by the ADC can then be estimated from the r.m.s. of the distribution of the data acquired in this modality, and has been found to be of 0.8 ADC.

5.4.2 Tests with low-energy X-rays

Calibration of the charge-to-voltage conversion gain

The charge collected in each pixel is sensed as a voltage variation in the diode, which is followed by the source of the M2 transistor in the pixel and is available for readout. The charge-to-voltage conversion gain is defined as the signal amplitude at the detector output for a single charge carrier collected in the pixel:

$$G_{q\to V} = \frac{\partial V_s}{\partial N_e} \tag{5.28}$$

that is the variation of the detector signal V_s as a function of the number of collected charge carriers N_e. The commonly used unit of measurement for this quantity is $\mu V/\mathrm{e}$. An analysis performed in [DepTh], taking into account the capacitances and the parameters of the pixel transistors, shows that $G_{q\to V}$ is determined by the total conversion capacitance C_{conv} which is seen at the collecting node during the readout, and by the slightly below unity voltage gain of the source follower transistor. The knowledge of the charge-to-voltage conversion gain is necessary in the characterization of MAPS devices in order to convert the measured signals from ADC counts to absolute units of collected charge, i.e. electrons.

The charge-to-voltage conversion gain can be estimated by illuminating the sensor with low-energy X-rays emitted by a ^{55}Fe radioactive source. The latter emits photons mainly in two monochromatic emission lines K_α and K_β of 5.9 keV and 6.49 keV with an emission probability of 24.4% and 2.86%, respectively [PDG04]. The absorption length for these photons is of $\sim$27 μm

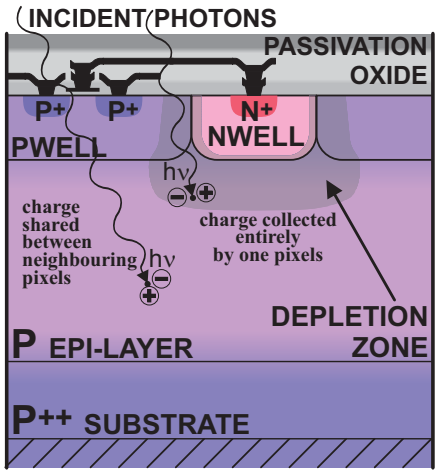

Figure 5.21: Illustration of photon detection in MAPS devices. The charge generated by the incident photons can either be shared between neighboring pixels or collected by one single pixel, depending on the depth at which the conversion occurs in the sensitive volume (from [DepTh]).

and ∼35 μm, respectively, and signals due to photoelectric effect are then generated across the whole depth of 14 μm of the epitaxial layer, i.e. the detector sensitive volume.

Photon detection in MAPS devices is illustrated in Fig. 5.21. In general, the photons hitting the detector will deposit their energy at a certain depth in the epitaxial layer. The charge generated inside the mostly field-free epitaxial layer will diffuse and spread among neighboring pixels; only a part of it will be collected by the closest hit pixel, leading to incomplete charge collection at the single pixel level. Nevertheless, a certain number of photons will interact in the non-zero electric field present in the shallow depletion region[10] around the charge collecting diode, and the charge thus generated will be rapidly collected by the latter. It is therefore possible to assume a 100% charge collection efficiency at the single pixel level for the charge generated by these photons. Considering that the mean energy for electron-hole pair creation in silicon is ϵ_{pair}=3.6 eV, photons of 5.9 keV and 6.49 keV generate on average 1640 and 1804 electrons, respectively. This results in two characteristic peaks in the signal amplitude distribution, and the position of the peaks, in ADC counts, can be used to determine the e/ADC conversion factor and therefore the charge-to-voltage conversion gain.

Figure 5.22 shows an example of ^{55}Fe spectrum obtained from the measurement of one prototype sub-matrix, performed at 0°C. The plot shows the signal height distribution in the central pixel of all clusters satisfying a cut of 10 on the S/N of the seed pixel, and of 2 on the S/N of the 8 neighboring pixels (see Eqs. 5.10 and 5.11, respectively). The broad peak which dominates the spectrum is related to the incomplete charge collection which happens for most of the events. On the right side of the spectrum the two peaks coming from the

[10]The depth of this depleted region can be estimated of ∼2 μm for an applied bias of 3 V and typical doping profiles, as discussed in Sect. 4.2.2.

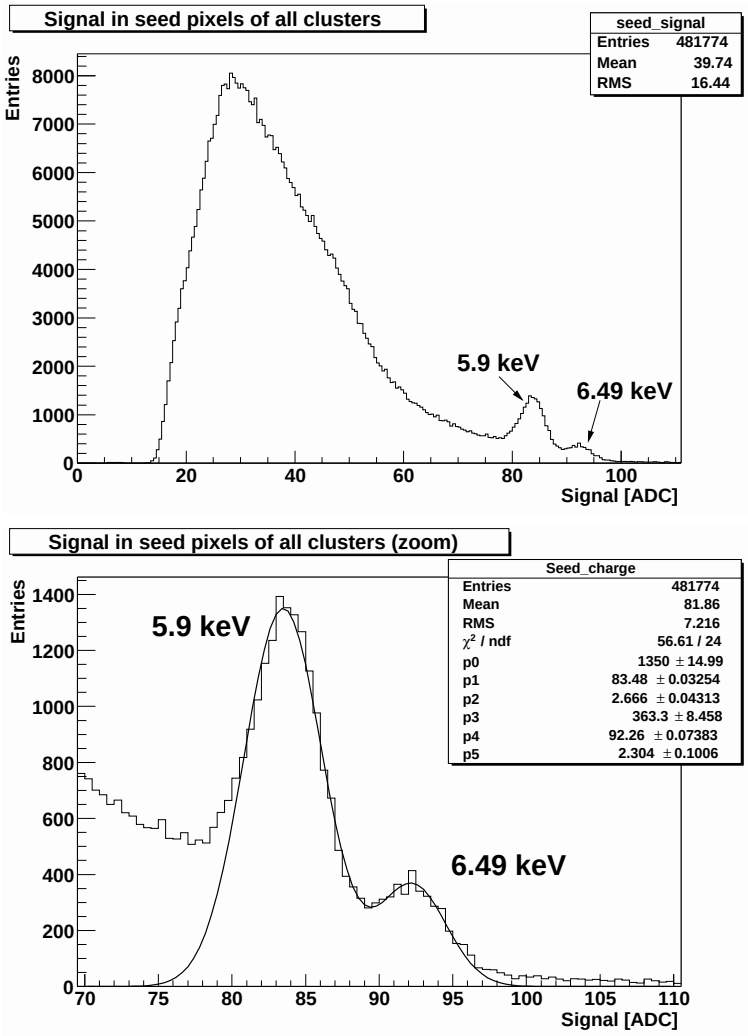

Figure 5.22: Example of ^{55}Fe spectrum in MIMOSA-5: signal in seed pixel of all reconstructed clusters (top), and zoom on the right part of the spectrum showing the peaks corresponding to the two emission lines at 5.9 and 6.49 keV (bottom). The measurement has been performed at 0°C on one sub-matrix equipped with 4.9×4.9 μm^2 ("big") diodes. The double Gaussian fit was performed in the interval between 80 and 95 ADC counts. The fit parameters (p_0, p_1, p_2) and (p_3, p_4, p_5) represent the amplitude, mean and standard deviation of the Gaussians fitting the 5.9 keV and 6.49 keV peaks, respectively.

5.9 keV and 6.49 keV emission lines are clearly visible. The two peaks can be fitted by two Gaussian functions, as shown in the bottom part of the same figure; the mean values of the two Gaussians are used to estimate the positions of the two peaks for the calibration of the charge-to-voltage conversion gain, while the dispersion of the latter over the pixels can be estimated from the values of the standard deviation (see below). Due to the larger emission probability of 5.9 keV photons, the corresponding peak is usually better defined, and is therefore used for

Chip	Matrix	Diode size [μm^2]	Conversion gain [μV/e]	Width of 5.9 keV peak [%]	Gain dispersion [%]	Conversion capacitance [fF]	Noise ENC [e]
603	T01	3.1×3.1	32.3	3.0	2.5	5.0	21
603	B01	3.1×3.1	31.7	3.4	2.9	5.1	22
603	T02	4.9×4.9	23.9	3.4	2.7	6.7	25
603	B02	4.9×4.9	23.9	3.5	2.8	6.7	25
401	T01	3.1×3.1	33.1	2.6	2.0	4.8	21
401	B01	3.1×3.1	32.9	2.6	2.0	4.9	21
605	T02	4.9×4.9	24.4	3.0	2.2	6.6	26
605	B02	4.9×4.9	24.8	2.8	1.9	6.5	27

Table 5.2: Summary of calibration measurements performed on tested MIMOSA-5 prototypes. Reported values refer to measurements performed at -10°C.

these purposes. The presence of the 6.49 keV peak is nevertheless useful as a confirmation of the calibration procedure. It can be seen from the fit parameters in Fig. 5.22 (bottom part), that the ratio between the peak positions, of 1.1, is the same as the ratio of the corresponding photon energies, confirming on one side the correctness of the identification of the two peaks, on the other side the linearity of the ADC calibration.

The two calibration peaks can always be recognized from the spectra of the seed pixels for all reconstructed clusters, their amplitude (i.e. the corresponding number of entries) depending on the particular cuts applied in the cluster definition. An alternative and unambiguous approach is to look for *single pixel* clusters, requiring, beside the usual cut on the S/N of the seed pixel, that the S/N of the neighboring pixels is below a certain threshold. The result of this analysis on the same data of Fig. 5.22 is shown in Fig. 5.23. The 5.9 keV and 6.49 keV peaks now clearly dominate the single pixel signal distribution. Moreover, from the values of the parameters obtained from the double Gaussian fit, it can be seen that the fitted peak positions are the same, within the errors, of the ones estimated in Fig. 5.22.

The gain dispersion over the pixels can be estimated from the width of the peaks after correcting for the fluctuation expected from the detector intrinsic energy resolution, which can be estimated as $\sigma_E = \sqrt{F \cdot \frac{\epsilon_{\text{pair}}}{E_\gamma}}$, where E_γ is the energy of the photon and F=0.115 is the Fano factor[11] of silicon, and from the average pixel noise. For example, referring to Fig. 5.23, the 5.9 keV peak is fitted at a position of 83.5 ADC; for this photon energy σ_E=0.84%, i.e. 0.7 ADC. The average pixel noise is of 1.5 ADC and subtracting quadratically the two contributions from the variance of the Gaussian fit (2.4 ADC) yields 1.7 ADC, i.e. a gain dispersion of 2%.

Table 5.2 summarizes the results from the calibration measurements performed with the ^{55}Fe source in all tested prototypes. All results refer to measurements performed at -10°C. The conversion gain is estimated in μV/e from an ADC resolution of 488 μV/ADC. We remind

[11]The Fano factor describes the fluctuations in the number of electron-hole pairs created in the medium by radiation for a fixed energy deposited in the detector.

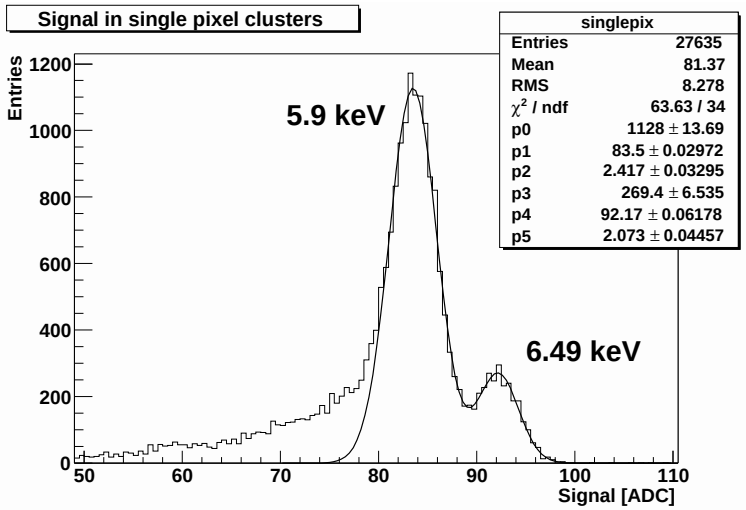

Figure 5.23: Fit of ^{55}Fe spectrum for single pixel clusters (i.e. an upper cut of 2 on the individual S/N of the neighboring pixels is applied) in the regions corresponding to the 5.9 keV and 6.49 keV emission lines. The double Gaussian fit was performed in the interval between 80 and 100 ADC counts. The fit parameters (p_0, p_1, p_2) and (p_3, p_4, p_5) represent the amplitude, mean and standard deviation of the Gaussians fitting the 5.9 keV and 6.49 keV peaks, respectively.

here (see Sect. 5.1.2) that in every MIMOSA-5 chip, sub-matrices T01 and B01 are equipped in every pixel with 3.1×3.1 μm^2 "small" diodes, while sub-matrices T02 and B02 implement 4.9×4.9 μm^2 "big" diodes. Indeed, the charge-to-voltage conversion gain clearly depends on the size of the charge collecting diode, and therefore on the capacitance of the collecting node. A higher capacitance of the charge collecting node is expected to yield a higher signal at the price of a higher noise. The detector signal-to-noise performance is nevertheless expected to be quite uniform for the two diode types, as will be shown in Sect. 5.5 from the experimental results of beam-test experiments. The measured ENC noise reported in the last column of Table 5.2 represents the mean of the noise distribution for all the pixels of one sub-matrix, showing a typical value of 21-22 electrons for matrices equipped with small diodes, and between 25 and 27 electrons for the matrices implementing big diodes.

Cluster signal distribution

The charge spreading onto neighboring pixels can be studied by considered the signal distribution in groups of pixels of different size, according to specific geometrical arrangements. Figure 5.24 shows as an example the signal distributions obtained for clusters of 4, 9, 16 and 25 pixels built around the seed pixels whose signal distribution was shown in Fig. 5.22. The data refer to geometrical arrangements of 2×2, 3×3, 4×4 and 5×5 pixels, respectively. While 3×3 and 5×5 pixel clusters are uniquely defined around the seed pixel (the latter being the largest cluster size selected in the analysis), the signal in 4 pixel (16 pixel) clusters was estimated as the average of

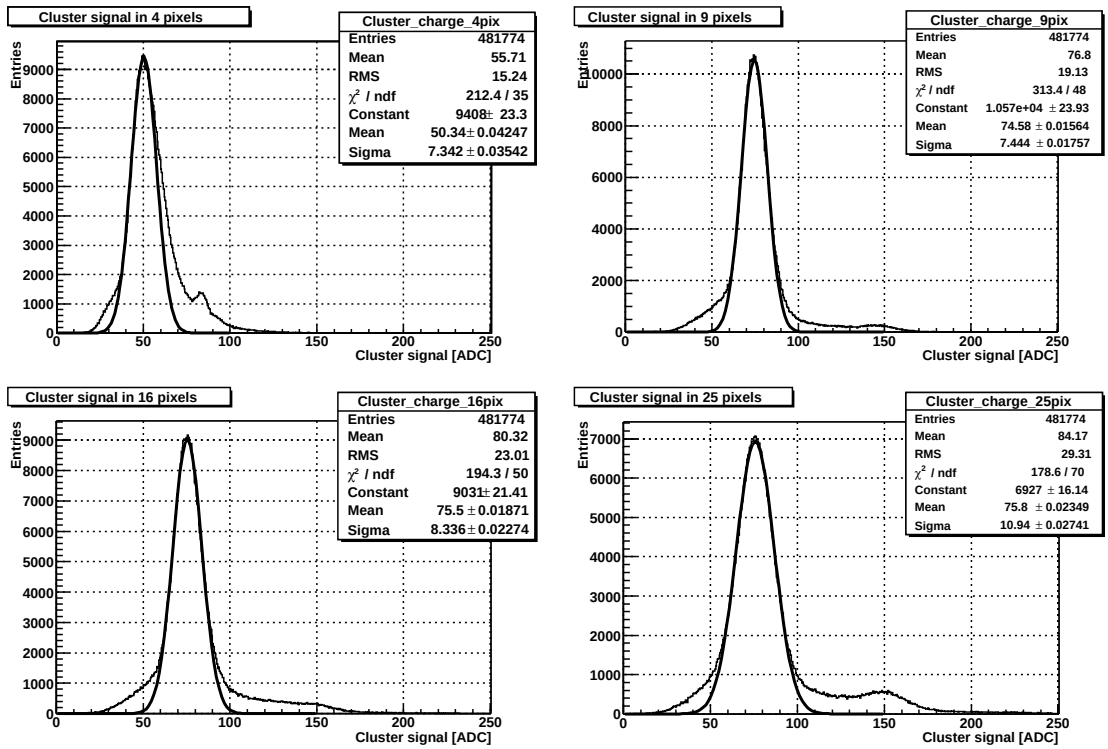

Figure 5.24: Cluster signal distributions for X-ray hits measured in 4, 9, 16 and 25 pixel clusters. The corresponding single pixel distribution is shown in Fig. 5.22.

the signals collected in the four possible arrangements of 2×2 (4×4) pixel clusters including the seed pixel. Each distribution is dominated by a main peak, which is fitted with a Gaussian fit in order to get an estimate of the peak position. The presence of long tails in the distributions for 9, 16 and 25 pixels is related to clusters collecting the charge deposited by more than one photon, whose hits are not distinguished by the analysis, e.g. photons hitting the detector very close to each other, or consecutive hits on the same pixel(s) during the integration time.

From the comparison with the single pixel distribution of Fig. 5.22, it is clear that the collected signal increases by increasing the cluster size, approaching on average values close to the full collection efficiency, i.e. the position of the main peak approaches the position of the 5.9 keV peak (in this case at ∼83 ADC counts, see Fig. 5.22). It should nevertheless be noted that the increase in the collected signal is significant up to 9 pixel clusters, and then tends to saturate for higher cluster multiplicities, indicating that most of the charge is collected already in 9 pixels.

As an alternative approach, the dependence of the mean cluster signal on the pixel multiplicity can be studied by sorting the pixels of each 5×5 pixel cluster according to decreasing pulse

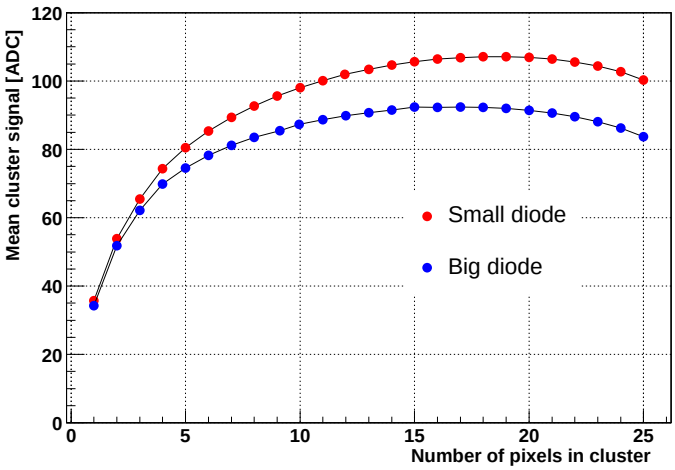

Figure 5.25: Mean cluster signal as a function of the cluster multiplicity, as measured at -10°C for small and big diode pixels on two sub-matrices of one MIMOSA-5 chip. The pixels in each cluster are ordered according to decreasing pulse height.

height[12], and by calculating the mean cluster signal corresponding to every cluster multiplicity, from 1 to 25 pixels, by consecutively adding pixels according to this ordering.

The result of this analysis is shown is Fig. 5.25 for two sub-matrices of one prototype chip, one with big diodes and the other with small diodes[13] The measurements were performed at -10°C, and clusters were selected by applying a cut of 5 on the S/N of the seed pixel and of 2 on the S/N of the 8 closest pixels. The 5.9 keV calibration peaks for these two matrices were measured at 80.1 ADC and 106.4 ADC for the big and small diode case, respectively, with corresponding e/ADC conversion factors of 20.4 and 15.4, respectively. At equal signal, i.e. from 5.9 keV photons, a larger position of the calibration peak for small diodes corresponds to a larger charge-to-voltage conversion, i.e. to a smaller conversion capacitance. The signals measured *in ADC counts* are thus found to be larger for small diodes with respect to big diodes, but in units of charge (electrons) the corresponding signals are, as expected, smaller for small diodes and larger for big diodes.

The experimental curves in Fig. 5.25 confirm, in both cases, the considerations done when discussing the data of Fig. 5.24. The increase of the cluster signal is significant for small cluster multiplicities, and the maximum mean cluster signal is approached already in ∼16 pixel clusters. The peculiar shape of the curves, which for larger pixel multiplicities show first a saturation and then a decrease in the mean cluster signal, is due to the bias introduced in the analysis by the procedure of sorting the pixels according to decreasing pulse height. Indeed, pixels displaying

[12]Equivalently, the 25 pixels can be sorted according to their decreasing individual S/N ratio. This approach has led to equivalent results as the ones presented in the text.

[13]In this work, the comparison between matrices with big diodes and with small diodes is always performed on data measured on the same chip, namely chip 603 (see Table 5.2).

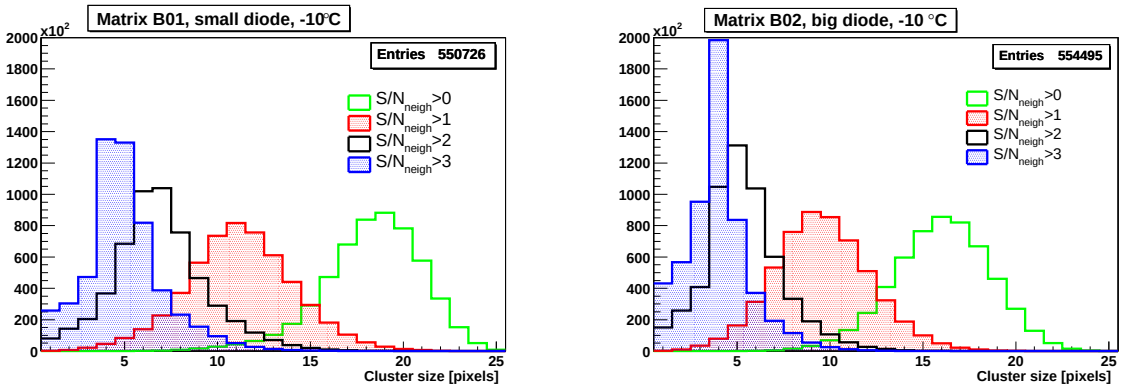

Figure 5.26: Cluster size distribution for X-ray hits as a function of the cut on the S/N of the individual neighboring pixels. The measurements were performed at -10°C. The left plot refers to a matrix with small diodes, and the right plot to a matrix with big diodes.

the lowest signals, and especially negative fluctuations which can occur at the cluster borders, are always introduced only when considering large (e.g. >20) pixel multiplicities.

The definition of the cluster size is clearly strongly dependent on the cut applied for cluster selection, i.e. on the cuts used in the selection of the pixels involved in the cluster formation. In order to study this dependence for X-ray hit clusters, the following analysis was performed. Initially, a cut of S/N>5 was applied as usual for the selection of all the potential seed pixels; afterwards, a pre-selection of clusters was done requiring that the total charge in the 3×3 pixel cluster around the seed pixel be positive; finally, the size of each cluster was calculated by applying a cut on the S/N of the *individual* pixels in the 5×5 pixel cluster other than the central one. Figure 5.26 shows the obtained cluster size distributions, in the case of a matrix with small diodes (left) and one with big diodes (right), for different values of the S/N cut on the individual pixels. It can be seen, besides the obvious decrease of the average cluster size as a function of the increasing S/N cut (the more severe the selection, the smaller the number of pixels that are included in the cluster), that a slightly higher cluster size is found in the small diode case for equal cuts. Indeed, a larger lateral size of the charge collecting diode results in a larger fraction of the pixel area below which a shallow depleted, non-zero electric field region is present. Hence, at equal pitch, pixels equipped with larger area diodes are more likely to limit the charge spreading.

5.5 Experimental results: test-beam measurements

This section presents the experimental results obtained from a series of beam-tests performed on MIMOSA-5 prototypes with the 6 GeV electron beam of the DESY-II test facility (Sect. 5.2.2). The particle hit positions were reconstructed in every plane of the reference telescope with the Double Centroid algorithm (Sect. 5.3.3), and one particle track was reconstructed for each event. The hit positions on the pixel sensor were determined by applying the center of gravity

algorithm, and the alignment with the reference tracks was done according to the procedure described in Sect. 5.3.4. In the following, results are presented concerning the sensor charge collection properties and signal-to-noise performance, for both cases of matrices with big and small charge collecting diodes. The detection efficiency will be discussed as a function of the cuts applied in the cluster selection and in the correlation procedure, and an estimation of the multiple scattering effect on the position resolution will be made. Unless otherwise stated, the results presented refer to measurements performed with a beam energy of 6 GeV at -10°C. A control of the reproducibility of the performances was also done over a temperature range between -10°C and +10°C.

5.5.1 Signal and signal-to-noise

The signal distributions measured in the seed pixel of correlated hits, i.e. hits in the MIMOSA sensor associated with the impact positions predicted by the reference tracks, are shown in Fig. 5.27, together with the corresponding noise and signal-to-noise distributions, as measured at -10°C. The left part of the figure refers to a sub-matrix with small diodes, the right one to a sub-matrix with big diodes on the same prototype chip. The hit clusters on the MIMOSA sensor have been selected by applying a cut of 4 on the S/N of the seed pixels, and a cut of 1 on the S/N of the 8 neighboring pixels. The signal distributions have a Landau-like shape, with a most probable value estimated from a corresponding fit of 256 and 334 electrons for small and big diodes, respectively. The average noise is of 20 and 24 electrons, respectively. In agreement with the measurements performed with low-energy X-rays in Sect. 5.4, a smaller charge collecting diode results in a smaller noise but also in a smaller signal. The S/N performance is nevertheless quite similar in the two cases. The average value of the S/N (of 21 and 23, respectively) is slightly higher in the big diode case, but depends substantially on the long tails of the distributions. Indeed, the peak position is between 10 and 15 in both cases.

Over a temperature range between -10°C and +10°C, the measured signal did not show a significant variation, while the average noise follows an increasing trend as a function of the increasing operational temperature. An example is shown in Fig. 5.28 (left) for a sub-matrix with big diodes. This results in only a slight decrease of the average seed pixel S/N with increasing temperature (right part of the same figure). The noise dependence on the temperature can be qualitatively fitted with a function

$$n = c_0 + c_1 \sqrt{T^2 \exp\left(-\frac{E_g}{2k_B T}\right)} \tag{5.29}$$

where E_g is the silicon band gap and k_B is the Boltzmann constant, consistent with the analogous parameterization of the dependence of the pedestal on the temperature (see Fig. 5.20 and Eq. 5.27), resembling a dependence on the increasing leakage current. Indeed, the noise is related to the fluctuation around the pedestal level, i.e. to the fluctuation in the signal which remains after pedestal correction. According to this parameterization, noise is expected to increase significantly by approaching room temperature. Nevertheless, a good noise and correspondingly signal-to-noise performance is obtained in a wide operational range which requires only moderate cooling.

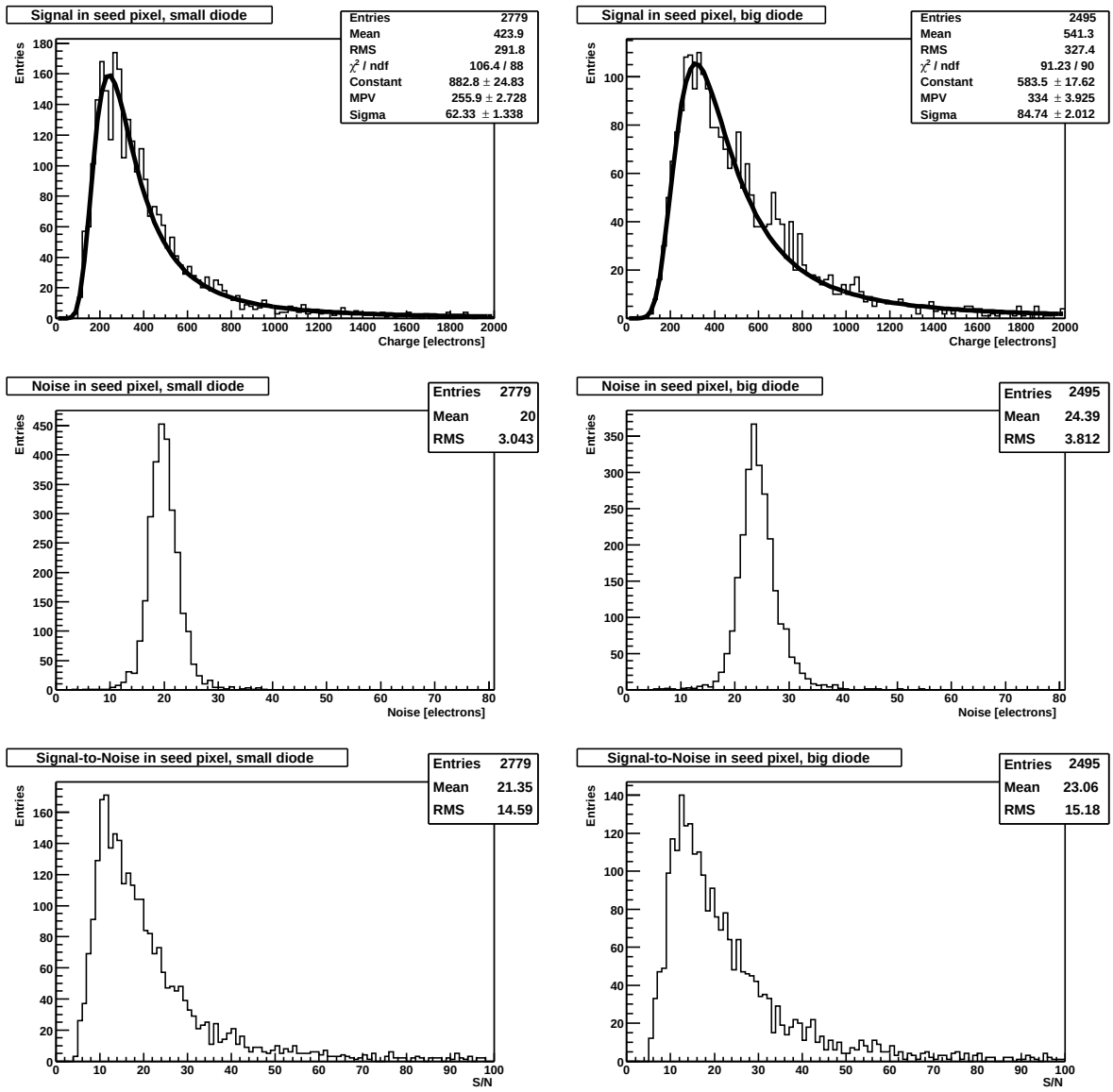

Figure 5.27: Signal, noise and signal-to-noise ratio in seed pixel measured at -10°C on one MIMOSA-5 sub-matrix with small diodes (left) and one sub-matrix with big diodes (right).

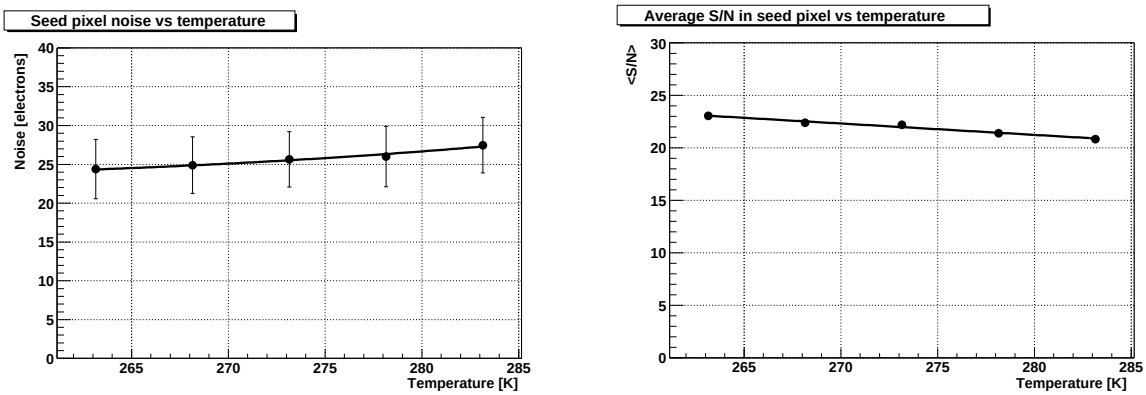

Figure 5.28: Noise (left) and average signal-to-noise ratio (right) in seed pixel as a function of the operational temperature. The measurements refer to a matrix with big diodes. The error associated with the experimental points for the average noise represent the r.m.s. of the corresponding distributions.

5.5.2 Cluster charge

The distributions of the charge collected in 3×3 and 5×5 pixel clusters around the seed pixel are shown in the top and bottom part of Fig. 5.29, respectively. The plots refer to the same measurements of Fig. 5.27; as above, the plots on the left side refer to a matrix with small diodes, the ones on the left side to a matrix with big diodes. The distributions are fitted with a Landau function. The most probable value of the charge collected in 9 pixels is of 703 and 835 electrons, respectively for small and big diodes. The charge collected in 25 pixels increases up to 791 and 882 electrons, with a relative increase of 13% and 6%, respectively. Most of the charge is then collected within a 3×3 pixel cluster in both cases, and the larger relative increase of collected charge for small diodes, when considering 5×5 pixel clusters, indicates a slightly larger cluster size in this case.

In the same way as done in Sect. 5.4.2 after measurements with low-energy X-rays, the dependence of the collected charge on the pixel multiplicity in the cluster can be studied by sorting the 25 pixels according to decreasing signal, and then adding consecutively the thus ordered pixels in the cluster formation. As explained above, this procedure introduces a bias in the analysis, since pixels with the highest signals are always considered first in the sum, while pixels with lower signals, especially negative fluctuations, are always included as last. An alternative, less biased approach is sorting the 25 pixels according to their increasing distance from the hit position. This is done for every hit by calculating the distance between the center of every pixel in the cluster and the reconstructed center of gravity position, and by sorting the pixels correspondingly. The result of this analysis is shown in Fig. 5.30, where the two approaches are compared. The cluster charge for each pixel multiplicity is estimated from the most probable value of the corresponding distribution. The left plot, obtained after sorting the pixels according to decreasing signal, shows the peculiar shape due to the bias introduced in the analysis: after a steady increase for small pixel multiplicities, the curves reach a maximum between 15 and 17 pixels, then for larger multiplicities follow a symmetric behavior around the

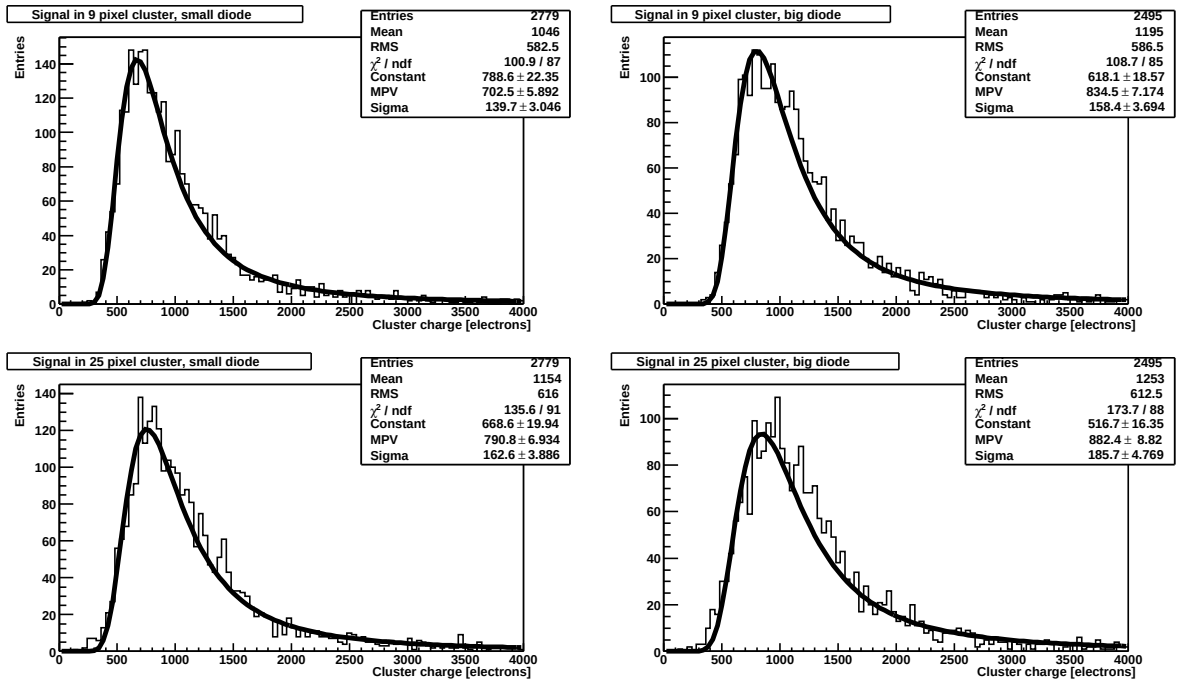

Figure 5.29: Charge collected in 3×3 (top) and 5×5 (bottom) pixel clusters, measured at -10°C on one sub-matrix with small diodes (left) and one sub-matrix with big diodes (right). The corresponding single pixel distributions are shown in Fig. 5.27.

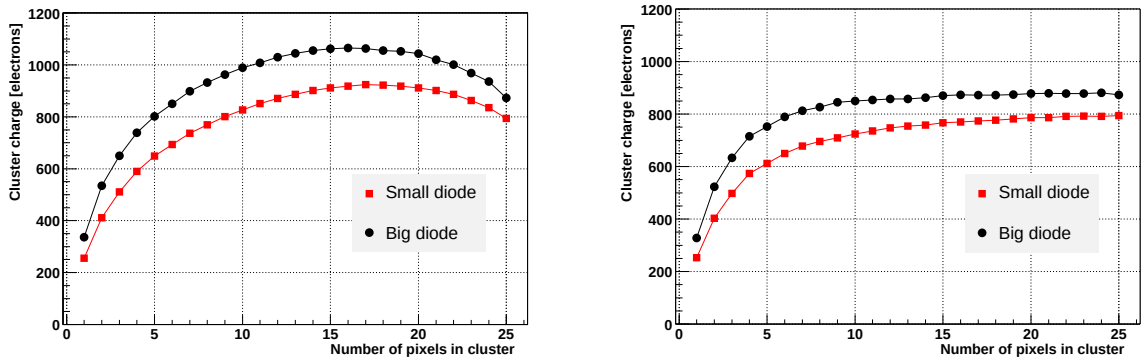

Figure 5.30: Cluster charge as a function of the pixel multiplicity in the cluster, measured at -10°C for big diodes and small diodes. The left plot results from the procedure of sorting the pixels according to decreasing pulse height, the right plot from sorting the pixels according to increasing distance from the hit position (see text).

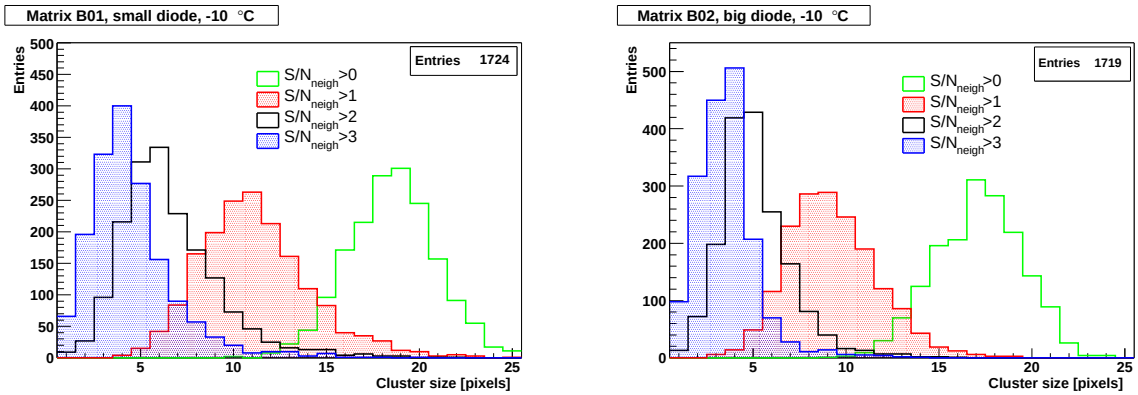

Figure 5.31: Cluster size distribution as a function of the cut applied on the S/N of the individual neighboring pixels. The left plot refers to a sub-matrix with small diodes, the right one to a sub-matrix with small diodes.

maximum decreasing towards values close to the ones obtained for 9 pixels and 6-7 pixels, for small and big diodes respectively. This indicates the presence of fluctuations at the borders of the 5×5 cluster, the positive signals entering in the sum first, the negative ones only later. The influence of these fluctuations is not present when ordering the pixels according to their distance from the hit position, as shown in the right plot of the same figure: the curves, after the initial increase, now start to saturate for pixel multiplicities larger than 9-10. The charge corresponding to the final plateau is an estimation of the total charge collected in the 25 pixel clusters, of ∼800 and 900 electrons for small and big diodes respectively. A smaller cluster size for big diodes is also evident from the earlier saturation of the corresponding curve.

The smaller cluster size associated with big diodes is also confirmed by the two plots in Fig. 5.31, which show the cluster size distributions as a function of the cut applied on the individual S/N of the 25 pixels (other than the seed pixel), for small diodes on the left and for big diodes on the right part. At equal cuts, the average cluster size is found to be typically 1-2 pixels larger for small diodes, a clear difference not being visible for the highest S/N cut of 3, when only a very few pixels are selected.

5.5.3 Comparison with simulation

The results obtained from test-beam measurements can be compared with the simulations presented in Sect. 4.2.2. The comparison is nevertheless not straightforward, since the simulations considered only hits through the center of the hit pixel, while in general the charge spreading between neighboring pixels, and therefore the fraction of charge collected in each individual pixel, depends on the particular impact position within the hit pixel. Hits at or closer to the center of the seed pixel result in a higher charge collected by it and smaller charge in the neighboring pixels. This is visible in the top-left part of Fig. 5.32, which shows the charge collected in the seed pixel versus the distance of the hit position, reconstructed with the center of gravity algorithm, from the center of the pixel, in the case of small diodes. It's clear that lower signals

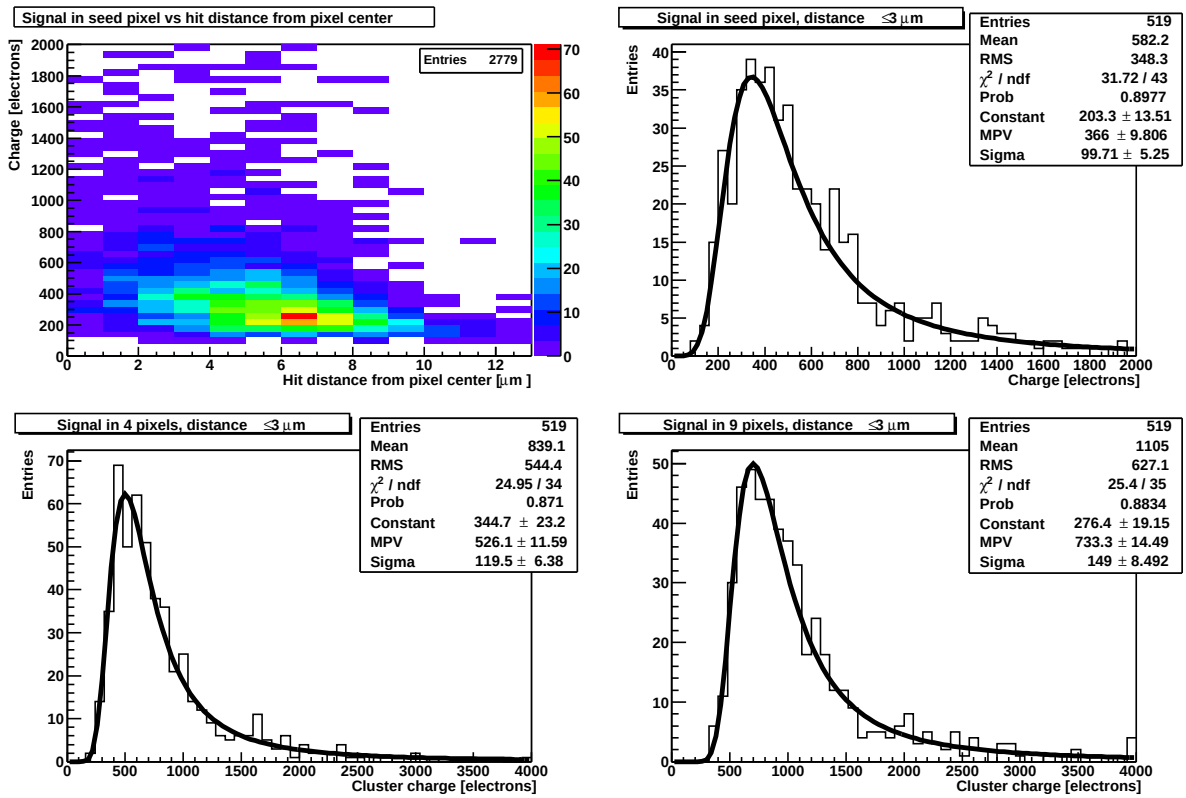

Figure 5.32: Correlation between charge collected in the hit pixel and distance of the hit position from the pixel center (top-left), and signal distributions in 1, 4 and 9 pixels for hits within 3 μm from the pixel center, for small diodes.

are related to hits which are away from the pixel center, while hits closer to the latter are more likely to yield a higher collected charge.

In order to compare the experimental results with the simulations shown in Fig. 4.12, only hits whose position is within 3 μm from the pixel center have been selected. The choice of the distance in this cut is a compromise between the need for a reasonable statistics and the selection of hits as close as possible to the pixel center. The corresponding signal distributions in 1, 4 and 9 pixels extracted from the test-beam data are shown in Fig. 5.32 in the case of small diodes. While a 9 pixel cluster is uniquely defined around the seed pixel, the charge in 4 pixels is estimated for every hit as the average of the charge collected in the 4 possible 2×2 pixel clusters around the seed pixel. The distributions can be fitted with a Landau function, and the most probable values estimated from the fit can be compared with the simulated ones, as in Table 5.3, which reports also the corresponding results obtained in the case of big diodes.

The agreement between measurements and simulations is quite good in both cases of 2×2 and 3×3 pixel clusters, the differences being within 6%; nevertheless, a different trend is evident between the two cases, i.e. the simulations tend to overestimate the measured signals in the

Cluster size (pixels)	Cluster charge Small diodes, sim. (electrons)	Cluster charge Small diodes, meas. (electrons)	Cluster charge Big diodes, sim. (electrons)	Cluster charge Big diodes, meas. (electrons)
1	434	366	494	476
2×2	559	526	616	637
3×3	740	733	786	832

Table 5.3: Comparison between simulated and measured values of charge in 1, 4 and 9 pixels. The measured values correspond to the most probable values of the signal distributions for hits within 3 μm from the pixel center.

small diode case, to underestimate them in the big diode case. The agreement between the values for 1 pixel is within 16% in the small diode case, and within 4% for big diodes. A significant difference between simulations and measurements was expected for the hit pixel due the approximation of comparing measured hits within a certain distance from the pixel center with simulated hits exactly in the pixel center. Hence, the value extracted from experimental measurements underestimates the ideal case. On the other side, uncertainties in the simulations are introduced by the limited knowledge of technological details, like material properties and doping profiles, and by the limited precision of the physical models used, as remarked also in [DepTh].

5.5.4 Detection efficiency

The detection efficiency ϵ is defined as the ratio between the number of good tracks from the reference telescope associated with a hit reconstructed on the MIMOSA sensor and the total number of good tracks which predict a hit inside the acceptance of the pixel detector, i.e. inside the projection of the trigger area on the MAPS active area.

The detection efficiency is found to be dependent on the S/N cuts applied in the cluster definition and on the maximum allowed track-to-hit distance, i.e. the interval around the predicted impact position from the reference track in which a corresponding hit on the pixel sensor is searched. A typical hit-track distance distribution for correlated hits is shown in Fig. 5.33. It can be seen that most hits are found within $\sim$50 μm from the predicted position. Nevertheless, the distribution has quite a long tail, extending up to $\sim$100 μm, and in some cases correlated hits can be found also beyond. This is due to the effect of multiple scattering on the particle track, which deviates from a straight line; in the presence of strong scattering, this can result in reconstructed tracks whose prediction on the pixel sensor is far away from the real hit position.

Fig. 5.34 shows the measured detection efficiency as a function of the cut applied on the S/N of the seed pixel of the hit clusters and for different values of the maximum track-to-hit distance. The plot refers to measurements performed on a matrix with big diodes, a similar behavior is also found in the small diode case. The statistical error associated with each experimental point

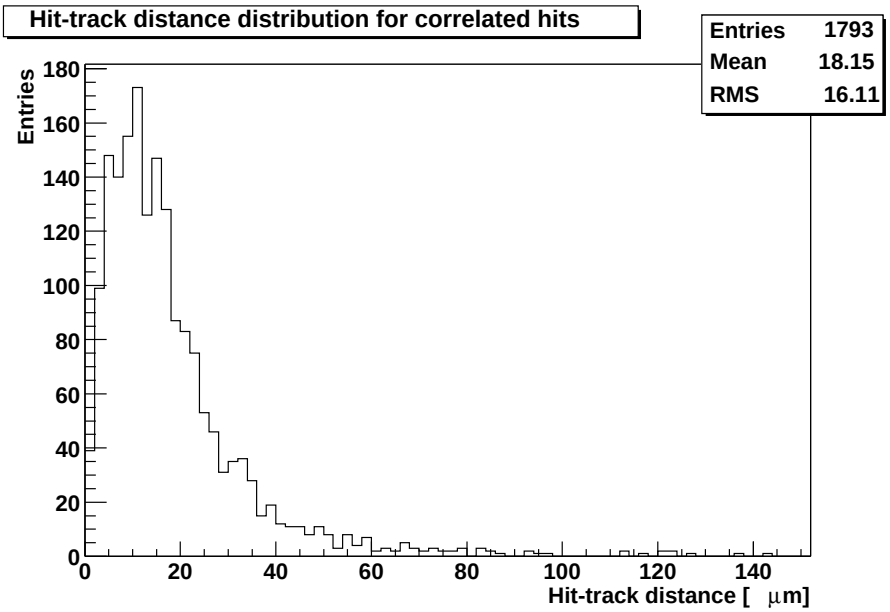

Figure 5.33: Example hit-to-track distance distribution. The hit-to-track distance is calculated as the distance between the position (x_{pred}, y_{pred}) predicted by the reference track and the closest hit position (x_{hit}, y_{hit}) reconstructed on the pixel sensor.

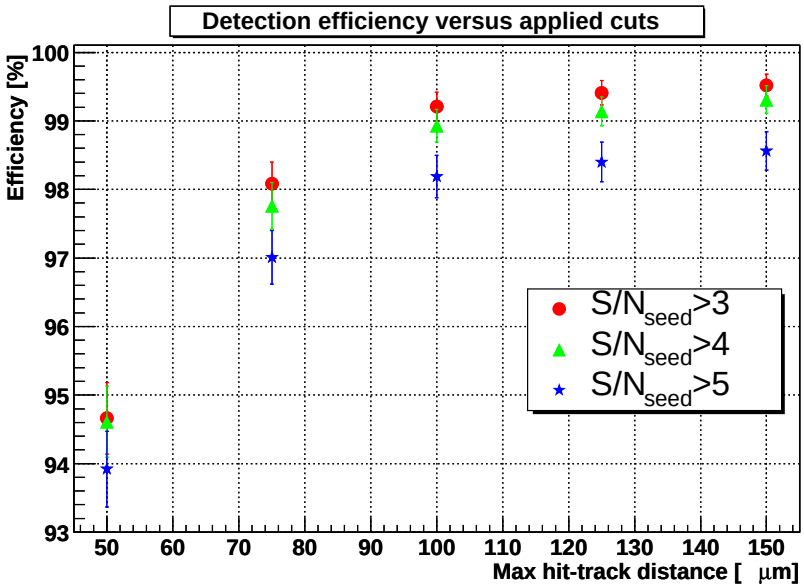

Figure 5.34: Detection efficiency as a function of the cuts applied on the maximum allowed hit-to-track distance and on the seed pixel signal-to-noise ratio.

is calculated from the formula for the variance of a binomial distribution as

$$\sigma_\epsilon = \sqrt{\frac{\epsilon(1-\epsilon)}{N}} \tag{5.30}$$

where N is the number of good telescope events predicting inside the MAPS acceptance. It can be seen that detection efficiencies of ∼99% can be achieved by allowing a maximum hit-track distance of 100 μm and by applying a cut of 3 or 4 on the S/N of the seed pixel. The efficiency is also found to increase slightly by enlarging the correlation interval up to 150 μm. On the other side, decreasing the allowed distance to 50 μm results in an efficiency decrease of several %, while the increase of the S/N cut to 5 generally gives a moderate decrease within 1%.

In practice, a cut of 3 on the S/N of the seed pixel introduces a difficulty in the data analysis, since it increases the probability of including background or noise fluctuations as potential hits, giving the so-called fake hits. At the same time, a large correlation interval results in a higher probability of correlating with a fake hit, especially if the pixel occupancy is high. Nevertheless, in the typical conditions described here, the pixel occupancy was always below 0.1%, so that the probability of correlating with a fake hit was very small even in the largest allowed interval of 150 μm. Moreover, noisy pixels or fluctuations are in most cases prevented from entering in the correlation procedure by the selection of clusters performed earlier in the analysis by applying a cut on the S/N or on the charge of the neighboring pixels (Sect. 5.3).

5.5.5 Position resolution

As mentioned above, the effect of multiple Coulomb scattering on the position resolution cannot be neglected at the beam energies here considered. The projected angular spread $\Delta\theta_{\mathrm{ms}}$ due to multiple Coulomb scattering along the particle direction can be written (in mrad) as:

$$\Delta\theta_{\mathrm{ms}} \approx \frac{13.6\mathrm{MeV}}{\beta cp\,[\mathrm{GeV/c}]} \cdot \sqrt{\frac{\Delta x}{X_0}} \cdot \left[1 + 0.038 \ln\left(\frac{\Delta x}{X_0}\right)\right] \tag{5.31}$$

where p and βc are the momentum and velocity of the incident particle, and $\Delta x/X_0$ is the thickness of the scattering medium in radiation lengths. This expression comes from a Gaussian approximation which does not account for the effect of large multiple scattering, which is described by the Molière theory [PDG04]. As a first approximation, the extrapolation error on the MAPS sensor due to multiple scattering can be estimated by taking into account the material introduced on the particle path by the sensor, the PCB board on which it is mounted, the aluminum foil used for shielding and the insulating box used for cooling. This amounts to a total $\Delta x/X_0$ of 0.016, which introduces for 6 GeV electrons a $\Delta\theta_{\mathrm{ms}}$ of 0.24 mrad; the track reconstructed by the first two telescope planes will consequently have an extrapolation error of ∼12 μm at the position of the pixel sensor.[14] This value is indeed reflected in the typical measured residual distributions with a width between 10 and 12 μm at 6 GeV.

[14] The MAPS sensor is positioned at d_1=69.9 mm from the first telescope plane, the second telescope plane at d_2=207.1 mm from the MAPS sensor. The predicted width of the residual distribution at the position of the MAPS sensor is obtained by multiplying $\Delta\theta_{\mathrm{ms}}$ by $\frac{d_1 \cdot d_2}{d_1 + d_2}$.

The major multiple scattering contribution is estimated to come from the material of the PCB board on which the pixel sensor is mounted. Nevertheless, as can be seen in Fig. 5.8 from the back view of the board, a circular hole of around 1 cm diameter is present, centered on the chip.[15] In order to determine the best possible position resolution, events on which the influence of multiple scattering is minimized have been selected by performing the following analysis:

- only the first two telescope planes were considered in the track fitting, the MAPS prototype being in-between, requiring the presence of a corresponding hit in the third telescope plane as a check of the event quality;
- a cut on the slope of the telescope tracks was applied in order to select tracks as parallel as possible to the Z (beam) direction; this was done in order to exclude events in which the position measurement on the second telescope plane is affected by strong multiple scattering, leading to predicted positions on the pixel sensor which are far away from the real ones;
- a cut on the the total cluster charge (in 9 pixels) was applied on the MIMOSA hits, in order to exclude events which are in the tail of the energy loss distribution, e.g. due to δ-rays; typically, only hits with $Q_{3\times3} < 1.7 \cdot Q_{3\times3,\mathrm{MPV}}$ were considered, where $Q_{3\times3,\mathrm{MPV}}$ is the most probable value in the energy loss distribution for 9 pixels;
- only MIMOSA hits reconstructed in the geometrical region corresponding to the hole in the PCB board were selected.

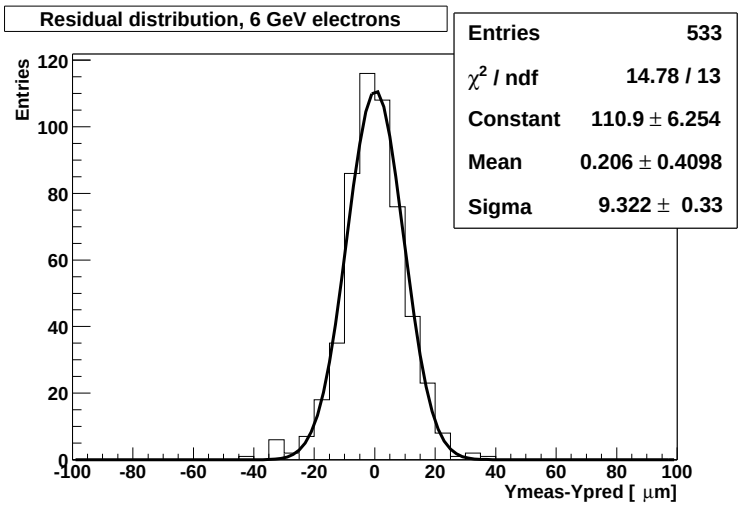

Figure 5.35: Residual distribution at 6 GeV for one coordinate, for events selected to minimize multiple scattering effects as explained in the text.

[15] The hole was originally introduced in the board design in order to perform laser injection tests.

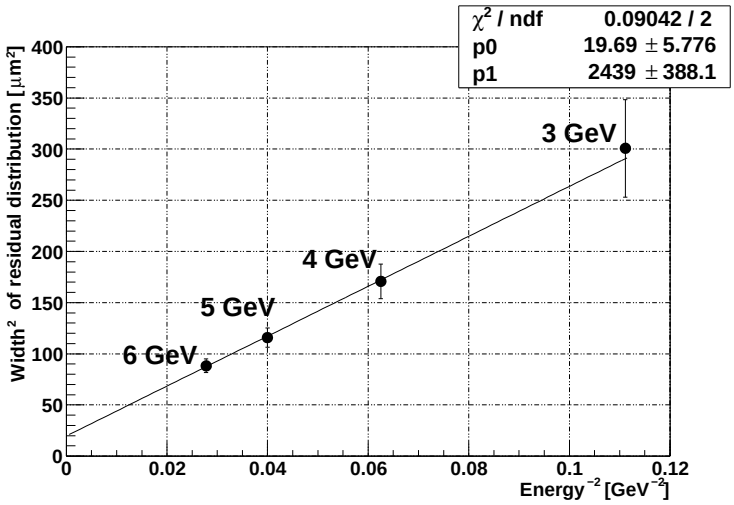

Figure 5.36: Squared width of the residual distribution as a function of the inverse squared electron energy, for events selected to minimize multiple scattering effects.

The application of all these consecutive cuts resulted in a very low final statistics, typically of a few hundred events starting from the initial 5000-6000 events in the run. An example of the obtained residual distribution at 6 GeV for one coordinate is shown in Fig. 5.35. The measured position resolution can be estimated from the sigma σ_{res} of the Gaussian fit, and is the convolution of several contributions:

$$\sigma_{\text{res}} = \sqrt{\sigma^2_{\text{intr,MAPS}} + k_1 \cdot \sigma^2_{\text{intr,TEL}} + k_2 \cdot \Delta\theta^2_{\text{ms,MAPS}}} \tag{5.32}$$

where $\sigma_{\text{intr,MAPS}}$ and $\sigma_{\text{intr,TEL}}$ are the intrinsic resolutions of the MAPS sensor and of the telescope modules, respectively, $\Delta\theta_{\text{ms,MAPS}}$ is the extrapolation error due to multiple scattering effects on the material layers at the position of the pixel sensor, expressed by Eq. 5.31, and k_1, k_2 are geometrical factors which depend on the relative distances between the telescope planes and the MAPS prototype.[16]

The above described procedure was repeated for a set of measurements with different beam energies, from 3 GeV to 6 GeV. It can be seen from Eqs. 5.32 and 5.31 that the squared width of the residual distribution depends linearly on the inverse squared electron energy. By performing a linear fit of the points measured at different energies, as shown in Fig. 5.36, it is possible to estimate the intrinsic position resolution of the MAPS sensor by extrapolating to infinite momentum, i.e. no multiple scattering effects. From the intercept of the linear fit, after correcting for the intrinsic resolution $\sigma_{\text{intr,TEL}}$=(2.8±0.1) μm of the reference telescope [MorTh], this gives for the intrinsic resolution of the MAPS sensor $\sigma_{\text{intr,MAPS}}$=(3.85±0.75) μm. This result can not be considered a precise measurement of the detector position resolution; indeed,

[16] It can be shown [MorTh] that $k_1 = \frac{d_1^2+d_2^2}{d_3^2}$ and $k_2 = \frac{d_1^2 \cdot d_2^2}{d_3^2}$, where d_1 is the distance of the MAPS sensor from the first telescope plane, d_2 the distance of the second telescope plane from the MAPS sensor, and d_3=$d_1 + d_2$.

the precision of the analysis is affected by the low statistics involved, with correspondingly large errors associated with the experimental points and low probability of the linear fit (see Fig. 5.36), besides several approximations introduced. Nevertheless, the result gives a qualitative indication of the high position resolution, of only a few μm, of these sensors. A precise measurement of (1.7±0.1) μm, obtained after beam-tests with high-momentum particles (∼100 GeV/c pions), for which multiple scattering effects are negligible, can be found in [Dep03].

5.6 Irradiation with low-energy electrons

5.6.1 Electron irradiation facility

One prototype MIMOSA-5 chip has been irradiated at the S-DALINAC facility of Darmstadt Technical University (Darmstadt, Germany) [DarLI], in order to test its radiation tolerance against low-energy (∼10 MeV) electrons. As explained in Chapter 1, such electrons are expected to play an important role in the radiation background in the first layers of the vertex detector at the ILC.

The S-DALINAC is a superconducting linear electron accelerator, reaching energies up to 130 MeV, used mainly for experiments in nuclear, radiation and accelerator physics. A ∼10 MeV electron beam can be extracted from the injector Linac, before injection in the main Linac, and sent to a test location for irradiation experiments. The MIMOSA-5 chip with its front-end board was mounted on a plastic holder facing directly the extracted beam, whose spot had a diameter of ∼6 mm and could be centered on one sub-matrix at a time (the size of one MIMOSA-5 sub-matrix is about 8.7×8.7 mm^2). During irradiation, the chip was kept biased and operated in a cyclic readout mode, without actual data storage on disk, in order to simulate real operational conditions with the presence of the digital control signals. The electron energy was tuned to 9.4 MeV, and the delivered fluences were estimated by integration of the beam current (of the order of ∼1 nA), measured by means of a Faraday cup mounted behind the chip front-end board. Two average fluences of ∼3·10^{12} and ∼1·10^{13} e/cm^2, roughly equivalent to 0.7 and 2.3 kGy, respectively, were delivered to two different sub-matrices of the chip; the highest fluence corresponds to the one expected in the innermost layer of the ILC vertex detector after 5 years of operation [Win05]. The irradiation was performed at room temperature and after irradiation the chip was also stored at room temperature.

5.6.2 Prototype performance after irradiation

After irradiation the chip was operable only by cooling it to temperatures of about -10°C. A strong increase was indeed observed in the pedestal level, i.e. in the pixel leakage current, leading to a fast saturation of the pixel output in time at temperatures close to room temperature, thus not allowing a proper detector operation. Figure 5.37 shows the average pedestal measured in each pixel at -10°C on the sub-matrix irradiated at the highest fluence: it can be seen that the increase in the pedestal level is stronger in the region in which the delivered fluence is higher, i.e. in the region in which the beam spot was centered during irradiation, decreasing towards

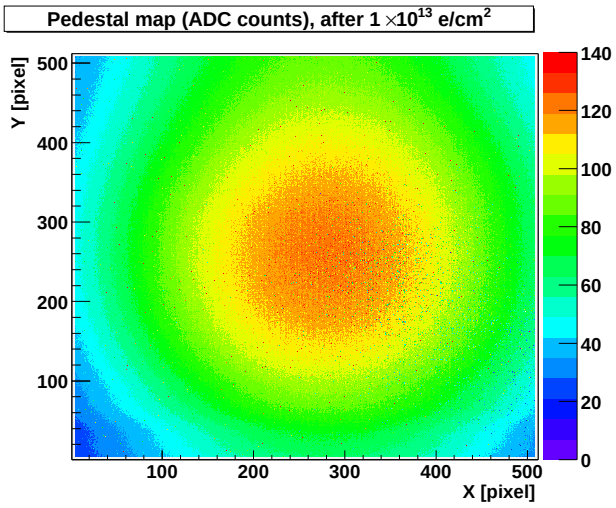

Figure 5.37: Average pedestal measured at -10°C after irradiation with $1{\cdot}10^{13}$ e/cm^2.

the matrix borders consistent with the Gaussian profile of the beam. Hence, the intensity of the damage is clearly not uniform over the detector surface. A direct comparison of the pedestal increase with the electron fluence is nevertheless not straightforward, due to the fact that both volume generated currents and surface currents can contribute to the pedestal level.

Correspondingly, an non-uniform increase of the pixel noise over the detector area was observed. Figure 5.38 shows the profile plots of the pixel noise as a function of the pedestal level, for the two matrices. From the comparison of the two plots, the same trend is visible for the two irradiations, with a non-linear increase of the noise as a function of the increasing pedestal with respect to the pre-irradiation values (of 27 and 26 electrons for matrix B02 and T02, respectively, see Table 5.2) up to values of ∼45 electrons for the lower fluence and of ∼54 electrons for the higher fluence.

Despite the loss in noise performance, at the fixed cooling temperature of -10°C, pedestals were found to be reproducible in time, and measurements with a ^{55}Fe radioactive source (see Sect. 5.4.2) could be performed. The result is shown in Fig. 5.39, which shows for the two matrices the single pixel signal distributions obtained after irradiation in comparison with the corresponding ones before irradiation. In both cases a slight shift in the position of the 5.9 keV peak is visible, indicating charge losses. The larger widths of the peaks have to be related to the increased pixel-to-pixel dispersion due to the non-uniformity of the damage in the matrices. The secondary peaks, corresponding to 6.49 keV photons, are also shifted after irradiation and appear convoluted with the first ones. All the observed effects are more significant at the higher fluence.

The degradation in the chip performances after irradiation can be interpreted as a combination of radiation-induced damage in the electronics on the chip surface, and of bulk damage in the detector sensitive volume. Threshold voltage shifts in the pixel transistors due to oxide

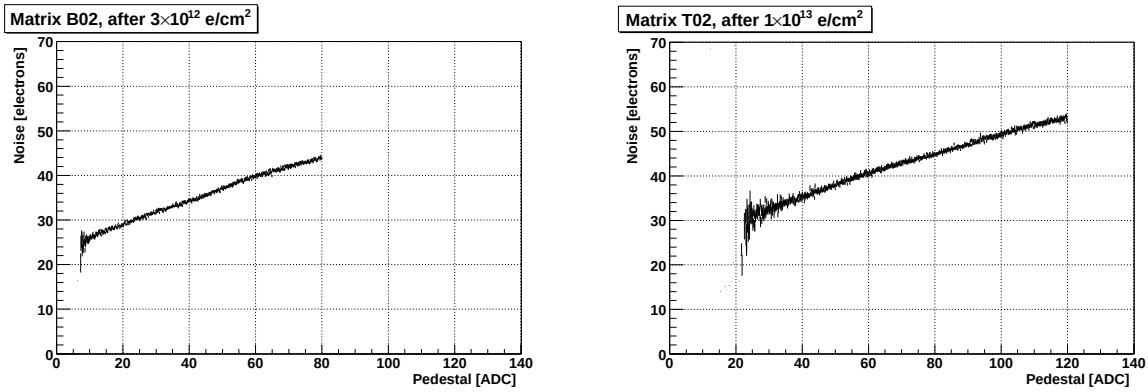

Figure 5.38: Profile plots of noise versus pedestal level measured at -10°C after irradiation with 9.4 MeV electrons. Matrix B02 has been irradiated with $3{\cdot}10^{12}$ e/cm^2 (left), matrix T02 with $1{\cdot}10^{13}$ e/cm^2 (right). The same scales are used in both plots for easier comparison. The average pedestal at -10°C before irradiation was of 3.3 ADC for matrix B02 and 2.6 ADC for matrix T02.

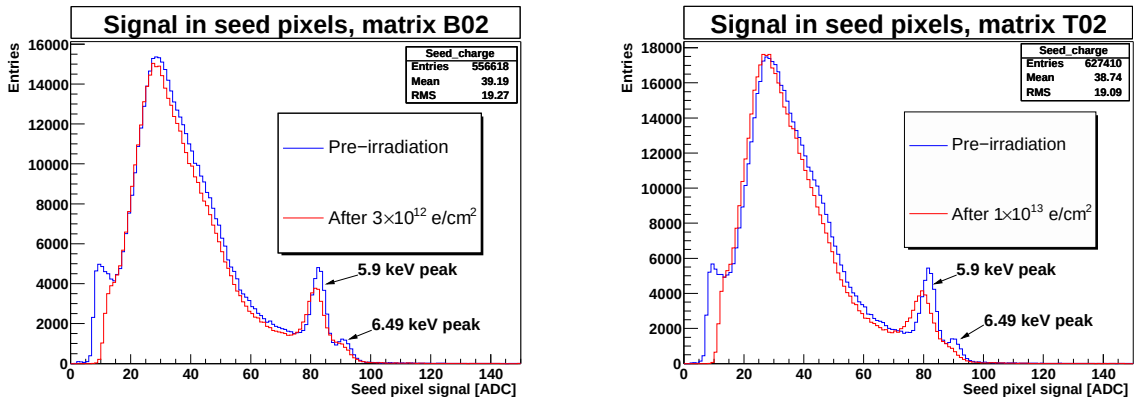

Figure 5.39: Single pixel spectra in the two irradiated sub-matrices after measurements with low-energy X-rays from a ^{55}Fe source, performed at -10°C. The left plot refers to the matrix irradiated with $3{\cdot}10^{12}$ e/cm^2, the right plot to the matrix irradiated with $1{\cdot}10^{13}$ e/cm^2. The corresponding distributions obtained before irradiation are also shown for comparison.

charge (see Sect. 2.3) may result in an inefficient readout at the pixel level; moreover, the degradation in the transconductance of the source follower transistor, related to the reduction of the channel mobility due to trapping levels at the silicon/oxide interface, results in a reduction of the output signal. On the other side, radiation-induced defect levels in the epitaxial layer or at the interfaces, especially around the charge collecting diodes, besides contributing to the strong increase in the dark current, can lead to charge losses due to trapping of the diffusing charges.

So far it was not possible to operate the irradiated chip in a beam-test experiment, since the event rate achievable with the present setup (between 0.5 and 1 Hz, see Sect. 5.2.2) is not high enough to guarantee a frequent reset operation and therefore avoid the saturation of the pixel output. Calibration measurements were indeed possible since a continuous, non-triggered readout mode was used, resulting in events acquired with a constant rate of $\sim$1.5 Hz. In any case, the significant increase in the pixel noise and the charge losses observed from the calibration measurements hint at a much reduced S/N performance, and ultimately a considerable loss of detection performance should be expected.

5.7 Summary of MAPS tests

This chapter has presented the experimental results obtained from the test of one Monolithic Active Pixel Sensor (MAPS) prototype, the MIMOSA-5 chip developed by the IReS/LEPSI institutes in Strasbourg. This sensor, which features $\sim$1 million pixels of 17 μm pitch distributed over a reticle size area of 3.5 cm^2, represents so far the only attempt at the fabrication of a large size CMOS sensor for particle tracking applications, and was mainly intended at the test of the reproducibility of the excellent detection performances obtained with the other, smaller prototypes of the same family. A dedicated experimental setup has been built at DESY in order to provide a contribution in this direction.

Calibration measurements have shown a significant dependence of the pedestal levels, which resemble the pixel leakage currents, on the operational temperature, pointing to the need of cooling the detector in order to keep the leakage current and the noise at a low level. Good performances could be reproduced in a wide temperature range, between -10°C and +10°C, requiring only moderate cooling. Measurements with low-energy X-rays from a ^{55}Fe source allowed the calibration of the sensor charge-to-voltage conversion gain, and ultimately the conversion of measured signals into absolute units of charge.

The sensor detection capabilities have been then extensively tested by exposing it to a 6 GeV electron beam at the DESY-II facility. Experimental results have shown that signals of 800-900 electrons are collected mostly within 3×3 pixel clusters, with noise figures of 20-25 electrons at the pixel level depending on the size of the charge collecting diode. In general, a larger size of the charge collecting elements yields a larger signal, but also introduces a larger noise; the resulting S/N performance is similar to the one of a smaller diode. An average S/N of $\sim$20 has been found for hit pixels in both cases, showing only a slight decrease with increasing temperature between -10°C and +10°C.

The size of the charge collecting element has an influence on the typical cluster size: at equal

cuts applied in the cluster selection, smaller clusters are found in matrices implementing bigger diodes, due to the larger area in the pixels below which the presence of an electric field limits the charge spreading.

The comparison of the measured signals with the simulations presented in Chapter 4 showed in general a good agreement, considering the approximations introduced in the simulations, coming on one side from the simulation of tracks passing only through the center of the hit pixel, on the other side from the limited knowledge of the technological details included in the detector modeling.

A detection efficiency of ∼99% has been found by applying cuts on the hit S/N and on the maximum allowed distance between the position predicted by the reference track and the one measured by the pixel sensor. The detector position resolution could not be estimated precisely due to multiple scattering effects which dominate the position measurement at the electron energies considered. An extrapolation of the resolutions measured at different beam energies allowed the rough estimation of an intrinsic position resolution below 4 μm, confirming the high spatial resolution of these detectors.

On the whole, these experimental results confirm the analogous tests performed by the Strasbourg team on the same devices, proving the high potential of this technology for particle tracking applications, since good detection capabilities could be reproduced with a large area sensor, despite the disadvantage of the higher noise, and correspondingly lower S/N.

The irradiation with low-energy (∼10 MeV) electrons caused a considerable degradation in the detector performances, due to a combination of surface effects (i.e. in the pixel transistors and at the interfaces around the charge collecting diodes) and of bulk damage introducing defect levels which limit the charge collection efficiency and contribute to the increase of the dark current. After irradiation, a strong increase in the dark current and in the pixel noise have been observed, and charge losses were detected from measurements with a ^{55}Fe source, together with a general increase of the pixel-to-pixel dispersion of the characteristics, related to the non-uniformity in the fluence delivered over the detector surface. These results confirm the possible impact of such radiation on the operation of CMOS sensors. Nevertheless, it should be kept in mind that the design of the MIMOSA-5 prototype had not been optimized in terms of radiation tolerant layout. As remarked in Sect. 5.1.1, results obtained after the same irradiation of prototypes fabricated in a different technology and with optimized layout, and operating with a much lower charge integration time, are indeed very encouraging [Win05].

Chapter 6

Outlook

6.1 Towards ultra radiation-hard silicon detectors for the SuperLHC

For the outer layers of a SuperLHC inner tracking detector, where particle fluences up to 10^{15} cm^{-2} are expected in 5 years of operation, the major problem is the strong change in the depletion voltage which will affect a large fraction of the detectors; hence, a radiation-hard solution which is also cost effective is required. In particular, if substrate type inversion occurs, the electric field inside the devices will be higher on the non-segmented side of the detector, resulting in a reduction of the charge collection efficiency if detectors are not properly overdepleted and in a slower charge collection due to the fact that mostly holes with respect to electrons are collected by the electrodes. With respect to this, very promising results have been obtained from measurements performed on test structures manufactured on Czochralski and Magnetic Czochralski substrates, which only recently became available with a high enough resistivity to be used as a detector material. No substrate type inversion has been observed in these devices after irradiation with high-energy protons with fluences up to 10^{15} p/cm^2, with variations of the depletion voltage comparable with or smaller than float-zone devices [Mol05]. Another option comes from the use of n-on-p detectors, which do not invert. Charge collection measurements have shown that signals of about 6500 electrons can be collected from a 280 μm thick detector after a fluence of $7.5{\cdot}10^{15}$ p/cm^2. In addition, no reverse annealing effects have been observed even after very long annealing times [Cas04]. Further studies are now under way in order to understand the influence of the oxygen content in p-type silicon, extending these investigations also to p-type Czochralski silicon [Mol05].

For the innermost layers of a SuperLHC detector, the fluences which detectors will have to withstand will be up to 10^{16} cm^{-2} during the 5 years of operation. In these conditions, the main drawback is the significant reduction of the collected signals due to trapping. As shown also in this work, the use of thin, low-resistivity detectors may be a viable option. An optimum thickness should nevertheless be found in order to have a trade-off between material budget, which is important for the precision of the tracking, and the collected signal, which can be quite low for

very thin detectors. From the comparison between n-type epitaxial devices of thicknesses of 25, 50 and 75 μm, a very good performance could be reproduced: no type inversion was observed up to an equivalent fluence of 10^{16} cm^{-2}, with very moderate variations of the depletion voltage, higher for a larger thickness [Lin05]. Charge collection measurements performed with β particles have shown that a signal of 2500 electrons can be obtained from 50 μm devices at SuperLHC fluences [Kra05]. A thicker epitaxial layer would result in a larger signal, nevertheless the production of very thick epilayers may prove technically challenging and a higher depletion voltage would be needed to deplete them. Thin epitaxial layers have also been compared with devices of the same thickness manufactured on n-type float-zone substrates; the latter exhibit a very small depletion voltage, nevertheless undergo type inversion and correspondingly a significant reverse annealing effect after thermal annealing, while epitaxial devices do not invert and even exhibit a positive effect of the reverse annealing [Mol05]. Indeed, it has been shown that this peculiar annealing behavior could be exploited in a real operational scenario at the SuperLHC, resulting in very small depletion voltage variations over the entire 5 years of operations if detectors are kept at room temperature during beam-off periods [Lin05]. Further investigations on thin epitaxial devices are foreseen by considering, besides different thicknesses, different resistivities and possibly also the utilization of p-type silicon.

An important issue to be considered in future investigations on the radiation hardness of silicon detectors is related to electric field profile effects. Recent measurements and corresponding device simulations [Swa03] have shown that the assumption of a uniform doping distribution in silicon devices after irradiation may not be correct, even at low particle fluences. The electric field profile in the substrate of irradiated detectors strongly deviates from linearity, resulting in the so-called double junction effect [Ere02]; it has indeed been shown that a doubly-peaked electric field is necessary to describe the charge collection profiles measured in heavily irradiated pixel sensors [Chi05].

6.2 Towards a CMOS-based vertex detector for the ILC

Monolithic Active Pixel Sensors have been shown to be a very promising candidate for application in the vertex detector at the ILC. A test-bench for this technology will be its planned application in the upgrade of the vertex detector of the STAR experiment at RHIC [Wie01], or at the Belle B-factory [Var05]. Nevertheless, a major R&D effort is still needed in order to fulfill completely the ILC requirements. The major constraints are posed on the innermost layers, which need to be extremely precise and fast, with a minimum amount of material introduced in the detector volume. The main achievements obtained so far and a complete outlook on the prospective R&D needed towards the realization of a CMOS-based vertex detector for the ILC can be found in [Win05], where a design of the detector layers using MAPS is proposed. This geometry is being used in physics simulations of benchmark reactions, in order to optimize the detector design as a function of the needed physics performance [Gra05].

The high granularity needed in the first detector layers can be accomplished by the scaling down of CMOS technology, which will also allow the inclusion of additional functionalities (e.g. Correlated Double Sampling) in each pixel without affecting the pixel size. In the outer layers, a

smaller position resolution is needed with increasing distance from the interaction point, so that pixels can feature a larger pitch, thus decreasing significantly the number of readout channels and therefore the data flux and the power dissipation.

A major issue is the exploration of the fabrication processes that will be actually available at the time in which the real detector will eventually be built; the need is for a technology, most likely taken from the imaging market, with a thick enough epitaxial layer, good quality of the surfaces and enough metal lines for the integration of complex readout electronics on the chip. Very promising results have been obtained on MIMOSA prototypes fabricated in a technology without epitaxial layer (e.g. the MIMOSA-4 prototype, see Table 5.1), so this option will also be considered in the future.

A fast, column-parallel readout architecture is foreseen in the first layers of the vertex detector, with digitization and discrimination electronics placed at the edge of the ladders. Several prototypes have been fabricated implementing a column-parallel readout; in particular, preliminary results obtained with the MIMOSA-8 prototype (see Table 5.1) are very promising. In the outer layers, where the background is much lower and therefore puts less severe constraints on the readout speed, the idea is to exploit the foreseen ILC duty cycle, i.e. storing inside the pixel different readouts performed during the 1 ms bunch train, and then reading out the signals during the following 199 ms in which the beam is not present. This can be accomplished with an approach similar to the one proposed by Flexible Active Pixel Sensors (FAPS), in which several memory cells (i.e. capacitors) are included in each pixel in order to store consecutive signals [Tur03]. A new prototype (MIMOSA-12) has been recently fabricated implementing 4 capacitors in every pixel; the goal is to implement as much capacitors as possible in one pixel, keeping at the same time a reasonable pitch.

Further investigations are needed in the assurance of the sensor radiation tolerance, in particular against low-energy electrons, which constitute the primary background in the detector volume, especially in the first layer. Preliminary results obtained on the MIMOSA-9 prototype (see Table 5.1) are very encouraging; when compared to the ones obtained in this work on MIMOSA-5, they also indicate that a good recipe against radiation damage is, beside a dedicated design in a radiation-tolerant layout, a proper cooling of the detector and a short integration time.

Significant developments are needed on engineering issues, which are driven by the requirement of a very low material budget. A thickness between 25 and 50 μm is aimed for the detector ladders, and the assessment of MIMOSA-5 prototypes thinned down to 50 μm is under way. In parallel, mechanical support structures should be very light, and as little material as possible should be introduced by the cooling apparatus. A proposed approach [Hau03] is to use evaporative cooling of C_3F_8 through very thin capillaries which pass underneath the edges of the detector ladders, where the readout electronics will be placed and thus most of the power dissipation will be present. An idea to reduce the power dissipation is to exploit the ILC duty cycle and switch detectors on soon before the occurrence of the bunch train and off soon after; power pulsing tests with MIMOSA-5 are under preparation in order to verify the feasibility of such an approach [Koe05].

A main concern in the vertex detector community is arising from the possibility of beam-

induced electromagnetic interference effects, which would affect every device in which charge is converted to voltage and therefore also MAPS. Tests of operation of MIMOSA-5 prototypes close to the Linac of the TESLA Test Facility (TTF) at DESY are also in preparation [Koe05].

Chapter 7

Summary and Conclusions

This thesis presents a number of contributions to the research and development on silicon sensors for application as tracking detectors at future particle colliders. On one side, for operation in high-rate environments such as in the innermost tracking layers of experiments at the LHC and at its proposed luminosity upgrade (the SuperLHC), radiation tolerance, speed and segmentation are the main challenges. On the other side, precise measurements such as those planned at the International Linear Collider (ILC) put severe constraints on the spatial resolution and material budget of the silicon vertex detector, thus requiring a new generation of thin and highly granular detectors. The contributions to the related R&D programs presented in this work have addressed the characterization of different silicon materials after irradiation, the simulation of charge collection in thin silicon pixel detectors, with collection mechanisms based on the drift or on the thermal diffusion of the generated charge, and the test of a prototype Monolithic Active Pixel Sensor (MAPS) developed for application as vertex detector at the ILC.

Material characterization after high-energy electron irradiation

Radiation hardness studies on silicon pad detectors manufactured on different substrates have been performed after irradiation with 900 MeV electrons up to a fluence of $6.1 \cdot 10^{15}$ e/cm^2. Experimental results on the variation of the effective dopant concentration N_{eff}, i.e. of the detector full depletion voltage as a function of the electron fluence, have confirmed the effectiveness of high-energy electrons in creating bulk damage in silicon. This is evident in the substrate type inversion observed in float-zone devices, in which a slightly beneficial effect of oxygenation is present.

A different behavior was shown by devices manufactured on epitaxial and Czochralski silicon, which are relatively new materials as far as detector application is concerned. In agreement with results obtained after irradiation with high-energy hadrons, type inversion was not observed in these substrates. Significantly smaller variations of N_{eff}, compared to high-resistivity float-zone devices, were also observed as a function of the thermal annealing time. This is related to the higher initial doping and the high oxygen concentration of these substrates. In particular, the advantage of combining a higher initial doping concentration with a reduced substrate thickness

is highlighted by epitaxial devices (of 50 μm thickness instead of 300 μm like all other devices studied), resulting in very small depletion voltage variations with irradiation. At the microscopic level, this can be explained with the generation of oxygen-related donor centers during irradiation which compensate the radiation-induced introduction of acceptor levels.

Only a slight degradation of the charge collection efficiency after irradiation has been observed for all devices. The measured increase of the leakage current as a function of the electron fluence was, as expected, independent of the specific material. The estimated hardness factor of 900 MeV electrons with respect to 1 MeV neutrons is 4 times smaller than the one predicted by the NIEL scaling hypothesis, hinting at a more pronounced introduction of point defects with respect to cluster formation in the silicon bulk. A predominance of electron trapping with respect to hole trapping is apparent from the measurement of the corresponding effective trapping probabilities, in contrast with what was reported after hadron irradiation: further investigations are needed in order to understand if this may have an explanation at the microscopic level.

Simulation of thin pixel detectors

The main impact of irradiation on the charge collection properties of silicon detectors is the trapping of the drifting charge which leads to charge losses. In order to cope with high fluence levels, such as those expected at the SuperLHC, an option in the detector design is the reduction of its thickness. A smaller thickness results in a faster charge collection, at the price of smaller collected signals. The simulation of high-resistivity, reverse-biased silicon pixel detectors with different thicknesses $\leq$100 μm has shown that signals of 1000-2000 electrons can be expected after irradiation at an equivalent fluence of 10^{16} cm^{-2}. Such signals may still be enough for proper detector operation, provided that radiation resistant, low-noise readout electronics is available.

Among the technologies proposed for vertexing at the ILC, Monolithic Active Pixel Sensors (MAPS) are a very promising candidate, due to their high granularity and thin sensitive volume, and to the possibility of integrating the detecting element and the signal processing electronics on the same substrate. The detector principle of operation is based on the diffusion of the generated charge in the field-free epitaxial layer rather than on drift. Nevertheless, device simulations have shown that an efficient charge collection can be reached, for example in less than 100 ns for an epitaxial layer of 15 μm thickness, yielding charge signals of close to 1000 electrons spread over several pixels. Such signals result in a good signal-to-noise performance, due to the intrinsically low noise of this technology.

The collected signal, the charge collection time and the charge spreading over neighboring pixels depend, for a fixed pixel pitch, on the thickness of the epitaxial layer: the choice of a fabrication process should then aim at an epilayer thickness which provides a reasonable signal combined with a moderate charge spread, in order to preserve a good spatial resolution.

The simulations have also addressed the possible limitations of this technology coming from the use of deep-submicron ($\leq$0.25 μm) fabrication processes, resulting in a decreased thickness of the sensitive volume and therefore in very small collected signals. Additionally, the presence of isolation structures, which in some cases are introduced by this technologies around the

charge collecting elements, is potentially dangerous for the sensor radiation tolerance, due to the possible trapping of charge by radiation-induced defects at the silicon/oxide interfaces.

Test of Monolithic Active Pixel Sensors

A reticle size MAPS prototype, the MIMOSA-5 chip, featuring ∼1 million pixels of 17 μm pitch on an area of 3.5 cm^2, has been extensively tested in a dedicated experimental setup, first with a radioactive source for the calibration of the detector charge-to-voltage conversion gain, then in a series of beam-tests performed with 6 GeV electrons and with a high-resolution silicon reference telescope for the reconstruction of the particle tracks.

Experimental results have shown the good detection capabilities of this technology. Signals of 800-900 electrons are collected within 9 pixel clusters, with a single pixel noise of 20-25 electrons depending on the size of the charge collecting diode: indeed, a larger charge collecting element yields a larger signal, but also a larger noise. An average S/N of ∼20 has been found in both cases. The good noise and signal-to-noise performance could be reproduced in a temperature range between -10°C and 10°C, requiring only moderate cooling. A good agreement between the measured signals and the prediction from simulations was also found. High detection efficiencies in excess of 99% were obtained, significantly dependent on the distance from the impact position predicted by the reference telescope into which the corresponding hit measured on the pixel sensor is searched for; this is due to the effect of multiple scattering which, at the energies considered, dominates the position measurement, thus making impossible to measure precisely the detector position resolution; the latter could nevertheless be estimated of a few μm only from an extrapolation of measurements performed at different beam energies.

A significant degradation of the detector performance has been observed after irradiation with ∼10 MeV electrons at fluences comparable to those expected in the inner layer of the vertex detector at the ILC; this result, which could be expected considering that the detector had not been designed with a radiation tolerant layout, confirms the impact of such radiation on CMOS sensors, and points to the need for further investigations in this direction.

Appendix A

Constants and Silicon Properties

Quantity	Symbol	value
Boltzmann constant	k_B	$1.3806505(24)\cdot10^{-23}$ J/K
Planck constant	h	$6.6260693(11)\cdot10^{-34}$ Js
Elementary charge	q_0	$1.60217653(14)\cdot10^{-19}$ C
Electron mass	m_e	$9.1093826(16)\cdot10^{-31}$ kg
Permittivity in vacuum	ϵ_0	$8.854187817\cdot10^{-12}$ F/m
Speed of light in vacuum	c	$2.99792458\cdot10^{8}$ m/s

Table A.1: Fundamental constants (from [NIST]).

Quantity	Symbol	value
Atomic number	Z	14
Atomic mass	A	28.09
Density	δ	2.33 g/cm^{-3}
Dielectric constant	ϵ	11.9
Energy gap	E_g	1.12 eV
Intrinsic carrier concentration	n_i	$1.08\cdot10^{10}$ cm^{-3}
Electron mobility	μ_e	1430 cm^2/Vs
Hole mobility	μ_h	480 cm^2/Vs
Effective density of states in conduction band	N_C	$2.86\cdot10^{19}$ cm^{-3}
Effective density of states in valence band	N_V	$3.10\cdot10^{19}$ cm^{-3}
Effective mass for electrons	m_e^*	1.09 m_e
Effective mass for holes	m_h^*	1.15 m_e

Table A.2: Silicon properties. The values for temperature dependent quantities refer to T=300 K (from [Gre90]).

Appendix B

Derivation of the Ramo Theorem

The Ramo Theorem of the induced current (Sect. 2.5.3) can be derived from the Reciprocity Theorem of the induced charge, which defines the relation of the potential and charges on a multi-electrode system for two different states. The derivation proposed in [KraTh] is here illustrated. If V_n, Q_n and V'_n, Q'_n denote the potential of one electrode before and after the change of state, respectively, then the Reciprocity Theorem can be written:

$$\sum_{electrodes} Q'_n V_n = \sum_{electrodes} Q_n V'_n. \tag{B.1}$$

Let us consider a two-electrode system with all the others at a fixed potential ($V_n = V'_n = 0$), and consider two states (Fig. B.1a):

- in the first state an external voltage V_1 is applied to the first electrode and the charge Q_2 is induced on the second electrode: $Q_1, V_1 \neq 0$, $Q_2, V_2 = 0$;
- in the second state an external voltage V'_2 is applied to the second electrode and the charge Q'_1 is induced on the first electrode: $Q'_1, V'_1 = 0$, $Q'_2, V'_2 \neq 0$.

It then follows from Eq. B.1 that $V_1 Q'_1 = V'_2 Q_2$ and therefore

$$C_{12} = C_{21} = \left(\frac{Q_2}{V_1}\right)_{V_{2,3,4,}=0} = \left(\frac{Q'_1}{V'_2}\right)_{V_{1,3,4,}=0}. \tag{B.2}$$

The Reciprocity Theorem in this case describes the simple fact that the mutual capacitance C_{nk} between any two electrodes n, k is independent of the direction in which it is measured.

A drifting charge q can also be seen as a small electrode at point m (see Fig. B.1b). In the actual operational state of the detector, with all the electrodes except the fictitious electrode m connected to low impedance ($V_{n\neq m} = 0$), the charge q induces charge on the sensing electrode Q_s which is at fixed $V_s = 0$. Relation B.1 can be applied between the actual state and another, electrostatically possible state, where the electrode potential $V'_s \neq 0$ results in the potential V'_m

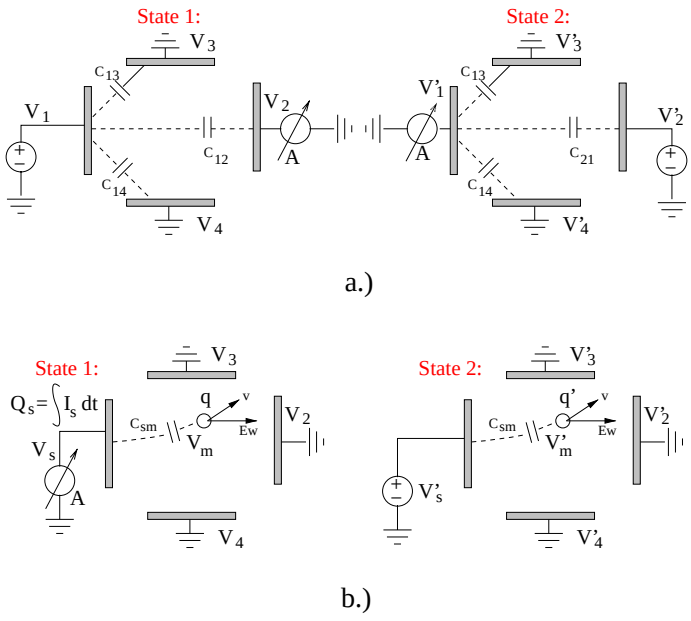

Figure B.1: a) Application of the Reciprocity Theorem to show that electrostatic coupling is independent of the direction of charge displacement ($C_{12} = C_{21}$). b) Illustration of the states considered in the derivation of the induced current due the motion of the charge q (from [KraTh]).

at the charge location and no charge is present there ($q'_m = 0$), so that

$$qV'_m + Q_s V'_s = q'V_m + Q'_s V_s \tag{B.3}$$

$$Q_s V'_s + qV_m = 0 \tag{B.4}$$

The induced current I_s flowing in the sensing electrode is then calculated as

$$I_s = \frac{dQ_s}{dt} = -\frac{d\left(q\frac{V'_m}{V'_s}\right)}{dt}. \tag{B.5}$$

By substituting $V'_m/V'_s = U_w$, which is referred to as *weighting potential*, equation B.5 is written

$$I_s = -q\frac{dU_w}{dt} = -q\frac{dU_w}{dt}\frac{d\vec{r}}{d\vec{r}} = -q\frac{dU_w}{d\vec{r}}\frac{d\vec{r}}{dt} = -q\nabla U_w \cdot \vec{v}_{\mathrm{dr}}, \tag{B.6}$$

where $d\vec{r}$ is the direction of the drift and $\vec{v}_{\mathrm{dr}}$ the drift velocity of the charge q in the electric field.

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