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M.Sc. Thesis

Integrated Measurement Systems for Electronic Devices Operating in Radiation Environment

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Contents

Integrated Measurement Systems for Electronic Devices operating in Radiation Environment

Electronic systems in High Energy Physics experiments are exposed to radiation. Such hard environment provokes damages and errors in electronic devices. This M.Sc. thesis describes the radiation effects on different types of electronic components. Three measurement systems are presented, for irradiation experiments on Light Emitting Diodes, semiconductor memories (SDRAM and FLASH) and FPGA chips. Results of several tests that have been done are included and discussed.

1 Introduction

This thesis concentrates on different electronic devices operating in various radiation fields during High Energy Physics experiments. Presented work undertakes only the most important points, because total problem is very wide and exceeds over this thesis.

1.1 Particle physics and High Energy Physics experiments

Particle physics is a branch of physics that studies the elementary constituents of matter and radiation, and the interactions between them. Modern particle physics research is focused on subatomic particles, which have less structure than atoms. These include atomic constituents such as electrons, protons, and neutrons (protons and neutrons are actually composite particles, made up of quarks), particles produced by radiative and scattering processes, such as photons, neutrinos, and muons, as well as a wide range of exotic particles. [11]

It is also called High Energy Physics (HEP), because many elementary particles do not occur under normal circumstances in nature, but can be created and detected during energetic collisions of other particles, as is done in particle accelerators. [11] There are two basic types of particle accelerators [12]:

- Circular (eg. LHC, introduced later in this thesis) - particles move in a circle until they reach sufficient energy.
- Linear (eg. XFEL, introduced later in this thesis) - particles are accelerated in a straight line, with a target of interest at one end.

1.2 Electronics in modern High Energy Physics experiments

Electronic systems for High Energy Physics experiments can be divided in three corelated together functional groups [17]:

- Frontend electronics.
- Data processing and aqusition systems.

- Global systems.

This thesis ephasises problems of frontend electronics in radiation environment. Frontend systems are situated directly on the detectors or accelerators. These two cases are presented on examples of:

- CMS detector - electronic devices for trigger system,
- XFEL accelerator - electronic devices for controlling accelerator.

1.2.1 LHC collider and CMS experiment

The Large Hadron Collider (LHC) is a circular particle accelerator (27 km diameter), which is being developed at the CERN (European Organization for Nuclear Research) research centre in Geneva.

LHC is a collider which will probe deeper into matter than ever before. Due to switch on in 2007, it will ultimately collide beams of protons at an energy of 14 TeV. The LHC is the next step in a voyage of discovery which began a century ago. Accelerator will be built in the same tunnel as CERN's Large Electron Positron collider (LEP). Proton beams will be prepared by CERN's existing accelerator chain before being injected into the LHC.[15]

Five experiments, with huge detectors, will study what happens when the LHC's beams collide:

- ATLAS,
- CMS,
- ALICE,
- LHCb,
- TOTEM.

The problem of effects of radiation on electronic components will be presented on the example of CMS detector.

Electronics exposed to radiation in CMS experiment

The Compact Muon Solenoid (CMS) will be universal detector for LHC. It will allow to probe many particles appearing during the collisions in the collider. CMS will consist of many detectors.

Due to large amount of data from detector, frontend electronics and optical communication systems must be placed on the CMS detector, in the radiation environment. Radiation level was simulated and is presented in Table 1. [25]

Particles	At the barell	At the endcap
charged hadrons $E = 10 - 100MeV$	$3.6 * 10^1 cm^{-2}s^{-1}$	$1.6cm^{-2}s^{-1}$
neutrons $E > 20MeV$	$1.1 * 10^3 cm^{-2}s^{-1}$	$84cm^{-2}s^{-1}$
neutrons $E = 2 - 10MeV$	$7.2 * 10^2 cm^{-2}s^{-1}$	$93cm^{-2}s^{-1}$
neutrons $E > 100keV$	$4.4 * 10^3 cm^{-2}s^{-1}$	$370cm^{-2}s^{-1}$
neutrons $E < 100keV$	$1.1 * 10^4 cm^{-2}s^{-1}$	$650cm^{-2}s^{-1}$
neutrons total $E = 10 - 100MeV$	$1.7 * 10^4 cm^{-2}s^{-1}$	$1100cm^{-2}s^{-1}$

Table 1: Particle fluxes in regions of CMS detector where optical communication systems will be placed

1.2.2 X-FEL experiment

The X-ray free-electron laser (X-FEL) is linear accelerator, which is being developed at the DESY (Deutsches Elektronen-Synchrotron) research center in Hamburg, in cooperation with European partners. The facility could take up operation in 2012.

This facility will produce high-intensity ultra-short X-ray flashes with the properties of laser light. This new light source will open up a whole range of new perspectives for the natural sciences. The X-ray laser opens up unsuspected perspectives for physics, chemistry, materials science and geophysical research, biological sciences and medicine. The radiation is also of considerable interest to industrial users. [13]

Examples for research with the X-ray laser [14]:

- femtochemistry: capturing chemical reactions on film,
- structural biology: shedding light on biomolecules,
- materials research: developing new materials,
- plasma physics: a different state of matter,
- cluster physics,
- and many more.

Electronics exposed to radiation in XFEL tunnel

Some of electronic components (eg. low level radio frequency controllers) will be placed in the same tunnel as accelerator tube, as it is now in Tesla Test Facility II. Crates for these devices are situated in the catwalk (see Figure 1).

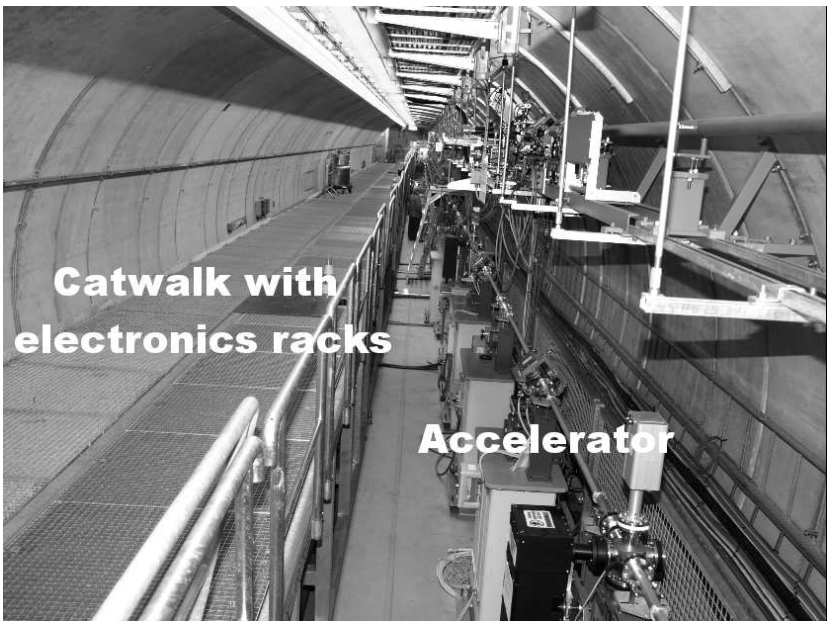

Figure 1: Tunnel of TESLA Test Facility II with crates for electronic systems in the catwalk

These devices will be exposed to parasistic pulsed radiation field, mainly due to [22]:

- beam loses in the tube,
- dark current from the superconducting cavities.

The roughly estimation of doses close to accelerating cryo module are to be [22]:

- 10^{12} neutrons$/\text{cm}^{-2}/20$ years
- 10 rad/hour for gammas (based on a maximum permitted additional cryo heatload of $0.1W/m^2$

2 Radiation effects on electronic components

Radiation causes damages in electronic components. The type and magnitude of these damages depend on irradiation environment. There are three main groups of mechanisms, the radiation effects in semiconductor materials [20][19][21]:

- Total Ionizing Dose (TID) effects,
- Single Event Effects (SEE),
- Displacement damage due to NIEL - Non Ionizing Energy Loss.

Briefly characteristics of these effects are presented in Table 2.

Effect	Caused by	Results	Time scale
TID	neutrons, protons, heavy particles or gammas	degradation of device as a function of ionizing radiation cumulation	long
SEE	high LET particles recoiled by neutrons	device upset or destruction	instantenous
NIEL	heavy or secondary particles	permanent damage of the semiconductor structure	medium/long

Table 2: Overview of the radiation effects in semiconductor devices

2.1 Total Ionizing Dose (TID) effects

Total Ionizing Dose effects are caused by neutrons, protons, heavy particles or gammas. It's degradation of device as a function of ionizing radiation cumulation.

Ionizing radiation causes electron-hole pairs creation in the oxides (see Figure 2). Some of these pairs recombinate, more in the absence of electric field. All remaining electrons, because of their high mobility leave the oxide. Holes, because of their very low mobility are mostly trapped. There is positive charge trapped in the oxide, resulting in the gradual degradation of the device.[20][19]

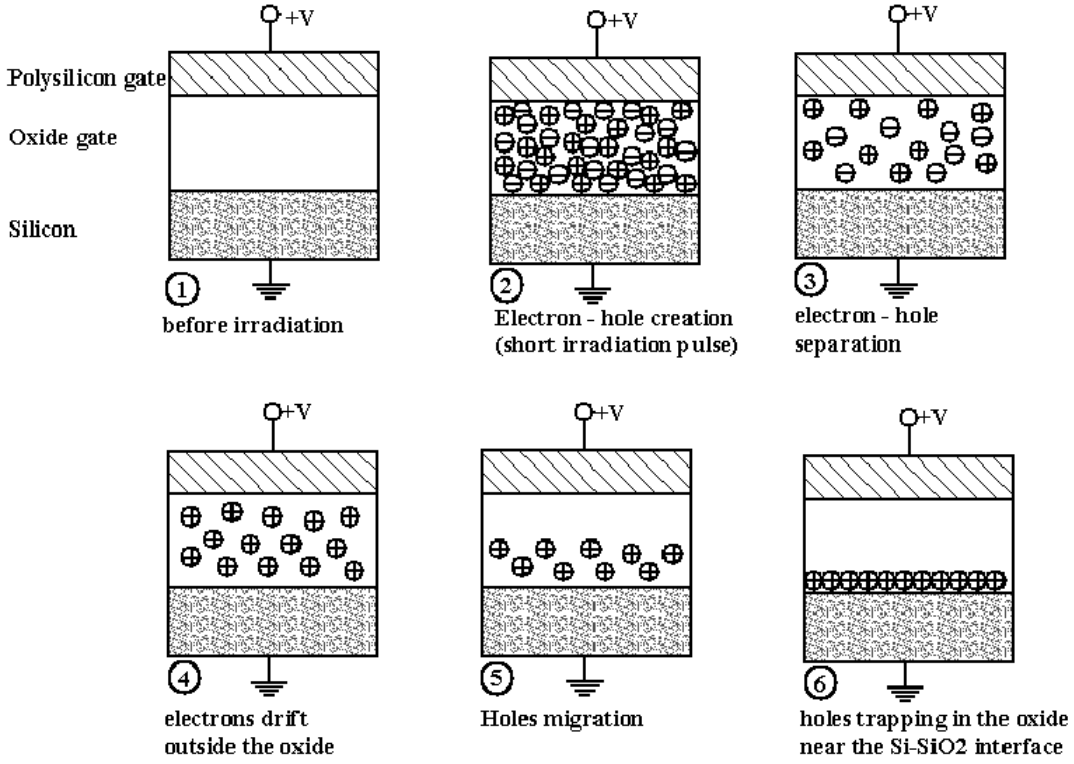

Figure 2: Cumulated ionization example in MOS oxide [20]

2.2 Single Event Effects (SEE)

Single Event Effects (SEE) can be generated by high LET (Linear Energy Transfer) particles recoiled by neutrons. It results in instantaneous device upset or destruction.

SEE occurs when highly ionizing particle penetrates through the oxide layer (see Figure 3). It provokes high electron-hole pairs density along its track and transient current across the oxide layer. In the results oxide breakdowns.[20][19]

There are different categories of Single Event Effects, depending on a place in the device where occur:

- with non-destructive results:
  - Single Event Upset (SEU) - bit flips in memory (see page 59),
  - Single Event Functional Interrupt (SEFI) - SEUs in device control logic (eg. in FPGA: JTAG TAP controller, Select Map interface),

  - Single Event Transient (SET) - changes in propagated signal,

- with destructive results:

  - Single Event Gate Rupture (SEGR) - gate-to-channel short circuit,
  - Single Event Burnout (SEB) - high instantaneous current → junction breakdowns,
  - Single Event Latch-up (SEL) - Vdd-to-Vss short circuit.

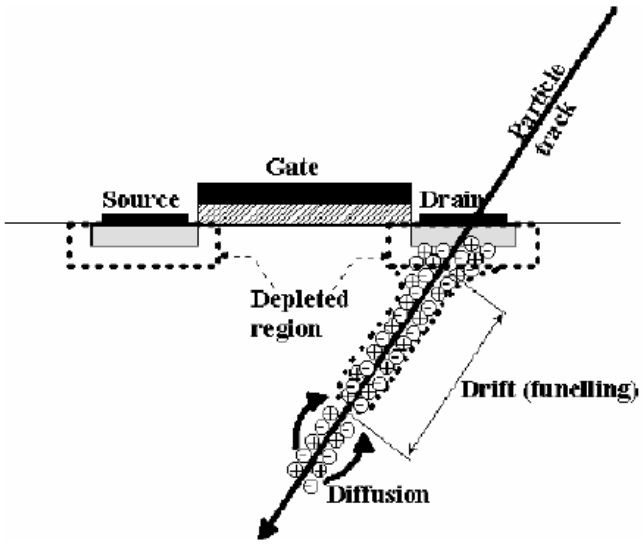

Figure 3: Example of Single Event Effect - Single Event Upset [20]

2.3 Displacement Damage due to NIEL - Non Ionizing Energy Loss

Displacement damages are caused by heavy or secondary particles. It's the result from particles producing Non Ionizing Energy Loss (NIEL).

Heavy or secondary particle collides with atoms from crystal structure of the semiconductor material. It causes defects in this structure along the track of particle.[20][19]

The effects of displacement damage could be:

- minority carrier's lifetime decreases,
- carrier's mobility decreases,

- effective majority carrier's concentration decreases - resistivity increases,
- creation of acceptor levels - type inversion (N → P).

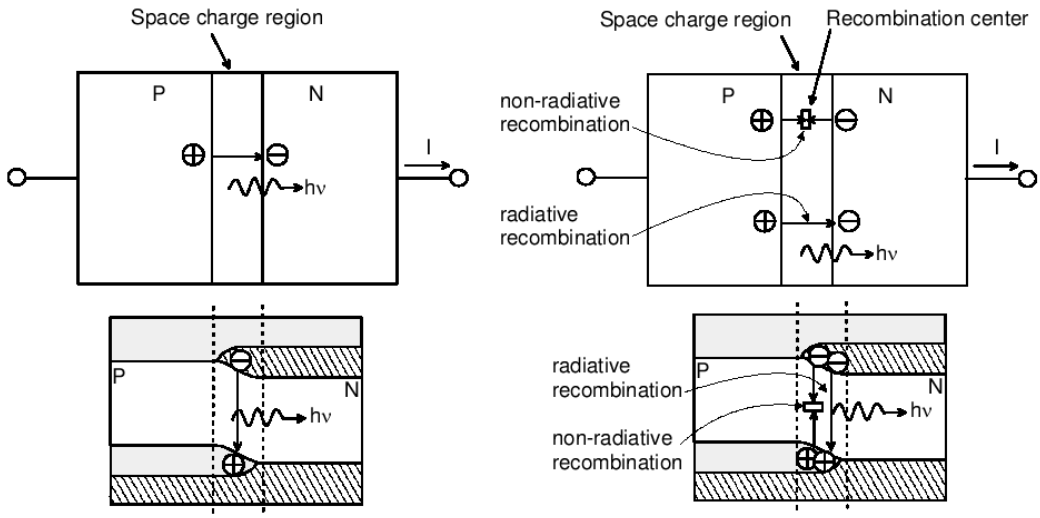

Figure 4: Creation of recombination center in P-N junction caused by displacement damage [20]

3 Radiation induced errors in electronic devices

This section describes radiation induced errors in electronic components. In details there are presented problems in devices, which are the objectives of radiation investigations presented in this thesis: Light Emitting Diodes, semiconductor memories (FLASH and SDRAM), FPGA chips.

3.1 Radiation induced damage in Light Emitting Diodes

Particles creating NIEL (Non Ionizing Energy Loss) causes the displacement damage in p-n junction of semiconductor devices, such as Light Emitting Diodes (LEDs). As the effect there is less luminescence of irradiated (e.g.: with protons, neutrons) LEDs, connected to constant current source. This permanent effect is much more noticeable than damages created after irradiation with gammas (see Figure 5, where KERMA - Kinetic Energy Released in Matter) [21][7][18].

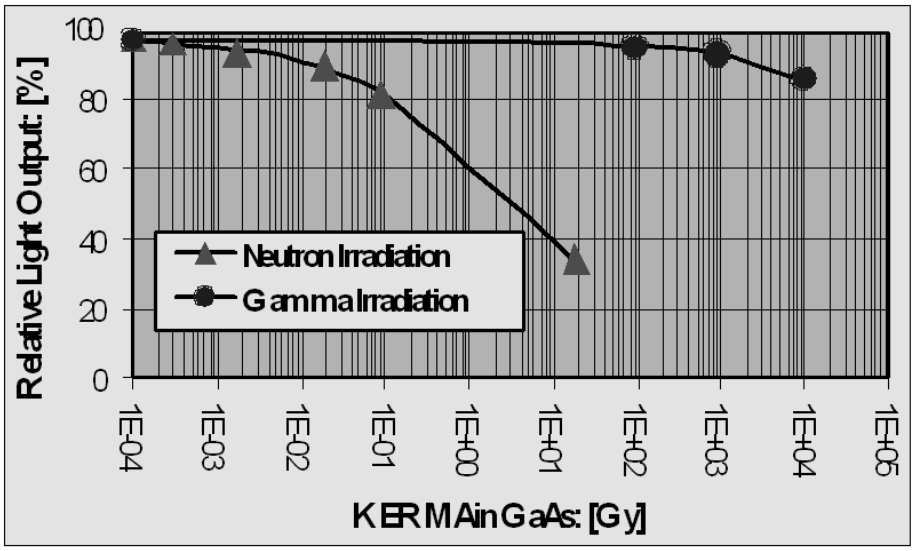

Figure 5: Relative light output of GaAs LED irradiated with ^{60}Co gamma rays ($E_g = 1.25MeV$) and fast neutrons ($E_n = 16MeV$) from a medical cyclotron[18]

3.2 Radiation induced errors in semiconductor memories

Depending on type of semiconductor memories there are different effects supposed to be induced in FLASH and SDRAM memories.

3.2.1 FLASH memories

In FLASH memories there are transistors with a modificated floating gate (FAMOS - Floating gate Avalanche-injection MOS) to store data (see Figure 6). Operation of the FAMOS transistor is based on the Fowler-Nordheim tunnelling of charge carriers from a source (drain) through the oxide to its floating gate.

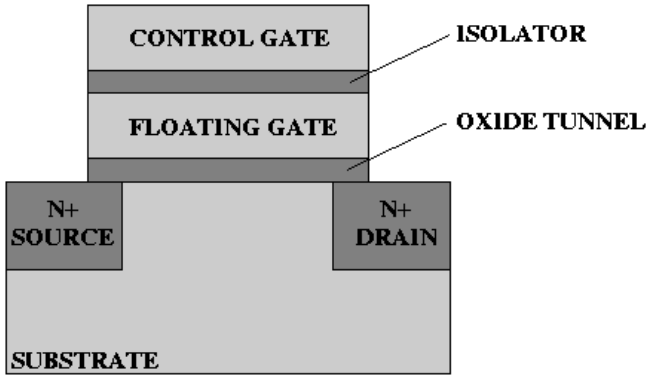

Figure 6: FAMOS transistor cross section

The writing operation injects electrons into the floating gate through the oxide layer. The erasing operation removes them from the floating gate. During erasing all bits are set to ’1’. The writing operation sets the bits to ’0’, thus the writing can be done only after erasing. [44]

Voltages required for writing and erasing operations (+12V, +7V and -9V) are higher than the power supply voltage. There are provided by the charge-pump circuit. A degradation of this subsystem of memory chip is very probable in a radiation environment, because the charge-pump works with relatively high voltages.

Ionizing radiation can destroy the isolator structure, allowing the charge accumulated in the floating gate to migrate out of it. As the result the memory cell changes its state from ’0’ to ’1’. There is no mechanism changing the state of a memory cell from ’1’ to ’0’. [31][36][37][30]

In the FLASH memory chip there are several registers and some logic, controling the memory, which are also vulnerable to radiation (see Figure 7).

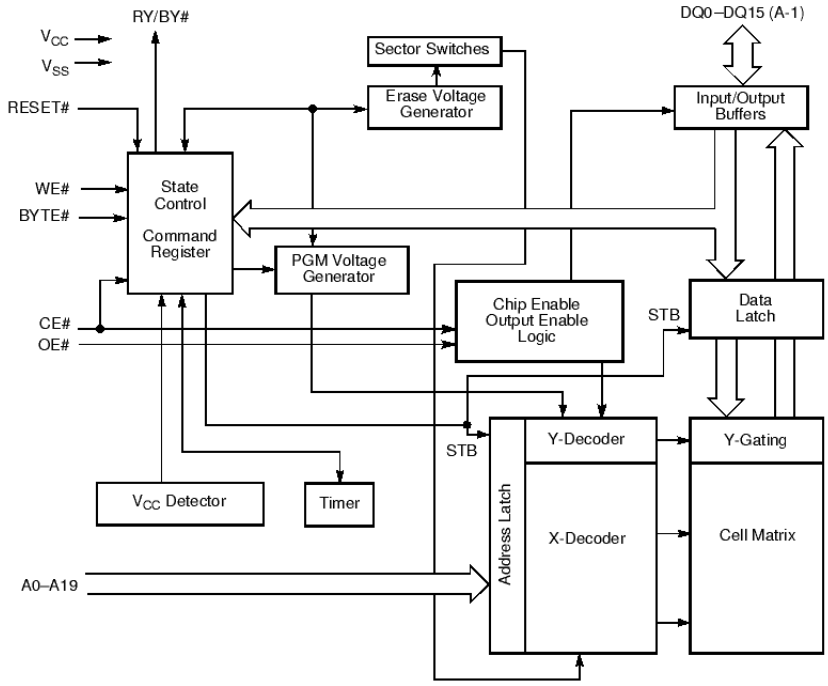

Figure 7: Schematic block diagram of Am29LV160D FLASH memory [45]

3.2.2 SDRAM memories

SDRAM (Synchronous Dynamic Random Access Memory) uses a capacitor as a data storage element and a transistor as a switch (see Figure 8). When the potential of the capacitor is at ground level, the state of the cell is ’0’. When this potential is equal to the supply voltage, the state of the cell is ’1’.

In a radiation environment, ionizing particles passing through the capacitor generate electron-hole pairs. The potential on the capacitor may then change, changing the memory state. This type of errors - SEUs - are the most frequent errors in SDRAMs [32][33]. Futhermore, two types of SEUs are observed:

- recoverable bit upsets - single or multiple errors in one word of memory,
- stuck bits - bits, which do not change their state even after reprogramming.

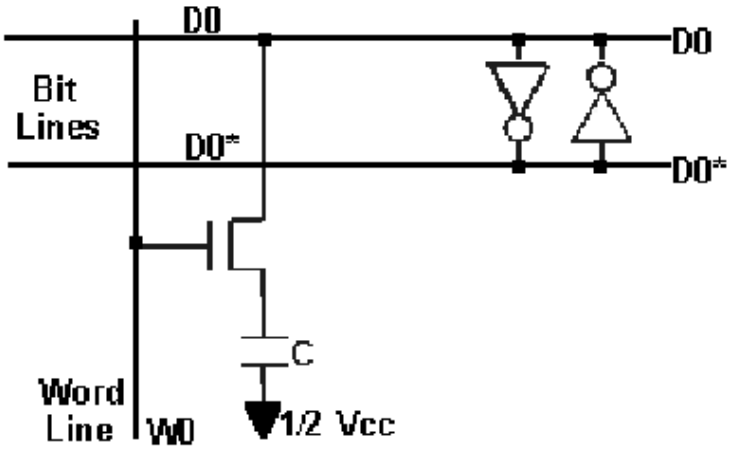

Figure 8: SDRAM memory cell

In the SDRAM memory chip there are several registers and some controlers of the memory, which are also vulnerable to radiation (see Figure 9).

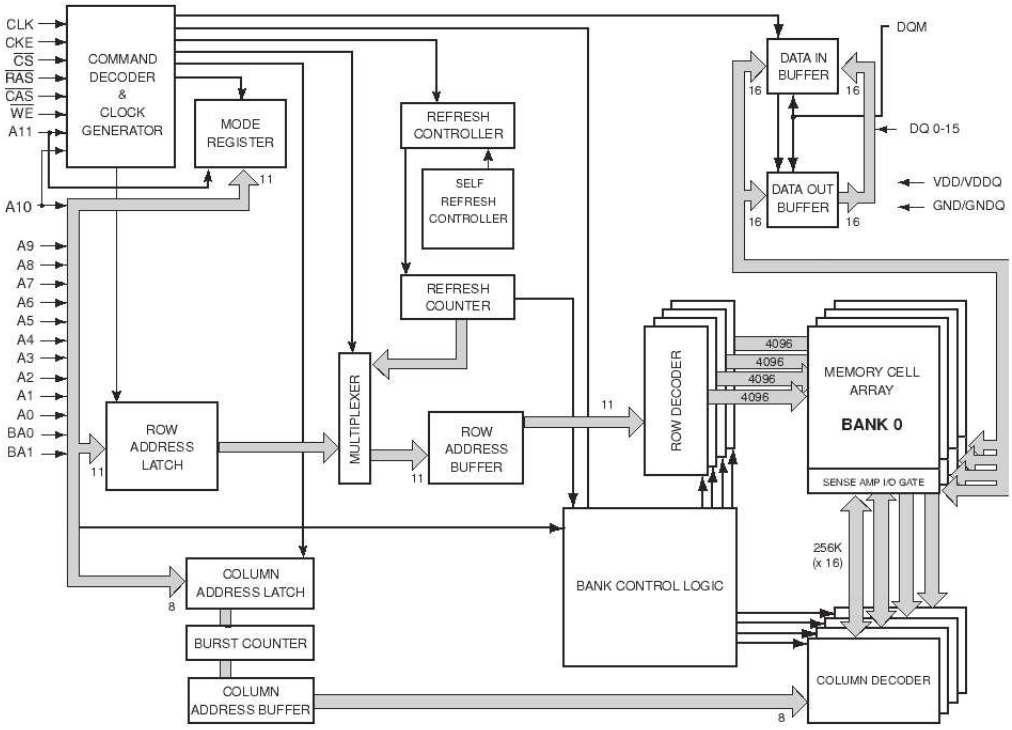

Figure 9: Block schematic of IS42S16400 SDRAM memory [46]

3.3 Radiation induced errors in FPGA chips

In this section the FPGA chips architecture is briefly presened. Single Event Effects in these devices are discussed.

3.3.1 FPGA architecture

Field Programmable Gate Array chips (FPGA) are type of programmable circuits, which are programmed by user to perform the designed functionallity. Project must be written in one of Hardware Description Language (HDL), e.g. VHDL, Verilog. It's compiled, synthesized and implemented in FPGA chip. The configuration bits can be stored in a chip using different techniques depending on technology [54]:

- Antifuse technology - programmable only once,
- Flash memory - programmable several times,
- SRAM memory - programmable dynamically.

The last possibility is dominating technology. It allows very fast, almost unlimited in system reprogramming.

Architecture of FPGA chips from different vendors may differ but the main idea is almost the same. It consists of some main blocks (description based on Xilinx Spartan-IIE chip, see Figure 10) [55]:

- Flexible, programmable Configurable Logic Blocks (CLB), which provide the functional elements for constructing logic. The basic block of the CLB is Logic Cell (LC). Two LCs form slice and two slices form CLB. Each LC includes a function generator, carry logic and a storage element. The function generator is implemented as look-up table (LUT). The storage element can be configured either as edge-triggered D-type flip-flop or as level-sensitive latch.
- Programmable Input/Output Blocks (IOB), which provide the interface between the package pins and the internal logic. The IOB features inputs and outputs that support

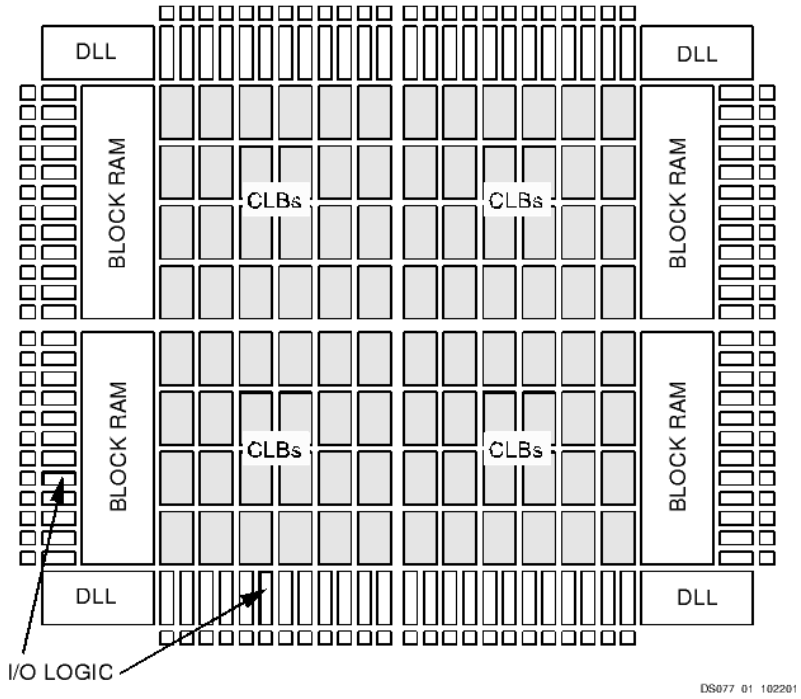

Figure 10: Basic Spartan-IIE Family FPGA Block Diagram [55]

a wide variety of I/O signalling standards. Each input and output can be configured to conform any of the low-voltage signalling standards.

- Delay-Locked Loops (DLL) for clock distribution. This blocks eliminate skew between the clock input pad and internal clock-input pins throughout the device. Additionaly delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input.

- Dedicated internal memory (Block RAM). This memory can be used to storage data inside the chip. The word length and type of memory is configured by system designer.

- Versatile multi-level interconnection structure. Local routing resources provide three types of connections:

  – interconnections among the LUTs, flip-flops,

  – internal CLB feedback paths, between LUTs in the same CLB,

– direct paths providing high-speed connections between horizontally adjecent CLBs.

The software automatically uses the best available routing based on user timing requirements.

Values stored in static memory cells control all the configurable logic elements and interconnection resources. These values must be loaded into the memory cells on power-up and can be reloaded to change function of the device, almost any time.

3.3.2 Single Event Effects (SEE) in FPGA chips

SRAM (Static Random Access Memory) cells in FPGA and internal flip-flops have similar structure to SDRAM memory cell (see Figure 8) and are immune to radiation. The most probable effects in FPGA chips are Single Event Effects, especially Single Event Upsets.

Single Event Upset (SEU) is a change of the logic state of an element storing one bit caused by radiation. Two types of SEUs may be distinguished (see Figure 11):

- static SEUs - changes in the configuration bits,
- dynamic (or transient) SEUs - changes in the logic state of the bits, which are supposed to change during normal operation (for example flip-flops).

SEUs affect the performance of FPGA in different ways. Changing the state of one flip-flop working as a latch results in a false value of one bit during one clock period only, while changing the state of one SRAM cell in the look-up table results in a permanent wrong answer for one combination of input bits. Changing the state of one SRAM that programs the interconnection between logic blocks can seriously modify the performance of whole circuit. [35][38]

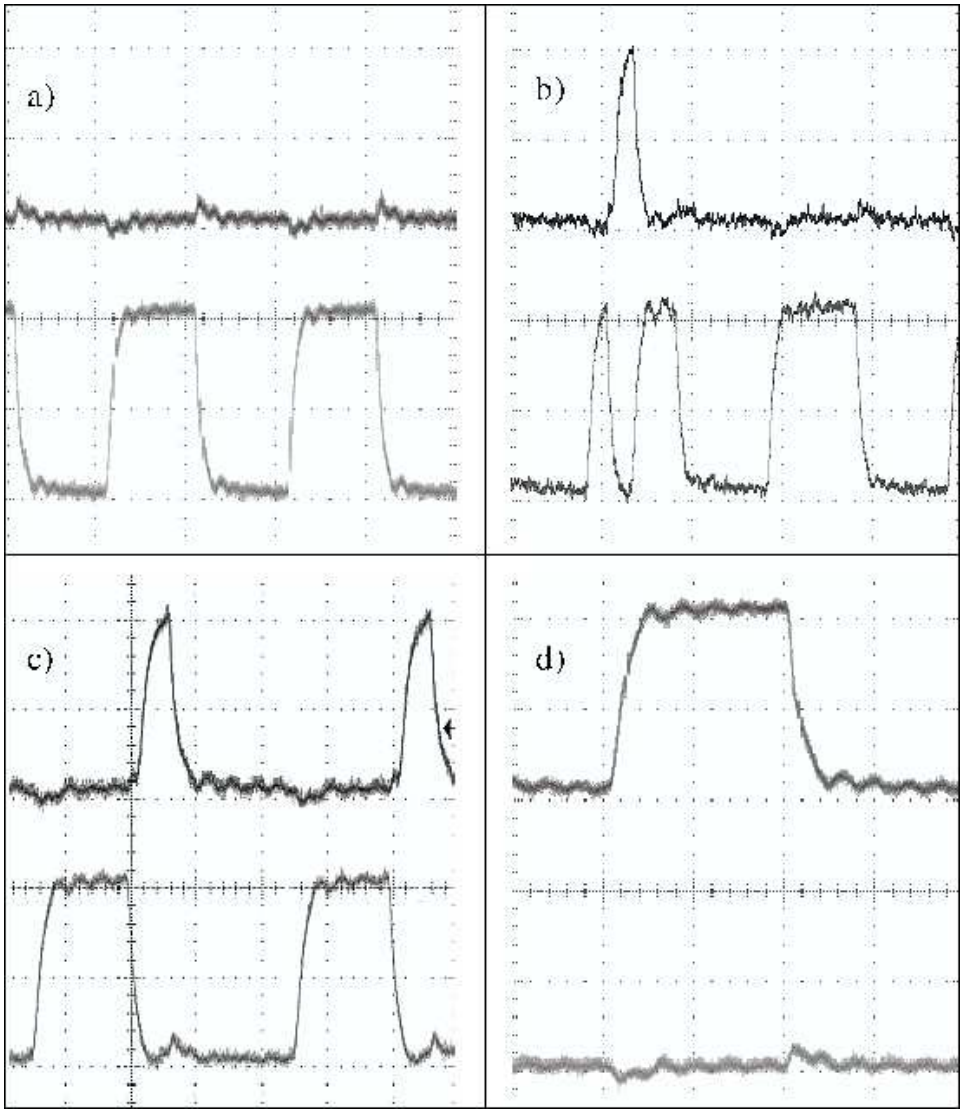

Figure 11: Examples of SEUs in the shift register design observed on the scope. Upper signal - the SEU indicator, bottom signal - the output of the shift register. a) normal operation; b) dynamic SEU ; c) static SEU - the shift register broken off and linked to other part of register; d) static SEU - the shift register broken off, input of register connected to ’0’.[1][2]

4 Thesis' objectives

A significant number of electronic systems for controling and diagnostics of modern HEP experiments (such as CMS, VUV-FEL, X-FEL, ILC) are ussually located in the accelerator tunnel, next to the accelerating tube, producing various radiation fields. In such environment problems with these systems are expected to occur. The studies on electronic components' radiation sensivity are needed. These investigations should provide vital information to optimize the design of electronic systems and to minimalize failures during long-term operation. [22]

The irradiation experiments could be divided into three steps [3][4][5]:

1. Radiation level measurements:
    - evaluation of radiation level,
    - understanding the radiation effects in accelerators (especially: superconducting linacs) and measurements of radiation level (neutrons, gammas).
2. Investigations of radiation effects on electronic components, circuits and complete systems:
    - determine Single Event Effects (SEEs),
    - determine Total Ionizing Dose (TID) effects,
    - determine radiation effects on different types of electronics,
    - predict performance and life-time of electronics in radiation environment.
3. Counter measures:
    - development of radiation mitigation concepts and evaluate their performance in the presence of radiation.

This thesis partially fulfills points 1 and 2 of presented scheme of work. There are described measurement systems for irradiation experiments of electronic devices, such as:

- FPGA (Field Programmable Gate Array) chips,
- semiconductor memories (SDRAM and FLASH),
- LEDs (Light Emitting Diodes).

Results of experiments are included and discussed.
The main objectives of thesis as follows:

- Understanding the radiation effects on electronic components.
- Development of digital photometer for the evaluation of COTS (Commercial-Off-The-Shelf) LED (Light Emitting Diodes) fast neutron dosimeter.
- Development of the test system for SEUs (Single Event Upsets) in FPGA (Field Programmable Gate Array) chips.

5 Measurement systems for electronic devices operating in radiation environment

We have developed three measurement systems for radiation experiments with electronic devices. First is a part of Commercial-Off-The-Shelf Light Emitting Diodes fast neutron dosimeter. It supports measuring light output from Light Emitting Diodes and calculating ratio of its degradation after irradiation with fast neutrons. Second test system was developed for experiments with semiconductor memories. Third measurement system allows us to investigate static Single Event Upsets in FPGA chips during irradiation.

5.1 Digital photometer for Commercial-Off-The-Shelf Light Emitting Diodes fast neutron dosimeter

The proposed experiment goal was to investigate the radiation damage phenomena of the Light Emitting Diodes irradiated with accelerator produced fast neutrons. Two measurements should be done:

- before irradiation,
- after irradiation.

The neutron flux could be further estimated using light attenuation (ratio between this two values) and calibration data.

We have built two devices:

- prototype test system, based on laboratory measurement instruments,
- specialized device based on microcontroller.

5.1.1 Prototype test system

The prototype instrument consisted of (see Figure 12):

- photometer (RS V10860, supplier: RS Components),

- power supply (EA-PS 2016-050, supplier: Conrad Electronic),
- digital multimeter (HP 34401A, supplier: Hewlett-Packard),
- custom designed aluminium cup.

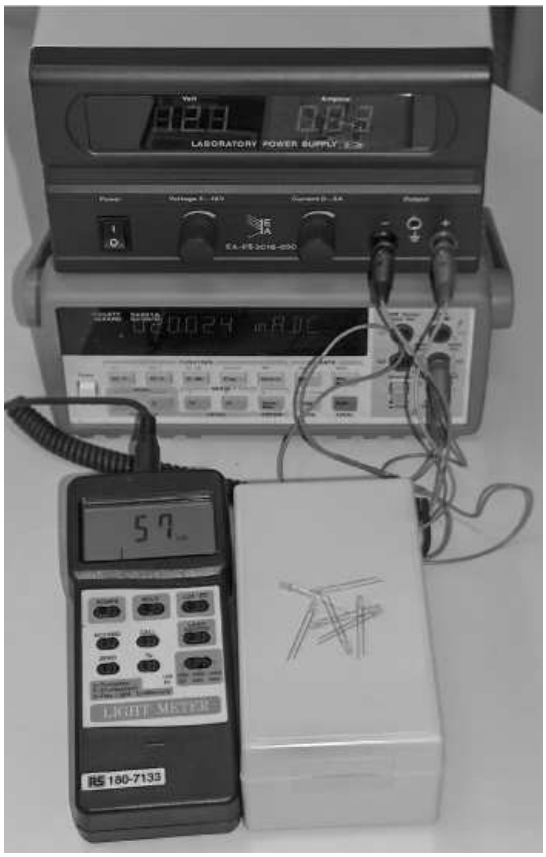

Figure 12: Prototype test system for COTS LED fast neutron dosimeter

The prototype measurement system was used for preliminary investigations, to prove that method of quantify neutron flux using degradation of light emission from Light Emitting Diodes works.

5.1.2 Device schematic

The device consists of three sections (see Figure 13):

- mictrocontroller,

- constant current supply,
- photometer.

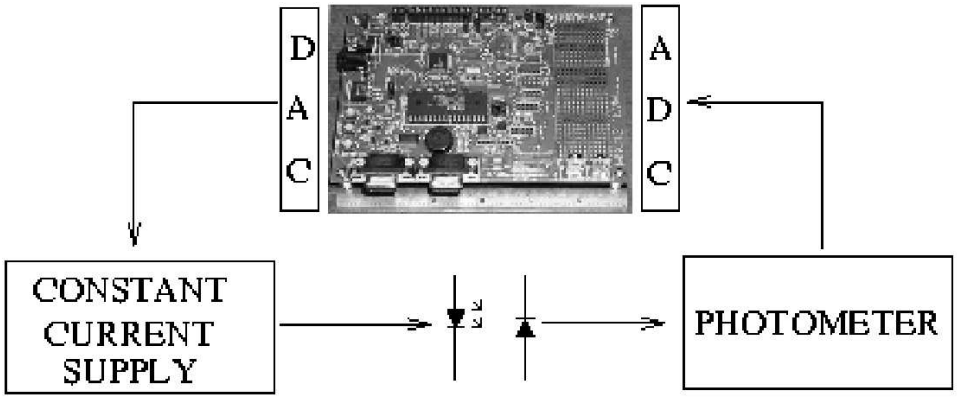

Figure 13: Block diagram of digital photometer for COTS LED fast neutron dosimeter

The device utilizes Texas Instruments MSC1211 Evaluation Module (see Figure 14) [47]. MSC1211 is precision analog to digital converter with 8051 microcontroller and FLASH memory inside [48].

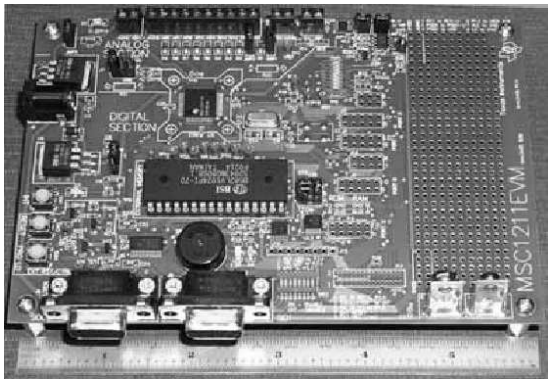

Figure 14: Texas Instruments MSC1211 Evaluation Module

Main features of module, which are used in project:

- 8051 microcontroller,
- 24-bit delta-sigma analog-to-digital converter,

- 16-bit digital-to-analog converter,
- serial port driver.

Microcontroller gives signals to the constant current supply to provide current for the measured LED and to the photometer to measure illuminance. It also communicates with PC computer through the serial port.

The constant current supply (see Figure 15) supplies current for measured LED. This current source gives 13 mA for every supplied diode.

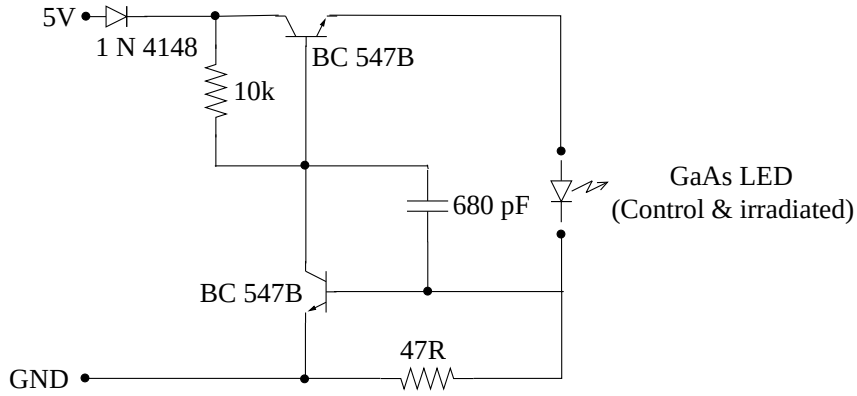

Figure 15: Schematic of constant current supply for digital photometer for COTS LED fast neutron dosimeter

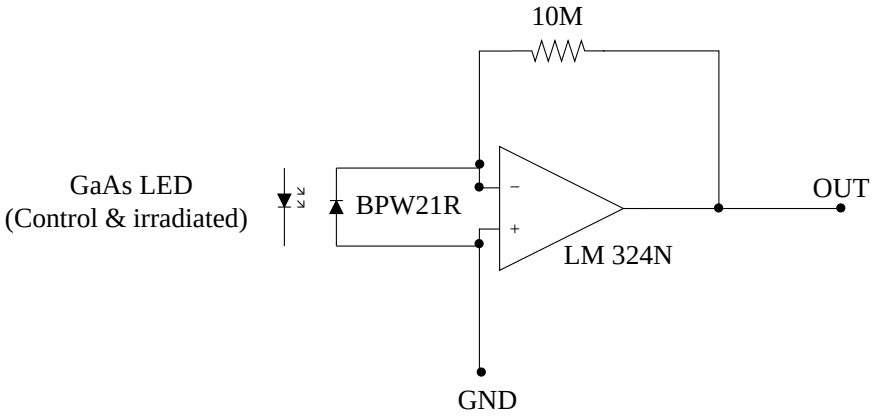

Figure 16: Schematic of photometer for digital photometer for COTS LED fast neutron dosimeter

The photometer section (see Figure 16) is based on planar Silicon PN photodiode BPW21R from Vishay Semiconductors [49]. This model was chosen because of its high sensivity and excellent linearity.

The precision operational amplifier was used to amplify measured value of illuminance. As this element there was used LM324 from STMicroelectronics [50].

Assembled digital photometer for COTS LED fast neutron dosimeter with special cup to hold LEDs is presented on Figure 17.

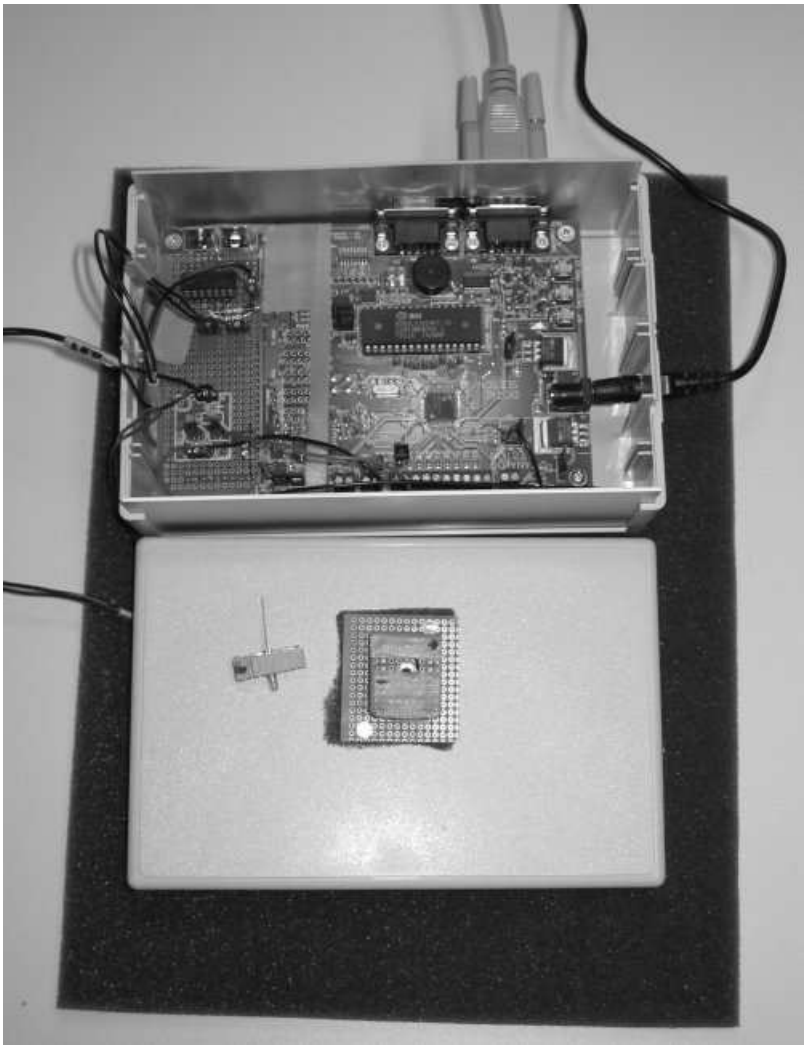

Figure 17: Assembled digital photometer for COTS LED fast neutron dosimeter with LED holder

5.1.3 Control application

The single measurement consists of:

- measurement trigger from PC,
- grabbing data from photodiode during flashes of measured LED,
- sending results to PC computer.

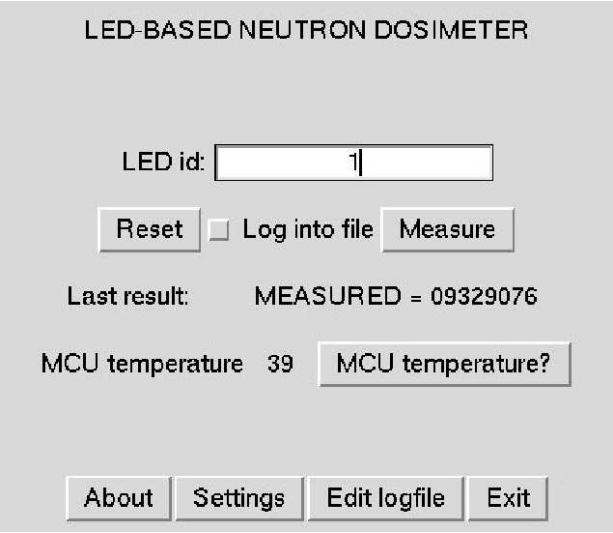

Figure 18: Control application panel for digital photometer for COTS LED fast neutron dosimeter

We have developed a dedicated software (see Figure 18) for controlling device using PC computer connected to instrument by serial port. The software was written in Python language using Tix/Tkinter libraries for Graphic User Interface (GUI).

Functions available in application:

- resetting the device,
- performing measurement,
- measuring microcontroler temperature,
- logging measurements to file with specific ID code for each LED.

5.2 Test system for investigations of Single Event Upsets in semiconductor memories

Measurement system for investigations of Single Event Upsets in semiconductor memories was developed in cooperation with Wojciech Zabołotny, Krzysztof Poźniak from Warsaw University of Technology and Maciej Kudła, Krzysztof Kierzkowski, Karol Buńkowski from Warsaw University. Software was written in cooperation with Wojciech Zabołotny.

5.2.1 System schematic

Test board (see Figure 19) consists of:

- FPGA chip (Altera ACEX 1K EP1K100FC256) [51],
- microcontroler (AVR AT90S8515) [52],
- SDRAM memory,
- ZIF socket for removable FLASH memories.

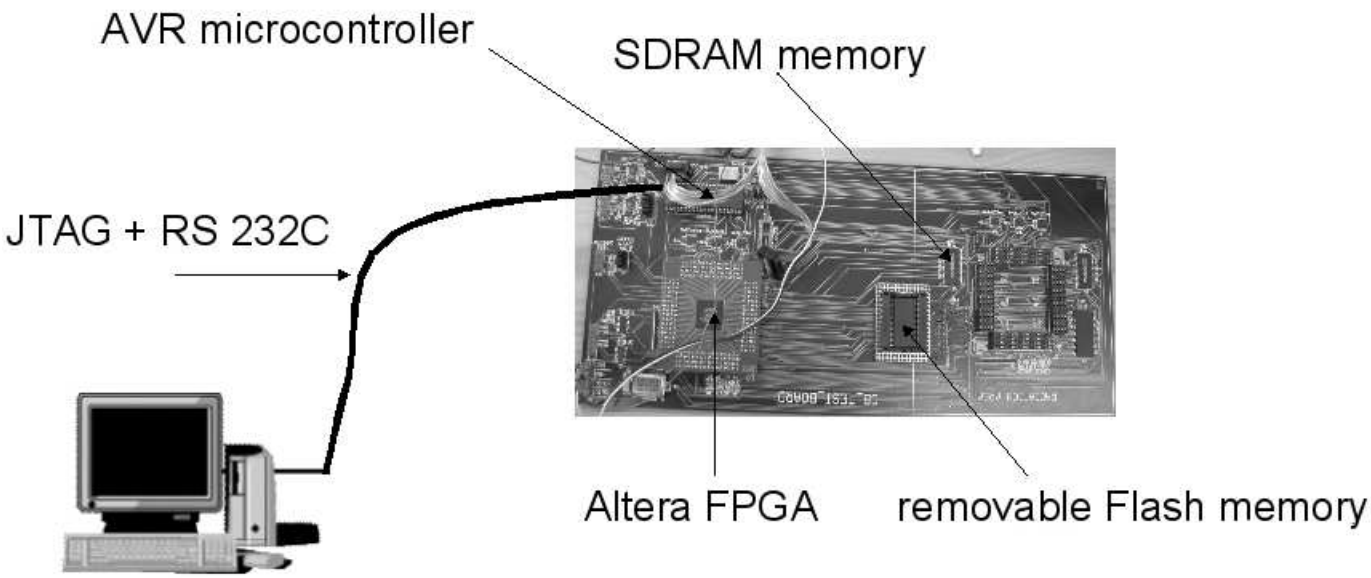

Figure 19: Test system for investigations of Single Event Upsets in semiconductor memories

5.2.2 Hardware

The AVR microcontroller was used to perform tests of the memories and to report errors to PC computer. FPGA chip worked as FLASH and SDRAM memories controller and random number generator. Devices communicated through internal bus.

FPGA had numerous registers:

- FPGA command, status registers,
- FLASH adrress, data, status registers,
- SDRAM adrress, data, status registers,
- random number generator register.

It allowed to perform some commmands, written to command register:

- reset FPGA,
- erase, write, read FLASH memory,
- write, read SDRAM memory,
- write, read, cycle random number generator.

Chip was programmed using JTAG port and Jam Player software.

Code for the microcontroller was written in C language and compiled with AVR-GCC software. The device was programmed using UISP interface. The microcontroler communicates with PC computer by the serial port (RS 232C). Following functions were implemented:

- read and write serial port,
- read and write FPGA registers,
- read, write, initialize and test FLASH memory,
- read, write, initialize and test SDRAM memory,
- initialize, read and cycle random number generator.

5.2.3 Control application

Dedicated application (see Figure 20) was written in Python language, using Tix/Tkinter libraries for building Graphic User Interface. It was used for communication with microcontroller and controlling the experiment. The software allows to:

- program and reset the microcontroller,
- program and reset the FPGA chip,
- set the random number generator,
- fill the memories with random values,
- start and stop test,
- communicate with microcontroller using serial port and low-level commands.

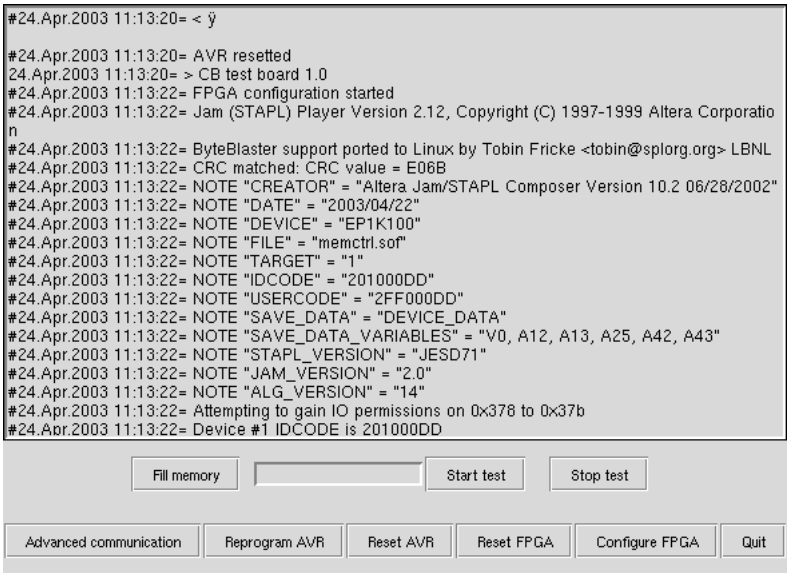

Figure 20: Application for investigations of Single Event Upsets in semiconductor memories

All commands and output data from microcontroller were logged into file and displayed in the application window.

5.3 Test system for investigations of static Single Event Upsets in FPGA chips

Because of higher incidence of static Single Event Upsets in FPGA chips than the dynamic one, test system was built for static SEUs [1][2]. Many attemps of dynamic SEUs investigations had failed. Main reason is the high complexity of the device. FPGA chips have a lot of internal connections, registers and configuration memory, all are based on SRAM technology. Because of higher probability to observe errors in these elements dynamic SEUs are hard to notice.

5.3.1 System schematic

Test system for investigations of static Single Event Upsets in FPGA chips consists of (see Figure 21):

- PC computer running dedicated software,
- JTAG → RS 485 signals converter board,
- RS 485 → JTAG signals converter board,
- Device Under Tests (DUT).

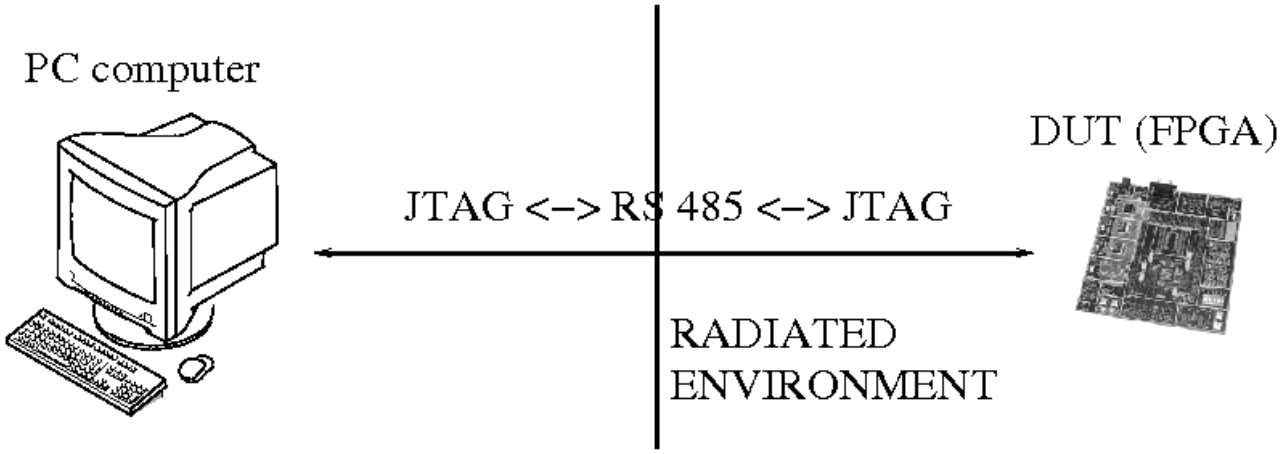

Figure 21: Test system for investigations of Single Event Upsets in FPGA chips

5.3.2 JTAG ↔ RS 485 converters

The PC with software to control irradiation experiments on the FGPA chips was placed outside the radiation area, far away from DUT. The JTAG signals doesn't allow to be tranfered using long cables. Two converter boards were developed to use RS 485 signals instead of JTAG. It allowed to extend range of cables and to put PC computer in safe place.

5.3.3 Investigation method of static Single Event Upsets in FPGA chips

Static Single Event Upsets in FPGA chips can be investigated using readback function. This functionality allows to get from device the configuration memory. At the begining FPGA is programmed with dummy logic. Then the reading of configuration is done continuously. The bitstreams (programmed and read) are compared. The number of different bits indicate the number of static Single Event Upsets in configuration memory of device.

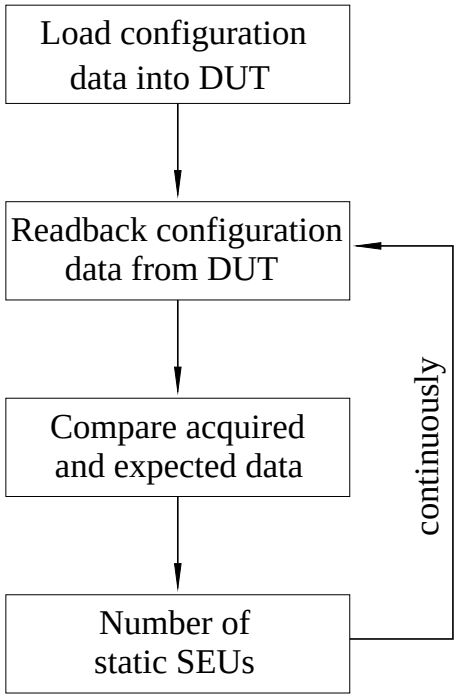

Figure 22: Test routine to investigate static SEU in FPGA chips

5.3.4 Control application

There was developed dedicated software (see Figure 23) in Python language, using Tix/Tkinter libraries for Graphic User Interface.

Figure 23: Control application panel for test system for static SEU in FPGA chips

The application uses Impact software in batch mode from Xilinx ISE development environment to perform programming and reading back configuration data of FPGA chip.

Start button starts the routine to investigate static Single Event Upsets. It is done continuously until the stop button is pressed. All output data from Impact application, run in background, is displayed in program window and can be logged into file.

6 Irradiation experiments

There were performed several experiments with developed test systems. Results are included in this section and discussed.

6.1 Measurements of light attenuation from Light Emitting Diodes

Light reduction was investigated after irradiation of GaAs (Galium Arsenide) Light Emitting Diodes:

- at Hahn-Meitner-Institut (see page 56),
- at superconducting medical cyclotron at Harper University Hospital (see page 57),
- in Linac II tunnel at DESY (see page 55),
- with $^{241}Am/Be$ neutron source (see page 58),

In all experiments we have used 5mm Panasonic LN48YPX GaAs diodes [53]. The colour was chosen to be yellow, because of highest sensivity of photodiode, used in developed photometer.

The light attenuation was evaluated using formula:

$$\text{Attenuation} = \frac{\text{Light output after irradiation}}{\text{Light output before irradiation (control)}} * 100\%$$

6.1.1 Experiments at Hahn-Meitner-Institut

Light Emitting Diodes were irradiated at various gamma dose levels and evaluated thereafter. The light attenuation was assessed. Results are presented in Table 3.

Dose [Gy]	Attenuation [%]
96.3	93
950	90
9810	84
98100	43

Table 3: The results of LEDs radiation experiments with ^{60}Co at Hahn-Meitner-Insitut - light attenuation

6.1.2 Experiments at superconducting medical cyclotron at Harper University Hospital

Light Emitting Diodes were irradiated with various neutron fluxes and then evaluated. The light attenuation was assessed. Results are presented in Table 4.

Neutron fluence $[n/cm^2]$	Attenuation [%]
$1.60 * 10^7$	95
$9.61 * 10^7$	92
$9.93 * 10^8$	91
$1.00 * 10^{11}$	82
$9.81 * 10^{11}$	29

Table 4: The results of LEDs radiation experiments with fast neutrons from superconducting medical cyclotron at Harper University Hospital - light attenuation

6.1.3 Experiments in Linac II tunnel at DESY

There are presented results from two experiments:

- investigations on the spatial distribution of neutrons,
- investigations on neutron shielding using polyethylene.

Experiment on the Spatial distribution of neutrons

Three sets of LEDs were placed in three positions, in the same distance (140cm) from electron/positron converter (inside of Linac II tunnel) - the source of neutron radiation (see Figure 24).

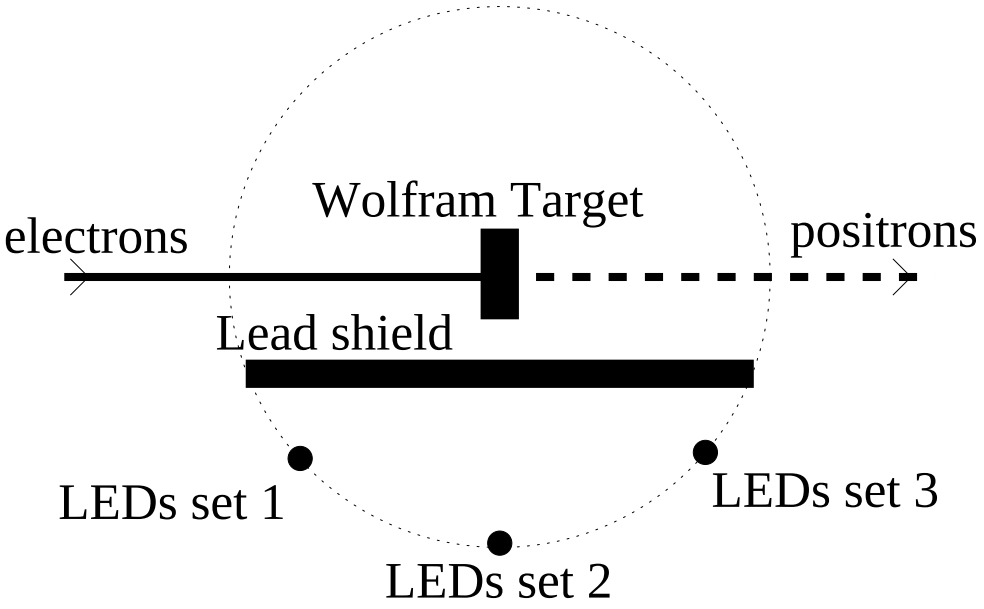

Figure 24: Placement of LEDs sets in neutron spatial distribution experiment in Linac II tunnel

The results of experiment are presented in Table 5. The light output attenuation is almost the same for these three measurement positions. The neutron radiation is isotropic - has the same intensity regardless of the direction of measurement.

Position	Angle from the tube [degree]	Attenuation [%]
1	135	75
2	90	76
3	45	74

Table 5: The results of neutron radiation isotropy experiment with LEDs in Linac II tunnel - light attenuation

Neutrons shielding investigations using polyethylene spheres

Four sets of LEDs were put inside of polyethylene spheres with different radius (polyethylene thickness) (see Figure 25). The spheres were placed in the Linac II tunnel in the same distance from electron/positron converter. One set of LEDs without any shielding was also put in the same position.

Figure 25: Polyethylene spheres for LEDs radiation experiments in Linac II tunnel

After irradiation the light attenuation was assessed. The results are presented in Table 6.

Different values of attenuation for different spheres radius shows that polyethylene absorbes the neutrons (see Figure 26). It can be used as a shielding material for electronic devices against the neutron radiation.

Sphere	radius [cm]	Attenuation [%]
E	3.735	98
D	6.22	97
C	9.8	96
B	12	95
bare	-	83

Table 6: The results of LEDs radiation experiments in Linac II tunnel - light attenuation

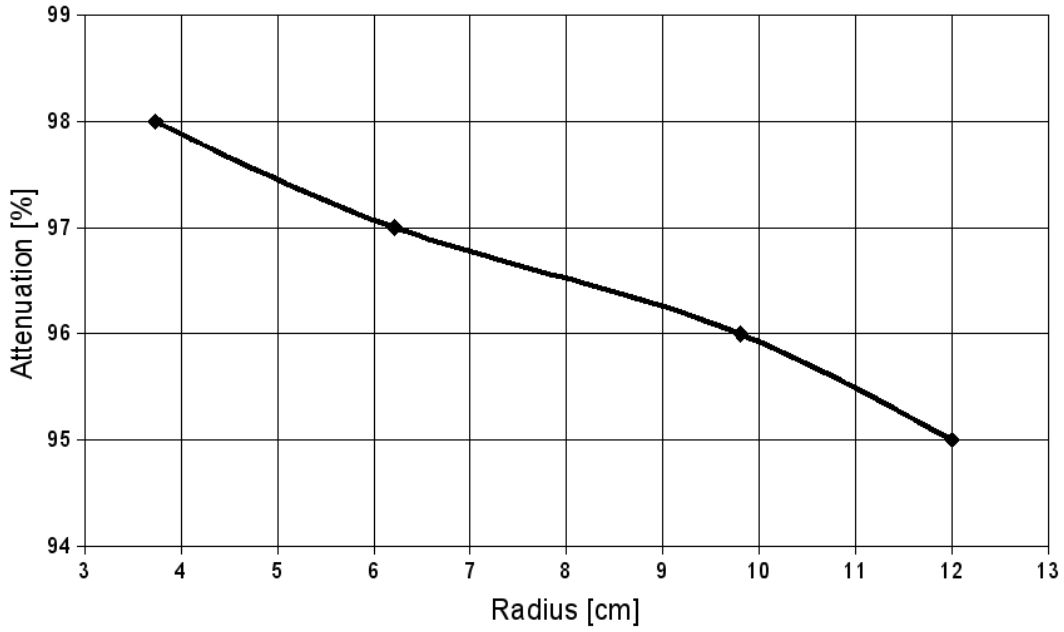

Figure 26: The results of LEDs radiation experiments in Linac II tunnel - light attenuation of photoneutrons in polyethylene

6.1.4 Experiments with $^{241}Am/Be$ neutron source

Sets of LEDs were placed in the same distance from $^{241}Am/Be$ neutron source, but for different times. This varied the neutron doses absorbed by samples.

After neutron irradiation, the light attenuation was assessed. The results are presented in Table 7.

Neutron fluence $[n/cm^2]$	Attenuation [%]
$1.0 * 10^5$	98
$1.0 * 10^5$	97
$1.3 * 10^9$	96
$4.7 * 10^9$	95
$1.2 * 10^{10}$	93
$2.0 * 10^{10}$	90

Table 7: The results of LEDs radiation experiments with neutrons from $^{241}Am/Be$ source - light attenuation

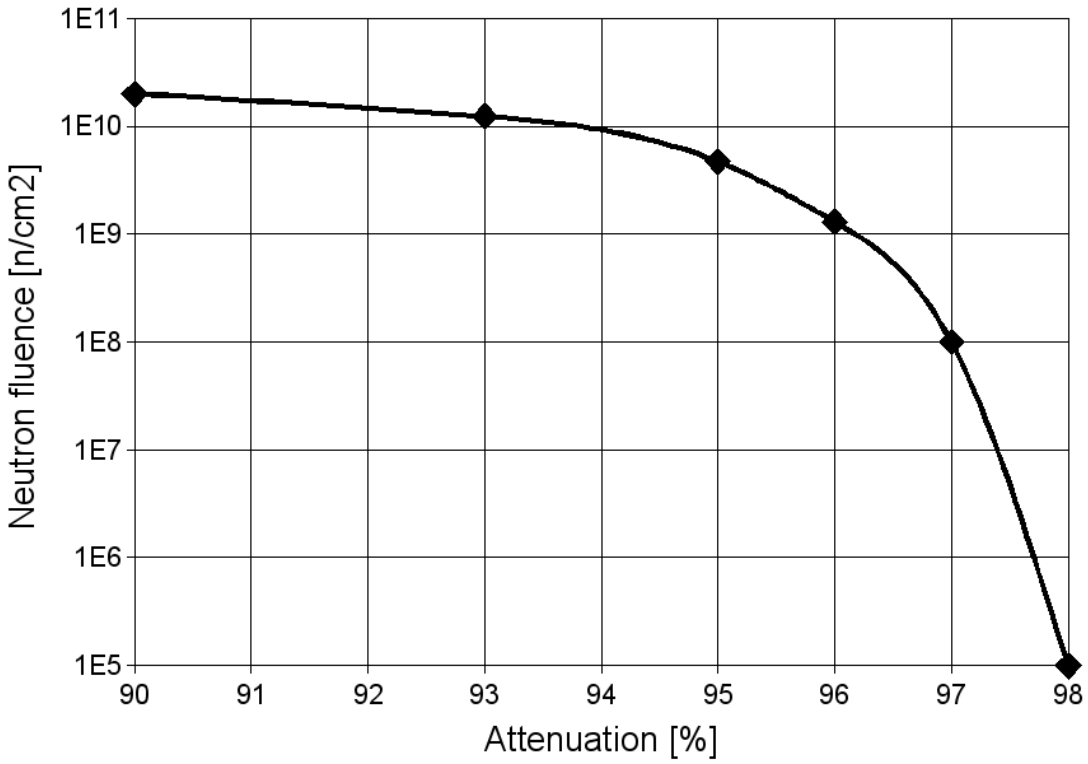

Figure 27: Calibration curve for LEDs irradiated with $^{241}Am/Be$ source

This experiment allows to calibrate Light Emitting Diodes for neutrons from $^{241}Am/Be$ source. The calibration curve is presented on Figure 27.

6.2 Estimation of irradiation effects in semicondutor memories at K130 cyclotron at University of Jyväskylä

Irradiation effects in semiconductor memories were investigated during irradiation at K130 cyclotron at University of Jyväskylä (see page 54).

We have tested folowing types of memories:

- SDRAM - ISSI IS42S16400 (64 Mbits, $0.18\mu m$ technology) [46],
- FLASH - AMD AM29LV160D (16 Mbits, $0.23\mu m$ technology) [45].

6.2.1 FLASH memories

We have tested three chips of FLASH memory. All memories survived the irradiation with beam intensity of $6*10^7 protons/cm^2/s$, up to the dose of $1.2*10^{11} protons/cm^2$, without any errors. Defects appeared during the irradiation with higher beam inensity (see Table 8).

There were only changes from ’0’ to ’1’, not in the other way. That’s because of method of storing data in the FLASH memory cell.

The errors appeared sequentially. First in the four least significant bits of the data word, then in the next eight bits, and so on. At the end, the values of all bits were ’1’. This complete damage of memory appeared after the total doses presented in Table 8. It is highly probable that these errors were a result of dynamic disturption of FLASH memory internal logic. [1][2]

Tests executed a few days after the irradiation experiments, revealed that FLASH memories stored the correct, programmed before data - the errors disappeared, but the erase function was still not working. This was probably caused by destruction of the charge-pump.

Confronting this results with other tests, it can be found that the most susceptible effects of Total Integrated Dose (TID) element in such devices is a charge pump. The memory cell itself is resistant enough and the SEEs during tests are results of SEUs in internal control logic.

# FLASH	First errors		Complete disturption	
	After total dose [$protons/cm^2$]	At beam current [$protons/cm^2/s$]	After total dose [$protons/cm^2$]	At beam current [$protons/cm^2$/s]
FLASH 1	$7.6*10^{11}$	$3.5*10^9$	$8.0*10^{11}$	$3.5*10^9$
FLASH 2	$5.95*10^{11}$	$3.5*10^8$	$6.5*10^{11}$	$3.5*10^8$
FLASH 3	$6.3*10^{11}$	$3.25*10^8$	Not investigated	

Table 8: The results of FLASH memories radiation experiments with proton beam K130 cyclotron at University of Jyväskylä - doses and beam currents for first errors and complete disturption

6.2.2 SDRAM memories

Complete, permanent destruction of memory was not observed. Only bit upsets (Single Event Upsets) appeared, but no stuck bits were detected.

The number of ’0’ to ’1’ upsets was approximately the same as the number of ’1’ to ’0’ upsets.

There were counted crosssections for tested memories:

- SDRAM 1 - $2.4*10^{-9}$ cm^2/device (2237 SEUs),
- SDRAM 2 - $1.6*10^{-9}$ cm^2/device (951 SEs).

Relatively lov values of crosssections may be a consequence of the high frequency of memory refreshing. Capacitors were charged to the proper voltage level so often that ionized particles could not change their potentials. [1][2]

The results are comparable with other made by different laboratories [30][31][32][33].

6.3 Measurements of static Single Event Upsets in FPGA chips

Static Single Event Upsets were investigated during irradiation of FPGA chips:

- at K130 cyclotron at University of Jyväskylä (see page 54),

- in Linac II tunnel at DESY (see page 55),
- in Tesla Test Facility II at DESY (see page 56),
- with $^{241}Am/Be$ neutron source (see page 58).

During experiments at K130 cyclotron at University in Jyväskylä there were used 3 boards Memec Spartan-IIE Development Kits (see Figure 28) [56] with Xilinx Spartan-IIE XC2S300E [55] chip onboard. The rest of irradiation experiments (in Linac II tunnel, in Tesla Test Facility II tunnel, with $^{241}Am/Be$ neutron source) were performed using Memec Virtex-II LC 1000 Development Kit (see Figure 29) [58] with Xilinx XC2V1000 [57] onboard. Characteristics of these devices are presented in Table 9.

Chip	XC2S300	XC2V1000
Technology	$0.18\mu m$	$0.15\mu m$
Power supply	1.8 V	1.5 V
System gates	300,000	1,000,000
Size of configuration bitstream	1,875,648 bits	4,082,592 bits

Table 9: Xilinx Spartan-IIE XC2S300 and Virtex-II XC2V1000 main parameters

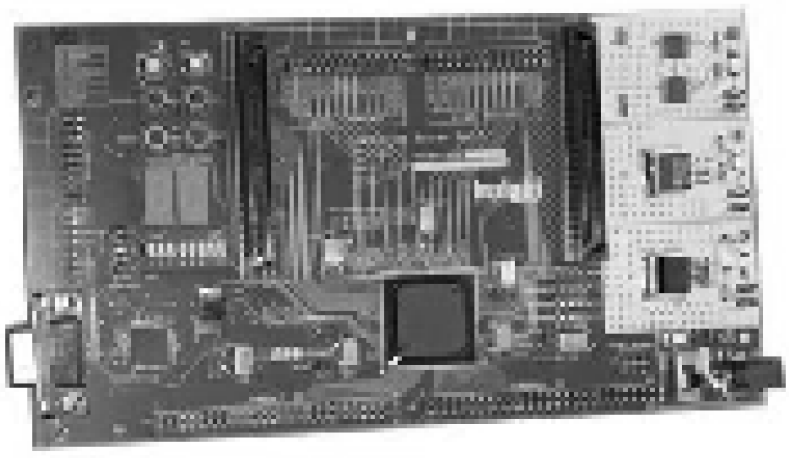

Figure 28: Memec Spartan-IIE Development Kit [56]

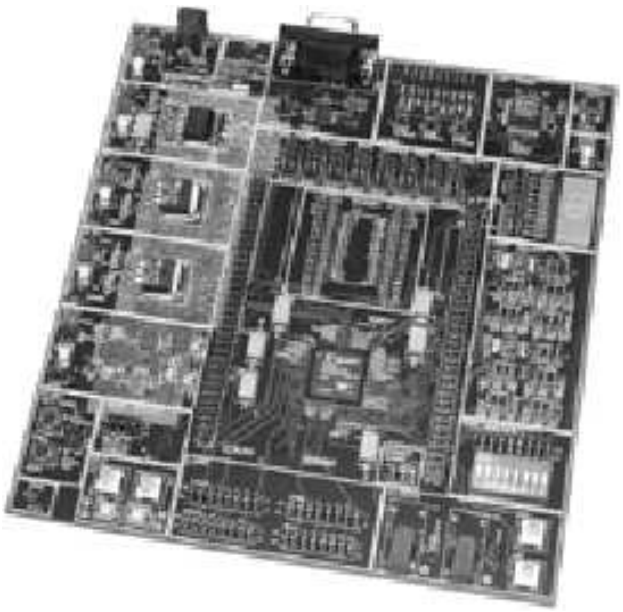

Figure 29: Memec Virtex-II LC 1000 Development Kit [58]

6.3.1 Experiments at K130 cyclotron at University of Jyväskylä

There were no permanent destruction of FPGA chips during irradiation experiments. Only dynamic Single Event Upsets were noticed. Using osciloscope there was attempt to observe dynamic errors, but there were none. Devices worked correctly after taking back from radiation environemnt. The results are presented in Table 10.

Protons energy [MeV]	# FPGA	dose [$1/cm^2$]	SEUs	σ/device [cm^2]	σ/bit [cm^2]
30	FPGA 1	$1.2*10^{12}$	25046	$2.0*10^{-8}$	$1.1*10^{-14}$
	FPGA 2	$2.5*10^{12}$	43859	$1.7*10^{-8}$	$9.3*10^{-15}$
	FPGA 3	$1.6*10^{12}$	29068	$1.9*10^{-8}$	$1.0*10^{-14}$
50	FPGA 3	$3.4*10^{10}$	770	$2.3*10^{-8}$	$1.2*10^{-14}$

Table 10: The results of FPGA radiation experiments with proton beam - SEU crossection

The results of irradiation experiments are very similar to achieved in other laboratories (see Table 11) [38][41][34].

Device	Technology	Protons energy [MeV]	σ/bit [cm^2]
Virtex XCV200	$0.22\mu m, 2.5V$	60	$1.3 * 10^{-14}$
Virtex	$0.22\mu m, 2.5V$	10-100	$2.4 * 10^{-14}$
Virtex E	$0.18\mu m, 1.8V$	10-100	$3.4 * 10^{-14}$
Virtex II	$0.15\mu m, 1.5V$	10-100	$7.5 * 10^{-14}$
Virtex II-Pro	$0.13\mu m, 1.5V$	10-100	$5.3 * 10^{-14}$
Spartan 3	$0.09\mu m, 1.2V$	10-100	$3.3 * 10^{-14}$

Table 11: The results of FPGA radiation experiments with proton beam achieved in other laboratories and experiments - SEU crossections

6.3.2 Experiments in Linac II tunnel at DESY

We have performed radiation experiments on configuration memory (static SEUs) of FPGA in Linac II tunnel. The device was placed near the entry to the tunnel, 20m from electron/positron converter, near the wall. Test was performed for 37 days of operational work of Linac II accelerator. During that time FPGA was programmed once a hour.

The results (number of Single Event Upsets per day and per hour and time before Single Event Upset) are presented on Figures 32, 30 and 31.

Figures 30 and 31 shows that there is not assurance that device survive without any errors for particular time. Time before first SEU after programming can be very short. In such strong radiation field, as is in Linac II tunnel, FPGA should be reprogrammed as often as it is possible.

The Figure 32 shows big dependence of Single Event Upsets number per day from PIA integrated current. That's the confirmation that SEUs are depended on radiation level.

No permanent damages were observed.

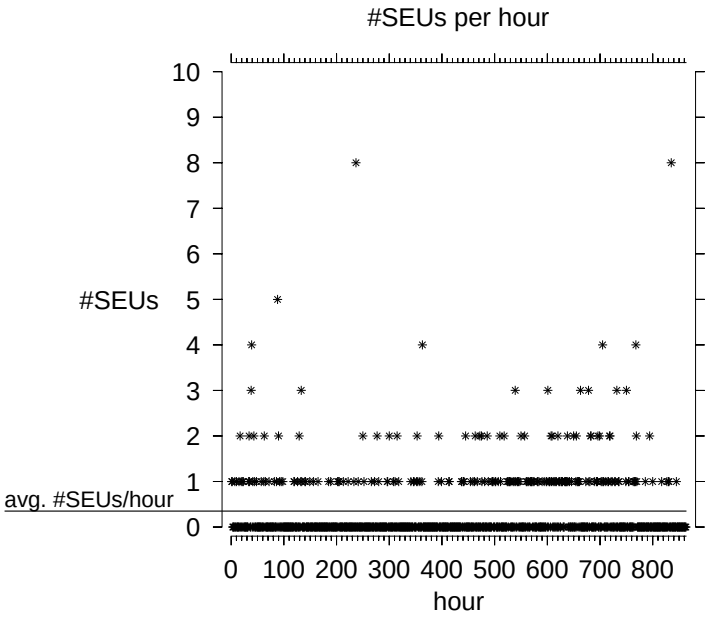

Figure 30: The results of FPGA radiation experiments in Linac II tunnel - Single Event Upsets per hour

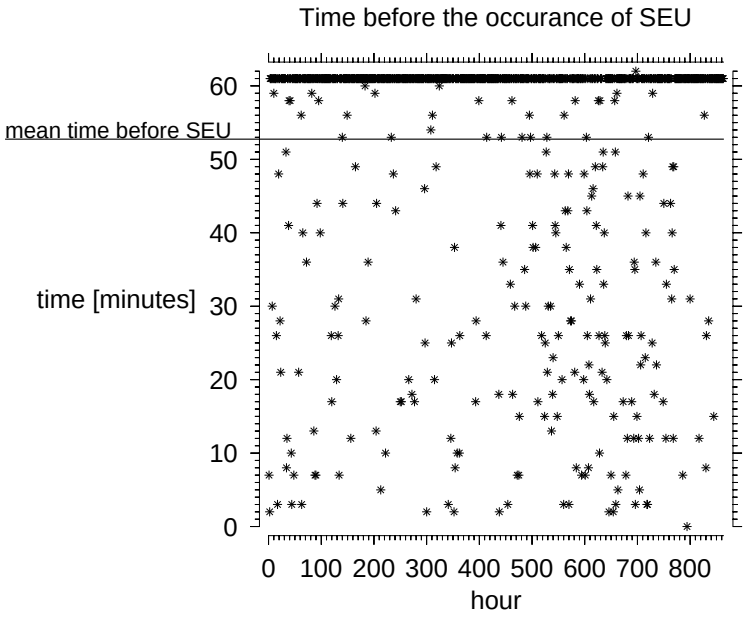

Figure 31: The results of FPGA radiation experiments in Linac II tunnel - Time before occurance of Single Event Upset

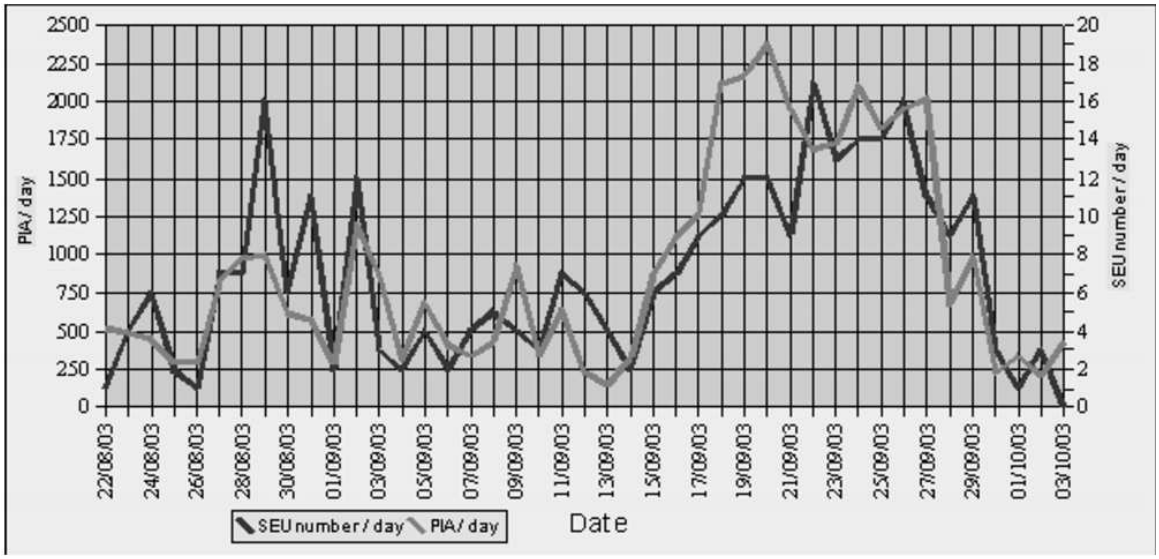

Figure 32: The results of FPGA radiation experiments in Linac II tunnel - Single Event Upsets per day and PIA integrated current per day

6.3.3 Experiments in Tesla Test Facility II tunnel at DESY

We have performed radiation experiments on configuration memory (static SEUs) of FPGA in Tesla Test Facility II tunnel. The device was placed just after first accelerating module, about 2 meters from accelerator tube, near the wall. Test was performed for 42 days of operational work of TTF II accelerator. During that time FPGA was programmed once a day.

The results (number of Single Event Upsets per day and time before Single Event Upset) are presented on Figure 33 and 34.

The avarage number of Single Event Upsets per day during the enitre experiment was about 1 (see Figure 33). It proves that FPGA could work in such environment without any severe problems because of SEUs.

The mean time from programming FPGA to first Single Event Upset during the whole experiment was about 15 hours (see Figure 34). It proves that often refreshing of the FPGA configuration memory prevents it from uncorrect work.

No permanent damages were observed.

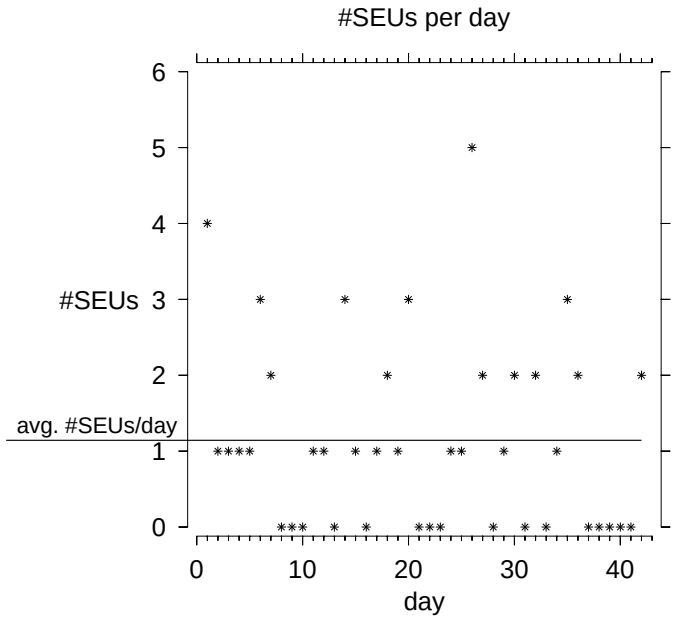

Figure 33: The results of FPGA radiation experiments in Tesla Test Facility II tunnel - Single Event Upsets per day

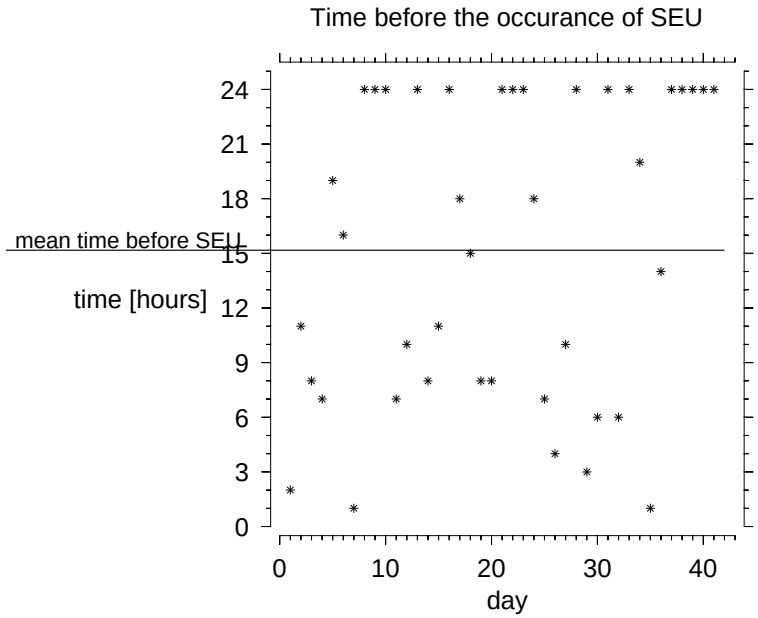

Figure 34: The results of FPGA radiation experiments in Tesla Test Facility II tunnel - Time before occurance of Single Event Upset

6.3.4 Experiments with $^{241}Am/Be$ neutron source

The configuration memory radiation experiments were done, to investigate static Single Event Upsets. The DUT was placed 10 cm away from the $^{241}Am/Be$ neutron source. The results of irradiation runs are presented in Table 12.

No	^{241}Am/Be source	water moderator	time [hours]	# SEUs
1	not present	not present	24	0
2	present	not present	24	9
3	present	present	24	2

Table 12: Results of FPGA irradiation experiments with $^{241}Am/Be$ source

In presence of light water moderator there are smaller number of Single Event Upsets. This moderator slows down the neutrons.

The results achieved in these experiments confirms with experiments presented in other publications [35]:

- small crossection of generation of ionizing particles by thermal neutrons,
- SEUs in FPGA caused mainly by fast neutrons.

7 Conclusions

The experiments presented in this thesis proved the radiation causes damages in electronic devices. There were presented measurement systems to investigate this phenomena in different kinds of components. All developed devices and software worked correctly, aiming the established goals.

Light Emmiting Diodes based fast neutrons dosimeter

The experiments with digital photometer for Commercial-Off-The-Shelf Light Emitting Diodes dosimeter proved that GaAs LEDs are useful as a detectors for fast neutrons. The idea of measuring neutron doses with Light Emitting Diodes introduces new method of dosimetry, which can be very competitve to other techniques, as for example to Thermo Luminescent Dosimeters (TLD). The comparison between TLDs and LEDs is presented in Table 13.

Important features of the dosimetry methods	Neutrons dosimetry using	
	TLDs	LEDs
Device sensivity	High	Low
Read-out method	Indirect, slow	Direct, fast
Cost of the sensor/detector	Low	Very low
Cost of the read-out device	High	Low

Table 13: Comparison of two dosimetry methods (with TLDs and LEDs) for the estimation of fast neutrons dose

The LED-based dosimeter can be useful in many applications:

- neutrons dosimetry for high fluxes (industrial and medical applications),
- fluence monitoring,
- electronic components damage monitorng,
- beam loss monitoring.

The main disadvantage is the necessity of calibrating Light Emitting Diodes for particular neutrons energy and type of used Light Emitting Diodes..

FLASH memories

The test system for semiconductor memories helped to understand that FLASH memories survives high dose before first errors, but the damage cannot be repaired. The experiments provide the informations needed to choose the memories to be used in CMS experiment in CERN. It was decided that FLASH memory is more reliable than SDRAM [1][2].

SDRAM memory and FPGA chips

The main problem in SDRAM memories and in FPGA chips (built in SRAM technology) are Single Event Upsets. There are caused by neutrons. Gamma radiation only limits the lifetime of devices but does not cause improper work.

Experiments proved that radiation mitigation methods should be used to ensure correct work of devices in radiation environment. Some of these techniques are presented in appendix for this thesis (see page 61).

A Irradiation facilities

This section presents the facilities which have been used for radiation investigations, presented in this thesis:

- The K130 cyclotron at University of Jyväskylä (Finland),
- Linac II tunnel at DESY (Hamburg, Germany),
- Tesla Test Facility II tunnel at DESY,
- Hahn-Meitner-Insitut (Berlin, Germany),
- The K100 neutron-therapy cyclotron at Harper University Hospital (Detroit, USA),
- $^{241}Am/Be$ neutron source.

A.1 The K130 cyclotron at University of Jyväskylä (Finland)

The K130 cyclotron is used to accelerate protons (2-75 MeV) and heavy ions. Area of beam illumination is adjustable and beam intensity is measured with the Faraday cup.[28] Devices Under Tests (DUT) are placed in the vacuum chamber (see Figure 35).

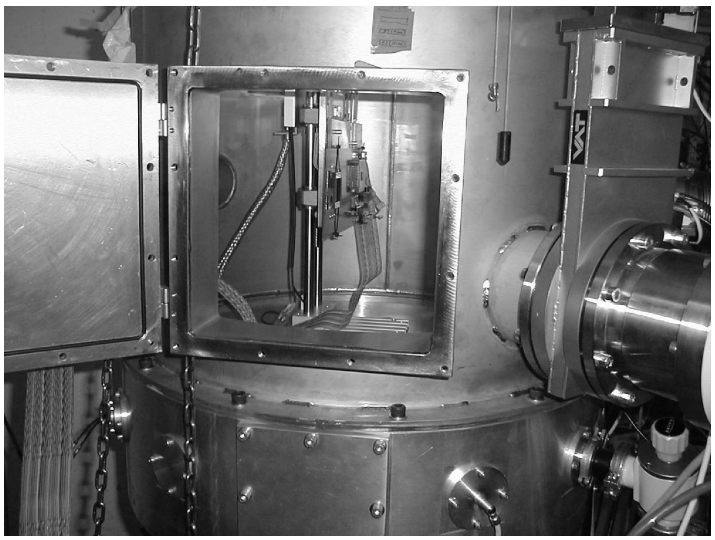

Figure 35: DUT inside vacuum chamber at K130 cyclotron at University of Jyväskylä

A.2 Linac II tunnel at DESY (Hamburg, Germany)

Linac II is DESY's only electron accelerator injecting high energy positrons or electrons (450 MeV) to booster synchrotron DESY II. It consists of two parts (see Figure 36). First one accelerates electrons produced by 150 keV electron source. Electrons with energy about 450 MeV hit the tungsten conversion target and produce electron-positron pairs. There are also neutrons and gamma radiation produced as a parrasistic radiation. The positrons are stored in Positron Intensity Accumulator (PIA), and then delivered to DESY II. [29]

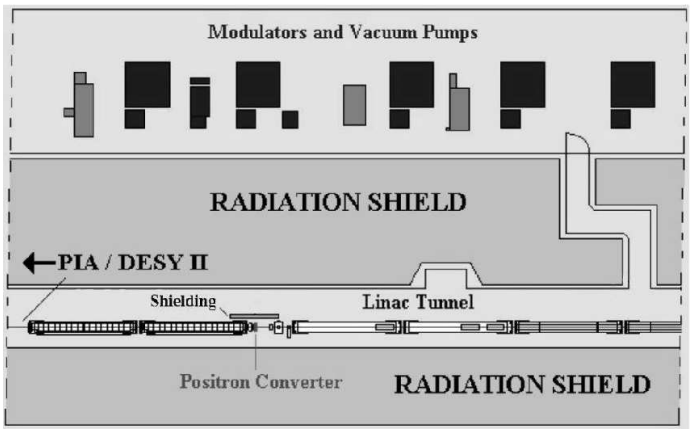

Figure 36: Linac II tunnel

The radiation environment in Linac II tunnel is not well known. The only value which can help quantify it is PIA current. PIA current coresponds to number of electrons hitting the converter and to parasitic radiation. The accumulated PIA current (PIA charge) corresponds to total neutron and gamma dose.

During the irradiation experiments Devices Under Tests (DUT) were placed in various positions along the tunnel (see Figure 36). Changing the distance between the DUT and e^-/e^+ converter allows to change radiation level. Its lowest value is near the entry corridor, about 20 meters away from the target and the highest value is near the converter. It should be pointed that electron-positron converter is placed behind the lead shield. This shielding reduces gamma radiation exposure to personel working in tunnel during the machine maintance, not affects the neutrons.

A.3 Tesla Test Facility II tunnel at DESY (Hamburg, Germany)

TESLA Test Facility II (TTF2) is a test system for TESLA technology and X-FEL experiment at DESY. It's built using the same technology as it will be used for future accelerators.

The DUTs were placed in different locations inside the tunnel (see Figure 37) to vary the radiation level. The experiments were done using unmeasured parasistic radiation during accelerator operation, mainly from cryogenic heatload.

Figure 37: TESLA Test Facility II tunnel

A.4 Hahn-Meitner-Insitut (Berlin, Germany)

At Hahn-Meitner-Institut large area irradiation of devices is possible by using a so called 'panorama' source. Several 30cm long ^{60}Co batons provide a radial field with very high intensity and Gamma rays avarage energy about $E_G = 1.25$ MeV during following phenomena:

$$^{60}Co \rightarrow ^{60} Ni* + e^- + \overline{\nu_e}$$

$$^{60}Ni* \rightarrow ^{60} Ni + \gamma$$

The calculated dose rates within a range from 1.6$kRad/h$ (2cm from source) to 220Rad/h (17cm from source) was achieved.

A.5 The K100 superconducting neutron-therapy cyclotron at Harper University Hospital (Detroit, USA)

This is the first superconducting cyclotron for medicine. It was designed and constructed at the NSCL (National Superconductiong Cyclotron Laboratory) and is now in use for cancer treatment at the Gershenson Radiation Oncology Center at Harper University Hospital in Detroit.

The cyclotron itself accelerates deuterons. Sometimes known as "heavy hydrogen", deuterons differ from normal hydrogen in that they have a neutron as well as a proton in their nucleus. The cyclotron's fast-moving deuterons are stopped in a target of beryllium just before their exit from the cyclotron. This produces a beam of high-energy (30 MeV) neutrons, which is then directed against the cancer patient's tumor (see Figure 38) or could be used for irradiation of electronic devices.

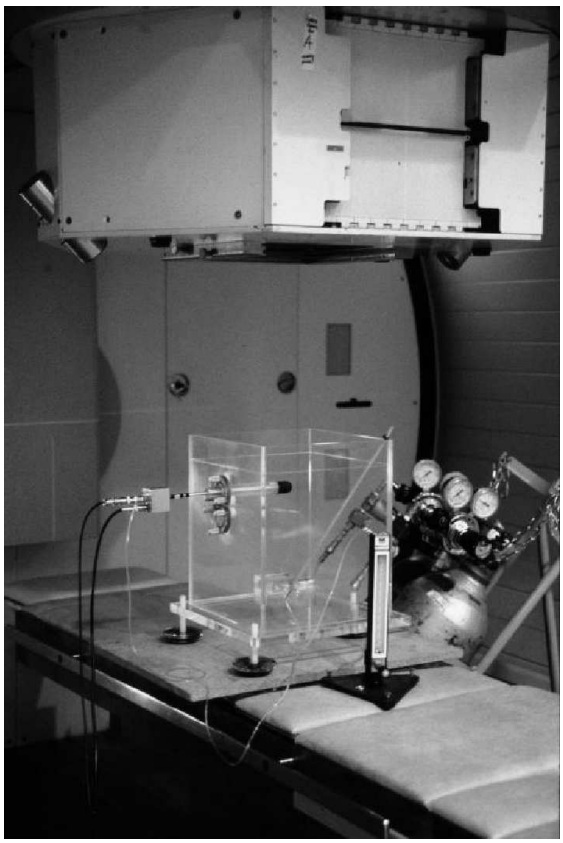

Figure 38: Harper Cyclotron phantom ion chamber for neutron calibration

A.6 $^{241}Am/Be$ neutron source

For the experiments there were used simple neutron irradiation facility with variable avarage energy using a light water moderated $^{241}Am/Be$ source (see Figure 39). The neutron spectrum of this setup is to be very similar to neutron field generated from electrons with energy about 1.6 GeV on niobium material. Niobium is the main constructing material of the TESLA cavities.

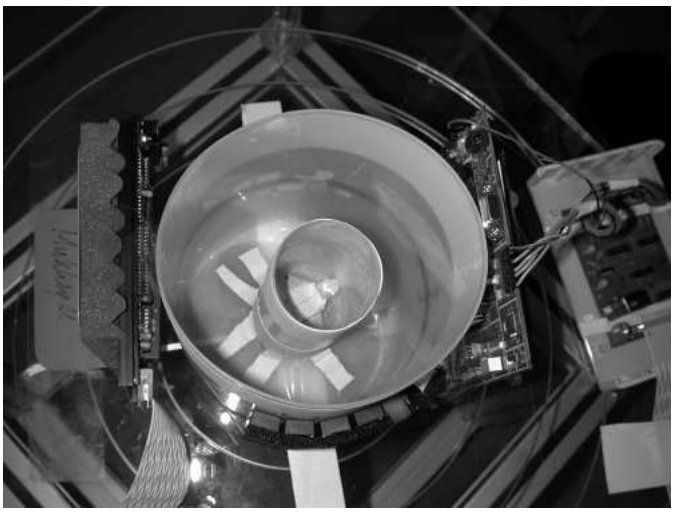

Figure 39: Plastic jar for $^{241}Am/Be$ neutron source and for water moderator

Using light water moderation the average neutron energy drops from 5.1 MeV to 3.3 MeV (for a moderator thickness of 6.5 cm). Maximum of neutron flux moves to low energy[10][26][27].

B Sources of Single Event Upsets

Relatively big charge should be deposited in a small (critical) volume to trigger SEU. Only heavy ions or alpha particles have big enough LET (Linear Energy Transfer) to produce such a big charge. But these particles have very short ramge (below about $10\mu m$), so they have to be produced near the most sensitive area by other particles with higher range (protons or neutrons).

There are different phenomenons producing secondary particles by neutrons or protons in the silicon [1][38]:

- Generation by high-energy hadrons ($E > 20MeV$).

  High-energy hadrons interact inelasticly with silicon nucleons producing the nuclear recoils (see Figure 40):

$$p(n) + Si \rightarrow \text{nuclear recoils} + ...$$

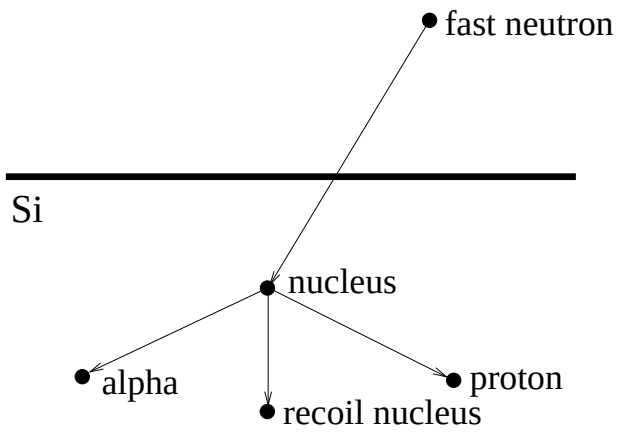

Figure 40: Generation of secondary particles by high-energy hadron (here: fast neutron)

- Generation by neutrons below $20Mev$.

  The low energy neutrons interacts with silicon nucleons mainly elasticly:

$$n + Si \rightarrow n + \text{recoiled } Si$$

- Generation by thermal neutrons.

  Thermal neutrons produce alpha particles in ${}^{10}B(n_{th},\alpha)^{7}Li$ phenomenon (see Figure 41):

$$ {}^{10}B + n \rightarrow {}^{7}Li + \alpha + \gamma $$

  Boron is a common dopant in the technology of ICs manufacture.

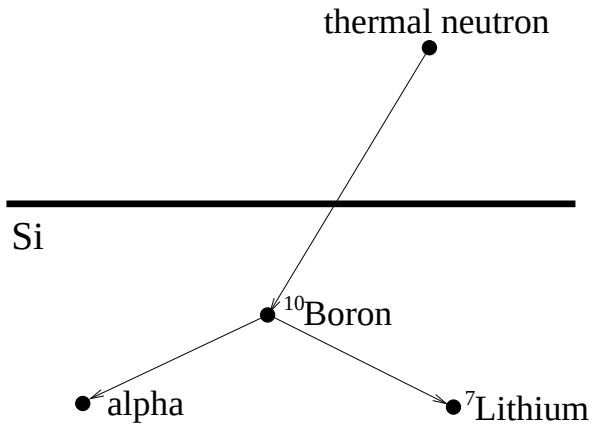

Figure 41: Generation of secondary particles by thermal neutrons in ${}^{10}B(n_{th},\alpha)^{7}Li$ phenomenon

C Overview on radiation mitigation techniques

Presented in this thesis experiments show the electronic devices suffer because of irradiation. To warrant proper work there are several radiation mitigation techniques:

- conventional shieldings,
- chips dedicated to work in irradiation environment,
- appropriate system design.

These ideas and methods are briefly discussed below. There are presented in details in other publications, eg. [20][39][40][41][42][43].

C.1 Conventional shieldings

The most important shielding is against gamma radiation. Neutrons for electronic devices is not a critical problem. They cause only not-permanent errors. Shielding against neutron radiation is less important.

Let us consider that the estimated maximum value of gamma radiation is about 10 rad / h = about 10^6 rad / 20 years (as it's predicted for ILC). The maximum Total Ionizing Dose for electronic devices is about a few krads. In this case gamma field should be reduced to 0.1 % to secure in-tunnel electronics. The best substance for this purpose is concrete. This material has HVL factor about 100 mm, for gamma radiation energy 5 MeV. Half-Value Layer (HVL) is the thickness of material to reduce gamma radiation to half [23]. To reduce gamma to 0.1 % there should be used $10 * 100mm = 1m$ of concrete wall.

C.2 Components dedicated to radiation environment

Some companies produce chips designed to work in high radiation environment. For example it could be XQR family of Xilinx FPGA chips (see Table 14. It has bigger (200 krads instead of tens krad) Total Ionizing Dose. This chips have longer lifetime exposed to high radiation.

There are also whole electronic systems dedicated to radiation environment. Maxwell company produces SCS750 board which includes 3 PowerPC on it (see Table 15). In comparison to commercial PowerPC it can withstand a dose in excess of 100 krad. It has also incredible high SEU rate ($< 9 * 10^{-6}$ upset per day on GEO orbit).

	Virtex-II (XC2V1000)	Virtex-II Q-Pro (XQR2V1000)
Technology	0.15 μm	0.15 μm
Number of system gates	1M	1M
Voltage supply	1.5 V	1.5 V
SEU rate		$< 1.5 * 10^{-6}$ upset/day (on GEO orbit)
TID	ab. tens krad (Si)	> 200 krad (Si)
Price	ab. 250 €	ab. 3500 €

Table 14: Comparison of commercial (Virtex-II) and rad-hardned (Virtex-II Q-Pro) FPGA chips

	Force Computers CPU-56	Maxwell SCS750
CPU	UltraSPARC-III+ 650MHz	3 * PowerPC 750FX with TMR in radhard FPGA
SDRAM	512MBytes ECC-Protected	256MBytes Reed-Solomon Protected
SEU rate		$< 9 * 10^{-6}$ upset/day (on GEO orbit)
TID	ab. few krad (Si)	> 100 krad (Si)
Price	ab. 5000 €	ab. 10000 €

Table 15: Comparison of commercial (Force Computers CPU-56) and rad-hardned (Maxwell SCS750) computers

These examples don't fullfil the market but there are good to show that the main disadvantage of rad-hard devices is the price (see Tables 14 and 15). It is even few times higher than price of normal, Commercial-Off-The-Shelf devices.

C.3 Appropriate system design

There are some methods to mitigate irradiation problems with electronic devices in earliest - designing stage. For example designer could use:

- cold redundancy (againsts problems with TID) [19][20],
- current Limiting (againsts problems with SEL, SEB) [19][20],
- software and hardware error detection and correction (againsts problems with SEU) [19][20],
- constant refreshing (againsts problems with SEU) [19][20],
- hot redundancy triple voting (againsts problems with SEU) [19][20][39][43].

D Overview on radiation safety

Experiments presented in this thesis were performed in irradiation environment, which is very hazardous to human health. Because of strict health safety regulations, the author had to obide by many restrictions, including the participation in radiation safety course every year.

The main safety rules are presented in this section. Thery are based on radiation protection instructions at DESY [24], and compying with international standards.

D.1 Authorities responsible for radiation protection

Every institute working with radiation has its own Radiation Protection Department. People working there (Radiation Safety Officers) are specialized to take care about radiation protection of other employees of the institute. In principle, they are responsible for:

- organising annual radiation safety courses,
- local dose measurements,
- personal dose measurements and monitoring these doses,
- reporting the exposure incidences.

D.2 Personal protection

The avarage background radiation dose for person per calender year is about $1mSv$. People, who may be exposed to higher dose, are regarded as occupationally radiation exposed persons. There are divided into two categories:

- category A - occupational health screening is necessary,
- category B - occupational health screening is not necessary.

Author of this thesis is consider as occupationally radiation-exposed person in category B. The maximum permissible doses are presented in Table 16.

Category	Dose
category A occupationally radiation-exposed persons	20mSv per calendar year
category B occupationally radiation-exposed persons	6mSv per calendar year
persons not occupationally radiation-exposed	1mSv per calendar year
pregnant women	1mSv during pregnancy
persons under the age of 18	1mSv per calendar year
occupationally radiation-exposed persons	400mSv dose throughout working life

Table 16: Maximum permissible personal doses

D.3 Radiation areas

Regarding local dose rates there are two types of radiation areas:

- Prohibited area - areas in which the local dose rate may exceed $3mSv/h$. If a local dose rate much higher can occur as a result of the operation of an accelerator, it must be secured by an interlock system. Access to a prohibited are is not allowed. Exceptions may be granted by a Radiation Safety Officer.
- Controlled area - area in which persons could receive an effective dose of more than $6mSv$ per calendar year (it corresponds to the maximum local dose rate of $3\mu Sv/h$). Controlled areas may only be entered if the following points are observed:
  - before entering persons must receive instructions,
  - persons enetring area must be equipped with the correst dosimeters,
  - area may only be entered in order to carry out the necessary work,
  - eating, drinking and smoking is not permitted.

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