The power chopper with forced extinguish and command realized with FPGA

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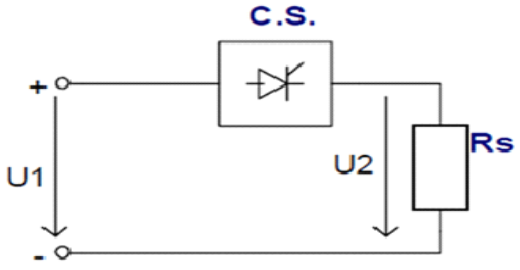
Abstract. This paper presents the operation of a chopper power with forced extinguish of reactive RC circuit whose control is obtained from a FPGA board (Nexis4DDR) for the adjustment of the frequency of the control software of the thyristors. Control signals for the two thyristors are obtained by dividing the clock frequency of the FPGA board which controls a 2-bit counter circuit made with flip-flops. The output of the FPGA board is connected to a current amplifying circuit realized with bipolar transistors in Darlington connection and a circuit for the galvanic separation with the pulse transformers and power supplies for opening the thyristor. The maximum frequency command value is limited by the recovery time of the main thyristor.

1. The paper's presentation

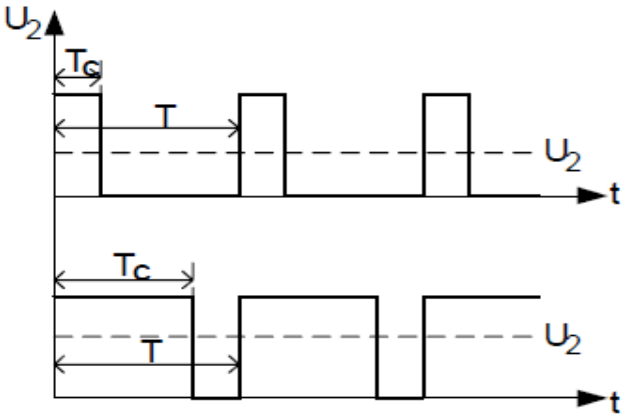
The modern conversion systems are power adjustable, with varying output parameters. The achievement of these systems involves the conversion of the electric car power source voltage, current, variable frequency, power converters known as static [1]. Old and new types of power semiconductor devices and the limits of voltages growth and currents work have enabled a much diversified range converters both in terms of type conversion and power voltages and work frequencies [1].

The power chopper is a CC-DC converter which allows the obtaining of a voltage and an output current variable in frequency according to the control switching element [2].

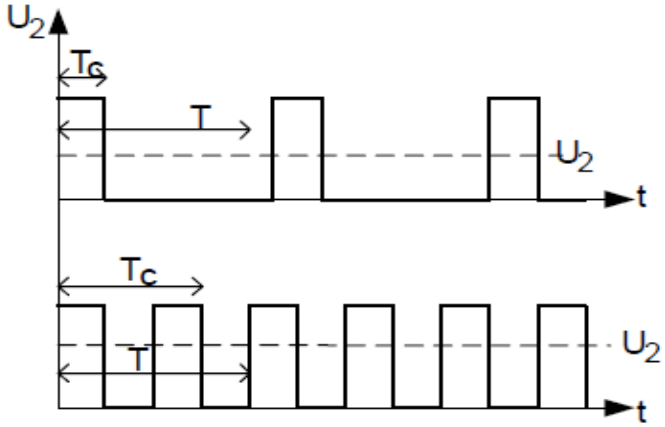
Figure 1.a) is the schematic diagram of a chopper power, whose essential element is the static contactor CS equipped with a thyristor [3]. Its role is to periodically interrupt the voltage applied to the load. In Figure 1b) is indicated how it interrupt the period T remains constant and modify hold time T_c voltage responses. In Figure 1c) it is constantly maintained the duration of the connection of the voltage tension and it is modified the switching period [3].



a)



b)



c)

Figure 1. a) The principle scheme of a chopper power, b) the operation to the constant T, c) the operation at constant T_c

Through U2 the voltage average load was noted. Referring to Figure 1b) and 1c), the average voltage will be:

$$U_2 = \frac{1}{T}\int_0^{T_c} u_2(t)dt = \frac{T_c}{T}U_1 = K \cdot U_1 \quad (1)$$

The size $K=T_c/T$ is called the command factor of the chopper [3], [4].

The control pulses are obtained from a FPGA development board (Nexis4DDR) programmable in Xilinx [5].

The control circuit designed in Xilinx contains a clock circuit and a two-bit binary counter and a selection circuit with logic gates [6].

Clock circuit consists of a frequency divider that divides the clock frequency (100MHz) board development [7]. The frequency divider software allows the set of the frequency command of the binary counter. The selection circuit allows obtaining control sequences output depending on the status counter [8].

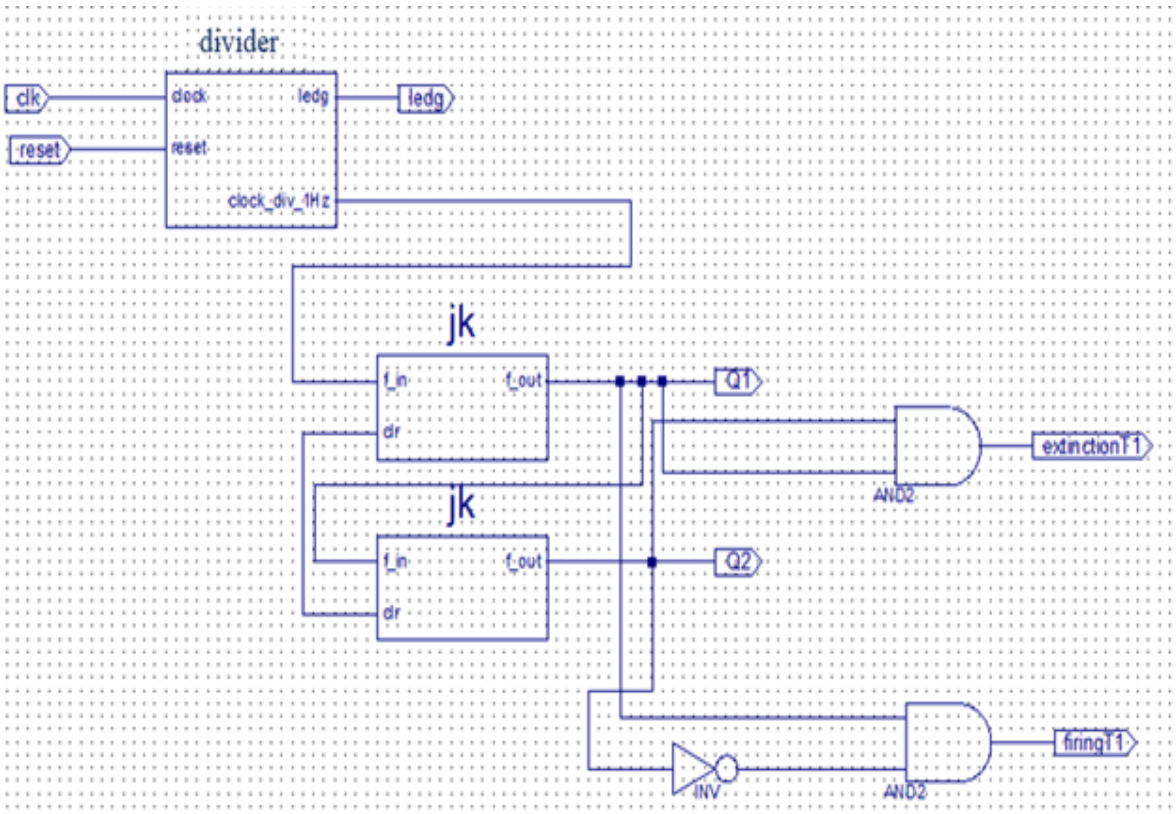


Figure 2. The control circuit designed in Xilinx

The frequency divider (Figure 2) provides an output frequency of 1 kHz which makes the output to have a frequency of 250 Hz, which value can be changed by setting soft divider [9]. This value can't grow more due to the time to return to the main thyristor that is of the ms order [10].

To obtain the command signal at the output pins of plaque development it was necessary to create the input and output file assignment of the designed circuit [11].

```
NET"clk"LOC="E3"  | IOSTANDARD = "LVCMOS33"; #Bank = 35, Pin name = #IO_L12P_T1_MRCC_35,
NET"clk" TNM_NET=sys_clk_pin;
TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 100 MHz HIGH 50%;
NET"reset"LOC=L16 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_RS0_15
NET"ledg"LOC=H17 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_A24_15
NET"extinctionT1"LOC=k15 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_RS1_15
NET"firingT1"LOC=j13 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_A25_15
NET"Q1"LOC=V12 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_A07_D23_14
NET"Q2"LOC=V11 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_A06_D22_14
```

Pin assignment file for the control circuit

The command signal for the thyristors chopper was visualized with the plate from Digilent Electronics Explorer Board (Figure 3).

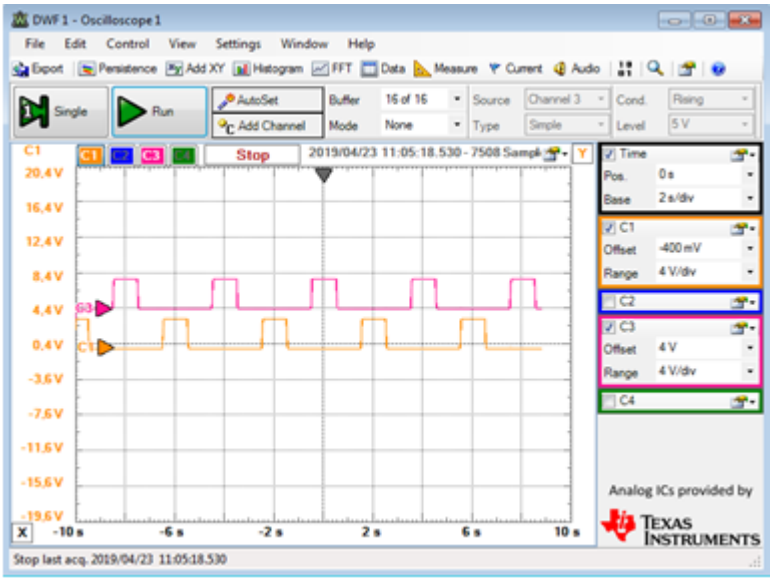


Figure 3. Command signals for the thyristors at the board's output FPGA

The output signals are passed through second inverting type CD 4069 which amplifies the power supplied by the FPGA board and also reverses the polarity (Figure 4).

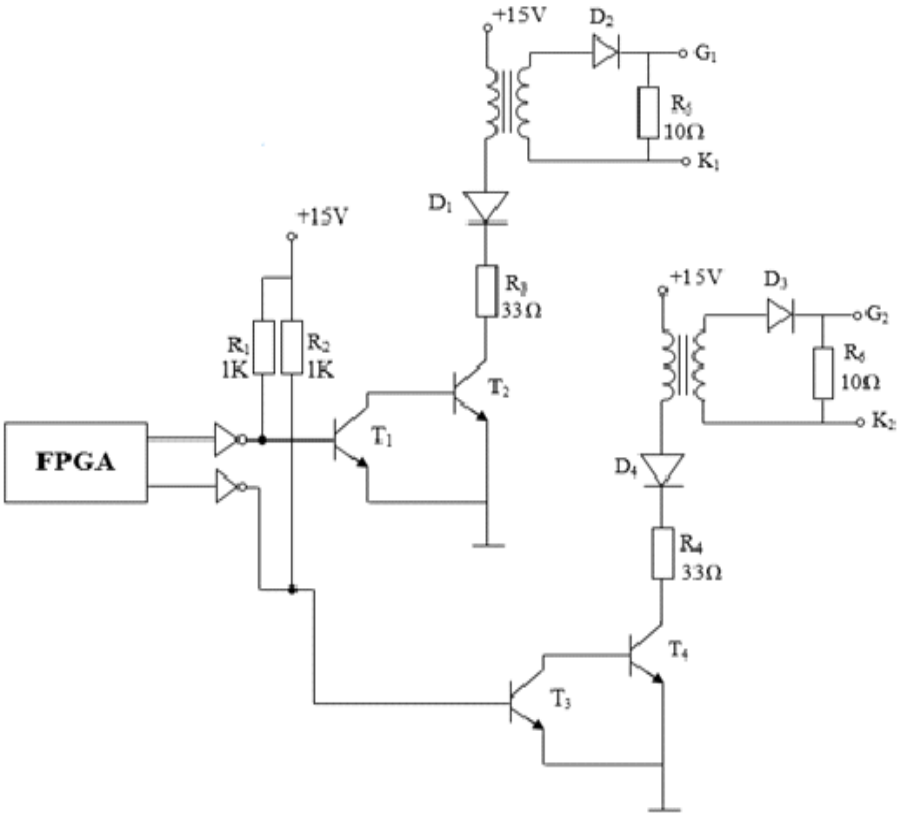


Figure 4. The thyristor command circuit

The transistors reverse again the command signal and so we have again the polarity of output signals corresponding to the thyristors' command. The needed power for the grid command circuits is obtained from the source of 15 V by pulse transformers controlled by Darlington connection [12].

Current amplifiers are made by a Darlington assembly BCY59 bipolar transistors (T_1, T_3) and 2N2891 (T_2, T_4). The pulse transformers are supplied from a secondary source of 15V and have protection diodes and resistors connected to the discharge junction of the thyristor GK. In series with the primary transformers protection diodes are connected to overvoltage of the transistors and current limiting resistors [13].

The signals output from the current amplifier circuit and galvanic separation matrices are brought to the thyristor chopper (Figure 5).

Chopper power with forced extinguish with circuit RC. The switching elements are thyristors of power, the main thyristor is TB171-200-10-444 type (T_{h1}) and the quenching thyristor T100N-1800-BOF-57 (T_{h2}) [14].

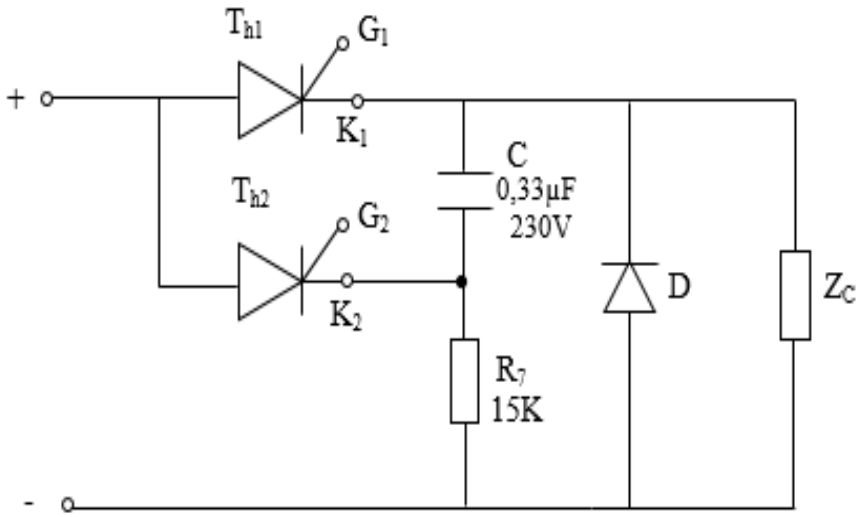


Figure 5. Wiring diagram of the chopper power

The condenser is charged through the resistance R_7 along with the main thyristor. To extinguish the thyristor T_1 the condenser will be connected, loaded with positive polarity+ in its cathode by priming the auxiliary thyristor T_2 [3]. The condenser must reverse biased Q_1 for a longer time than the time of his return. After blocking the thyristor T_1, the thyristor T_2 will be blocked due to the decrease of current that passes through it below the value of the latching current [3].

2. Experimental results

Highlighting the chopper operation was made on resistive load with a digital oscilloscope signal acquisition. For the frequency of 1 kHz are showed command signals to the thyristor grid (Figure 6) or the auxiliary thyristor (Figure 7).

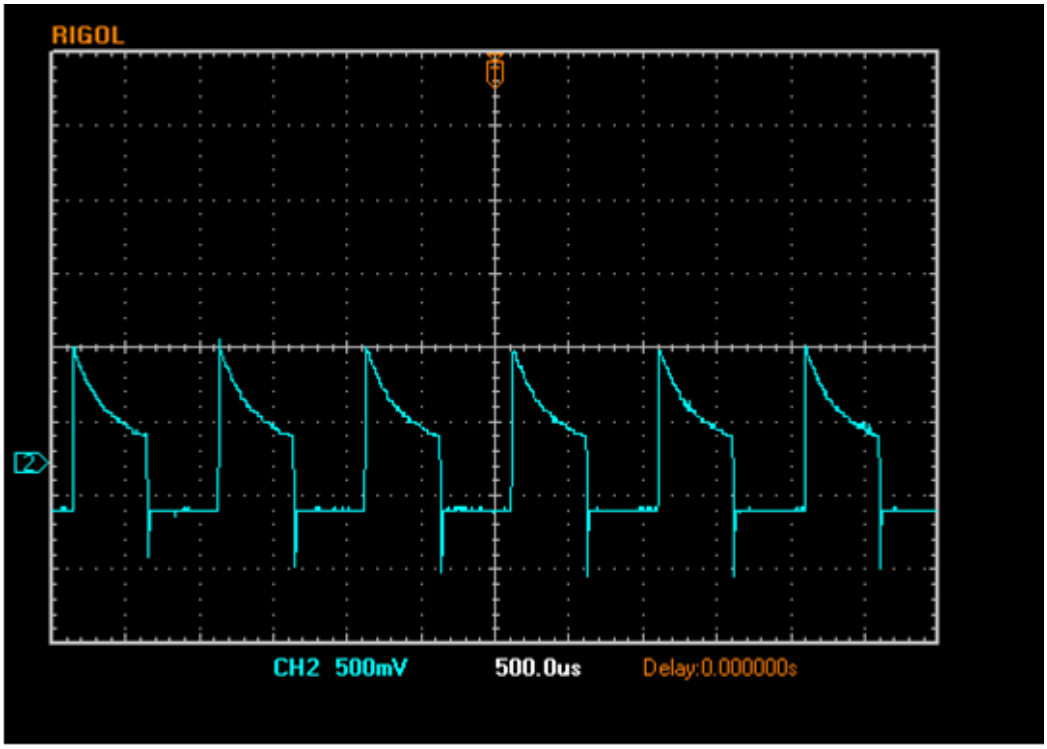


Figure 6. Command impulses main thyristor

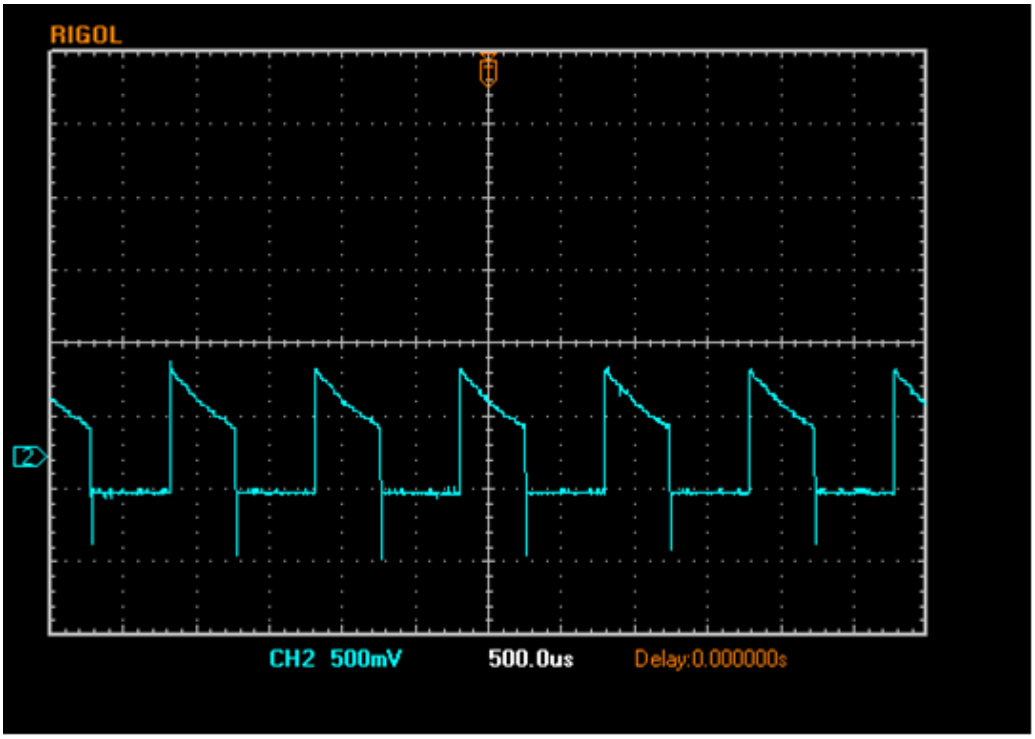


Figure 7. Command impulses auxiliary thyristor

Waveforms in the cathode of the thyristors (Figure 8) reveals the operation of a chopper voltage of the resistive alimentare100 V and a consumer of 300 W. The signals were acquired through the probe attenuation of 1:10. It can be seen around zero value the auxiliary thyristor and the main thyristor

blocking during the jump of the ignition voltage at its cathode main thyristor. SCR cathode auxiliary tension begins to decrease with load capacitor fighting, a value which is consistent with the representation of the capacitor voltage (Figure 9).

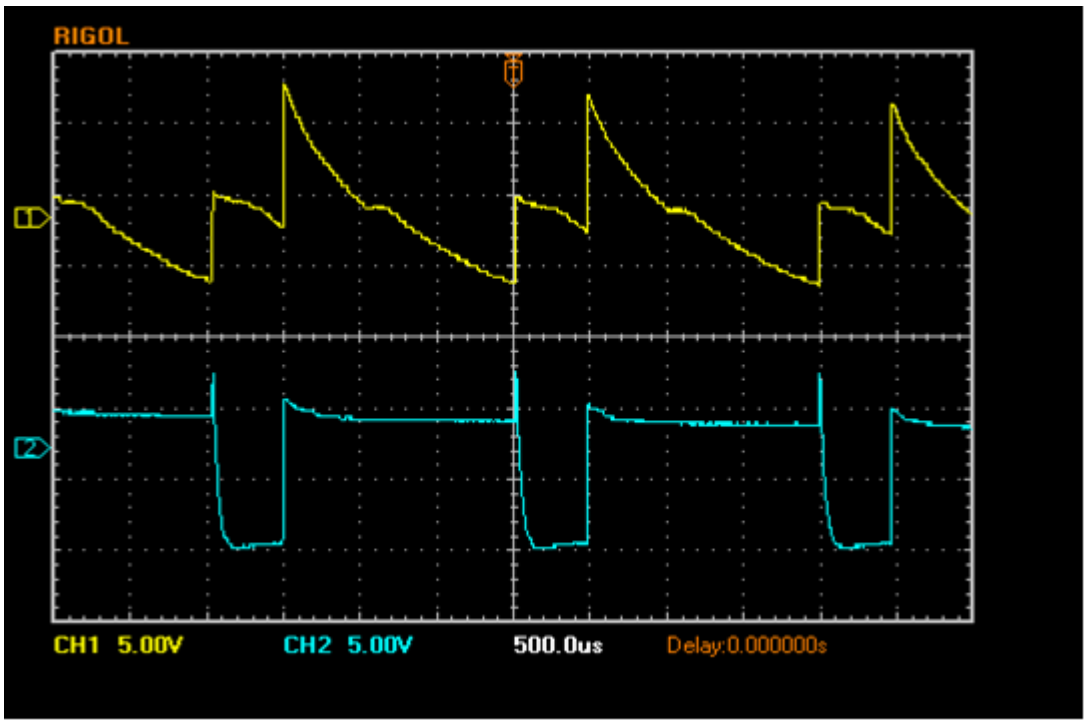


Figure 8. The tension of the thyristor cathode 1-voltage in the auxiliary thyristor cathode, 2- the main thyristor cathode voltage

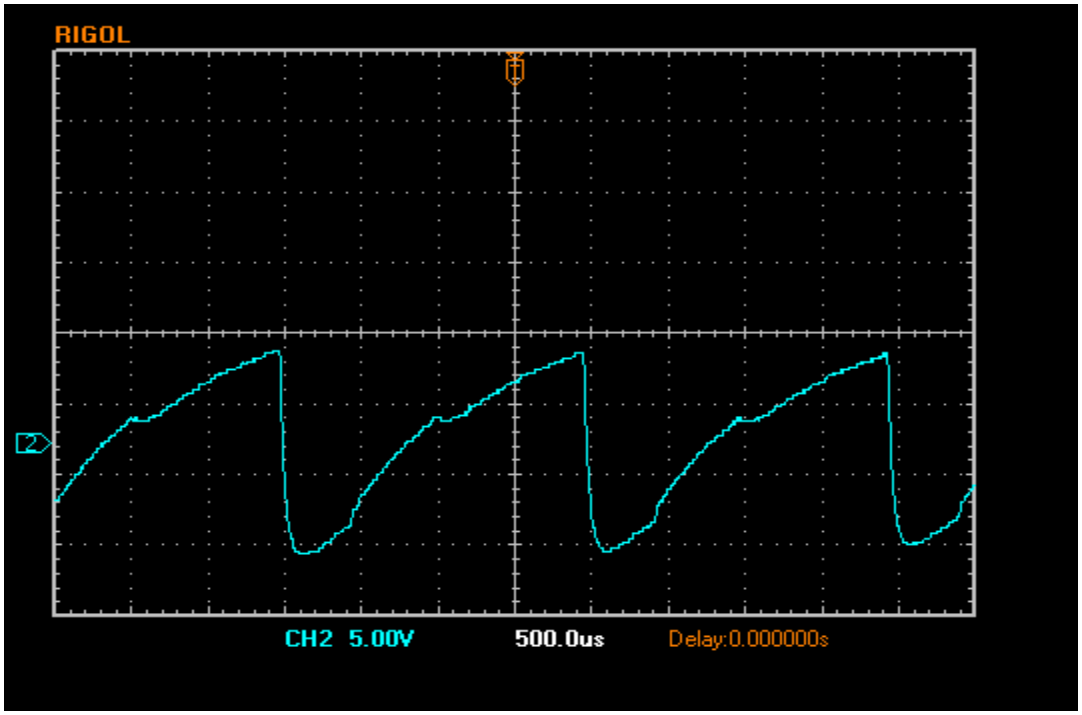


Figure 9. The tension on the extinguishing condenser

The practical realization of the assembly (Figure 10) highlights the connections of the chopper to the FPGA board (Nexis4DDR) and to the current source respective to the resistive consumer of 300W.

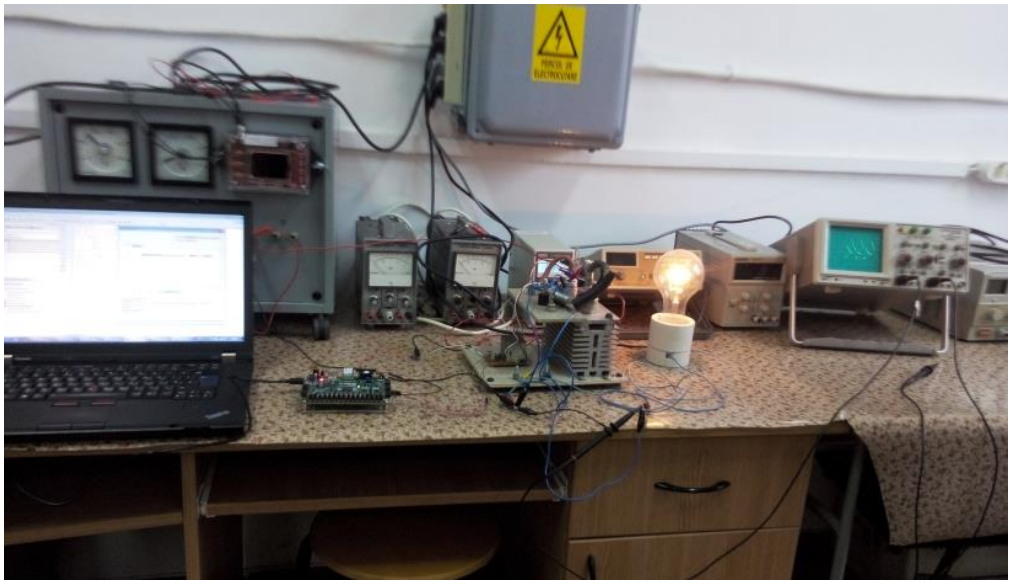


Figure 10. The reals scheme of the chopper functioning

3. Conclusions

The chopper power circuit of extinguishing RC has the advantage of eliminating the induction of the extinguishing circuit.

The chopper is controlled in open loop and allows adjustment of frequency control software.

The present diode of null of the output circuit performs the protection of the main thyristor overvoltage.

The experiments were done for the resistive load but the functioning is similar to the inductive load.

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