# Design and Implementation of Diode Clamp five-level Inverter Topology based on the modified SPWM method

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**Abstract**. The development of power electronics especially the inverter is required to be able to convert DC voltage to AC voltage. Multilevel inverters can provide an AC voltage power output, which has lower THD and better sinusoidal waveform. In this case, the voltage which is not sinusoidal and contains higher THD can shorten the durability of applied electronic devices. IEEE has a standard that has been established as a general guideline for the use of power supply standards which is not more than 5%. The modified SPWM technique is able to provide a good quality of output by shifting the phase of the carrier signal. In this paper is proposed diode clamp five-level inverter topology based on the modified SPWM, the whole system has been simulated through PSIM software and the laboratory tests have been carried out to verify the proposed method. Several waveforms are shown to validate the performance of this five-level inverter.

## 1. Introduction

The developments of power electronics are increasing in need of good quality resources. Alternative energy sources such as inverters, which are able to convert DC (Direct Current) voltage to AC (Alternating Current) voltage. Conventional inverters have a poor shape of sinusoidal waveforms and high percentage of THD (Total Harmonic Distortion). In this case, the voltage which is not sinusoidal and high THD can shorten the life of electronic devices. Conventional inverters produce poor sinusoidal waveforms [2]. Conventional inverters have an output waveform which is greatly affected by the switching frequency. The higher the frequency of switching, the output waveforms are getting closer to sinusoidal [3]. Inverter required low output THD, so it can be applied as a power supply for better performance [4]. Better voltage conversion results can be obtained through multilevel inverters based on the SPWM technique [5].

The multilevel inverter of diode clamp topology produces an AC voltage level by dividing the voltage sources. Many types of inverters are able to supply the demand for high-quality power and lower output of the THD [7, 8]. Inverters multilevel based on topology are divided into three types. The types are half-bridge cascades [9], diode-clamps [10], and flying capacitors [11]. The cascade inverter combines two inverters connected in series [9]. Inverters with diode clamp topologies use diodes to limit the voltage flow that occurs in semiconductor devices [11]. Multilevel inverters with a flying capacitor topology use a capacitor to divide the input DC voltage. Even though the inverter with Half-Bridge topology is widely used, this topology has many disadvantages such as higher THD and power loss. This has an impact on electronic devices [12, 13].

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In the proposed five-level inverter, two IGBTs (Insulated Gate Bipolar Transistor) is used as power switches which contains eight MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) switches and four diodes. This paper describes the modes of operation and the SPWM (Sine Pulse Wide Modulation) strategy by shifting phase degree. The spectral errors of the pulse width modulated waveforms are mainly caused by the commutation dead time, the conducted switch and fall time [14]. Spectral errors caused by the above two inherent distortion sources are usually in the acceptable range and can be neglected if proper switching devices and switch timing are used [14]. In this case, it has the most significant impact on the inverter output waveform spectral errors [15]. This proposed method is presenting the modified SPWM method for diode clamp topology types of a multilevel inverter. Various output wave simulation and experimental output of THD is presented to verify the performance and to validate the IEEE standard (under 5%), that appropriate of output THD of the proposed method.

## 2. Research and Method

This paper is made to validate the ability of the proposed method and the results of simulated of the proposed inverter. In this case, five-level inverter diode clamp topology of used. This section presents circuit design configuration, operation modes, strategy, and system of the configuration that use of the proposed method.

### *2.1 Circuit Design Configuration*

The five-level inverter of diode clamp topology uses eight static MOSFETs switches and four passive diodes that have high-frequency switching in the form of two IGBTs, that are supplied by two DC voltage sources adjusted to produce a voltage level. The power circuit operates at a 50 Hz frequency to produce AC voltage output.

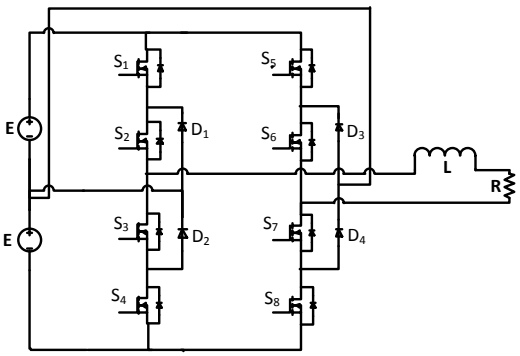
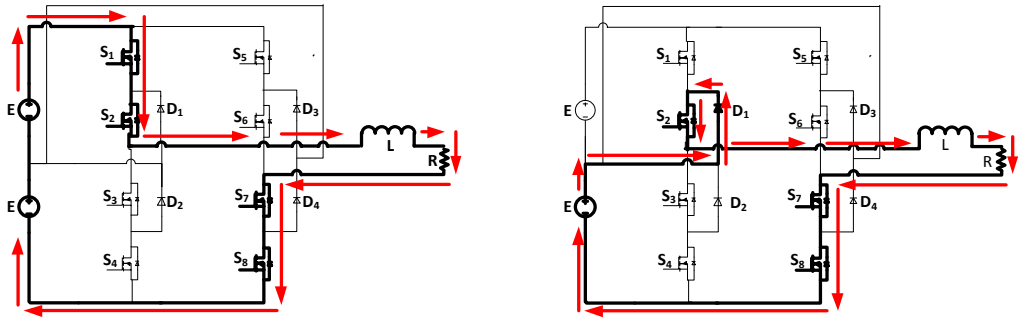



**Figure 1.** The proposed five-level inverter diode clamp topology

### *2.2 Switching Operation Modes*

In this 5-level inverter has three operation modes : positive, negative, and freewheeling. The working principle of this 5-level inverter is shown in these operation modes as follows:




(a) (b)

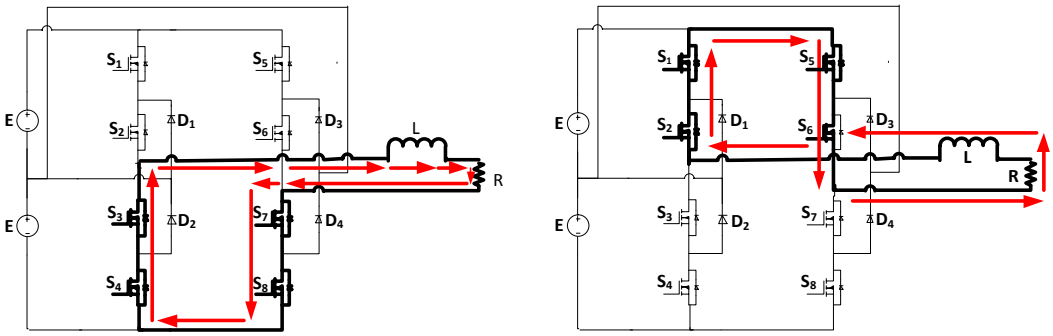
**Figure 2.** Operation modes with positive cycles (a) the first operation mode at output voltage (+2E) switching flows in $S_1$, $S_2$, $S_7$, and $S_8$. (b) the second operation mode at voltage output (+E) switching flows in $S_2$, $D_1$, $S_7$ and $S_8$.

Positive cycle at first operation mode, the equation can be stated as follows:

$$V_{in} = V_L + V_o$$
$$2E = L\frac{di_1}{dt} + V_o \quad (1)$$

Positive cycle at second operation mode, the equation can be stated as follows:

$$V_{in} = V_L + V_o$$
$$E = L\frac{di_1}{dt} + V_o \quad (2)$$



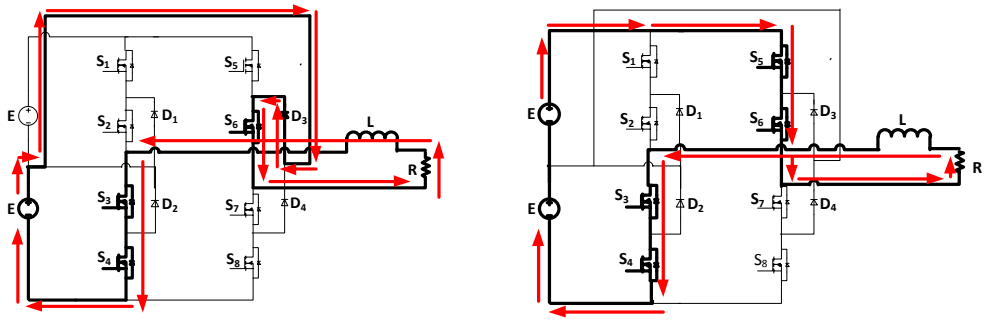

(a) (b)

**Figure 3.** Operation modes with freewheeling (a) The third operation mode at freewheeling (0) switching flows in $S_3$, $S_4$, $S_7$ and $S_8$. (b) The fourth operation mode at freewheeling (00) switching flows in $S_1$, $S_2$, $S_5$ and $S_6$.

Freewheeling conditions occur in the third and fourth operating modes. The current flow in the positive cycle ($S_1$, $S_2$, $S_6$, $S_5$) and the negative cycle ($S_3$, $S_4$, $S_7$, $S_8$). The equation for the third and fourth operation modes are stated as follows:

$$V_o = L\frac{di_0}{dt} \quad (3)$$

Negative cycles those occur in the fifth and sixth operating modes:




(a) (b)

**Figure 4.** Operation modes with negative cycles (a) the fifth operation mode at voltage output (-E) switching flows in $D_3$, $S_6$, $S_3$ and $S_4$. (b) the sixth operation mode at voltage output (-2E) switching flows in $S_5$, $S_6$, $S_3$ and $S_4$.

Negative cycle at fifth operation mode, the equation can be stated as follows:

$$V_{in} = V_L + V_o$$
$$-E = L\frac{di_1}{dt} + V_o \quad (4)$$

Negative cycle at sixth operation mode, the equation can be stated as follows:

$$V_{in} = V_L + V_o$$
$$-2E = L\frac{di_2}{dt} + V_o \quad (5)$$

Based on the switching conditions above, the operation switching modes displayed in Table.1.

**Table 1**. Operation Switching Mode

| Operation Mode | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | Vout |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 2E |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | E |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 4 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 00 |
| 5 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | -E |
| 6 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | -2E |

Where number "1" in order to explain the switch conducting and "0" explain the switch non-conducting.

*2.3 Strategy of Configuration*

The multilevel inverter produces output similar to sinusoidal wave and has lower output THD. Lower output THD means better inverter quality, the amount of THD is regulated by IEEE standard [14]. Conventional SPWM method created higher THD that cause many disadvantages, such as shorten the durability of applied devices and losses power. In order to reduce the distortion, it can be solved by proper control technique. This paper proposed SPWM modified control techniques by shifting the electrical phase degree to reduce the harmonic components.

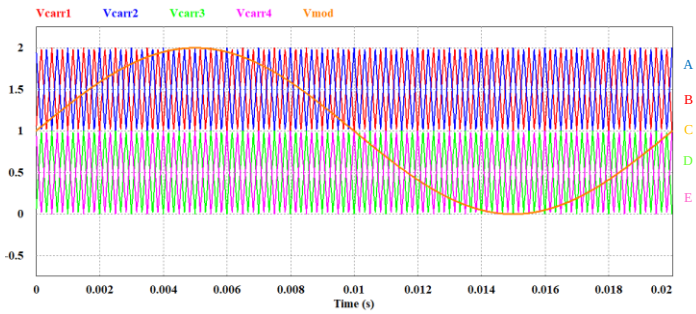



**Figure 5.** The simulated carrier signals and SPWM output (A) The output of $V_{carr1}$ carrier signal (B) The output of $V_{carr2}$ carrier signal (C) The output of sinusoidal modulation carrier signal (D) The output of $V_{carr3}$ carrier signal (E) The output of $V_{carr4}$ carrier signal

The equation based on signal modulation for the first operation mode in output voltage.

$$V_o = \frac{Vref}{Vcarr} \times E \tag{6}$$

The equation based on signal modulation for the second operation mode in output voltage.

$$V_o = \frac{Vref}{2Vcarr} \times E \tag{7}$$

The equation based on signal modulation for the third operation mode in output voltage.

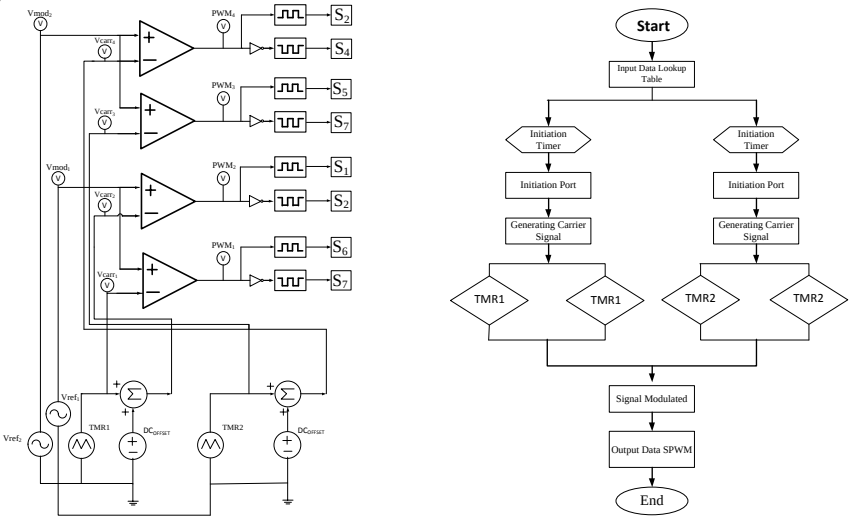
$$V_o = \frac{Vref}{3Vcarr} \times E \tag{8}$$

The equation based on signal modulation for the fourth operation mode in output voltage.

$$V_o = \frac{Vref}{4Vcarr} \times E \tag{9}$$

Where $V_o$ is generated by carrier signal and divided by reference signal then, multiplied by the input voltage.

*2.4 System Configuration*




(a) (b)

**Figure 6.** The proposed configuration system (a) SPWM technique control of the proposed inverter (b) flowchart of the proposed inverter

The process of generating SPWM signals is conducted by adding lookup table data to create the sinusoidal signal. The initialization of the timer (TMR) and PORT in microcontroller are required for carrier signal generation. The signals are created after port initiation and port declaration of four carrier signals were conducted. After those four carrier signals are modulated with lookup table data (sine reference) to produce SPWM signal which is the output signal of the microcontroller. SPWM schematic control is shown in figure 6 (a). The flowchart of the switching pattern using logic control is shown in figure 6 (b).

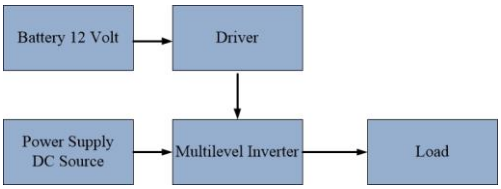



**Figure 7.** Block diagram of the proposed inverter

The proposed inverter diode clamp topology is divided into two parts, the power section and the control section with separate voltage sources. The block control has been supplied by 12 DC Voltage. The block control consists of dsPIC30f4012 microcontroller, 74HC541AN buffer IC, and optocoupler TLP250. The DC power supply voltage value can be adjusted as power source to the inverter.

## 3. Results and Discussion

Experimental results and analysis were conducted in the laboratory. Parameters of the prototype are presented in Table 2. The results of laboratory tests of the proposed inverter can be seen as follows:

### *3.1 Hardware Implementation of proposed inverter*

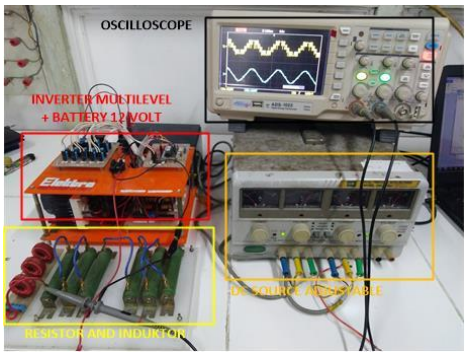


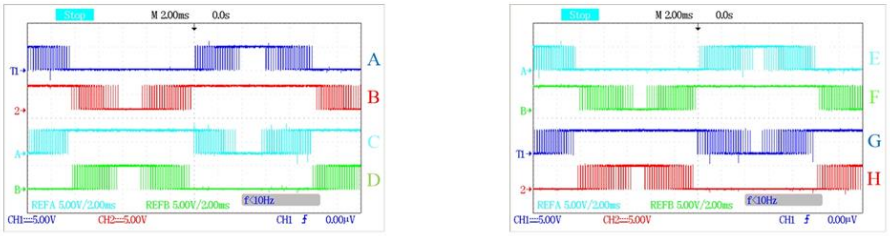

**Figure 8.** Hardware implementation of the proposed inverter

*The proposed inverter has a DC input power source with an adjustable DC voltage and has two output voltages. In this case, the output voltage is set to 25 DC voltage. This inverter is loaded with a 7.5 mH inductor and a 62 Ohm resistor.*

**Table 2.** Parameter of the experimental hardware implementation

| Parameters | Units |
|---|---|
| Vin | 2 x 25 $V_{DC}$ |
| Inductor | 7.5 mH |
| Resistor | 62 Ohm |

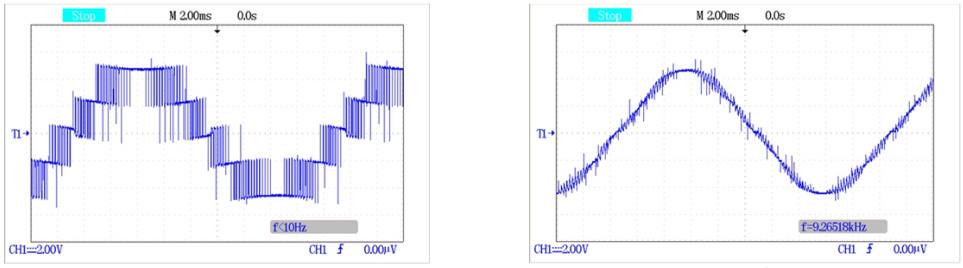
*3.2 Prototype results of the Proposed Inverter*




(a) (b)

**Figure 9.** Experimental results of the output signals SPWM (a) where A is $S_1$, B is $S_2$, C is $S_3$, D is $S_4$. and (b) where E is $S_5$, F is $S_6$, G is $S_7$, H is $S_8$.

The SPWM signal generated from the microcontroller is passing to the buffer for optimize the signals. So that it can be processed by the optocoupler in order to operate the static switches. The sinusoidal signal obtained from a 50 Hz frequency lookup table data.




(a) (b)

**Figure 10.** The prototype results of the output voltage waveform (a) after resistor and inductor (b) at resistor voltage of the proposed inverter

The voltage in the resistor after passing the inductor is shown in figure 10 (a). The voltage in the resistor is shown in figure 10 (b). The output voltage level is generated from first level to fifth level sequentially +50V, +25V, 0V, -25V, -50V. The proposed inverter can produce a voltage that can be adjusted to the input voltage and needs.

*3.3 Experiment Result of Total Harmonic Distortion*

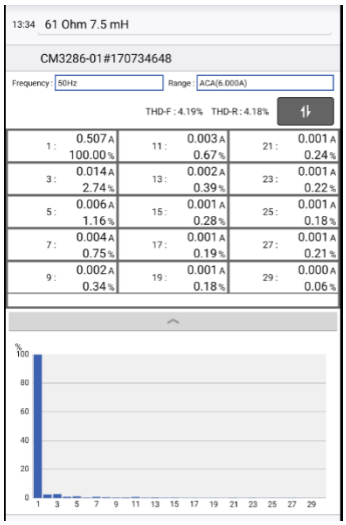



**Figure 11.** THD experimental result in the proposed inverter at measurment device

The laboratory test result is shown in figure 11. The results of the THD output are obtained from the Hioki AC power meter clamp CM3286.

## 4. Conclusion

Five-level inverter diode clamp topology is presented in this paper. The proposed method is able to reduce harmonic components that cause the higher THD output compared to other multilevel inverter methods. The proposed modified SPWM control schemes can achieve the desired fundamental amplitude and eliminate harmonic components caused by the DC voltage source variation. The proper THD output standard is under 5% (IEEE guidelines). THD value can adversely affect electronic devices. The proposed inverter has been operated to verify the proposed method. This proposed inverter has 4.18% THD output. Based on the results the proposed inverter can be recommended as an alternative power supply in accordance with the guidelines given by the IEEE.

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