A SPWM Controlled Input in Dual Buck DC-DC Converter – Full Bridge for Single-Phase Five-Level Inverter

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Abstract. The inverter is very important to be implemented on a power plant system, the principal operation of inverter is a power conversion from DC to AC output. A five-level inverter produces a high-quality total harmonic distortion output side. This paper presents a single-phase five-level inverter using a sinusoidal pulse width modulation (SPWM) controlled in dual buck DC-DC converter and full bridge inverter. The proposed topology is a hybrid converter: dual buck DC-DC converters to generate SPWM voltage level with high frequency and full bridge inverter to generate polarity. This method is very effective to predict the high frequency power semiconductor in dual buck DC-DC converters. The other side the full bridge inverter just need a low frequency. By this method, the gating signals for power semiconductor switches are generated by employing simple pulse width modulation. The fist verification of this topology is by simulation using PSIM software. Finally, a microcontroller dsPIC30F4012 is used in laboratory experiment for the last verification.

1. Introduction

The development of technology in term of power electronic nowadays has already advanced especially in the field of the power system. The use of renewable energy system such as solar cell has now been on raising demand. The output produced by a renewable energy plant is direct current type (DC) which is incompatible with the most standard electrical equipment supplied (Alternating Current) [1]-[2]. Presence of the inverter is very important in power plant system, it converts direct current (DC) to alternating current (AC) so that the output can be used to supply electrical equipment [3]. The power conversion could be done by using conventional H-Bridge inverter [4]. However, conventional H-Bridge inverter is suggested only for less sensitive equipment due to its higher of THD percentage [5].

Multilevel inverter (MLI) is built to overcome the disadvantages of H-Bridge inverter [6]-[7]. Multilevel produces voltage wave on stages according to the number of levels that resemble to a sinusoidal form. The main classification of MLI is known as: flying-capacitor [8] cascaded H-Bridge [10]; diode-clamped [11]. Multilevel inverter is capable to fulfill the demand of power quality and higher power rating along with lower THD$_{-V}$ or THD$_{-I}$ rate [11]-[12]. The standard of harmonic limit has been stipulated by IEEE, the stipulated standard for general system is 5% [13]. The higher THD causes errors or damage to electronics applied [14]. The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

This paper proposed a five-level inverter topology, uses 6 active power semiconductor switches (MOSFET) and 3 passive power semiconductor switches(DIODE) where the conventional multilevel inverters such cascaded H-bridge MLI, diode-clamped, and flying capacitor, need more semiconductor switches and several capacitors or diodes. Due to its complexity, this proposed inverter topology proposes simpler switch configuration and decrease the number of semiconductor switches used. The proposed configuration is divided into two parts, the first part or stage A is to generate level and the second part or stage B is to generate polarity. The switching control is based on sinusoidal pulse width modulation method for gating signal in stage A. Finally, a microcontroller dsPIC30F4012 is used to support the course of hardware prototype testing and to validate the proposed topology.

2. Research and Method

2.1. Design Configuration

The proposed five-level inverter uses 6 active power semiconductor switches (MOSFET), 3 passive power semiconductor switches (DIODE), and 2 separated DC voltage sources. The design of the proposed five-level Inverter is shown in Fig. 1 the proposed topology has two stages. The first stage $A(S_1, S_2)$ is dual buck DC-DC converters to generate high frequency level of voltage (five-level in proposed design) and the second part stage $B(S_3-S_6)$ is a square-wave full bridge inverter to generate polarity. The first part or stage A (S_1, S_2) operates at the high frequency switching and connected to two DC sources (V_{in}) which nominal value is configured as E and 2E.

The effective number of the output levels ($N_{-levels}$) in the proposed inverter may be related to the number of implemented separate DC sources (N_{-dc}) and the number of switches (N_{switch}). The relation is expressed as:

$$N_{level} = 2 \times (N_{dc}) + 1 \tag{1}$$

$$N_{switch} = (N_{dc}) + 4 \tag{2}$$

The maximum output voltage (V_{-max}) of the proposed inverter can be calculated by this equation below:

$$V_{max} = N_{dc} \times V_{dc} \quad V_{dc} = \text{voltage magnitude} \tag{3}$$

Through the equation (1), (2), and (3) above, it can be obtained the formula as follows:

$$N_{level} = 2 \times N_{switch} - 7 \tag{4}$$

Based on the formulas above, the proposed five-level inverter needs two separated DC sources and six active semiconductor switches. The circuit of the proposed topology is shown below
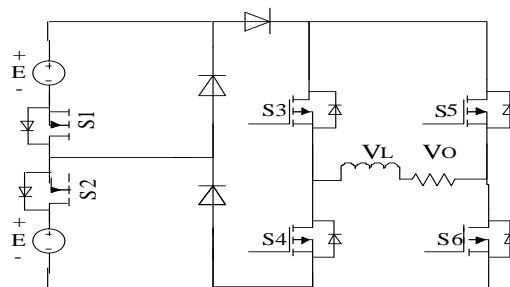

Figure 1. The proposed topology circuit

2.2. Operation Modes

The proposed five level switching configuration is divided into two work cycles : in positive and negative cycles. Those cycles create operation modes (1-6). Those operation modes are explained below:
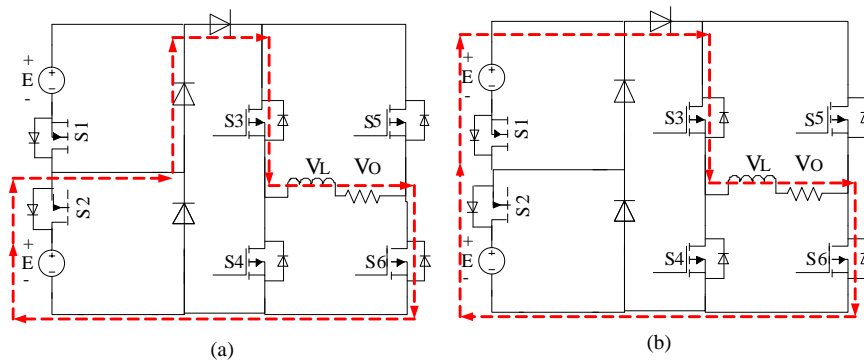

Figure 2. Operation mode 1 (a) the switches that on are S_2, S_3, and S_6 and the others are off. Operation mode 2 (b) the switches that on are S_1, S_2, S_3, and S_6 and the others are off

Operation mode 1 is shown in Figure 2(a): Switches that on are S_2, S_3, and S_6 and the others are off. The maximum positive output obtained (+E) :

$$V_{in} = V_L + V_O$$

$$E = L\frac{di_1}{dt} + V_0$$

$$L\Delta i_2 = (E - V_O)t_{ON} \tag{5}$$

Operation mode 2 is shown in Figure 2(b): Switches that on are S_1, S_2, S_3, and S_6 and the others are off. The maximum positive output obtained (+2E):

$$V_{in} = V_L + V_O$$

$$2E = L\frac{di_2}{dt} + V_0$$

$$L\Delta i_2 = (2E - V_O)t_{ON} \tag{6}$$

Operation mode 3 and 4 are shown in Figure 3 : maximum positive output obtained is (0). This condition is when there is no any supplied voltage across the inverter V_{in}=0. the switches that on in positive cycle are S_3, S_6 (mode 3) and in negative cycle (mode 4) the switches that on are S_4, S_5 ($V_0 = 0$)
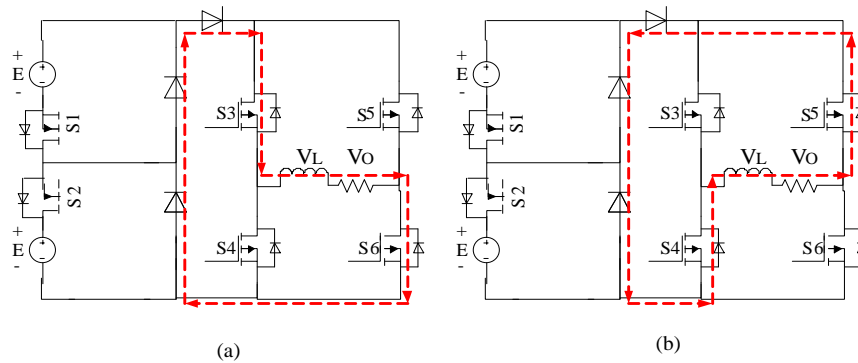
(a)　　　　　　　　　　　　　　　　　　　　(b)

Figure 3. Operation mode 3 (a) the switches that on are S_3 and S_6 and the others are off. Operation mode 4 (b) the switches that on are S_4 and S_5 and the others are off.

The equation for operation mode 3 and 4 are shown in Figure 3 (a) and (b):

$$V_o = L\frac{di_0}{dt}$$

$$L\Delta i_0 = [Vo]t_{off} \tag{7}$$

The mode of operation $5-6$ are in a half negative output as the same as the modes of operation 1-2. For further explanation according to the operation modes above, below are the switching function created in table I. as follows :

Table I. Mode operation switching

Operation	S1	S2	S3	S4	S5	S6	Vout
1	0	1	1	0	0	1	**E**
2	1	1	1	0	0	1	**2E**
3	0	0	1	0	0	1	**0**
4	0	0	0	1	1	0	**0**
5	0	1	0	1	1	0	**-E**
6	1	1	0	1	1	0	**-2E**

Where:

　　1: switch is conducting (ON).

　　0: switch is not conducting (OFF).

2.3. Switching Control Method
In this modulation scheme, the gating pulses of the switching (MOSFET) are modulated by comparing sinusoidal modulation voltage (Vmod) with carrier voltage (Vcar) to create pulse width modulation (PWM).

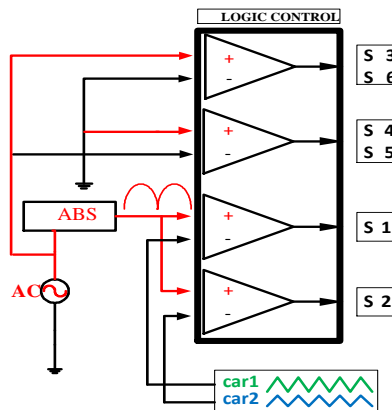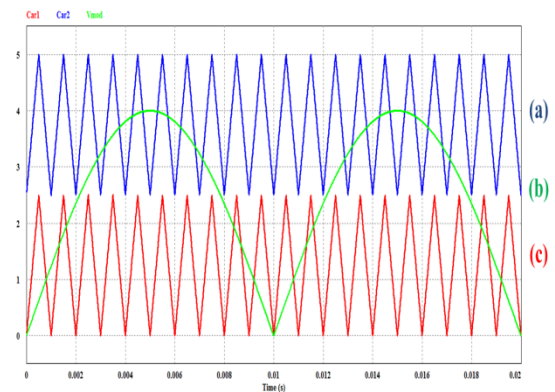**Figure 4.** Proposed technique of SPWM

Figure 5. SPWM method used in the simulation: (a) modulation wave, (b) Vcar$_1$, (c) Vcar$_2$

Value of the output voltage according to modulation signal can be shown as follows:
This formula below applies on mode operation (1)

$$V_{output} = \frac{V_{ref}}{V_{car}} \times E \tag{8}$$

This formula applies on mode operation (2)

$$V_{output} = \frac{V_{ref}}{2V_{car}} \times E \tag{9}$$

The waveform (carrier and sine modulation) must be upper zero (0) to fit in the micro-controller's rule

3. Results and Discussion
3.1. Simulation Results
Results and analysis in simulation were taken by using power simulation software. The parameters for the proposed inverter topology are shown in table II.

Table II. Simulation Parameters

Parameters	units
V$_{input}$	2x12 VDC
Inductive Filter	7.5 mH
Resistive Load	62 Ω
Cariers frequency	5000 Hz

According to the parameters given in table II above. Below are the samples of simulation result:
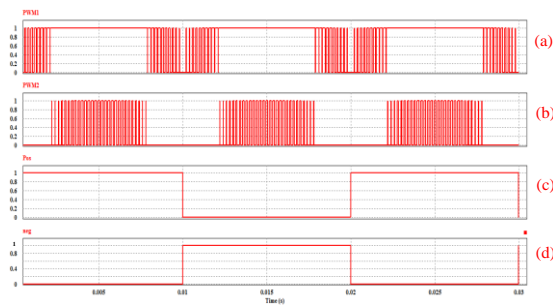
Figure 6. Simulated control waveform (a) PWM$_1$ (b) PWM$_2$ (c) positive polarity (d) negative polarity
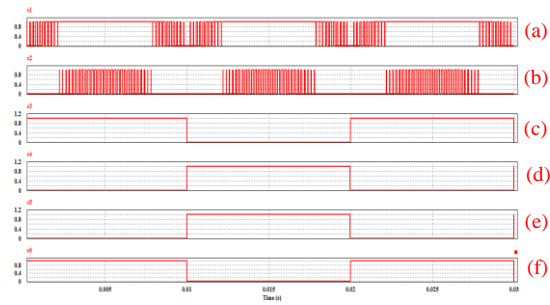

Figure 7. Proposed inverter switching (a) S$_1$ (b) S$_2$ (c) S$_3$ (d) S$_4$ (e) S$_5$ (f) S$_6$.
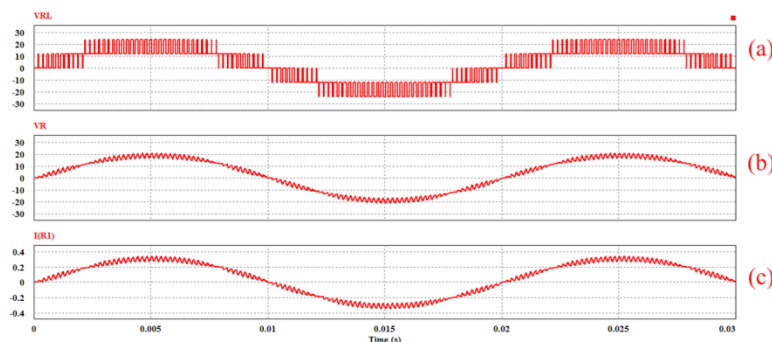

Figure 8. Proposed inverter simulation output analyzed at linear loads (a) output before filtered L (b) output after filtered L (c) current waveform 0.3 A

Figure. 6 shows the control wave in this proposed inverter (a) PWM$_1$ and (b) PWM$_2$ are aimed to generate voltage level. Figure 6 shows the polarization (c) positive cycle and (d) negative cycle. The proposed inverter switching is shown in Figure 7. Figure 8 shows the inverter output in simulation.

3.2. Experimental Results

To validate the research and simulation, hardware prototype of the proposed inverter topology is tested in the laboratory using simulation parameters in table II. The inverter switching is controlled by using SPWM method through microcontroller dsPIC 30f4012. The amount of THD that represent the quality of the inverter output is checked through digital power meter HIOKI. The experimental results are shown below:
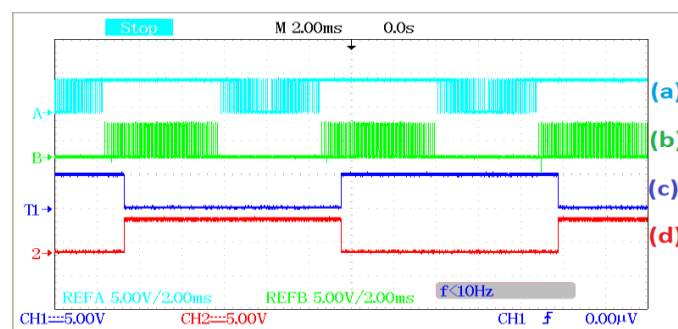

Figure 9. Implemented SPWM waveform in micro-controller dsPIC 30f4012 (a) PWM$_1$ (b) PWM$_2$ (c) positive polarity (d) negative polarity
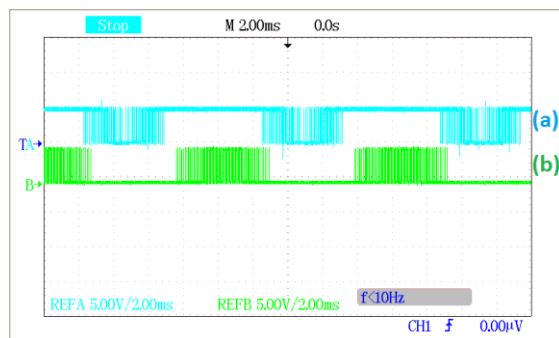
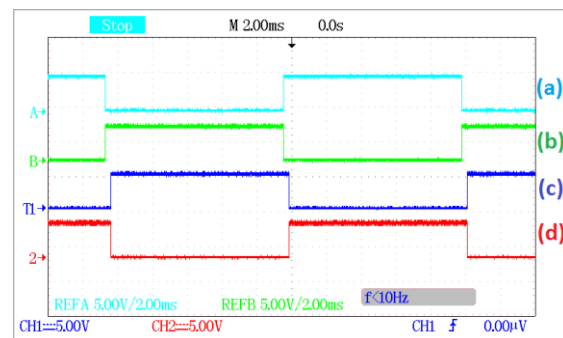**Figure 10.** The switching condition of stage A (a) S_1 (b) S_2

Figure 11. The switching condition of stage B (a) S_5 (b) S_6 (c) S_7 (d) S_8

SPWM lookup table data with high frequency switching 5000 Hz are employed to generate stage A (Figure 10). Stage B (Figure 11) is an conventional Full-Bridge inverter with low frequency switching 50 Hz to generate polarization. By installing linear loads (resistive-inductive) at its output.The results are shown below:
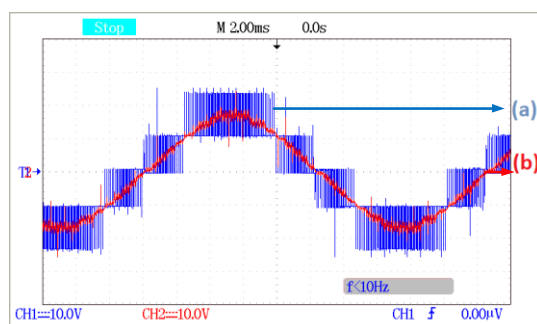

Figure 12. Experimental result of the proposed inverter (a) the output before filter L, shown in color blue (b) the output after filter L, shown in color red
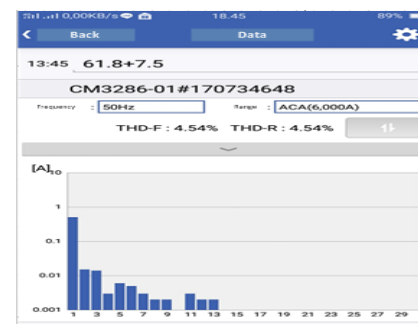

Figure 13. THD result of experimental testing taken from digital power meter HIOKI

The dual buck DC-DC converters (stage A) must be predict cause of high frequency switching, the other stage needs a low frequency. Based on the results above Figure 13 and 12 shows the proposed inverter output and its THD value. After installing inductive filter 7.5 mH at load, the output voltage becomes smoother resembling to an ideal 50Hz sine wave. The THD value of proposed design is 4.54 % which is still under IEEE regulation 5 % and reliable to be used. Harmonic voltage limits for power producers (public utilities or co-generators) at 2.3 - 69kV, 2.5% for 69 - 138 kV and 1.5% for $\geq$ 138kV.

4. Conclusions

The topology that was presented in this paper consists of dual buck DC-DC converters and full bridge inverter. This method is very simple, there is no need for controlling negative voltage. The polarity reversing was done by full bridge inverter. The implemented five-level inverter topology has more advantages compared to the conventional MLI; the proposed topology uses less semiconductor active switches. The THD result also qualified to the standard set by IEEE, so this proposed inverter topology is reliable to be implemented. The high frequency switches can be operated at the fundamental frequency so overall cost and complexity of the circuit can be reduced. This topology is suitable for power plant application. The computational simulation and experimental results confirm the validity of the proposed topology.

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