Design and simulation of an asymmetrical control strategy in single-phase five-levels inverter

Daniel Santoso[*] and Leonardus Heru Pratomo

Department of Electrical Engineering Soegijapranata Catholic University Semarang, Indonesia

[*]Corresponding author's e-mail: 16f10004@student.unika.ac.id

Abstract. The revolution of 4.0 industry refers to power electronics technology development, including multilevel converter that more superior than conventional converter. Multilevel converter has less harmonics disruption, a few switches, and a lower cost. This paper is discussing about the new strategy in the five levels of asymmetric inverter, and some comparison to a conventional inverter which already existed. Focused on the design construction from five levels of the converter resolve the limitations of the conventional converter. Produce lower harmonic distortion, this construction was designed and stimulated using PSIM software. The result in real time shows THD value of 3,75%.

1. Introduction

The development of power electronics technology very needed in 4.0 industrial revolution. Digital transformation makes the development of power electronics technology increase. Multilevel inverter included in the development of power electronics technology. The enhancement of efficiency and flexibility in building a strategy to control five levels of the inverter be the main challenge. Conventional converter which already existed have some shortcoming. Besides limited by their component power ratings, less efficient, and less flexible, also had a higher THD than a multilevel converter [1]. Multilevel inverter complete and improve what become the deficiencies. The general configuration of the Multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages typically from n number of levels of voltages [2]. Asymmetric Topology means that we give different values of voltages to each number of input sources [3]. The proposed asymmetrical configuration uses a less number of switches to get more levels [4]. Asymmetric multilevel inverters can be used to provide a large number of output levels without increasing the number of switches [5]. The disadvantage of multilevel power conversion is in terms of the higher number of semiconductor switches [6]. But multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM) [7]. The five-level inverter adopts from unipolar inverter. With the filter circuit which gave a better sinusoidal output waveform compared to the bipolar inverter [8]. Therefore, the five-level inverter gave a better performance in power quality output [9]. In this topology had a zero-crossing detector. Zero crossing measure the signal correctly if had an unbalanced signal form, includes spike / sags between positive and negative periods which made the system unstable [10]. The THD of the five-level inverter is much less than the conventional multistring three-level inverter because of additional auxiliary circuit has high switching losses [4].

2. Inverter operation and control strategy

2.1. Inverter switching mode operation

The five levels of diode clamped inverter have 8 main switches [11]. Other new five-level of flying capacitors inverter using six power semiconductor switches [6]. This paper discusses about a new topology of the five-level inverter which has fewer semiconductor switches, shown in figure 1. A new five-level inverter only using five semiconductor switch, one diode, but needs two DC sources. The Diode is operated in forward bias from in the between the first DC source (Vdc1) and the second DC source (Vdc2), heading after semiconductor switch (S5). At the end of the inverter output before heading to the load there is a filter. This inverter work with 5 mode operation[12].
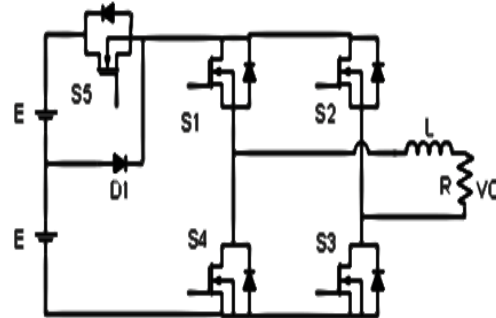
Figure 1. Topology

2.1.1. The Operation mode 1

When the power switch S5 and S1 are conducted. The current flow from the voltage DC source (-E-E) to the load. Through the power switch S3, the current flow returns to the voltage DC source (-E-E). The illustration of operation mode 1 shown in figure 2. This represented in question (1).
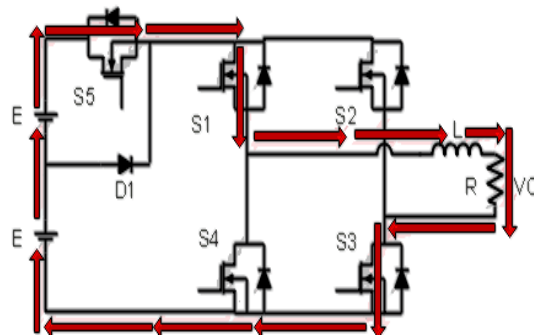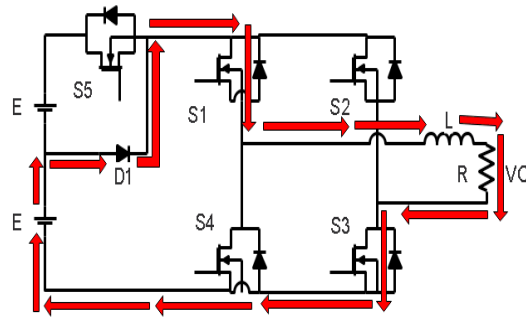
Figure 2. The operation mode 1

$$\mathbf{E} - \mathbf{E} = V_{(L)} + V_{(O)}$$
$$\mathbf{L}\Delta\mathbf{i}_{(L)} = \big(\mathbf{2E} - \mathbf{V}_{(O)}\big)\Delta\mathbf{t} = \big(\mathbf{2E} - \mathbf{V}_{(O)}\big)\mathbf{t}_{(on)} \tag{1}$$

2.1.2. The Operation mode 2

When the power switch S1 and diode D1 are conducted. The current flow from the voltage DC source (E) to the load. Through the power switch S3, the current flow returns to the voltage DC source (E). The illustration of operation mode 2 shown in figure 3. This represented in question (3).
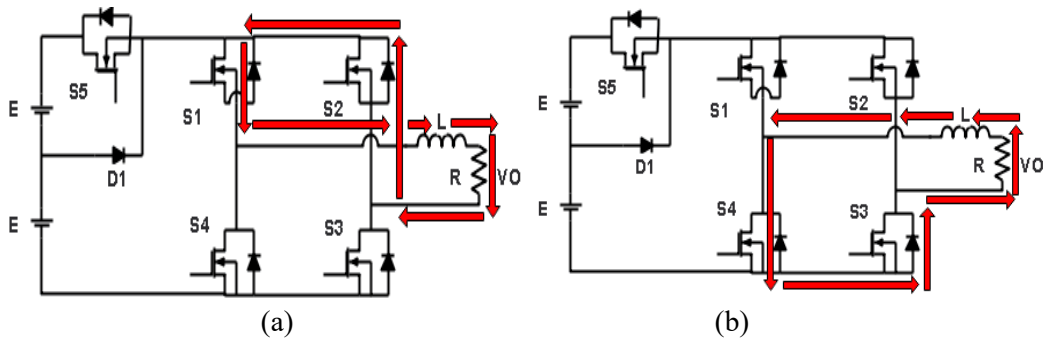
Figure 3. The operation mode 2

$$\text{E} = V_{(L)} + V_{(O)}$$
$$L\Delta i_{(L)} = \left(E - V_{(O)}\right)\Delta t = \left(E - V_{(O)}\right)t_{(on)} \tag{2}$$

2.1.3. The Operation mode 3

This operation mode 3 is freewheeling condition. A freewheeling condition for a positive value had occurred, after the power switch S1 and S3 are conducted. While the power switch S2 and S4 are conducted, produced a freewheeling condition for negative values. The illustration of operation mode 3 shown in figure 4. This represented in question (3).
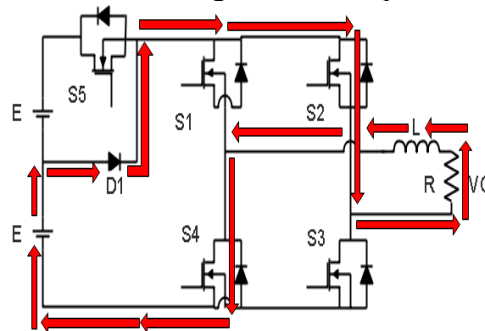

(a)   (b)

Figure 4. The operation mode 3. (a). Positive cycle (b). Negative cycle

$$\boldsymbol{0} = \boldsymbol{V}_{(L)} + \boldsymbol{V}_{(O)}$$
$$\boldsymbol{L\Delta i_{(L)}} = \left(\boldsymbol{V}_{(O)}\right)\boldsymbol{\Delta t} = \left(\boldsymbol{V}_{(O)}\right)\boldsymbol{t_{(off)}} \tag{3}$$

2.1.4. The Operation mode 4

When the power switch S2 and diode D1 are conducted. The current flow from the voltage DC source (E) to the load. Through the power switch S4, the current flow returns to the voltage DC source (E). The illustration of operation mode 4 shown in figure 5. This represented in question (4).

Figure 5. The operation mode 4

$$-\mathbf{E} = \mathbf{V}_{(L)} + \mathbf{V}_{(O)}$$

$$\mathbf{L}\Delta\mathbf{i}_{(L)} = (\mathbf{V}_{(O)} - \mathbf{E})\Delta\mathbf{t} = (\mathbf{V}_{(O)} - \mathbf{E})\mathbf{t}_{(on)} \tag{4}$$

2.1.5. The Operation mode 5

When the power switch S5 and S2 are conducted. The current flow from the voltage DC source (E+E) to the load. Through the power switch S4, the current flow returns to the voltage DC source (E+E). The illustration of operation mode 5 shown in figure 6. This represented in question (5).
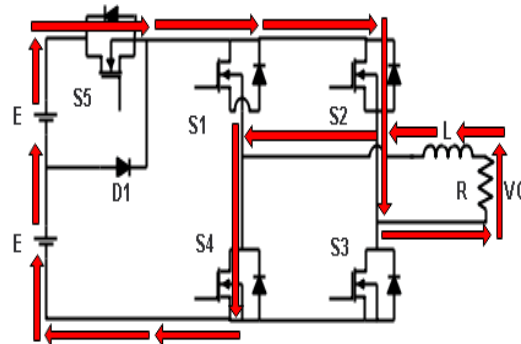

Figure 6. The operation mode 5

$$-(\mathbf{E} - \mathbf{E}) = \mathbf{V}_{(L)} + \mathbf{V}_{(O)}$$

$$\mathbf{L}\Delta\mathbf{i}_{(L)} = (\mathbf{V}_{(O)} - 2\mathbf{E})\Delta\mathbf{t} = (\mathbf{V}_{(O)} - 2\mathbf{E})\mathbf{t}_{(on)} \tag{5}$$

2.2 Control Strategy

Pulse-Width Modulation switching in S1, S2, S5 gates are compared with 4 tiers of triangular waves car1, car2, car3, car4. Triangular waves car1, car2 and car3, car4 had a different DC offset with carrier frequency of 9 kHz. The configuration of overall switches to achieve the level desired is shown in table 1

Table 1. SPWM Gate Switching

S1	S2	S3	S4	S5	Vo
1	0	1	0	1	2E
1	0	1	0	0	E
1	0	0	0	0	0
0	0	0	1	0	0
0	1	0	1	0	-E
0	1	0	1	1	-2E

To built the five – level inverter needs 4 carriers. The carriers divided into two sections. The first section, comp3 for S1 and comp4 for S2 has same carrier DC offset. The second section, comp 1 and 2 for S5 has same carrier DC offset. But, between stage 1 and stage 2 has a different DC offset. Also, needs a zero crossing detector as a reference to adjust the ignition angle of S3 and S4 .
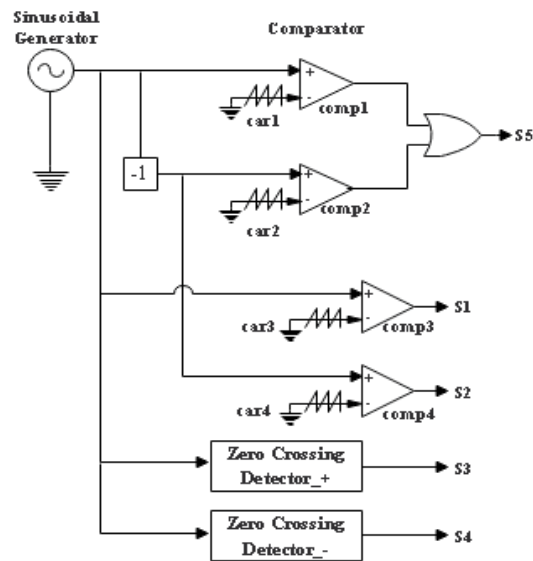
Figure 7. A new strategy SPWM control

3. Simulation and Harmonic Analyzed

3.1. Simulation

Design and simulation of an asymmetrical control strategy in single - phase five - level inverter are simulated in PSIM software by Power Sim Tech. Fig 8. describes the SPWM switching in S1 until S5. Design control circuit output sinusoidal pulse width modulation (SPWM) produced by the comparison of reference and carrier waves [1]. The simulation parameters are shown in Table 2.

Table 2. Simulation Parameter

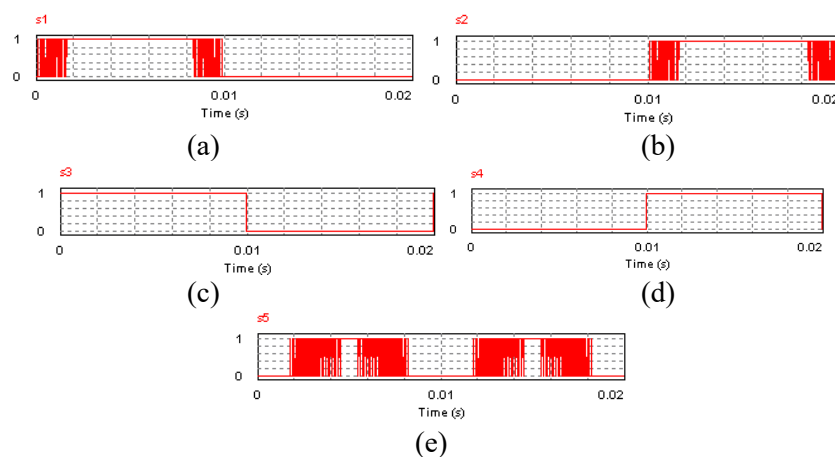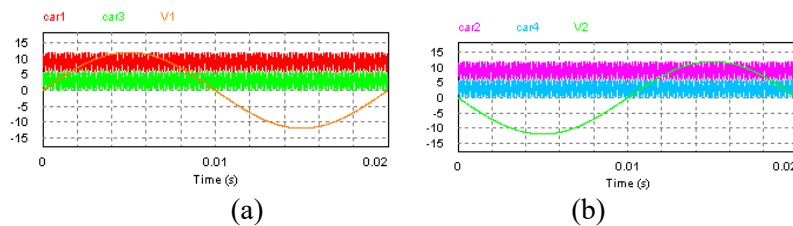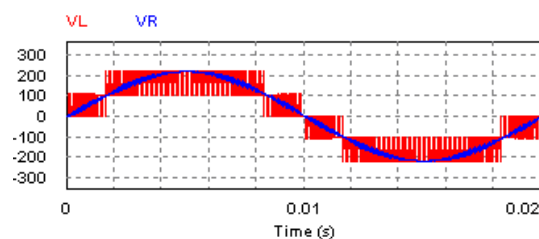| Device	Value
DC Input E	110V
Inductive Filter	2mH
Load Resistor	20Ω
Carrier Triangular Frequency	9kHz

Figure 8. SPWM for S1 (a), S2 (b), S3 (c), S4 (d), S5 (e)
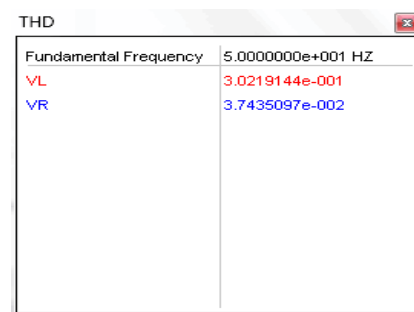
(a)   (b)

Figure 9. Triangular wave 9 kHz comparison with, (a) sine wave, 50 Hz after -1 element, (b) sine wave 50 Hz before -1 element

At the first $\frac{1}{2}$ positive cycle inducted by the carrier signal car1 and car3. At the $\frac{1}{2}$ negative cycle inducted by carrier, signal car2 and car4. This describes has shown in figure 9. The car1 generated the fifth level, the car2 generated the first level, the car3 generated the fourth level, and the car4 generated the second level.

Figure 10. Triangular wave 9kHz

3.2. Harmonic Analysed

Figure 11. *Harmonic Analysed*

THD level analyzed at load with 50Hz output frequency is shown in figure 11. PWM high frequency switching at 9kHz and inductor filter 2mH can reduce the THD level of 3.75% (VR). [13], [1].

4. Conclusion

This paper has already discussed about a new strategy control for asymmetrical five level inverter. Compared to other five level inverter (flying capacitor, diode clamp) deals on a number of switches. A new strategy control for asymmetrical five level inverter has fewer semiconductor switches. A new strategy in control circuit in high frequency switching of SPWM and coupled with inductor filter, can reduce the THD value. THD value has been analysed and simulated in PSIM software by PowerSimTech.is 3.75%. That value is included in the range of IEEE standards 5% of harmonic voltage limits for power producers (public utilities or co-generators) at 2.3 - 69kV, 2.5% since 69 - 138 KV and 1.5% for _138 kV.

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