Design and simulation full control strategy in single-phase five-level inverter

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Abstract. A five-level inverter has been used for many applications in renewable energy systems. In terms of harmonic distortion is lower compared to conventional two-level inverters. The five-level converter has several disadvantages such as the number of semiconductor power switches, pulse width modulation control methods, and the semiconductor switch power loss. This paper aims to propose a new control strategy and design on a five-level inverter. Unipolar control strategy modulation of sinusoidal pulse width modulation is used for each power semiconductor switch. This converter only requires 2 carrier signals and is simulated in real-time with a THD of 3.36%.

1. Introduction

Multilevel inverters have been developed to obtain good quality power [1]. The general concept of an inverter is to use a power semiconductor switch to conduct power conversions. When compared with conventional power conversion approaches, there are several advantages such as the quality of the waveforms of higher power production, the reduction in voltage on the load, the ability of high voltage, and the low electromagnetic compatibility. Multilevel voltage source inverters have been broadly classified into three main groups [2], [3]: diode-level inverters or multi-pinch converters [4],[5], multi-celled flying capacitors or multi-celled inverters [6], [7] and multilevel invert cascades separating a DC source or multilevel H-bridge multilevel inverter [8]. Each group has a different set of controls. To make a five-level inverter a control circuit that has lower harmonic distortion is needed. The disadvantage of multilevel power conversion is in the case of a higher number of semiconductor switches. Another disadvantage is that the sinusoidal pulse width modulation control method can affect harmonic distortion. The full control strategy method can reduce the harmonic distortion of the converter five levels. This control is suitable for renewable energy such as photovoltaics, wind turbines where the efficiency and quality of power are of great concern to researchers [9].

2. Research Method

2.1. Circuit Design Configuration

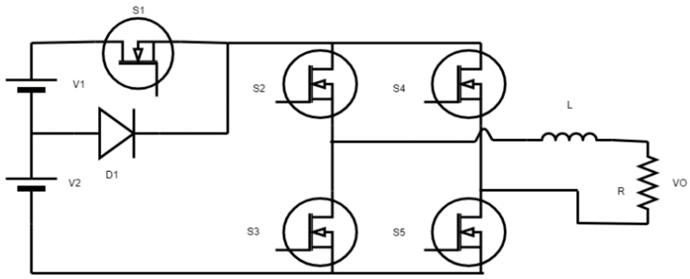


Figure 1. The multilevel inverter topology in five levels

In conventional multilevel inverters, a power semiconductor switch is used to produce high frequency waveforms in positive and negative polarity [10]. However, the utilization of all power semiconductor, switches is needed to produce unipolar levels as simulated [11]. This idea has been simulated with a design like figure 1. The first part (S1) is referred to as the generation level of positive and negative polarity. The second part (S2-S5) as forming 3 levels, seen in figure 1.

2.2. Switching Operation Modes

This five level inverter has 5 operating modes [12]. Each mode of operation is explained in the text below.

2.2.1. The Operation Mode 1

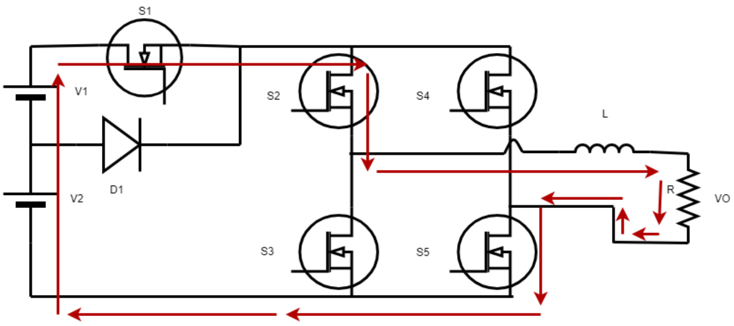


Figure 2. The operation mode 1

Mode of operation 1 produces an output of 2E. S1, S2, S5 are ON and S3, S4 are OFF. Figure 2 shows the current path that is active at this stage. Mode of operation, 1 has the following equation:

$$2\mathrm{E} = L\frac{di_{(1)}}{dt} + V_{(O)}$$
$$L\Delta i_{(L)} = \left(2E - V_{(O)}\right)\Delta t = \left(2E - V_{(O)}\right) \quad (1)$$

2.2.2. The Operation Mode 2

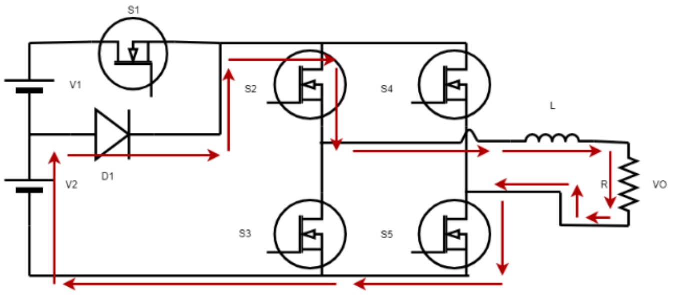
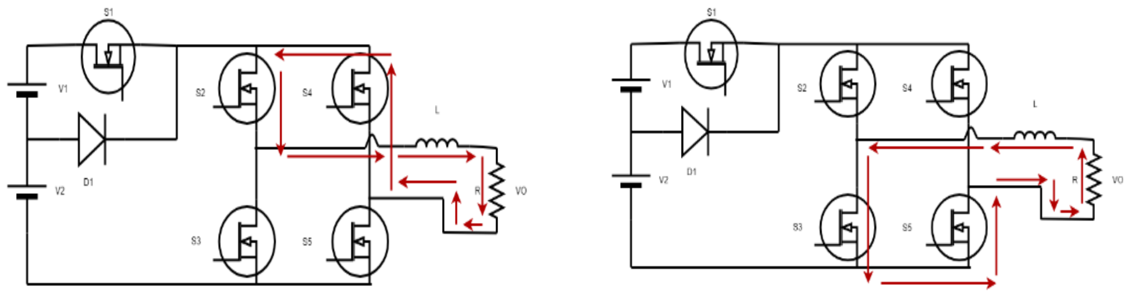


Figure 3. The operation mode 2

Mode of operation 2 produces an output of E. S2, S5 are ON and S3, S4, S5 are OFF. Figure 3 shows the current path that is active at this stage. Mode of operation, 2 has the following equation:

$$E = L\frac{di_{(1)}}{dt} + V_{(O)}$$
$$L\Delta i_{(L)} = \left(E - V_{(O)}\right)\Delta t = \left(E - V_{(O)}\right)t_{(on)} \qquad (2)$$

2.2.3. The Operation Mode 3



(a) (b)

Figure 4. The operation mode 3 (a) Positive cycle (b) Negative cycle

Mode of operation 3 is a freewheeling condition, producing two outputs of zero. In positive cycle S2, S4 is ON and S1, S3, S5 OFF. Figure 4 (a) shows the current path that is active at this stage. In negative cycle S3, S5 is ON and S1, S2, S4 OFF. Figure 4 (b) shows the current path that is active at this stage. Mode of operation, 3 has the following equation:

$$0 = L\frac{di_{(1)}}{dt} + V_{(O)}$$
$$L\Delta i_{(L)} = \left(V_{(O)}\right)\Delta t = \left(V_{(O)}\right)t_{(off)} \qquad (3)$$

2.2.4. The Operation Mode 4

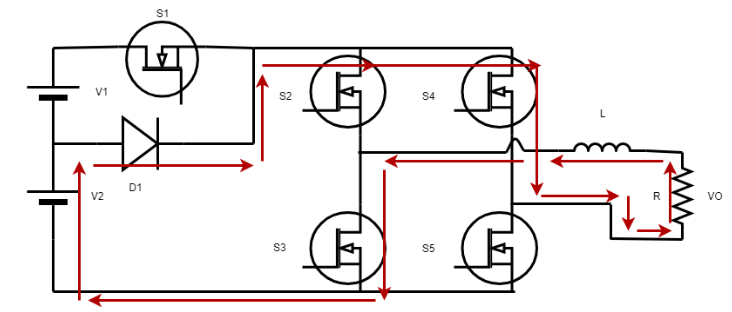


Figure 5. The operation mode 4

Mode of operation 4 produces an output of -E. S3, S4 are ON and S1, S2, S5 are OFF. Figure 5 shows the current path that is active at this stage. Mode of operation, 4 has the following equation:

$$-\mathrm{E} = L\frac{di_{(1)}}{dt} + V_{(O)}$$

$$L\Delta i_{(L)} = \left(V_{(O)} - E\right)\Delta t = \left(V_{(O)} - E\right)t_{(on)} \qquad (4)$$

2.2.5. Operation Mode 5

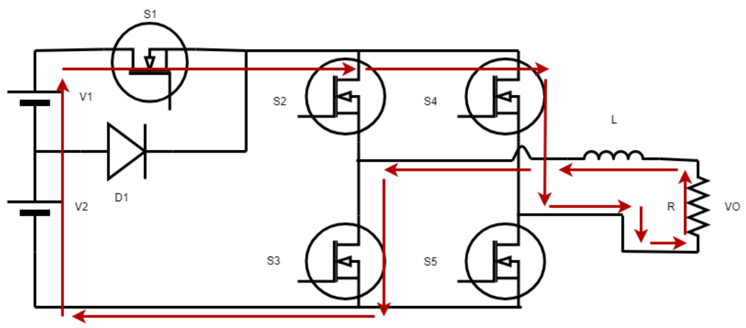


Figure 6. The operation mode 5

Mode of operation 5 produces an output of -2E. S1, S3, S4 is ON and S2, S5 are OFF. Figure 6 shows the current path that is active at this stage. Mode of operation, 5 has the following equation:

$$-2\mathrm{E} = L\frac{di_{(1)}}{dt} + V_{(O)}$$

$$L\Delta i_{(L)} = \left(V_{(O)} - 2E\right)\Delta t = \left(V_{(O)} - 2E\right)t_{(on)} \qquad (5)$$

Based on the above operating modes the switching function table can be created as in table 1.

Table 1. SPWM gate switching

S1	S2	S3	S4	S5	Vo
1	1	0	0	1	2E
0	1	0	0	1	E
0	1	0	1	0	0
0	0	1	0	1	0
0	0	1	1	0	-E
1	0	1	1	0	-2E

Where:
1: Power semiconductor switch conducting
0: Power semiconductor switch is not conducting

3. Unipolar Pwm Modification Strategy

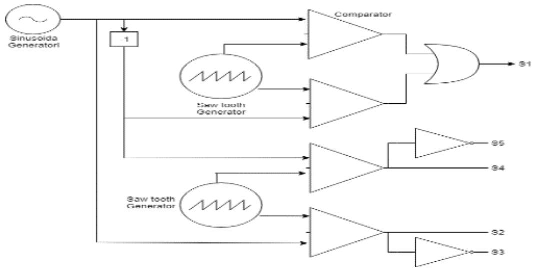


Figure 7. The proposed scheme

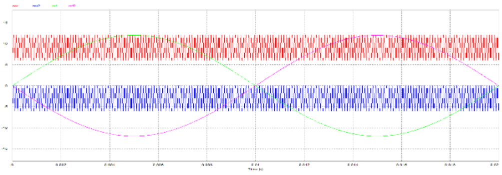
Figure 7. Describe the overall control circuit for the proposed inverter. Using logic gates on the S5. The reference signal will be modulated by 2 carriers so that the SPWM is formed for each power semiconductor switch.

3. Simulation and Harmonic Analysis

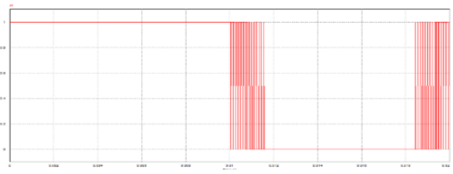
The real-time simulation design and analysis of the proposed five-level inverter design are simulated in PSIM software by PowerSimTech. Simulation parameters for the proposed inverter circuit are shown in table 2.

Table 2. Simulation Parameters

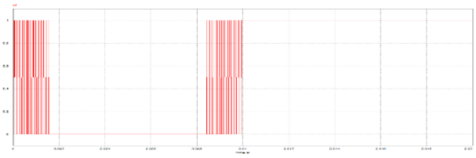
Device	Value
DC Input E	110V
Inductive Filter	2mH
Load Resistor	20Ω
Carrier Triangular Frequency	10kHz



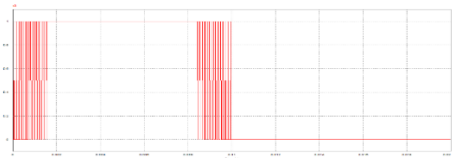
(a)



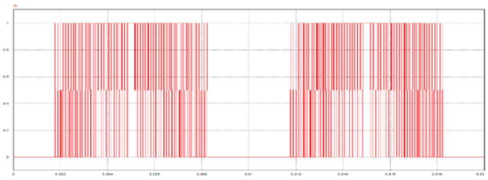
(b)



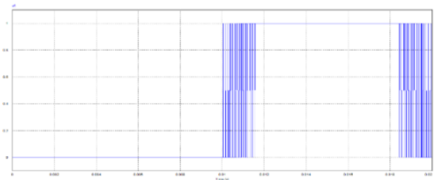
(c)



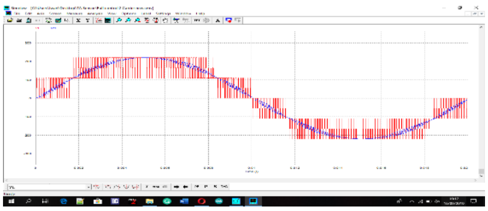
(d)



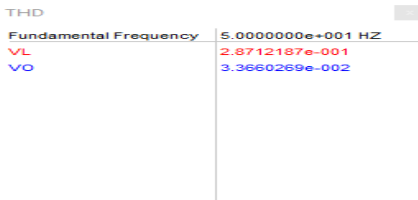
(e)



(f)



(g)



(h)

Figure 8. Simulated waveform: (a) Reference signal modulation, (b) Switching on s1, (c) Switching on s2, (d) Switching on s3, (e) Switching on s5, (f) Switching on s4, (g) Five level inverter output, (h) THD value

The full control strategy uses 2 carrier signals and a reference signal in the form of 2 sinusoidal waves. Sinusoidal waves are 180º phase change with each other to produce a five-level inverter output voltage. 2 reference signals are modulated by 2 carrier signals to produce SPWM. From the simulation results of this 5 level inverter has a THD of 3.72% (figure 8 (h)).

4. Conclusion

This five-level inverter design has 5 power semiconductor switches. Compared to conventional 5 level inverters the number of semiconductor switches is less. In terms of size and cost to make this inverter less. This inverter uses a full control strategy that uses 2 carrier signals and has a THD much better than conventional five-level converters. Suitable for renewable energy applications such as Photovoltaic, wind turbines where power efficiency and quality are of great concern.

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