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Design of a cyclic column-parallel ADC for Monolithic Active Pixel Sensor

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Abstract: This paper describes a 5-bit cyclic column-parallel ADC for Monolithic Active Pixel Sensor. The column-parallel ADC combines the dedicated sample phase and the signal conversion phase into a single phase. Moreover, it has a high tolerance to the offset of the comparators in the ADC by generating 1.5 bit in every stage. Each column-parallel ADC covers a small area of 100 μm × 200 μm, consumes 4.5 mW at 3.3 V supply and provides the sampling rate of 10 MS/s with the dynamic range of 1000 mV. The results show that the ADC has a signal-to-noise and distortion ratio (SNDR) of 28.47 dB. Its DNL and INL are −0.039/0.055 LSB and −0.048/0.095 LSB, respectively.

Keywords: Analogue electronic circuits; Particle tracking detectors; Pixelated detectors and associated VLSI electronics; VLSI circuits

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1 Introduction

Considering the increasing number of cancer patients, China has built its own carbon ion therapy facility [1]. The beam monitoring system in the therapy facility ensures the beam energy deposition can accurately cover the dedicated tumour region. The full image of the beam energy deposition is needed for accurate beam calibration, thus a Monolithic Active Pixel Sensor (MAPS), which can provide the energy deposition in each pixel, is being designed in a 130nm CMOS process. As the key part in realizing this MAPS for full-image output, a 5-bit cyclic column-parallel ADC with a novel architecture has been designed to serve the pixels in each column. To satisfy the restrict constraints on power dissipation, size, working speed and accuracy for the MAPS, the column-parallel ADC combines the dedicated sample phase and the signal conversion phase into a single phase. Moreover, the column-parallel ADC has a high tolerance to the offset of the comparators in the ADC by generating 1.5 bit in every stage. This paper discusses the design, optimization and performance of the column-parallel ADC.

2 Architecture of the column-parallel ADC

The column-parallel ADC is an optimized fully differential cyclic ADC. As shown in figure 1, the column ADC consists of a sub-ADC, a multiplying digital-to-analog converter (MDAC) and a digital calibration block. As shown in figure 2, the sub-ADC is constituted of two fully differential comparators, each of which consists of a switched capacitor circuit and a dynamic comparator. The switch capacitance captures the input voltage. The dynamic comparator compares the captured voltage with the reference voltage and generates digital data. Figure 3 shows the schematic of the dynamic comparator, which consists of a differential preamplifier followed by a regenerative latch. In each conversion step, the sub-ADC generates 1.5-bit digital data ($[a_i b_i] \in \{00, 01, 10\}$).

The schematic of the MADC is shown in figure 4. The MDAC is the combination of a sub-DAC, a Sample and Hold block and a Residue Amplifying block. The sub-DAC converts the outputs of the sub-ADC into analog signal. Afterwards, subtraction is performed between the output of the sub-ADC and the voltage captured by the Sample and Hold block. The residue is amplified with the gain of 2 by the two-stage operational amplifier, as shown in figure 5. The two-stage operational

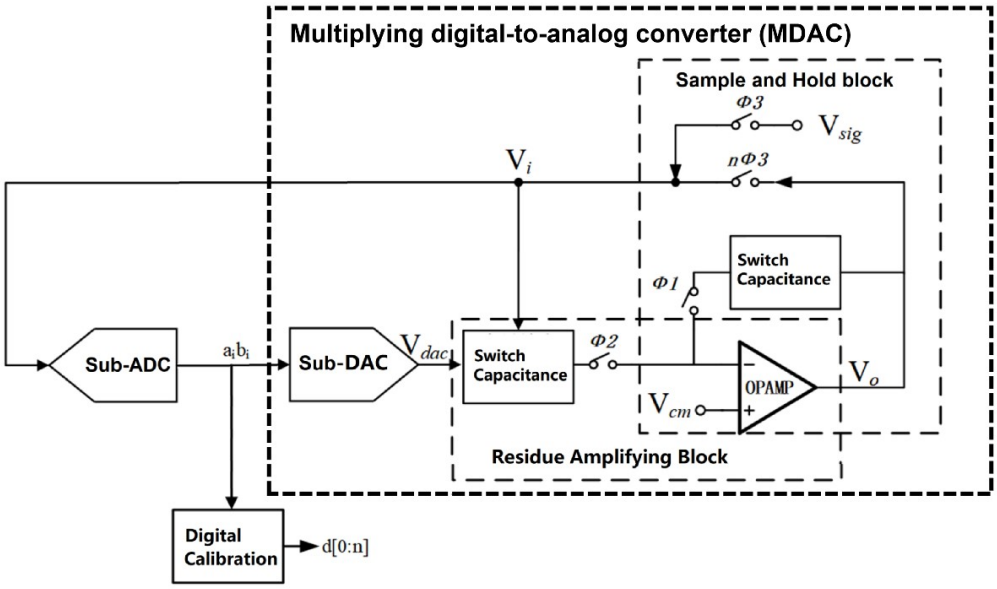

Figure 1. Architecture of the column-parallel ADC.

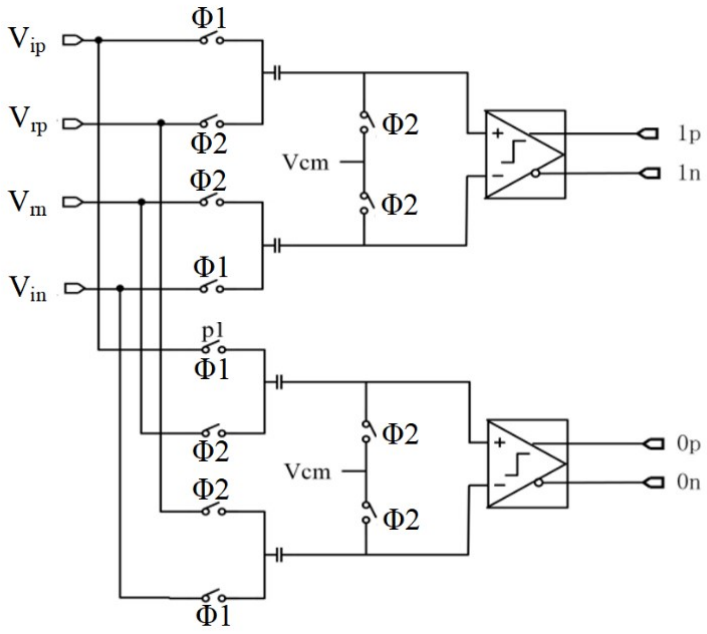

Figure 2. Schematic of the sub-ADC.

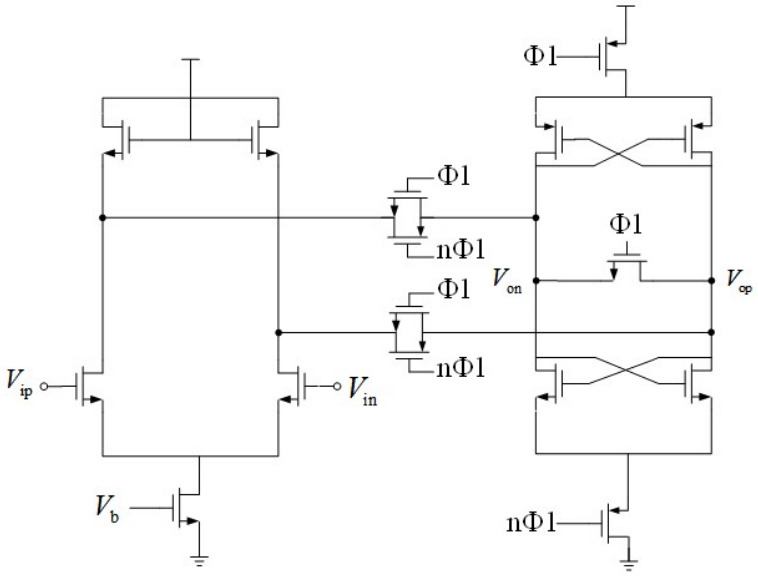

Figure 3. Schematic of the dynamic comparator in the sub-ADC.

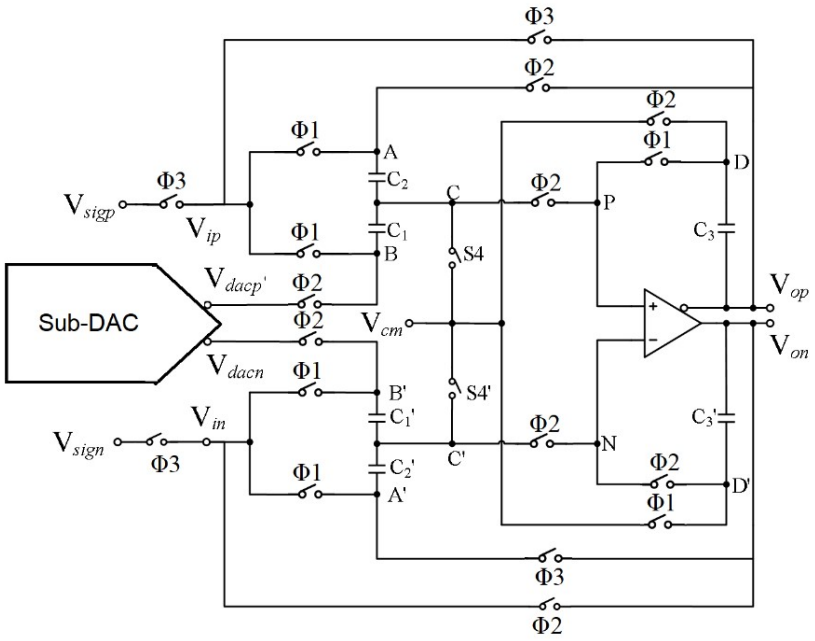

Figure 4. Schematic of the MDAC.

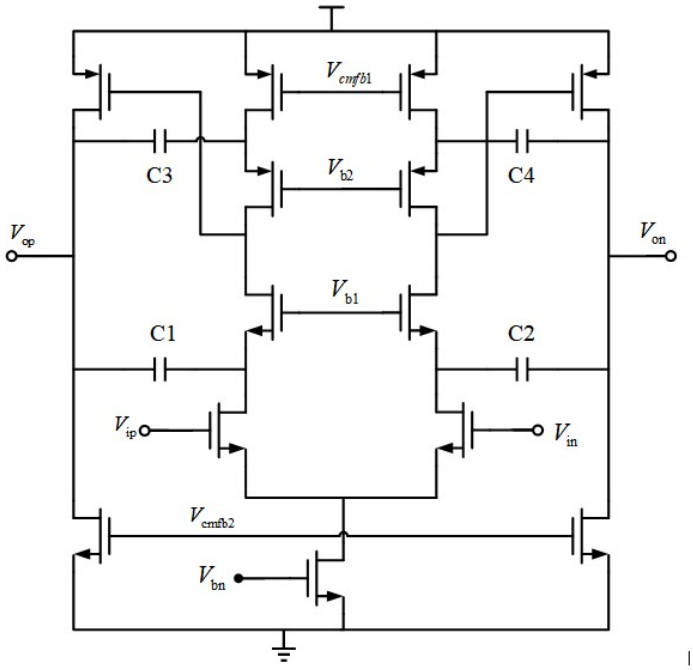

Figure 5. Schematic of the two-stage amplifier in the MDAC.

amplifier consists of a cascode stage and a common-source stage. The second stage is employed to maximize the output signal swing. The capacitor $C1$ and capacitor $C2$ serve as cascode Miller compensation which is employed to improve the bandwidth. The capacitor $C3$ and capacitor $C4$ are placed to avoid the peaking of the magnitude response caused by $C1$ and $C2$ [2].

Figure 6 shows the schematic of the digital calibration block, which mainly consists of the shift registers and the adders. In the converting process, the 1.5-bit digital output ($[a_i b_i]$) from the sub-ADC is pushed into the shift register chain and the 5-bit output is generated by the adders.

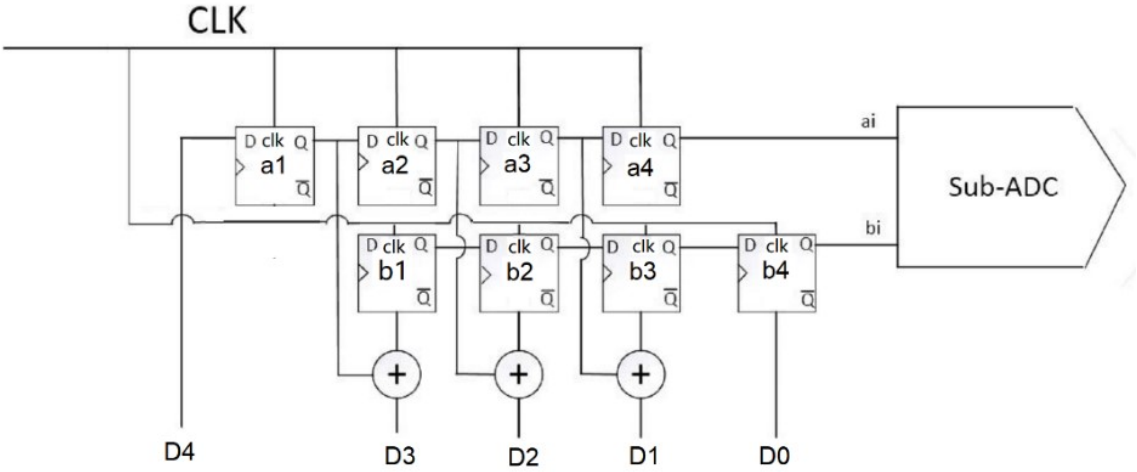

Figure 6. Schematic of the digital calibration block.

3 Operation timing of the column-parallel ADC

As shown in figure 7, the column-parallel ADC has three working phases: the internal sampling phase (Φ1), the charge transfer phase (Φ2) and the external sampling phase (Φ3). Functionality of the MADC is changed with working phases. The simplified MDAC without DAC is shown in figure 8.

In each converting loop, the first phase Φ1 starts with the phase Φ3. Both the sub-ADC and the capacitance $C1$, $C2$, $C1'$ and $C2'$ in the MDAC, as shown in figure 8 (a), track the input signal voltage V_{in}. In the following phase Φ2, the sub-ADC generates the 1.5-bit code $[a_i b_i]$. As presented in equation (3.1), the sub-DAC generates the signal V_{dac} for the two-stage amplifier in the MDAC (shown in figure 8 (b)).

$$V_{\text{dac}} = V_{\text{dacn}} - V_{\text{dacn}} = DV_{\text{ref}} = \begin{cases} V_{\text{ref}} \mathrm{a}_i b_i = 00 \\ 0 \mathrm{a}_i b_i = 01 \\ -V_{\text{ref}} \mathrm{a}_i b_i = 10 \end{cases} \tag{3.1}$$

The charge stored in the previous phase Φ1 transfers to generate the amplified residue voltage V_{res}. Capacitance $C1$, $C2$, $C1'$ and $C2'$ are equal, thus the V_{res} can be expressed as

$$V_{\text{res}} = 2\,V_{\text{in}} + DV_{\text{ref}} \tag{3.2}$$

Afterward, it comes to phase Φ1 again, the operation amplifier and the capacitance $C3$ an $C3'$ are connected to a negative feedback form (shown in figure 8 (c)) to hold the V_{res} from last phase.

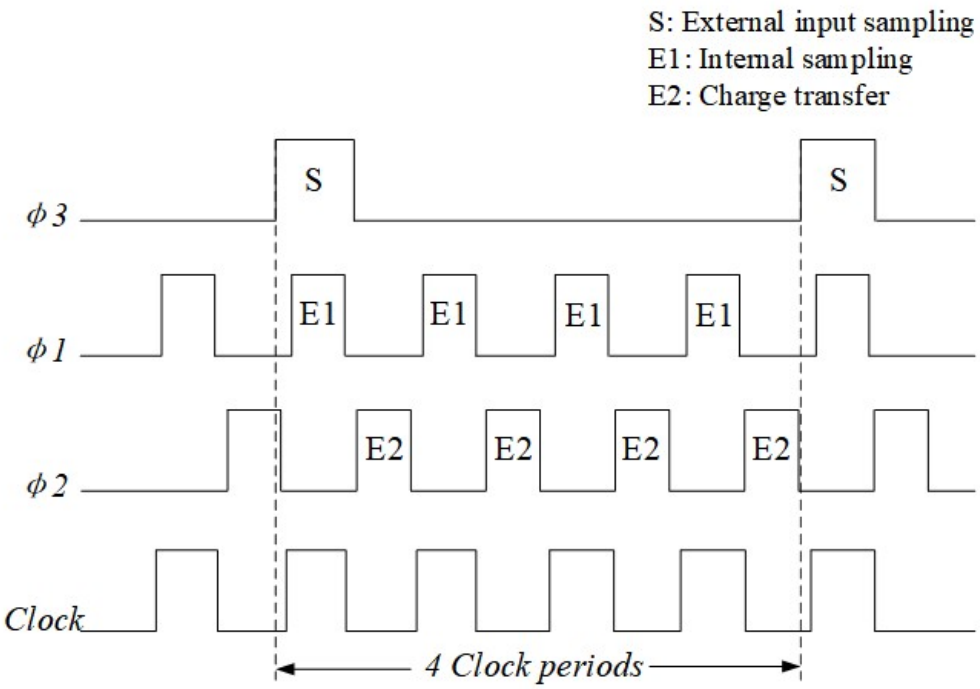

Figure 7. Schematic of the digital calibration block.

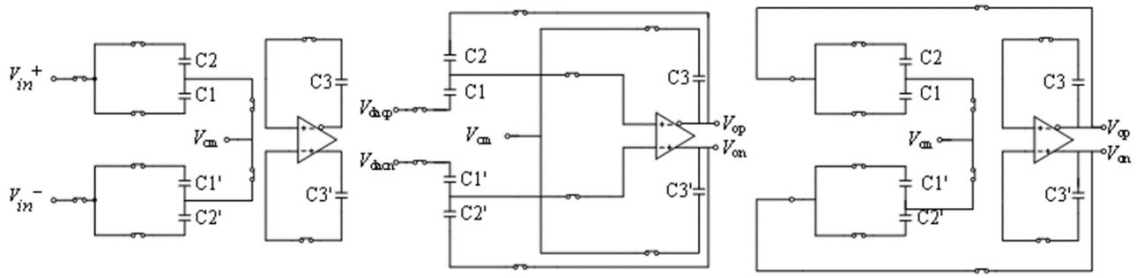

Figure 8. Schematic of simplified MDAC in (a) external input sampling phase, (b) charge transfer phase and (c) internal sampling phase.

The V_{res} works as the input for the sub-ADC and the MDAC. Phase Φ1 and phase Φ2 are repeated until the next external input sampling phase occurs, where the final output $D[4:0]$ of the ADC is calculated as equation (3.3), where the comma is a connector.

$$D\,[4:0] = \{a_1, a_2 + b_1, a_3 + b_2, a_4 + b_3, b_4\} \tag{3.3}$$

It is noticed that the last bit is the 0.5-bit of the output of the sub-ADC. At the beginning of each converting loop, the first internal sampling phase Φ1 and the external sampling phase Φ3 and are combined, thus it needs only four clock cycles for generating 5-bit.

4 Performance and discussion

Compared with the conventional cyclic ADC [3], this column-parallel ADC has the following major optimization. Firstly, the sub-ADC generates 1.5-bit in each interation, which improves the comparator's tolerance to the offset, thus prevents the residue from being out of scale. This ensures the system operates accurately as long as the offset voltage is less than Vref/4 [4]. Besides, the Sample and Hold block and the Residue Amplifying block in MDAC shares the same operational amplifier, instead of the two seperate amplifiers in the conventional cyclic ADC [3]. This significantly reduces power consumption. In addition, this column-parallel ADC combines the input signal sampling phase and the first converting phase into a single phase. Thus, it needs only $N-1$ clock cycles to complete N-bit conversion, which breaks the limitation on the speed of the conventional cyclic ADC.

This column-parallel ADC has been fabricated in 130-nm CMOS technology and the layout is shown in figure 9. The chip area occupies only $100\,\mu\text{m} \times 200\,\mu\text{m}$. With the voltage supply of 3.3 V, the power consumption is 4.5 mW, which includes 4.2 mW for analog part and 0.3 mW for digital part. The column-parallel ADC provides the sampling rate of 10 MS/s with the dynamic range of 1000 mV. Figure 10 shows the measured DNL/INL. The maximum DNL is $-0.039/0.055$ LSB and the maximum INL is $-0.048/0.095$ LSB. Figure 11 shows the fast Fourier transform power spectrum. The SNDR is 28.47 dB and the ENOB is 4.44 bits.

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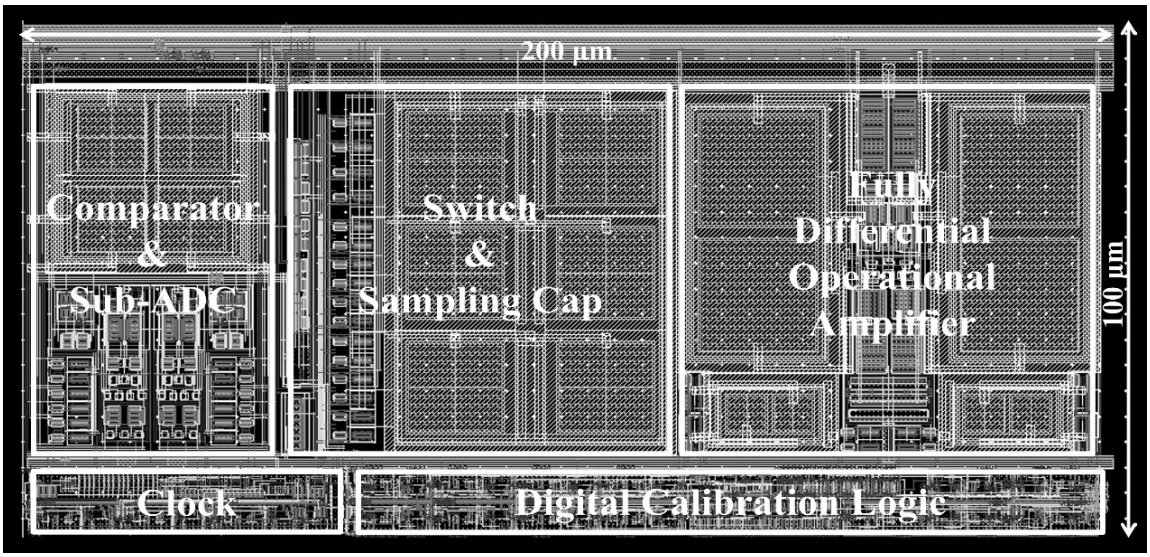

Figure 9. Layout of the proposed column-parallel ADC.

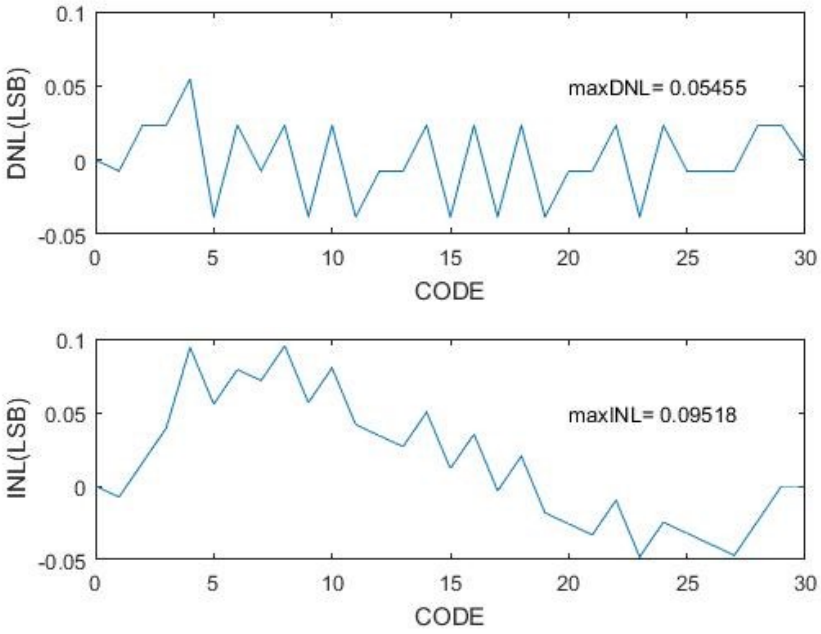

Figure 10. Measured DNL & INL of proposed ADC.

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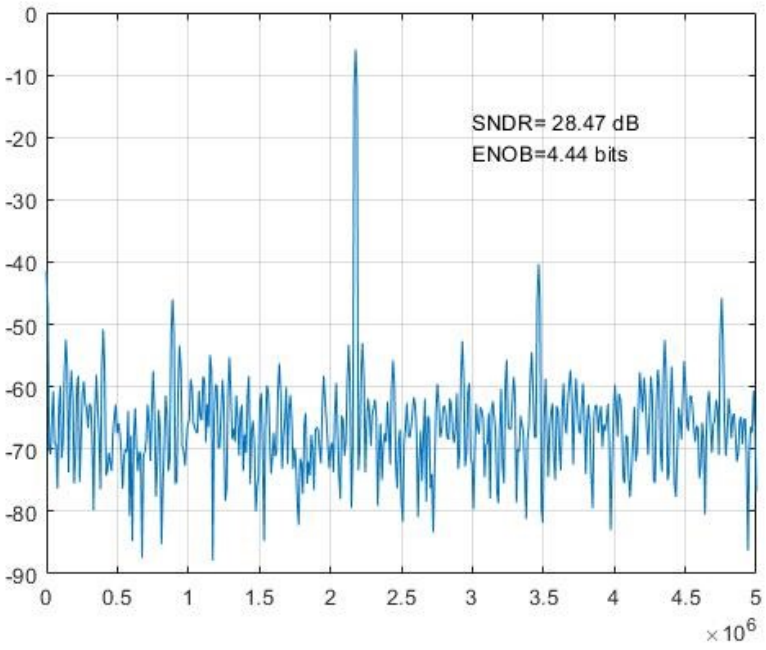

Figure 11. Measured power spectrum of proposed ADC.

Acknowledgments

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References

[1] H. Zhao, *Carbon Ion Therapy at Lanzhou*, *presented at the Workshop on "Ideas and technologies for a next generation facility for medical research and therapy with ions"*, Archamps, France, 19–21 June 2018.

[2] H.-C. Liu, Z.-M. Lee and J.-T. Wu, *A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration*, *IEEE J. Solid-State Circuits* **40** (2005) 1047.

[3] P. Li, M. Chin, P. Gray and R. Castello, *A ratio-independent algorithmic analog-to-digital conversion technique*, *IEEE J. Solid-State Circuits* **19** (1984) 828.

[4] Y.-C. Huang and T.-C. Lee, *A 0.02-mm^2 9-bit 50-MS/s cyclic ADC in 90-nm digital CMOS technology*, *IEEE J. Solid-State Circuits* **45** (2010) 610.

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