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Organic thin-film transistors with flame-annealed contacts

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Abstract

Reducing contact resistance is critical to developing high-performance organic field-effect transistors (OFETs) since it impacts both the device mobility and switching speed. Charge injection and collection has been optimized by applying chemical treatments to the contacts, such as self-assembled monolayers (SAMs), oxide interlayers, or dopants. Here, we tested how flame annealing the surface of the electrodes impacts the interface and bulk components of the contact resistance, as well as the overall device performance. A butane micro torch was used to flash-anneal the gold electrodes, which allowed gold grains to crystallize into larger domains. We found that, along with the grain size, the surface roughness of the contacts was also increased. SAM treatment created a lower work function shift on a flame annealed electrode than when deposited on an untreated surface, due to the greater surface roughness. This resulted in a larger interface contact resistance. However, flame annealing also produced an order of magnitude reduction in the density of trap states in the semiconductor layer, which reduced the bulk contact resistance and channel resistance. These competing effects yielded OFETs with similar performance as untreated devices.

1. Introduction

The organic field-effect transistor (OFET) is the basic building block for advanced electronics that can address an increasingly digitized age, from printable RFID tags to flexible displays, from skin-conformable biosensors to circuitry for smart solar cells. These exciting applications can become a reality when the OFET performance allows operation at high speeds. The transit frequency, i.e. the highest frequency at which the transistor can amplify signals, is dependent on the mobility of the charge carriers within the transistor channel, the contact resistance, and several geometrical factors, including the channel length and the gate-to-contact overlaps [1]. Radio frequency communication circuits require a minimum operating speed in the MHz range, while circuits for displays and computation demand GHz transistor switching speeds. Mobility values of organic semiconductors have increased significantly in the past decade and enabled high DC performance of OFETs [2–6], but contact resistance remains the bottleneck that limits

the performance of these devices [1]. Several different methods have been proposed for reducing contact resistance, such as the use of self-assembled monolayers (SAMs), doping, insertion of thin layers, and device geometry optimization [7–11]. We have recently shown that reducing the deposition rate of the electrode metal led to a drastic decrease in contact resistance and a corresponding increase in performance in both small molecule and polymer OFETs [12]. We obtained contact resistances as low as 200 Ω cm, and device mobilities as high as 19.2 cm² V⁻¹ s⁻¹ with the small-molecule 2,8-difluoro-5,11-bis(triethylsilyl)ethynyl anthradithiophene (diF-TES ADT) and 10 cm² V⁻¹ s⁻¹ with the polymer indacenodithiophene-co-benzothiadiazole (C₁₆IDT-BT) in devices with almost ideal current-voltage characteristics. This slow deposition rate of 0.5 Å s⁻¹ resulted in large, very flat grains of gold, which led to a high degree of order within the applied SAM and created high work function channels that enhanced charge injection. Here we attempt to increase the gold grain size further through post-

processing, by flash annealing the gold film using flame annealing. Flame annealing is a popular technique for creating flat domains of Au(111) crystal surfaces [13, 14], but, to the best of our knowledge, has never been used in conjunction with organic thin-film transistor (OTFT) devices. In this study, we employ the flame annealing technique to modify the source and drain contacts and explore its effect on OTFT performance. While the high temperatures characteristic to the flame annealing process make it incompatible with flexible electronics manufacturing, this method allowed us to alter the electrode surface properties in a unique way, which is inaccessible by chemical treatments [7]. We found that flame annealing the contacts does not significantly change the device performance due to the competing effects of a higher interface contact resistance as a result of a rough electrode and a lower bulk contact resistance and channel resistance through a reduction in the density of trap states within the polymer layer.

2. Materials and devices

2.1. Flame-annealed gold fabrication

To test the effects of flame annealing on the properties of the gold electrodes, films of gold were first deposited on a highly doped silicon substrate terminated with 200 nm of silicon dioxide (SiO_2). The SiO_2 layer was necessary in order to prevent the gold from forming an alloy with the underlying silicon during the flame annealing process [14]. To prepare the substrates for gold evaporation, they were rinsed with acetone and placed in an acetone bath at 85 °C for 10 min; rinsed with acetone, followed by isopropyl alcohol (IPA), and placed in an IPA bath at 85 °C for 10 min; rinsed with IPA, dried with a stream of nitrogen gas and exposed to a UV-ozone treatment for 10 min; thoroughly rinsed with deionized (DI) water and dried under a stream of nitrogen gas. A 5 nm titanium adhesion layer was first deposited using electron-beam evaporation at a pressure of 2×10^{-8} Torr and rate of 1 Å s^{-1} , followed by a 40 nm gold layer deposited through thermal deposition at a rate of 0.5 Å s^{-1} .

Shortly after deposition, the samples were flame annealed using a butane micro torch (Blazer GB-2001) with 'super refined' butane gas (Blazer RF-300). Samples were placed face-up on a steel stage, which acted as both the holder and the heat sink. In order to avoid oxidizing the gold surface, the butane torch was adjusted to a reducing flame by starting with a neutral flame and then restricting airflow until the flame was a lighter shade of blue (this was accompanied by an audible hiss in the micro torch). The torch was held at approximately 45° to the substrate so that the tip of the interior cone of the flame, the hottest part of the flame at ~1300 °C [15], was touching the gold surface. The flame was moved at a moderate rate by hand over the entire substrate (covering the entire surface

approximately every 2 s) for varying total anneal times from 0 to 5 min. Immediately after annealing, the films were rinsed with acetone and IPA to both cool them and provide a final cleaning. Samples were then rinsed with ethanol and treated for 30 min with a room-temperature 30 mM solution of pentafluorobenzene thiol (PFBT) in ethanol.

2.2. Flame-annealed gold characterization

The surface energy of the PFBT-treated gold samples was characterized through water contact goniometry (Ramé-Hart Model 200 Standard with DROPimage Standard). Samples were measured in air immediately after PFBT treatment, and contact angles of DI water and diiodomethane were measured at multiple spots on each sample. Surface energy was calculated from water and diiodomethane contact angles in the DROPimage Standard software using the Owens-Wendt geometric mean method [16].

AFM topology scans were carried out using an Asylum MFP-3D Bio AFM (Asylum Research, USA) in ambient atmosphere. A silicon cantilever (Asylum Research AC160TSA-R3, force constant: 26 N m^{-1} , resonance frequency: 250–300 kHz) was used in tapping mode with a feedback setpoint of 460–600 mV, and $1 \mu\text{m} \times 1 \mu\text{m}$ scans were performed at a rate of 0.3 Hz. Images were processed with Gwyddion software. Roughness values are the average of multiple spots and measurements per sample.

Kelvin probe measurements were made with a Trek Model 325 Electrostatic Voltmeter [17, 18]. Tip to sample height was 0.4 mm, and work functions were calculated by referencing measured voltage values to freshly cleaved highly-oriented pyrolytic graphite with a known work function of 4.48 eV [18].

2.3. Transistor fabrication

The top gate, bottom contact (TGBC) staggered geometry (figure 1(a)) was chosen for OFET fabrication. In this structure charges are injected over a larger surface area (roughly the contact width multiplied by the transfer length—a few to tens of microns) compared to coplanar devices, where injection occurs over an area roughly corresponding to the contact width multiplied by the thickness of the channel (a few nanometers) [7]. Thus, the TGBC devices are more sensitive to the post-processing explored in this study. In addition, since injection primarily takes place through the top surface of the contact, this surface is identical to the blanket gold films that we characterized, which allows us to relate the observed changes in the gold surface properties with the device parameters.

Substrates identical to those used for the blanket gold film characterization were also employed for transistor fabrication and the cleaning, gold deposition, flame annealing, and PFBT treatment were performed following the same procedures, with the only difference that now the Ti/Au layer was patterned by

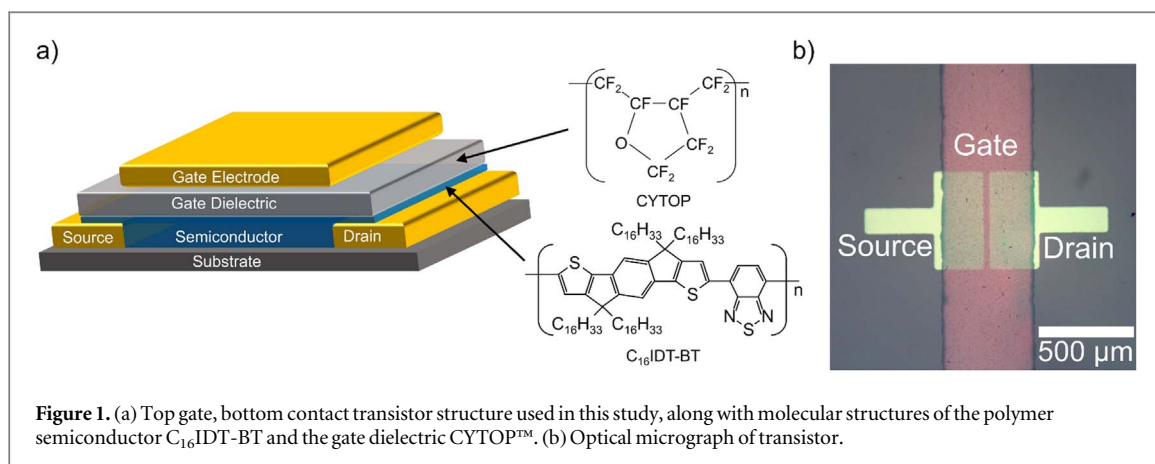


Figure 1. (a) Top gate, bottom contact transistor structure used in this study, along with molecular structures of the polymer semiconductor C₁₆IDT-BT and the gate dielectric CYTOP™. (b) Optical micrograph of transistor.

depositing it through a shadow mask to define the bottom contacts. OFETs were fabricated on electrodes that had not been annealed, serving as control samples, as well as on contacts that were flame-annealed. The polymer indacenodithiophene-*co*-benzothiadiazole (C₁₆IDT-BT, see chemical structure in figure 1(a)) was used as the semiconductor. It has been shown to exhibit high hole mobilities [19, 20], despite an apparent lack of long range order. An image of a device is included in figure 1(b). After PFBT treatment of the contacts, the samples were brought into a nitrogen glovebox and a 5 mg ml⁻¹ solution of C₁₆IDT-BT in chlorobenzene was spin-coated at 208 rad s⁻¹ (2000 RPM) for 60 s and then annealed on a hot plate at 100 °C for 10 min. A layer of CYTOP™ CTL-809-M top-gate dielectric ($\epsilon = 2.1$, structure shown in figure 1(a)) was spin-coated at 208 rad s⁻¹ (2000 RPM) for 60 s. Samples were then removed from the glovebox and placed in a vacuum oven at 50 °C for 8 h to anneal the dielectric layer. Transistors were completed by depositing a 30 nm gold top gate electrode through a shadow mask using electron beam evaporation at a rate of 2 Å s⁻¹.

2.4. Transistor characterization

OFETs were characterized using an Agilent 4155 C semiconductor parameter analyzer. Transistors were measured in the dark in a chamber that was first pumped down to the 0.1 mTorr range and then back-filled with nitrogen gas. A low flow of nitrogen gas was fed into the chamber during testing. Over 100 devices were measured for the control and flame anneal samples, and data was consistent across multiple fabrication runs. Linear mobility was calculated as [21]

$$\mu = \frac{L}{C_{diel} W V_{DS}} \frac{\partial I_D}{\partial V_{GS}}, \quad (1)$$

where L is channel length, C_{diel} is capacitance of the gate dielectric, W is channel width, V_{DS} is drain-source voltage, I_D is drain current, and V_{GS} is gate-source voltage. The slope of a linear fit to the I_D versus V_{GS} plot approximated $\partial I_D / \partial V_{GS}$. Contact resistance was estimated using the gated transfer length method (gTLM) by calculating the total device resistance in the

linear regime at an overdrive voltage of $V_{GS} - V_{th} = -35$ V (where V_{th} is the threshold voltage), plotting with respect to L , and extrapolating a linear fit to zero channel length [21] (see figure SI1, available online at stacks.iop.org/FPE/5/014015/mmedia). The trap density of states (DOS) spectrum was evaluated using the Grünewald's model [22, 23], which employs the linear regime transfer characteristics of the device. The linear $I_D - V_{GS}$ curves essentially give a V_{GS} -dependent conductivity. As the gate voltage is increased, traps are filled, and the resulting curves are fitted to give the trap DOS as a function of energy above the valence band.

Semiconductor film thickness for the control and flame annealed samples were characterized with the same AFM and silicon cantilevers used for the blanket films. Device films were first scored in several locations with a sharp probe tip, and then scans 25 μm × 25 μm in size were taken of the resulting trenches at a rate of 0.2 Hz and with a feedback setpoint of 600 mV. Film thickness was measured as the height difference between the trench and the surrounding level film. Images were processed in Gwyddion software.

3. Results and discussion

3.1. Blanket films

Figure 2(a) shows the water contact angle at the surface of the PFBT treated gold films that have been subjected to flame-annealing, while figure 2(b) (black symbols) provides quantitative details about this process. It can be observed that the contact angle decreases gradually from $93.6^\circ \pm 0.15^\circ$ in the control film to $55.9^\circ \pm 2.0^\circ$ after 5 min of flame annealing. Consequently, the surface energy of the films increased from 36 mJ m⁻² for the control to 47 mJ m⁻² for a 5 min anneal (see table SI1). Water contact angle is dependent on the surface energy of the substrate and both provide information about the effectiveness of SAM attachment. In the context of this study, the large contact angle obtained before flame annealing points to a highly ordered PFBT layer, in agreement with earlier work [24]. This order is reduced with the

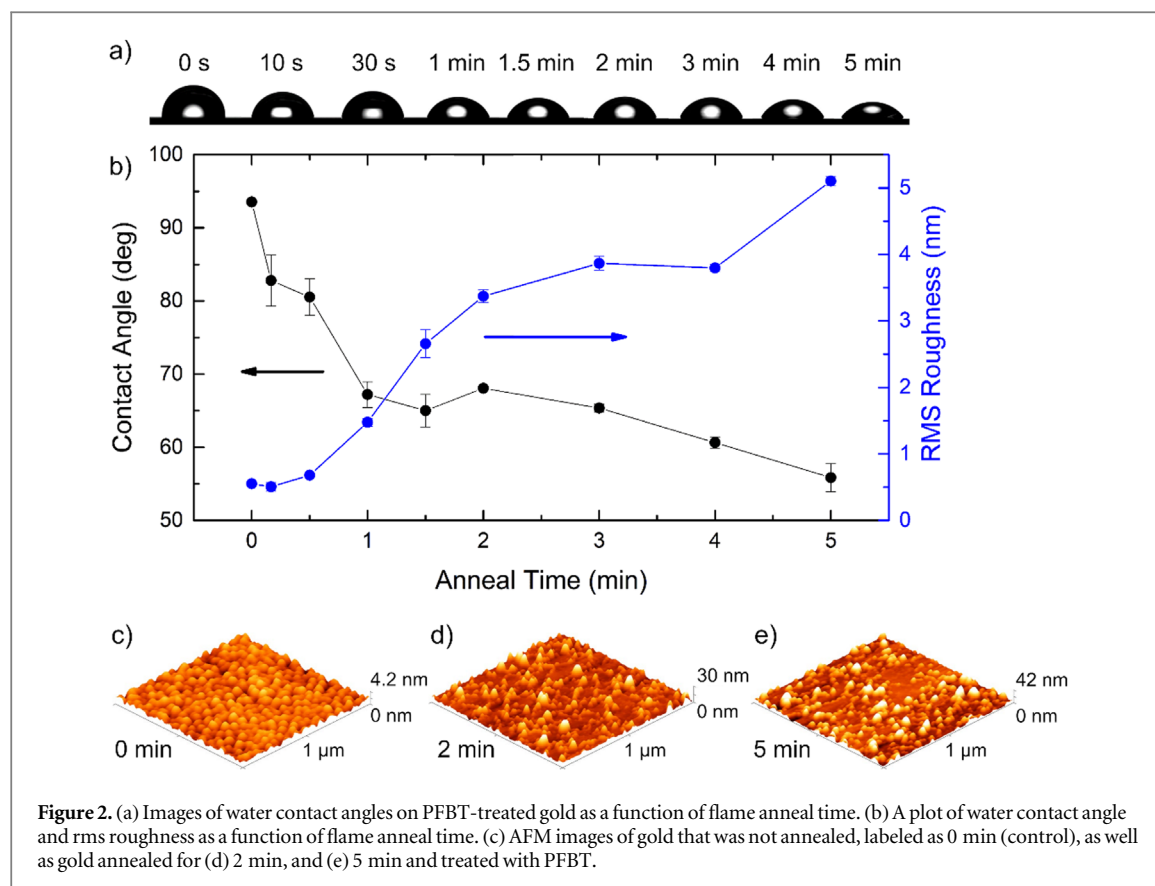


Figure 2. (a) Images of water contact angles on PFBT-treated gold as a function of flame anneal time. (b) A plot of water contact angle and rms roughness as a function of flame anneal time. (c) AFM images of gold that was not annealed, labeled as 0 min (control), as well as gold annealed for (d) 2 min, and (e) 5 min and treated with PFBT.

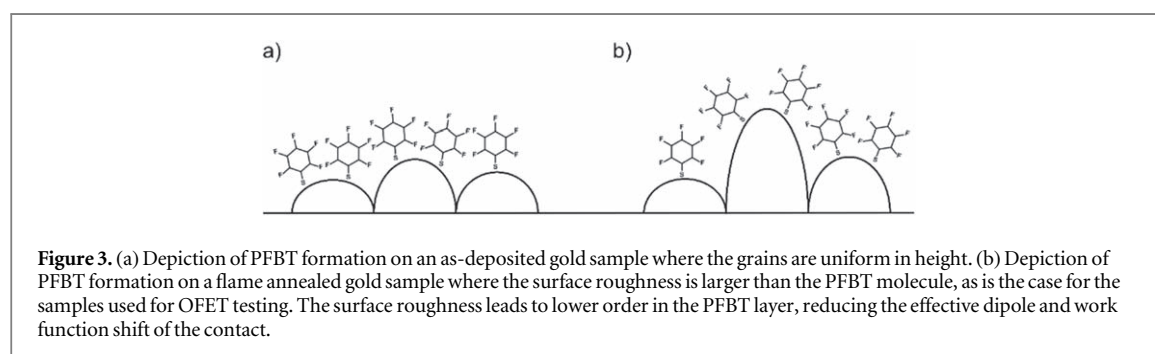
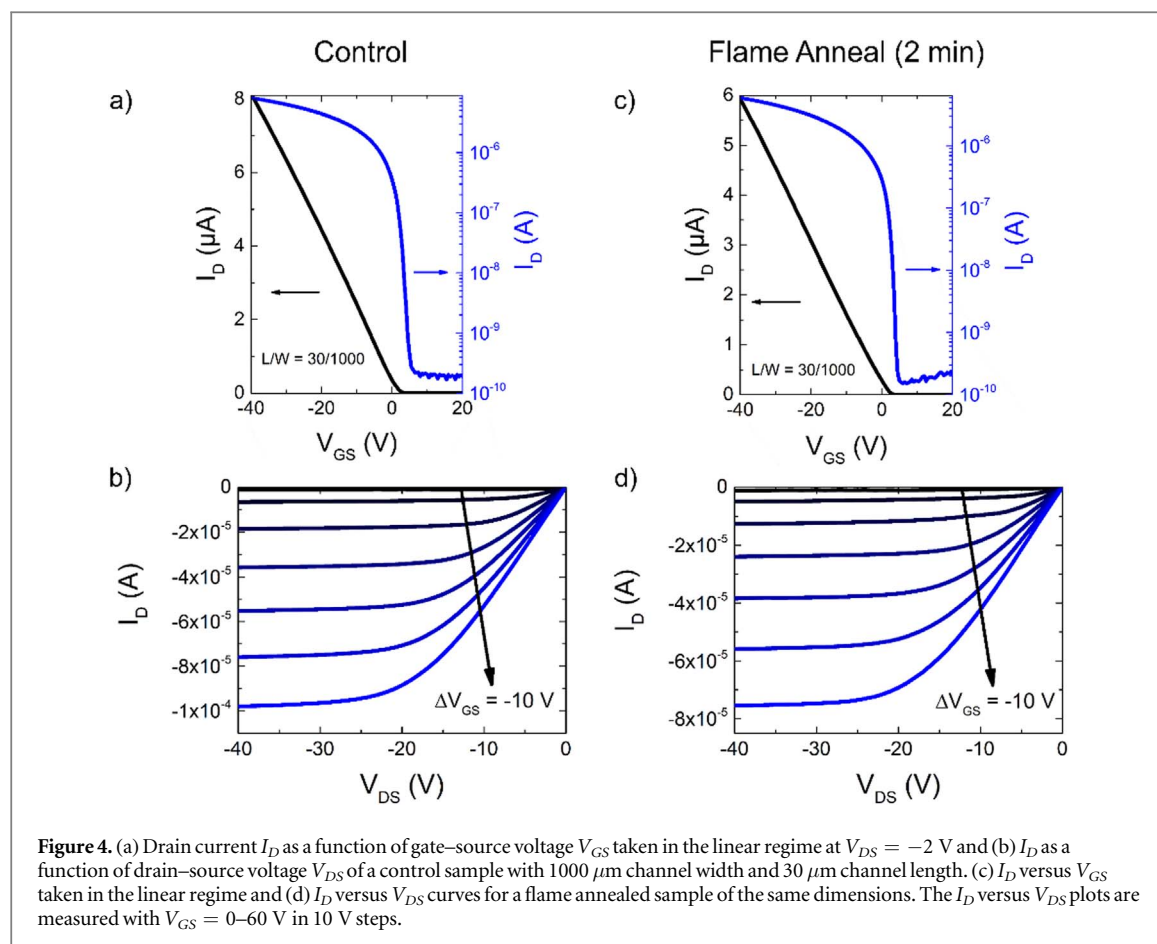


Figure 3. (a) Depiction of PFBT formation on an as-deposited gold sample where the grains are uniform in height. (b) Depiction of PFBT formation on a flame annealed gold sample where the surface roughness is larger than the PFBT molecule, as is the case for the samples used for OFET testing. The surface roughness leads to lower order in the PFBT layer, reducing the effective dipole and work function shift of the contact.

annealing time, suggesting that the PFBT layer is less uniform on the annealed gold substrates, consistent with the larger surface energy. To better understand the mechanism responsible for this behavior, we measured the roughness of PFBT-treated gold surfaces with respect to annealing time; the results are displayed in figure 2(b), in blue. We found that the reduction in the contact angle is accompanied by an increase in the surface roughness by one order of magnitude after 5 min annealing, from 0.53 ± 0.02 nm in the control film to 5.1 ± 0.7 nm. As can be seen in the AFM images (figure 2(c)), unannealed surfaces consist of small grains, and the surface is very uniform. (Note that these grains are small only compared to the grains on annealed surfaces; the grains on this control are still larger than for gold deposited at a faster rate [12].) On the contrary, flame-annealed gold surfaces exhibit grains that are larger in both diameter and height, and they

are spaced farther apart. As-deposited gold films are typically amorphous and/or exhibit random crystal orientation, but heating the gold post-deposition allows larger crystalline domains to form that are also preferentially terminated in a (111) surface [14], the ideal crystal face for SAM formation [25, 26]. This annealed surface influences SAM formation and charge injection.

While the long-range order of the PFBT layer is reduced when flame-annealing is performed prior to SAM deposition, given the topography of the gold surface, it is possible that local domains of highly ordered PFBT form on the surface of the grains or in the flats in between large grains. This process would yield high work function regions, enhancing charge injection at the larger grains, where static charge is likely to accumulate. However, the PFBT molecule is only 5.9 \AA long, a length similar to the roughness of the control electrode and an order of magnitude smaller than the



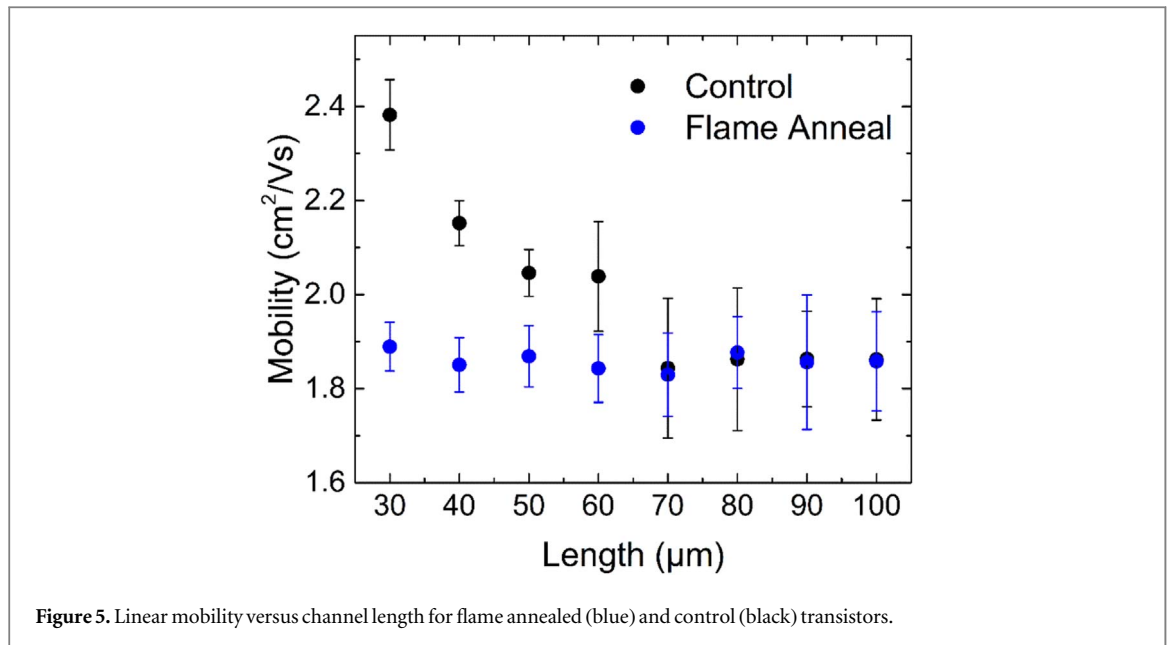
roughness of the 5 min flame-annealed electrode. As depicted in figure 3(a), similar length scales between the SAM and the surface allow for a more even monolayer than when the surface roughness is much larger than the SAM, such as the case of the samples subjected to long flame annealing times and schematically shown in figure 3(b). The large disparity between surface roughness and SAM molecule size in annealed samples might also lead to a lower-density SAM layer since the aggressive topography will interrupt SAM packing.

A uniform SAM layer has parallel molecular dipoles, which maximizes the overall effective dipole of the surface and thus the work function shift. A lower degree of order of the molecules within the SAM layer results in more randomly oriented dipoles, a smaller effective dipole and therefore a less significant work function shift. A decrease in SAM density will also lessen the effect. Indeed, Kelvin probe measurements indicate a work function value of 5.4 eV for unannealed gold treated with PFBT, in agreement with earlier reports [17, 24, 27, 28]. The electrode work function shifts to 5.0 eV for the 2 min flame annealed samples used for device work. This 0.4 eV difference is congruent with the changes detected in the water contact angle, surface energy, and surface roughness. Since the ionization potential of C_{16} IDT-BT is 5.4 eV [29], the injection is expected to be efficient in the case of the unannealed contact, while the flame annealed

contact forms a Schottky barrier, although effects like Fermi-level pinning, surface chemistry, and semiconductor film morphology do not guarantee this scenario [7].

3.2. Transistor characterization

To test the effect of flame annealed contacts on transistor performance, we fabricated OFETs with unannealed contacts (control) and compared them to OFETs with flame annealed contacts. Figure 4 shows the current-voltage characteristics of a control transistor (panels (a) and (b)) and a 2 min flame-annealed contacts transistor (panels (c) and (d)). Results for other annealing times are included in table SI2. The linear operating regime of the transfer plot is the most important for switching and signal applications, and we focus on that here. Both device types exhibit low threshold voltages, sharp turn on, a linear response of the drain current (I_D) with the gate voltage (V_{GS}), and gate-independent mobility (μ). The reliability factors for these two devices are both 0.93 (a reliability factor of 1 corresponds to an ideal device) [30]. This reliability factor implies that, even if bad contacts were present, the true mobility of the devices is within 7% of the measured value, and 0.93 is on par with or better values reported for other systems [31–33], with the exception of single crystals [30]. Measurements on a large set of devices (over 100) resulted in a lower average threshold voltage in the flame annealed



OFETs, $V_{th} = 2.7 \text{ V} \pm 1.2 \text{ V}$, compared to $V_{th} = 6.2 \text{ V} \pm 1.2 \text{ V}$ in the control, suggesting a lower density of traps in these samples. This is in agreement with the smaller sub-threshold slope ($S = 1.7 \text{ V/dec} \pm 0.6 \text{ V/dec}$ in flame-annealed devices versus $S = 1.9 \text{ V/dec} \pm 1.2 \text{ V/dec}$). Output curves (I_D versus V_{DS}) are devoid of the S-shape response near $V_{DS} = 0$, which, if present, would be a marker for excessive contact resistance.

Performance in terms of linear mobility was similar for both sets of devices, with the flame annealed set exhibiting an average of $\mu = 1.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \pm 0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and the control set showing an average of $\mu = 2.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \pm 0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, in agreement with earlier reports [34]. Higher mobilities are possible by reducing IDTBT film thickness [12].

Examining of the evolution of the mobility versus channel length L yields additional insight (figure 5). It can be clearly seen that the mobility decreases with channel length for the control samples and it is constant for the flame annealed samples. The dependence of mobility on channel length is governed by several factors. A mobility that decreases with channel length results from electronic traps within the organic semiconductor layer (i.e. within the channel), while a mobility that increases with channel length is a signature of high contact resistance. The overall slope of the μ versus L plot is a convolution of the two, and in the following we will focus on describing them separately.

Charge carrier traps are ubiquitous in organic semiconductors and originate from various intrinsic and extrinsic sources such as structural defects, chemical impurities, bias stress, exposure to environmental contaminants and from interfacing with different materials [35]. A threshold voltage shift from a value of zero is indicative of trapping. Indeed, the greater

threshold voltages for the control devices compared to the flame annealed devices indicate that a higher density of interface trap states is present in the control. Trapping is also directly related to the subthreshold slope S :

$$S = \frac{k_B T \ln(10)}{q} \left(\frac{N_{it} q^2}{C_{diel}} + 1 \right), \quad (2)$$

where N_{it} is the density of interfacial traps, k_B is Boltzmann's constant, T is the temperature, q is the elementary charge, and C_{diel} is the dielectric capacitance per unit area. The average subthreshold slope of the flame annealed samples is slightly lower than that of the control ($S = 1.7 \text{ V/dec}$ versus $S = 1.9 \text{ V/dec}$), confirming that the density of trap states is decreased in the flame annealed samples.

To access the density of traps with greater accuracy and characterize their energetic distribution, we performed a spectral analysis of the trap DOS for the two types of devices. In OFETs, the application of the gate-source voltage moves the quasi-fermi level of the organic semiconductor, initially located around the midgap, towards the band edges thereby probing any trap states present in that energy interval and enabling the extraction of the trap DOS as a function of energy above the valence band edge. Figure 6 shows the trap DOS spectra obtained from a representative subset of control (black lines) and flame annealed (blue lines) devices. The spread in the DOS observed for each sample type is a result of variations in film quality, and such a spread is typical for organic semiconductors, including single crystals [36]. While the distribution of shallow traps (within a few kT above the valence band edge) was found to be similar, there is a prominent difference in the DOS lying deeper in the band-gap. In order to gain further insight into the trap parameters, the DOS spectrum of each sample type was individually modeled using a double exponential function to

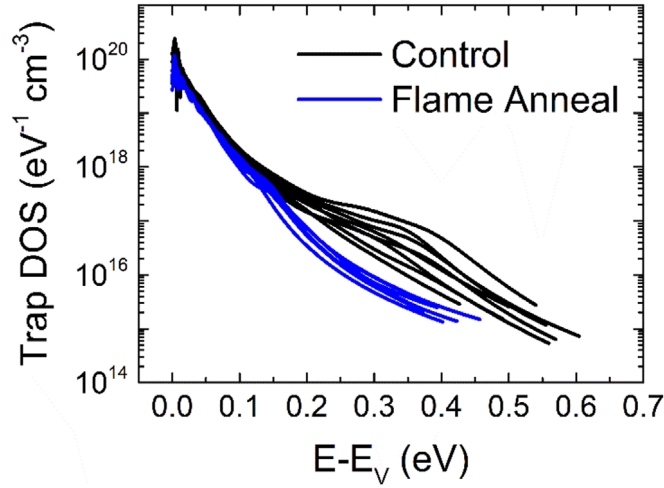


Figure 6. Trap density of states for select devices from the control group (black) and flame anneal group (blue). Trap density is given as a function of energy above the valence band edge. The flame annealed samples show an order of magnitude decrease in the trap density centered around 0.3 eV above the band edge.

Table 1. Fit parameters for the double exponential and Gaussian distributions. The flame-annealed devices were modeled using only exponential fits and so the Gaussian parameters (A , E_{peak} , and σ) are not applicable.

Model parameter	Control	Flame annealed
N_1 ($\text{eV}^{-1} \text{cm}^{-3}$)	1.2×10^{20}	7.0×10^{19}
E_1 (meV)	20.3	24.4
N_2 ($\text{eV}^{-1} \text{cm}^{-3}$)	5.3×10^{18}	3.5×10^{17}
E_2 (meV)	67.4	71.2
A ($\text{eV}^{-1} \text{cm}^{-3}$)	9.1×10^{16}	—
E_{peak} (meV)	250	—
σ (eV)	0.1	—

describe the distribution of shallow and deep states, respectively, with the addition of a Gaussian function to model the control curve according to the following equation:

$$N(E) = N_1 \exp\left(-\frac{E}{E_1}\right) + N_2 \exp\left(-\frac{E}{E_2}\right) + A \exp\left[-\frac{(E - E_{peak})^2}{2\sigma^2}\right], \quad (3)$$

where E_1 and E_2 are the characteristic decay energies, N_1 and N_2 are the amplitudes of the respective exponential distributions, and E_{peak} defines the position of the Gaussian distribution with an amplitude A and standard deviation σ . The model parameters and the fits to experimental data are provided in table 1 and figure SI2, respectively. We found that the characteristic energy for the double exponential distributions are similar for the control and flame annealed devices (~ 20 meV for shallow states and ~ 70 meV for deeper states), but there is a significant difference in the trap densities, especially those of deep states ($N_2 = 5.3 \times 10^{18} \text{ eV}^{-1} \text{cm}^{-3}$ for the control and $3.5 \times 10^{17} \text{ eV}^{-1} \text{cm}^{-3}$ for the flame-annealed devices). The Gaussian distribution centered at 0.25 eV from the valence band edge accounts for the

broadening of the density of deep states evident in the spectrum of the control, a feature that is absent in the flame annealed devices. The nature of the predominant trap centered around this energy is still under investigation, but we suspect it might originate from water trapped at the SiO_2 interface and that is eliminated during the flash annealing step. Water residing in the voids present within the $\text{C}_{16}\text{IDT-BT}$ film has been shown to generate electronic traps responsible for performance degradation [37, 38]. By calculating the area under each curve, the total trap densities were determined to be approximately $2.5 \times 10^{18}/\text{cm}^3$ for the control and $6.9 \times 10^{17}/\text{cm}^3$ for the flame-annealed devices—more than an order of magnitude reduction in the trap densities upon flame-annealing.

The lower trap densities in the $\text{C}_{16}\text{IDT-BT}$ layer deposited on flame annealed electrodes reduces both the channel resistance, R_{ch} , and the bulk component of the contact resistance, $R_{C,bulk}$, as we will detail later. A thorough description of the mechanism through which this occurs is still under investigation, but we hypothesize that the order in the semiconductor film is superior when deposited on flame-annealed surfaces, and that the traps present on the SiO_2 surface are passivated. The passivated traps could otherwise diffuse into the polymer film, much like a dopant, or influence polymer order by causing dislocations. In a staggered-structure device, like the TGBC we use here, there are two contributions to contact resistance. First, the interface contact resistance $R_{C,int}$ corresponds to the voltage necessary to transfer charges from the surface of the electrode into the semiconductor. Second, the bulk contact resistance $R_{C,bulk}$ is the resistance resulting from moving injected charge from the interface between the semiconductor and contact through the thickness of the semiconductor and into the channel [7]. We estimated the contact resistance in our devices using the gated transfer length method (gTLM

—see figure SI1; note that we restricted our analysis to the regions of constant mobility, as extracted from figure 5, to ensure the validity of the gTLM model). The width-normalized contact resistance of the control group is $R_C = 1.8 \text{ k}\Omega \text{ cm}$, while the contact resistance for the flame annealed group is $R_C = 2.6 \text{ k}\Omega \text{ cm}$. We note that the contact resistance in the control sample is higher than the value of $200 \text{ }\Omega \text{ cm}$ previously reported for IDTBT devices with source and drain fabricated using similar conditions. The high contact resistance obtained in this work is a result of a thicker semiconductor layer that we had to adopt due to the rough surface and that leads to a larger $R_{C,bulk}$. The measured semiconductor thickness of the control and the flame annealed samples were within error of each other ($28 \text{ nm} \pm 3 \text{ nm}$ for the control and $30 \text{ nm} \pm 4 \text{ nm}$ for the flame annealed—see figure SI3), therefore the difference in $R_{C,bulk}$ results only from the change in the properties of the semiconductor layer. In the context of device structure, we can surmise that there are two competing effects in play. First, the flame annealing step increases the $R_{C,int}$ component of the contact resistance. In the case of the unannealed electrodes, the good alignment between the HOMO level of C_{16} IDT-BT and the electrode work function is favorable for injection. On the contrary, the lower order in the PFBT film characteristic to flame-annealed devices results in an injection barrier, which translates to a larger $R_{C,int}$. Second, flame annealing reduces $R_{C,bulk}$ by lowering the density of trap states in the polymer film, effectively increasing the mobility of the semiconductor in the direction perpendicular to the channel. The overall result is an increase in the contact resistance due to the larger contribution of the $R_{C,int}$ component.

4. Conclusion

We evaluated the effect of flame annealing on the performance of OFETs and found that that it impacts both the channel and the contact resistance. On one hand, it results in a high interfacial contact resistance, $R_{C,int}$ due to the creation of a less uniform layer of PFBT on surface of the contacts, as evidenced by reduced water contact angle, increase in surface roughness, and a decrease in electrode work function. On the other hand, flame annealing led to an order of magnitude reduction in the density of interfacial trap states, lowering the semiconductor bulk component of the contact resistance, $R_{C,bulk}$ and the channel resistance, R_{ch} . As a result, OFETs with flame-annealed contacts exhibit similar mobility as those not annealed due to the competing effects of lower trap density within the organic semiconductor layer and higher interface contact resistance.

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