Research on Clock Source Correction Method based on Wireless Sensor Network and TPSN Network Protocol

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Abstract. By analyzing TPSN synchronization protocol and various uncertain factors, this paper summarizes the concept of wireless sensor network and the research status of clock synchronization technology in wireless sensor network. To solve the problem that TPSN did not estimate the clock frequency drift, a new idea of wireless sensor network development is proposed: the node local clock self-correction method. The average clock deviation index is designed to evaluate the clock accuracy in a synchronous period. The experimental results show that this method is easy to implement. The synchronization period can be extended, the synchronization cost can be reduced and the energy consumption can be saved.

1. Introduction

In recent years, with the rapid development of MEMS technology and microprocessing technology of microelectromechanical system, sensor technology tends to be intelligent. The fusion of MEMS technology and radio frequence communication technology promotes the birth of wireless sensor network and lays a foundation for the development of Internet of things[1]. As a key technology in wireless sensor network, clock synchronization technology has become a hot topic of many scholars[2]. More and more applications of this technology, such as power management, energy saving detection, transmission scheduling, positioning and tracking, data fusion, marking data acquisition time and security protocol, must ensure that the network node clock is consistent. Therefore, it is of great significance to study the clock synchronization technology of wireless sensor network. The clock synchronization algorithm in traditional network has achieved mature and reliable results and been widely applied. However, due to the limitation of battery energy and hardware resources, the synchronization mechanism of traditional network is not suitable for wireless sensor network[3].

2. WSN clock synchronization technology concept

Wireless sensor networks (WSNS) are generally defined as nodes that work in a collaborative manner, using sensors to sense and control the surrounding environment and communicate wirelessly[4]. A typical WSN architecture of wireless sensor network is composed of three parts, namely sensor node, sink node (gateway) and monitoring center (task manager)[5]. The sensor node and sink node constitute the sensor field, and the sink node and the user are interconnected through the Internet. The basic framework of wireless sensor network is shown in figure 1.

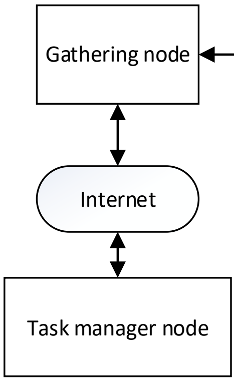

Figure 1 Basic framework of wireless sensor networks

Each sensor node typically consists of a sensor, CPU, wireless unit, and power supply[6]. Firstly, the sensor is used to monitor and monitor the surrounding environment data. Finally, the calculated data is transmitted to the sink node through the wireless cell through the wireless channel between nodes, and then the collected data is sent to the user.The core of wireless sensor network node is sensor. Sensors convert environmental variables such as light, heat and sound into electrical signals[7].The node structure of wireless sensor network is shown in figure 2.

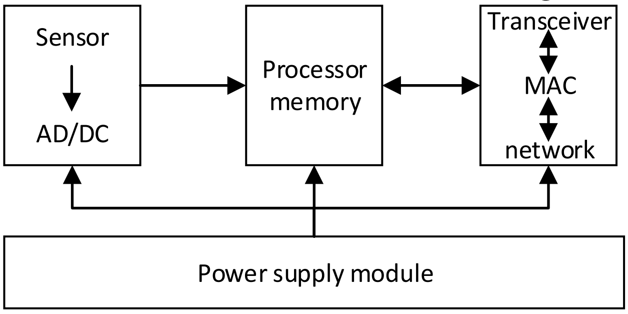

Figure 2 Node structure of wireless sensor network

3. TPSN synchronization protocol

TPSN protocol adopts hierarchical network structure. A root node is set as the clock source of the whole wireless sensor network, and the time synchronization of all wireless sensor nodes and root nodes is realized through switching packet[8]. However, the energy consumption of switching packet is much higher than that of information processing. The synchronization process between each two nodes is shown in figure 3.

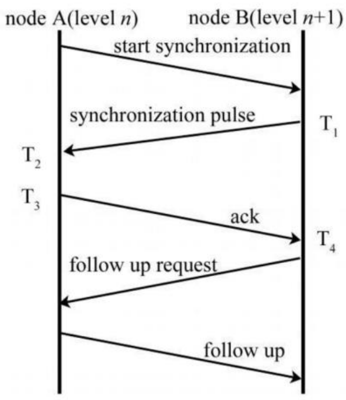

Figure 3 TPSN synchronous grouping crossover

T1, T2, T3 and T4 are timestamps of node A and node B sending and receiving grouping respectively.

If the clock deviation value of the two nodes is Δ, and the packet transmission delay is δ_1、δ_2, then:

$$T_2 = T_1 + \Delta + \delta_1$$
$$T_4 = T_3 - \Delta + \delta_2 \tag{1}$$

Δ can be calculated from the above formula:

$$\Delta = \frac{(T_2 - T_1) - (T_4 - T_3)}{2} - \frac{\delta_1 - \delta_2}{2} \tag{2}$$

The calculation process of formula (2) is completed in node B, and the synchronization of node B and node A only needs to add deviation Δ on the local clock of node B. TPSN aims to eliminate the influence of δ_1、δ_2 on Δ through symmetry of interaction grouping between nodes.

4. Clock deviation uncertainty analysis

4.1 Packet transfer delay uncertainty

The packet transmission time is composed of four parts: transmission time, access time, transmission time and reception time. Each part causes a certain time delay and is expressed by $\delta_s, j, t_p, \tau, \delta_r, i$ respectively. For groups of equal size, 7 and 8 in two directions are equal. Combining with formula (2), we get:

$$\frac{\delta_1 - \delta_2}{2} = \frac{\delta_{s,i} - \delta_{s,j}}{2} + \frac{\delta_{r,j} - \delta_{r,i}}{2} \tag{3}$$

If the packet to send, receive timestamp in MAC layer, guarantee the symmetry group interaction, from TPSN synchronous deviation calculation formula can follow in this case deviation of packet transmission delay Δ can eliminate the influence of [9].

4.2 Clock frequency uncertainty

IIdeally, the clock frequency of each node should be the same, and it will run stably after synchronization without any cumulative deviation. In fact, due to the difference of crystal frequency between different nodes, the actual clocks CA(t) and CB(t) of the two nodes will drift after synchronization. Due to the stability of crystal frequency, there is a certain linear relationship between them:

$$C_A(t) - C_A(t_0) = k\left(C_B(t) - C_B(t_0)\right) \tag{4}$$

$$C_A(t) = kC_B(t) + C_A(t_0) - kC_B(t_0) \tag{5}$$

CA(t0) and CB(t0) are the clock real time values of two nodes after the completion of each synchronization process. K represents the crystal vibration drift rate of node A relative to node b. ideally, the value of k should be 1, but normally the PPM of crystal vibration is 10 ~ 100, that is, 1s will produce the drift of 10 ~ 100 muons, and k will also produce the deviation of ±0.00001 ~ 0.0001.

In figure 4, the solid line represents the linear relationship of the actual clock of the two nodes after synchronization, and the point line represents the linear relationship of the clock of the two nodes in the case of no crystal oscillator drift

$$d = C_A(t_0) - kC_B(t_0) \tag{6}$$

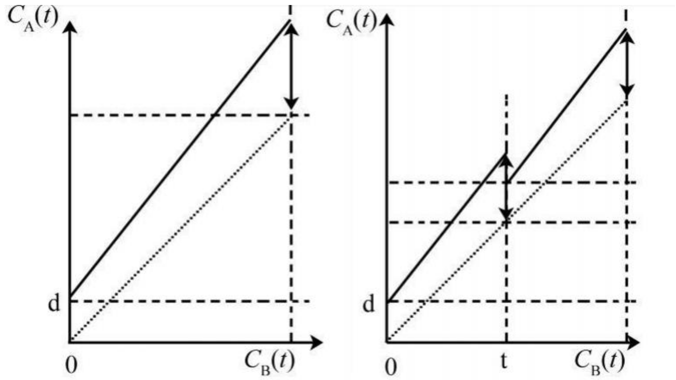

Figure 4 linear relationship between the two synchronous nodes' actual clocks

The left figure in figure 4 shows the result curve after one synchronization, and the right figure in figure 4 shows two synchronization at time 0 and time t.

As can be seen from both figures, the absolute deviation of d will be generated after each synchronization. With the passage of time, the cumulative deviation of the two nodes clock caused by crystal oscillation drift increases gradually, and the longer the synchronization period, the greater the clock deviation before the next synchronization [10].

5. Clock self-correcting method

According to formula (5), the deviation between the local clock and the reference clock at time t is:

$$\begin{aligned}\Delta &= C_A(t) - C_B(t) = \\ &(k-1)C_B(t) + C_A(t_0) - kC_B(t_0)\end{aligned} \tag{7}$$

5.1 Realization of self - correction

After the TPSN protocol synchronization, get a local clock synchronization cycle and the reference clock deviation, the two nodes counter ticks value difference, record for Δ, synchronous cycle for T, according to the linear relationship between Δ and T, and produce a tick deviation of time:

$$T\_comp = \frac{T}{\Delta} \tag{8}$$

According to the previous T_comp and Δ, to adjust the CCR moment t_sec can be calculated, when the moment arrives according to T_comp. The sign of positive and negative values for CCR, plus or minus one do when the counter value of ticks again arrived at the new CCR set data, which completed a clock compensation, reset the CCR after each compensation value and calculate the next moment t_sec compensation, after the completion of Δ, the end of the clock synchronization cycle compensation. The formula for calculating the moment of the NTH regulation is as follows:

$$\mathrm{t\_sec} = \mathrm{T - comp.sec} \times n + (\mathrm{T\_comp.ticks} \times n) \div 32768 \tag{9}$$

5.2 Average clock deviation indicator algorithm

Converts T_comp to a real value in seconds for g, I to compensate time serial number, its value is 1 to Δ, figure 5 for each deviation curves before and after compensation, with the figure of two synchronous process between the area of the shaded part divided by synchronous cycle, can get a synchronous cycle average clock deviation.

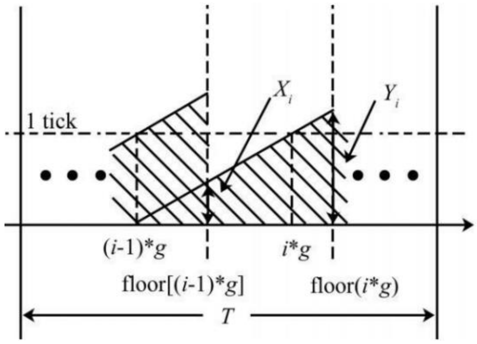

Figure 5 variation of clock deviation after compensation

The shadow between each compensation time in the figure is trapezoid, and the upper and lower bases are X_i and Y_i, respectively, and the height is Hi. Floor () is the upper integer function. Then X_i can be obtained according to the proportion relationship in the figure:

$$\frac{\text{floor}[(i-1)g]-(i-1)g}{g}=\frac{X_i}{1} \tag{10}$$

$$X_i=\frac{1}{g}\{floor[(i-1)g]-(i-1)g\} \tag{11}$$

In the same way, we get Y_i:

$$\frac{g}{floor(i\times g)-(i-1)g}=\frac{1}{Y_i} \tag{12}$$

$$Y_i=\frac{1}{g}[floor(ig)-(i-1)g] \tag{13}$$

The height of the trapezoid H_i is:

$$H_i= floor(i^\circ g)- floor[(i-1)g] \tag{14}$$

The area of trapezoid S_i is:

$$S_i=\frac{1}{2}\circ(X_i+Y_i)\circ H_i=$$

$$\frac{1}{2g} floor^2(i\circ g)- floor^2[(i-1)g]-$$

$$(i-1)\circ\{floor(i\circ g)- floor[(i-1)g]\} \tag{15}$$

$$S=\sum_{i=1}^{\Delta}S_i=\frac{1}{2g} floor^2(\Delta\circ g)+ floor(\Delta\circ g)-\sum_{i=1}^{\Delta}i\times\{floor(i\circ g)- floor[(i-1)g]\} \tag{16}$$

Substitute g into:

$$S=T+\sum_{i=1}^{\Delta} floor[(i-1)g]-\frac{\Delta\circ T}{2} \tag{17}$$

Then the average deviation $\overline{\Delta}$ is:

$$\overline{\Delta}=\frac{S}{T}=1+\frac{1}{T}\sum_{i=1}^{\Delta} floor[(i-1)g]-\frac{\Delta}{2} \tag{18}$$

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6. Experimental results and analysis

The experimental method is two-node two-stage synchronization. The reference clock node initiatively initiates the synchronization request, and the clocks of the two nodes are sampled respectively. The sampling period is 1s.

Figure 6, figure 7 and figure 8 are the deviation curves of different synchronization periods (20s, 10s and 1s) without applying the self-correction algorithm.It can be seen from figure 6 to figure 7 that the synchronization deviation has the following characteristics: after each synchronization, the deviation is gradually increased due to crystal vibration drift until the next synchronization. Shorten the synchronization period, can reduce the maximum deviation before each synchronization. 7 is the deviation curve after applying the node self-calibration algorithm when the synchronization period is 20s.

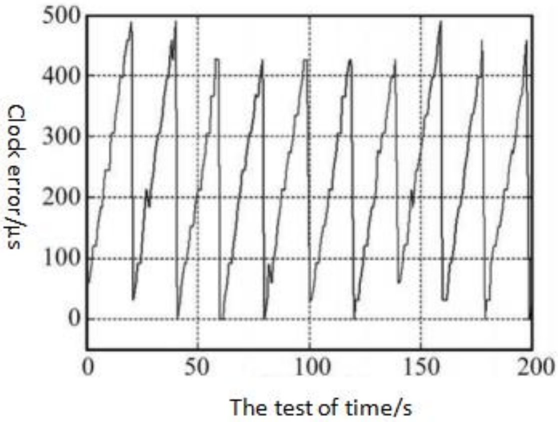

Figure 6 synchronization deviation curve with 20s synchronization cycle

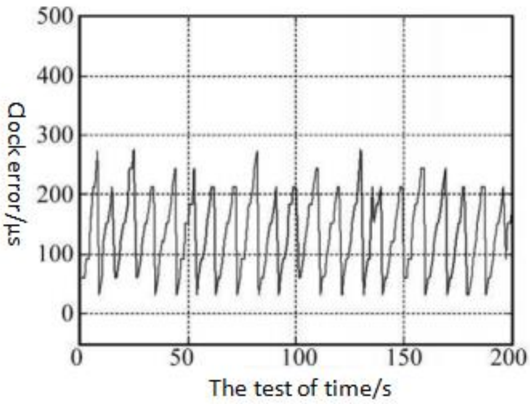

Figure 7 synchronization deviation curve with a synchronization period of 10s

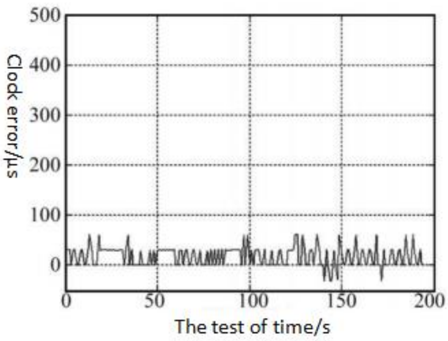

Figure 8 synchronization deviation curve with a synchronization period of 1s

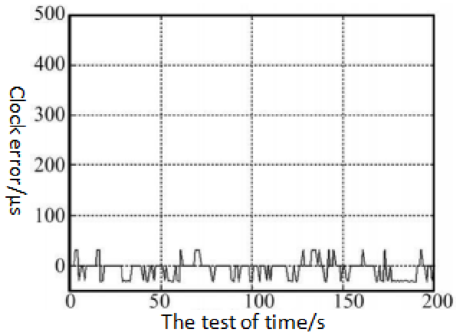

Figure. 9 synchronization deviation curve with 20s synchronization cycle after self-correction

By comparing the experimental results before and after using the node self-correction algorithm, it can be seen that after compensation, the clock deviation no longer has obvious drift and tends to a stable state. The deviation is mainly distributed within ±100 microns, which has reached the effect that the synchronization period before self-correction is 1s, and no obvious synchronization time can be distinguished. Theoretically, the synchronization period can be extended indefinitely until the synchronization error or the device power off and restart.

Experiment for synchronous cycle of 20 s clock bias is 14 ticks, so the need for 14 times compensation, the time interval 1 tick deviation of 20 present 14 material 1.428, each time 1 tick deviation corresponding compensation time 2 s, 3 s, 5 s, 6 s, 8 s, 9 s, 10 s, 12, 13, 15, 16 s s s s, 18, 19, 20 s s s, will be more than the value in equation (5-18), Δ = 1.65, the average deviation is about 1.65 x 1 present = 50 mu 32768 s, in accordance with the basic figure 6.4.

7. Conclusion

The traditional clock synchronization method requires a precise phase microstep regulator, and the drift rules of various driving sources are also different. Even if the clocks are fully aligned at the time of two kinds of alignment, errors will occur after alignment. It is still necessary to observe the drift rules of the drive source of the compared clock relative to the standard clock. The initial short-wave timing was only in the order of milliseconds, followed by microseconds in the longer wave, but global coverage was difficult to achieve. Although the traditional clock synchronization algorithm has achieved reliable results and applications, it still has many limitations due to battery energy and hardware resources. The proposed method can maximize cut two synchronization process between the crystal frequency drift, has important significance for long-term stable operation of the network, in practice, exists in the adjacent nodes at the same time and the reference node synchronous interaction, and adjacent level synchronization hidden terminal, coordinator should be effective scheduling allocation for each node synchronization time; For errors in synchronization process, the stability of synchronization correction can be ensured by feedback of synchronization deviation value in addition to the backup of the previous synchronization clock.

Acknowledgments

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