

Simulation and experiment of a new DC fault current limiter topology

Wenjie Wang, Jianzheng Liu

Department of Electrical Engineering, Tsinghua University, Beijing 100084, China

*Corresponding author's e-mail: wangwj17@163.com

Abstract. With the development of high voltage direct current (HVDC) power transmission system, it is imperative to develop a practical current limiting device which can effectively protect the converter from the influence of fault current. Based on the topology of current limiter proposed in previous papers, considering the requirements of practical application conditions, an optimized topology is proposed, which consists of snubber circuit and arrester, both in simulation and experiment. In addition, the RC buffering circuit is added and the parameters are optimized to reduce the voltage impulse that the IGBT of fault current limiter would else bear. Simulation and experiment are carried out in DC system. Both simulation and experiment results can prove the effectiveness of the optimized current limiter circuit.

1. Introduction

Due to its technical and economic advantages, HVDC power transmission has been applied more and more widely at the present stage. Faults such as load short-circuit of the DC system will affect its own operation, for example shock current will cause damage to components and failure of commutator commutation. The key to the development of HVDC transmission system is to develop and optimize a device, that is, the DC current limiter which can effectively limit the DC current when there is a fault.

There has been a lot of researches on DC fault current limiter (FCL) [1-5]. Usually the emphasis of these papers is about the theoretical analysis, topological optimization or simulation. But there are very few engineering cases that can be directly applied to physical objects, which take practical problems into account.

There has also been effective inductance current limiter, which uses the characteristics of inductance, that it passes low frequency current and stops high frequency current, to change the DC current into high-frequency alternating current, so as to control the current within a certain range to achieve the effect of current limiter [6].

Solid DC current limiter topology that uses IGBT and coupled reactor is also a research hotspot [7]. It also compares the effect of different schemes of current limiter topologies with same parameters, the simulation results show that the topology that uses coupled reactor or a single inductor then make the current flow alternately in the positive and negative directions can get better effect on reducing the current.

In this paper, more practical simulation and experiment are carried out. Based on the fundamental topology of FCL, the simulation considers snubber circuit and arrester, and the circuit is improved to solve the emerging new problems. The optimized circuit is used in the experiment to test its real effect.



2. Working principle of DC fault current limiter

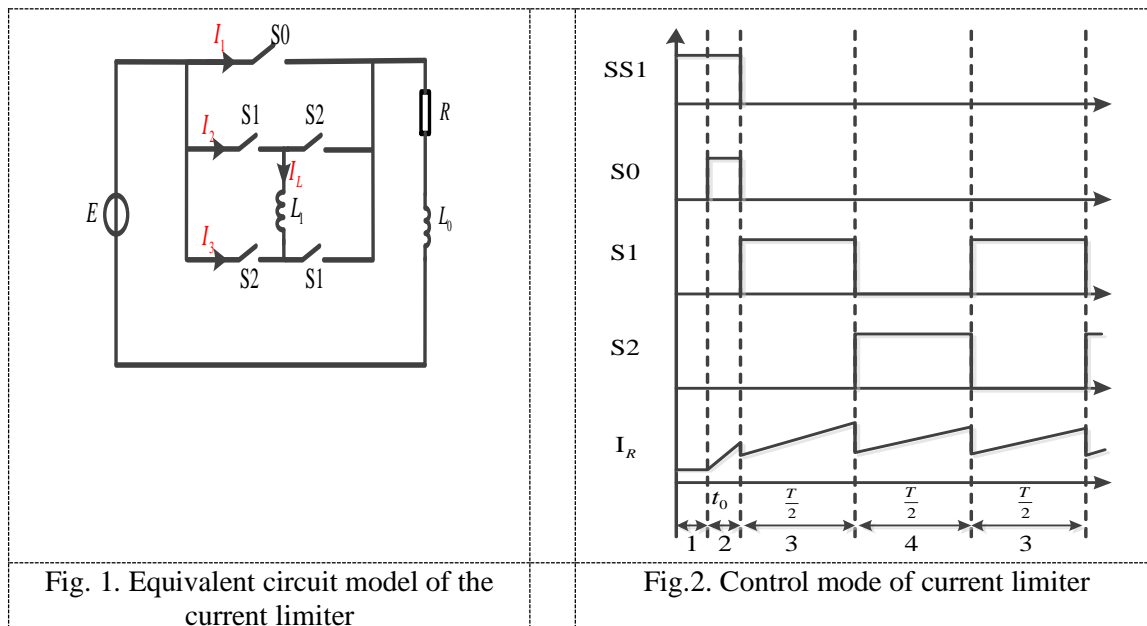


Fig.1 shows the equivalent circuit model of the current limiter topology. It consists of four IGBTs, S1, S2, S3, S4, and Mechanical switch S0. E is DC power. R, L0 are the parameter of the DC circuit, among them R is resistance, and L_0 is flat wave reactance. I_L is current limiter inductance.

The control mode is shown in Fig.2. As shown in Fig.2, the current limiter has four different working conditions.

The major characteristics of FCL in every state are:

- 1) Before the fault arises, the current flow in the mechanical switch SS1 branch.
- 2) When the fault is detected, switch S0 is turned on, but SS1 is still on, and the current transfers to the branch of switch S0.
- 3) Turn on S1, and turn off S0. S2 is off. Therefore, the current flows to the branch of inductance.
- 4) Turn on S2, and turn off S1. Therefore, the current flows to the branch of inductance from the opposite direction. Because of the Flux conservation, the current of falls when state of the switches changes.

Table 1. Current expressions of DC main circuit for different states

State0: I_R	I_0
State1: Current expression	$I_1(t) = \frac{E}{R} + (I_0 - \frac{E}{R})e^{-\frac{R}{L_0}t}$
State1: Boundary value	$I_1(t_0) = \frac{E}{R} + (I_0 - \frac{E}{R})e^{-\frac{R}{L_0}t_0}$
State2: Current expression	$I_2(t) = \frac{E}{R} + \left\{ \frac{L_0}{L_1 + L_0} \left[\frac{E}{R} + (I_0 - \frac{E}{R})e^{-\frac{R}{L_0}t_0} \right] - \frac{E}{R} \right\} e^{-\frac{R}{L_1 + L_0}t}$

State2: Boundary value	$I_2\left(\frac{T}{2}\right) = \frac{E}{R} + \left\{ \frac{L_0}{L_1 + L_0} \left[\frac{E}{R} + \left(I_0 - \frac{E}{R}\right) e^{-\frac{R}{L_0} t_0} \right] - \frac{E}{R} \right\} e^{-\frac{R}{L_1 + L_0} \frac{T}{2}}$
State3: Current expression	$I_3(t) = \frac{E}{R} + \left\{ \frac{L_0 - L_1}{L_1 + L_0} \left\{ \frac{E}{R} + \left\{ \frac{L_0}{L_1 + L_0} \left[\frac{E}{R} + \left(I_0 - \frac{E}{R}\right) e^{-\frac{R}{L_0} t_0} \right] - \frac{E}{R} \right\} e^{-\frac{R}{L_1 + L_0} \frac{T}{2}} \right\} - \frac{E}{R} \right\} e^{-\frac{R}{L_1 + L_0} t}$
State3: Boundary value	$I_3\left(\frac{T}{2}\right) = \frac{E}{R} + \left\{ \frac{L_0 - L_1}{L_1 + L_0} \left\{ \frac{E}{R} + \left\{ \frac{L_0}{L_1 + L_0} \left[\frac{E}{R} + \left(I_0 - \frac{E}{R}\right) e^{-\frac{R}{L_0} t_0} \right] - \frac{E}{R} \right\} e^{-\frac{R}{L_1 + L_0} \frac{T}{2}} \right\} - \frac{E}{R} \right\} e^{-\frac{R}{L_1 + L_0} \frac{T}{2}}$

Table 1 shows the current of DC main circuit for different states. The current of main circuit equals to the current of inductance when there is a fault.

3. Simulation

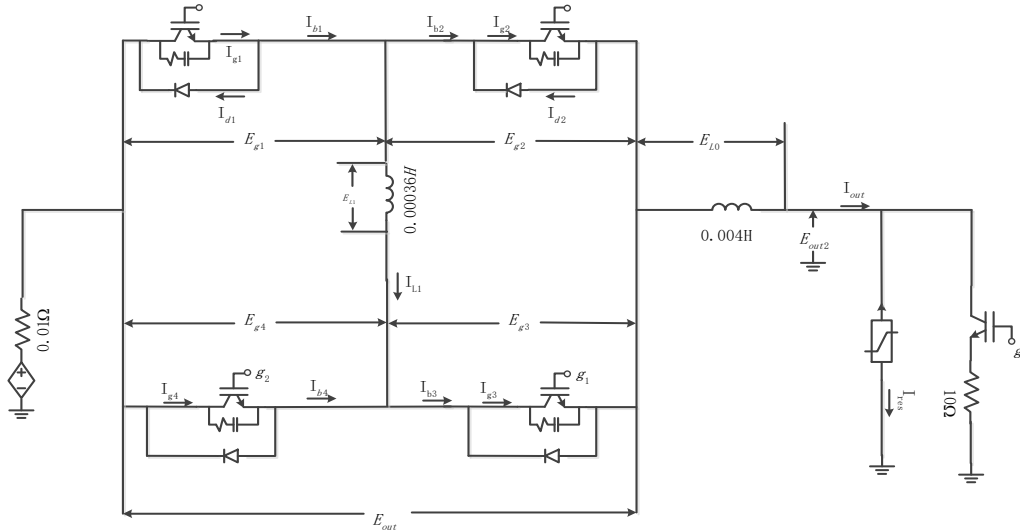


Fig.3. Primary topology of FCL in PSCAD/EMTDC

Use the topology in Fig.3 to build a model of fault current limiter in PSCAD/EMTDC. Comparing with the original topology, this circuit considers snubber capacitance and resistance. The voltage of DC power is 750V. Snubber capacitance is $0.1 \mu F$, and snubber resistance is 33800Ω. Other parameters of the circuit are in Fig.3. Switching frequency of Current limiter IGBT is 1500Hz.

The simulation results in Fig.4 show that the FCL can limit fault current to a small size through inductance conduction in different direction.

But there is a problem that come up when we detect the voltage on the IGBTs of FCL. They will suffer a really large voltage shock that is up to more than 100kV, which will cause irreversible damage to the devices.

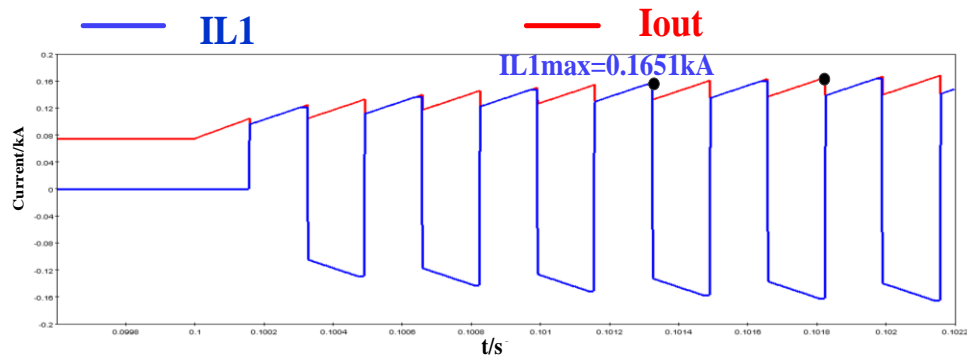


Fig.4. Fault current and current of FCL inductance

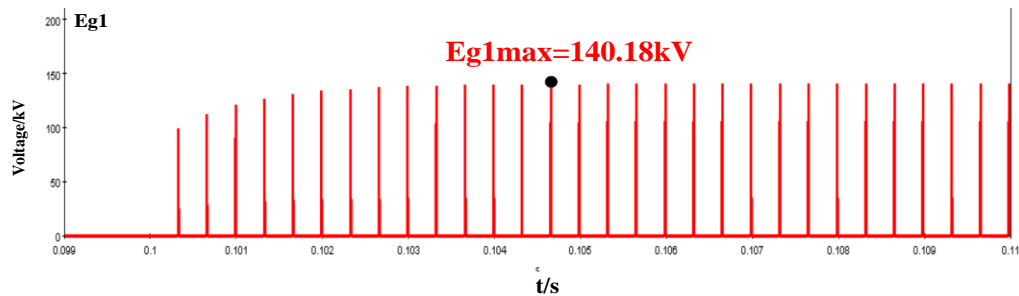


Fig.5. Voltage between two ends of one IGBT of FCL

In order to solve the voltage shock, we decide to adjust the circuit. When we replace the inductance L1 in FCL with an inductance and a branch in parallel of resistor capacitor series, as shown in Fig.6, the voltage shock disappears. The simulation results of new topology is shown in Fig.7. From Fig.7 we can see that the voltage between two ends of one IGBT of FCL is limited to 0.75kV, which is much smaller than it in the original circuit.

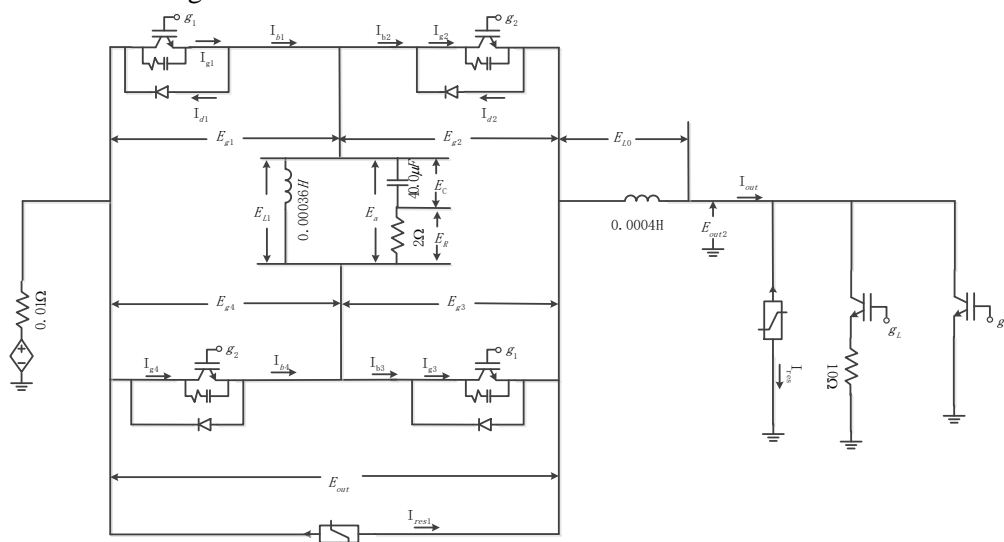


Fig.6. New topology with RC parallel circuit

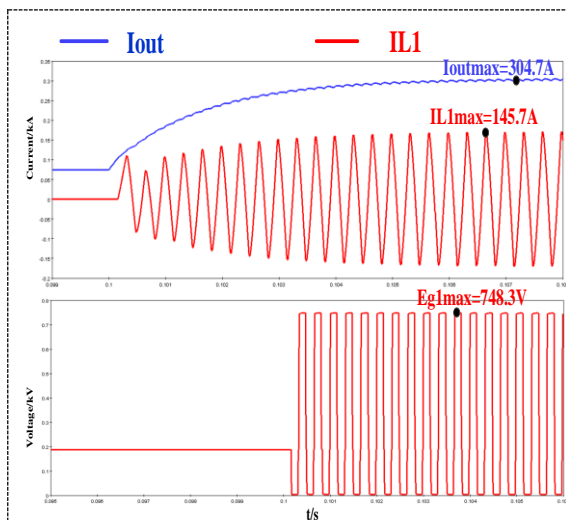


Fig.7. Output current and inductance current of new topology in simulation

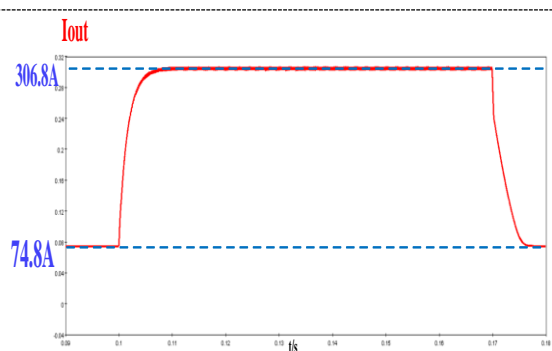


Fig.8. Output current during the whole process in simulation

After solving the problem, the output current during the whole process, which is from before the fault begins to after the fault ends, is shown in Fig.8. It indicates that the output current can still be limited to a small value, which proves that the modified topology is feasible.

We also need to pay attention to the change of input and output voltage. Fig.9 and Fig.10 show the curves of the input and output voltage respectively for when the fault begins and ends. The simulation results show that when the fault begins the input voltage will almost not decrease, but the output voltage will almost drop to zero. This is mainly because the short circuit fault is in load side, and the input voltage is closed to DC power.

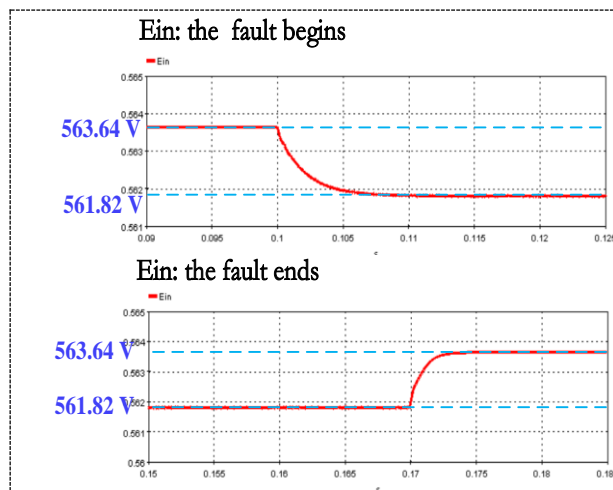


Fig.9. Input voltage for fault beginning and ending in simulation

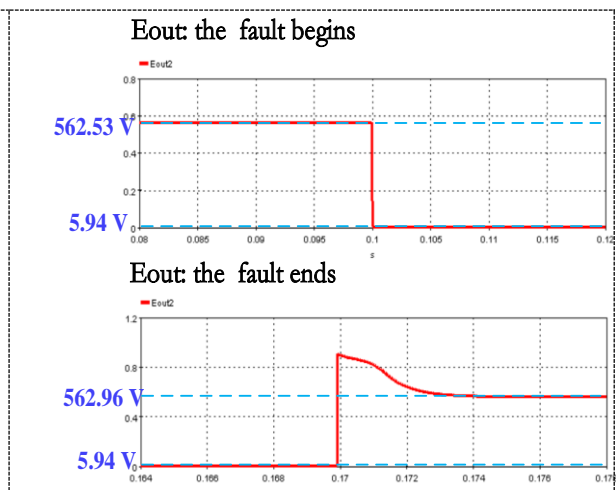


Fig.10. Output voltage for fault beginning and ending in simulation

4. Experiment

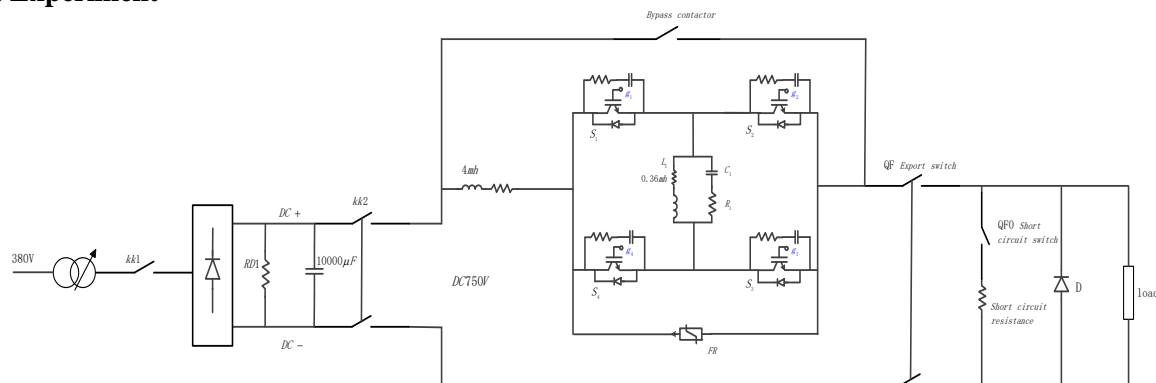


Fig.11. Schematic diagram of the FCL test platform

Fig.11 gives the schematic diagram of the FCL test platform. It consists of three parts, which are power supply, fault current limiter and load. Power supply part contains voltage regulator and rectifier, which transform 380V AC current into DC current, and it also consists of resistance RD1 and a flat wave reactance that can guarantee a stable DC output voltage. Fault current limiter is in parallel with a bypass contactor and arrester. Load part consists of the resistance and switch which can be used to simulate short circuit condition.

During the test, the normal working condition is no load. With switch state change of the AC switch kk1, DC switch kk2 in source side and export switch QF, short circuit switch QF0 in load side, the platform can be used to analyse different fault conditions such as metallic ground short circuit and nonmetallic ground short circuit, by using different short circuit resistance.

According to the schematic diagram, experimental platform is built. Devices used in this experiment and their interconnected relationship are shown in Fig.12. Additionally, the cooling system of IGBTs is water-cooling.

In order to ensure the safety of the devices used in the experiment and get more data to analyse, we set the DC voltage to a small value at the start of the test and improve it gradually. The DC voltage are respectively set to 30V, 100V, 200V, 300V, 400V, 500V, 600V during the whole test.

Test steps are as follows:

- 1) Close switch kk1 and kk2, adjust DC bus voltage to the corresponding value.
- 2) Open the four IGBTs T1, T2, T3, T4.
- 3) Close the export switch QF, and observe the output current and voltage.
- 4) Set the start value of short circuit protection.
- 5) Close short circuit switch QF0, and the short circuit resistance is 0.12 ohm.
- 6) Use oscilloscope to detect voltage and current waveform at each position.

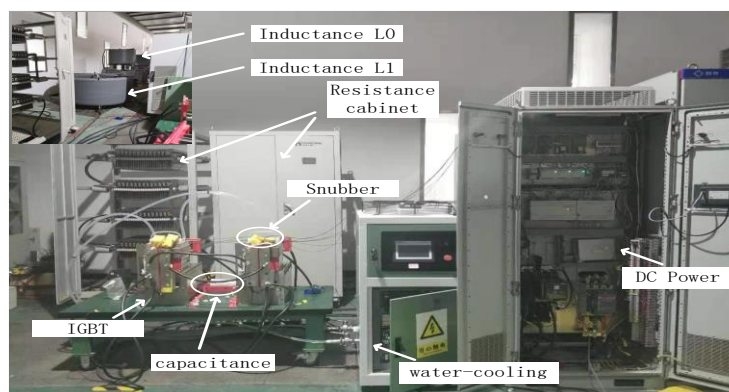


Fig.12. Experimental platform to test FCL

5. Test Results

After the experiment, curves of the variables we care about are obtained. Fig.13 shows the output current during the whole process. We can see that the curve of the output current in experiment is similar with which in simulation, except that because of the difference in power supply circuit the current in experiment without fault is smaller than in simulation. The experiment can further prove that the FCL circuit is practical in limiting the fault current.

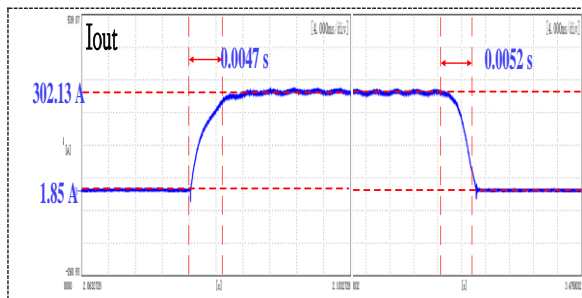


Fig.13. Curve of output current from fault beginning to fault ending in experiment

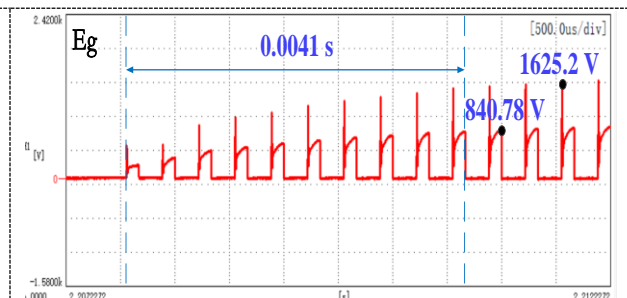


Fig.14. Curve of the voltage on IGBT in experiment

Fig.14, Fig.15 and Fig.16 respectively give the curves of voltage on IGBT, input voltage and output voltage. Fig.14 indicates that besides a voltage of about 800V, IGBT also need to bear a two times large voltage surge, which is also within its endurance capacity. In Fig.15, the input voltage has a drop of about 70V and fluctuates with an amplitude of about 40V when there is a fault. Output voltage drops to about 30V when the fault begins and recover when it ends.

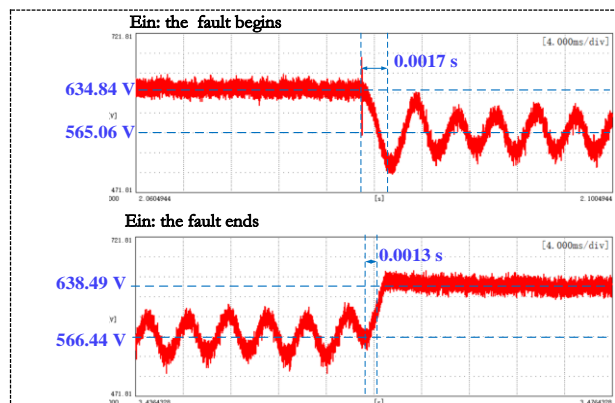


Fig.15. Input voltage for fault beginning and ending in experiment

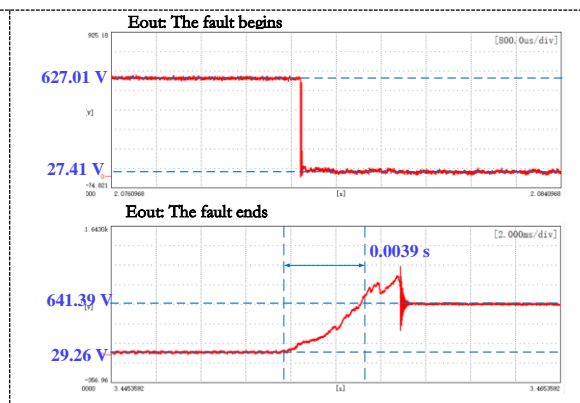


Fig.16. Output voltage for fault beginning and ending in experiment

Table 2 shows the simulation and experiment results for other DC power voltage. The results indicate that experiment corresponds with simulation.

Table 2. Simulation and experiment results for other DC power voltage

DC Power (V)	Iout (A)		IL1 (A)		Eg1 (V)	
	simulation	experiment	simulation	experiment	simulation	experiment
30	15.12	15.32	7.06	8.03	43.26	47.6(voltage spike 96.14)
100	49.68	49.73	19.14	18.94	136.98	140.25 (voltage

						spike 220.88)
200	105.36	105.35	40.47	42.43	290 (voltage spike 515)	306.3 (voltage spike 596.13)
300	158.1	157.9	57.04	58.96	431 (voltage spike 1790)	458.75 (voltage spike 884.25)
400	204.78	209.63	73.74	77.87	560 (voltage spike 1950)	597.03 (voltage spike 1151.7)
500	253.48	256.72	88.1	98.625	690 (voltage spike 1999.9)	747.3 (voltage spike 1410.9)
600	296	297.05	112.3	109.81	825 (voltage spike 2040.0)	839.84 (voltage spike 1624.5)

6. Conclusion

The test and simulation prove that when the input voltage is about 600V, the current limiter can limit the fault current within 300A. The test waveform is consistent with the simulation waveform, and the test data of other voltage levels can also correspond with the simulation, which fully verifies the working principle and control effectiveness of the current limiter.

Acknowledgement

This paper is supported by National key research and development program of China (NO.2016YFB0900205).

References

- [1] Heidary A, Radmanesh H, Rouzbehi K, et al. A DC-Reactor Based Solid-State Fault Current Limiter for HVDC Applications [J]. IEEE Transactions on Power Delivery, 2019:1-1.
- [2] Ghanbari T, Farjah E, Tashakor N. Thyristor Based Bridge-Type Fault Current Limiter for Fault Current Limiting Capability Enhancement [J]. IET Generation, Transmission & Distribution, 2016.
- [3] Lee H Y, Mansoor A, Park K H, et al. Feasible Application Study of Several Types of Superconducting Fault Current Limiters in HVDC Grids[J]. IEEE Transactions on Applied Superconductivity, 2018, 28(4):1-5.
- [4] Khan U A, Lee J G, Amir F, et al. A Novel Model of HVDC Hybrid-Type Superconducting Circuit Breaker and Its Performance Analysis for Limiting and Breaking DC Fault Currents[J]. IEEE Transactions on Applied Superconductivity, 2015, 25(6):1-9.
- [5] Noe M, Hobl A, Tixador P, et al. Conceptual Design of a 24 kV, 1 kA Resistive Superconducting Fault Current Limiter [J]. IEEE Transactions on Applied Superconductivity, 2012, 22(3):5600304-5600304.
- [6] Eryong G, Xinzhou D, Teng F. A Solid DC Current Limiter Topology [J]. Proceedings of the Csee, 2017.
- [7] Chunhua L I, Zhao C, Liu Y, et al. Analysis and Design of Topological Structure for A New HVDC Current Limiter [J]. Power System Technology, 2015.