Design of a CMOS Two-stage Fully Differential Operation Amplifier

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Abstract. Based on SMIC 0.18um CMOS process model, the operation amplifier designed in the thesis is simulated in the simulation software Cadence. In the regular environment, it has DC gain of 107dB, unity gain bandwidth of 57.48MHz, phase margin of 64.83° and output amplitude more than 3 V.

1. Introduction

Since the latter half of the 20s Century, integrated circuits have been developed rapidly and been widely applied in the field of Electronics and Information. As a result, the industry proposed more and more strict demands upon the performance of the integrated circuits [1]. The performance of the operation amplifier is tightly related to the one of the integrated circuits. Hence, it is quite essential to dedicate to produce high-performance operation amplifiers [2].

Op-amp (short for operation amplifier) is a circuit unit with very high gain. Op-amp, together with the feedback network could be designed for some functional units [3]. These units could be used to do mathematical manipulation such as 'add, subtract, multiply, divide, integrate, differentiate and logarithm' [4]. Moreover, the op-amp was once used in analogue computers to do math manipulation. That is why it was called operation amplifier. However, op-amp can also be used for precise measurement, source control, telecommunication, information processing and some other fields such as comparator, switching amplifier, active filter, and high-DC-gain amplifier [5]. Op-amp has several main parameters: voltage gain, input resistor, output resistor, common mode rejection ratio, supply voltage rejection ration, unity gain bandwidth, slew rate and so on. In the process of designing op-amp, designers should consider all parameters [6].

CMOS (short for complementary metal oxide semiconductor), a voltage-controlled amplifier, is a basic unit of CMOS digital integral circuits. With CMOS technology, people could integrate pairs of MOSFET (PMOS and NMOS) on a single silicon slice. CMOS integral circuits have many advantages, such as low power consumption, high input resistor, high noise immunity, wide voltage supply range and so on. The paper will discuss designing process and simulation result analysis.[7]

2. Designing Process

2.1. Performance Requirement

Open-loop gain over 80 dB, unit gain bandwidth over 50M Hz, load capacitor of 2 pF, phase margin over 60°, output amplitude over 2 V, power consumption less than 1.8mW.

2.2. Designing Analysis

The single-stage op-amp cannot meet the requirement of high open-loop gain and wide output amplitude range at the same time. Therefore, the paper chooses the two-stage amplifier. The first stage is fully differential cascade and the second stage is common-source amplifier. Because the folded amplifier has a higher power consumption, the paper chooses the telescopic amplifier. The integral circuits usually have limited landscape area. Therefore, the paper chooses MOS current source loads instead of large resistors. RC Miller compensation is needed between two stages to meet the demand of phase margin. DC bias voltage is 1.8 V. To keep the power consumption less than 1.8mw, the paper sets the bias current of 1st stage 120μA and the one of the 2nd stage 240μA. A CMFB is needed to enhance common mode rejection ratio. Using P-well CMOS model, all substrates of NMOS hook to a communal ground and substrates of all PMOS hook to their own sources to avoid influence of bulk effect.

2.3. Design of the First Stage Amplifier

The first stage amplifier is bilateral symmetrical. M1 works as current source load. First, confirm voltage of 4 feet of every MOS. $|v_{DS}|$ of all MOS is 0.3V. The DC bias voltage is 1.8V. The grid voltage of M1, M2, M3, M4, and M5 are 1.22V, 0.92V, 0.62V, 0.88V and 0.58V. All substrates of NMOS hook to a communal ground and substrates of all PMOS hook to their own sources to avoid influence of bulk effect. When MOS is at saturation region, $I_D = \frac{1}{2}\mu C\frac{w}{L}(v_{Gs} - v_{Th})^2$ or $:I_D = -\frac{1}{2}\mu C\frac{w}{L}(v_{Gs} - v_{Th})^2$. Hence, through changing channel length, L, and channel width, W, the current $|I_D|$ could be changed. Revise W and L to ensure each MOS at saturation region and meet the DC current demand. The condition of saturation region is $|V_{ds}| > |V_{gs}|-|V_{th}|$. Through doing DC simulation, the paper gets DC operation points of all MOS.

After fixing all MOS (all MOS working at saturation region) DC operation points, add two ideal-balun at both input side and output side. Set the common mode input voltage 0.92V and the differential mode input voltage sine-1V (amplitude)-0° to do AC simulation. Then, gain BODE diagram.

At last, change the differential mode input voltage sine-0.2mV-0° to do transient simulation. Gain output voltage diagram.

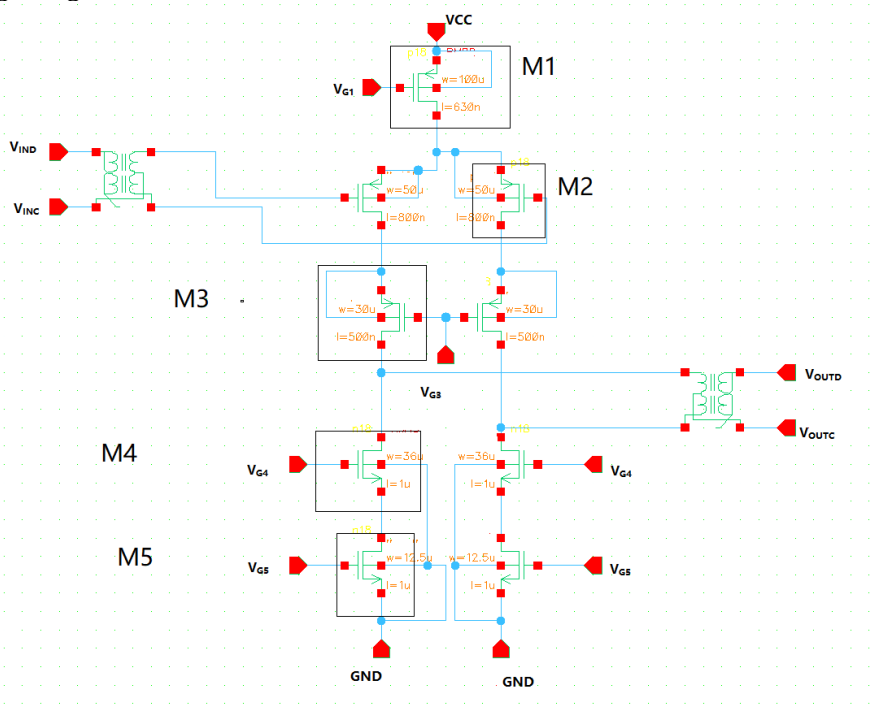

Figure.1 the first stage op-amp circuit

2.4. Design of the Second Stage Amplifier

M6 works as DC current source load. First, confirm 4 feet voltage of M6 and M7. The DC bias voltage is 1.8V. The grid voltage of M6 is 1.22V. The grid electrode of M7 links to the output of the first stage amplifier. The substrate of M7 hooks to the ground and the substrate of M6 hooks to its own source to avoid influence of bulk effect. Set the input differential mode voltage 0V. Do DC simulation to check DC operation points of M6 and M7. Change W, L of M6, M7 to ensure both MOS working at saturation region and make sure the current of M6, and M7 is 240μA.

Set the input differential mode voltage sine-1V-0° to do AC simulation. Gain output BODE diagram.

Set the input differential mode voltage sine-0.2mv-0° to do transient simulation. Gain output voltage diagram.

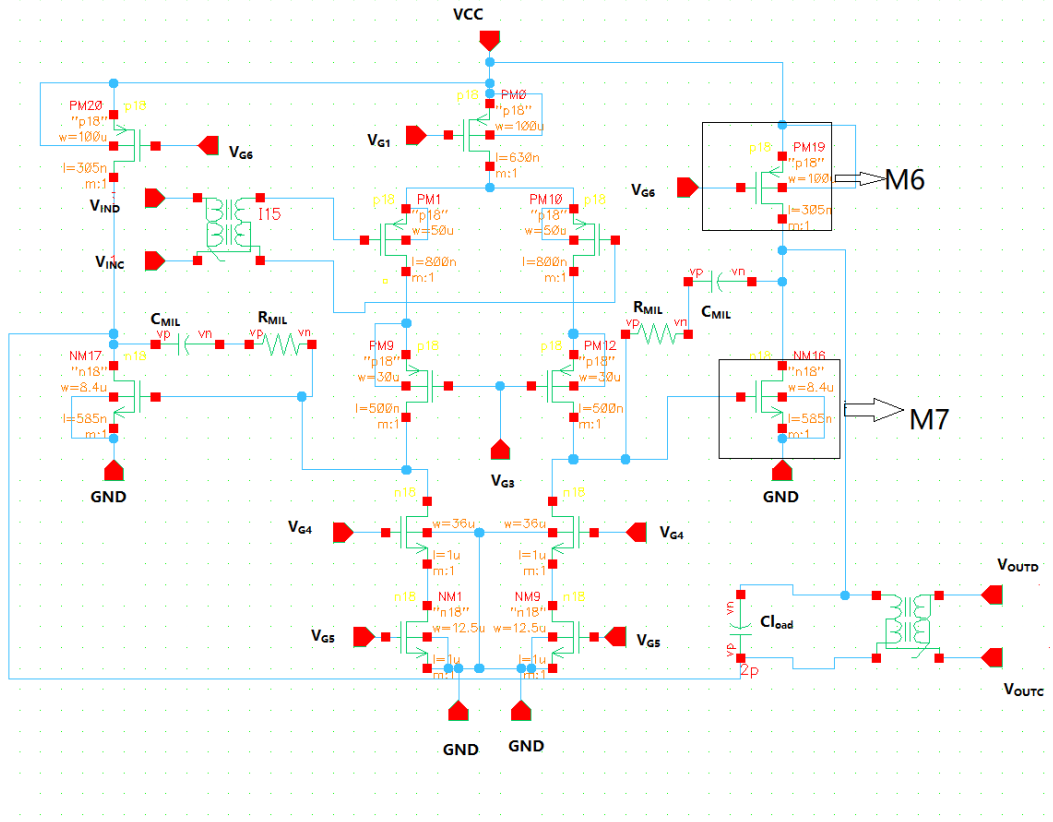

Figure 2 the second stage op-amp circuit

3. Simulation Result Analysis

3.1. Simulation of the First Stage

DC simulation:

Because the first stage is bilateral symmetrical, the paper could analyze just one side of the amplifier. The condition of saturation region is $|V_{ds}| > |V_{gs}|-|V_{th}|$. As Table.1 shown, all MOS work at saturation region and the DC bias current is 120μA.

Table 1. DC simulation of the first stage

MOS	V_{GS} (mV)	V_{DS} （mV）	V_{TH} （mV）	V_{GD} (mV)	I_s (μA)
M1	-580	-283	-437	-296	120
M2	-596	-288	-430	-307	60
M3	-607	-466	-443	-141	60
M4	577	458	498	118	60
M5	580	302	412	277	60

AC simulation and transient simulation:

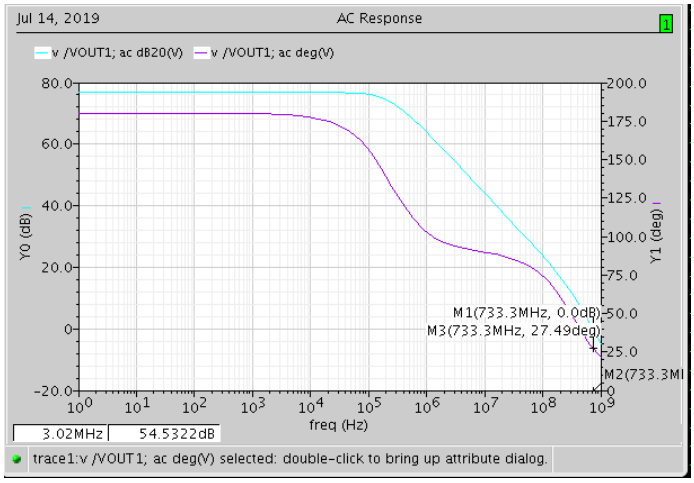

Figure 3. AC simulation result of 1st stage

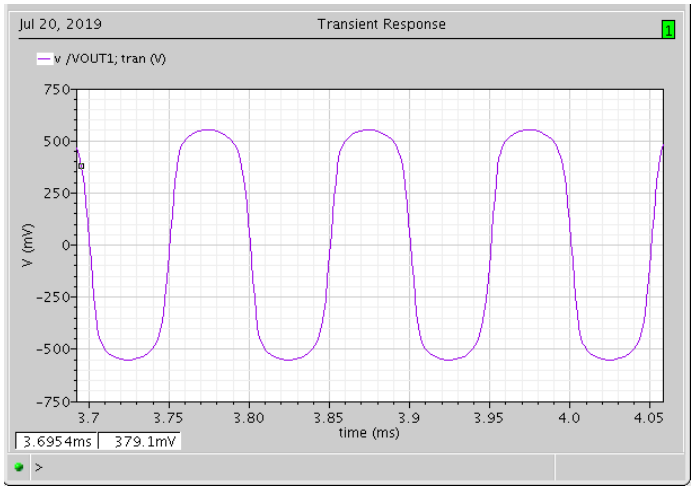

Figure 4. TRAN simulation result of 1st stage

As Figure 3 and Figure 4 shown, the gain of the first stage is 73DB and the output voltage range is about 1V, less than 2V. Moreover, the transient output is distorted. Therefore, the second stage amplifier is needed.

3.2. Simulation of the Second Stage Amplifier

DC simulation:

Table 2. DC simulation of the second stage

MOS	V_{GS} (mV)	V_{DS} （mV）	V_{TH} （mV）	V_{GD} (mV)	I_s (μA)
M6	-580	-841	-455	261	238
M7	761	958	429	-197	238

AS Table.2 shown, both MOS work at saturation region. M6 works as current source load and M7 works as common-source amplifier. Moreover, the DC bias current is 238μA.

AC simulation:

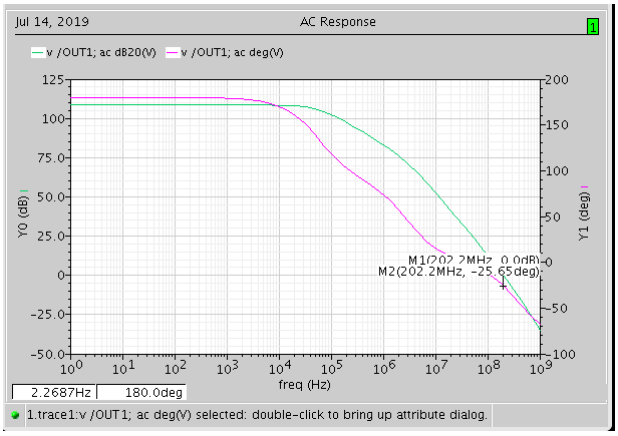

Figure 5. AC simulation without Miller-comp

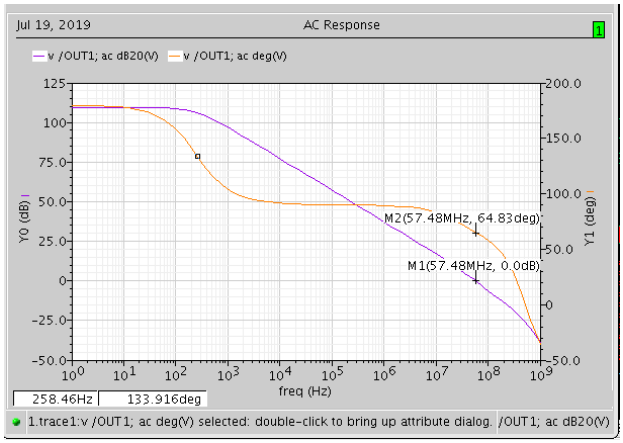

Figure 6. AC simulation with Miller-comp

As Figure 5 and Figure 6 shown, Miller-compensation is vital for the frequency domain stability of the op-amp. Op-amp without Miller-compensation has phase margin of -25.65° (unstable). After adding RC Miller-compensation, the op-amp has phase margin of 64.83°,unit gain bandwidth of 57.48 MHz and gain of 107 dB.

Transient simulation with Miller-compensation:

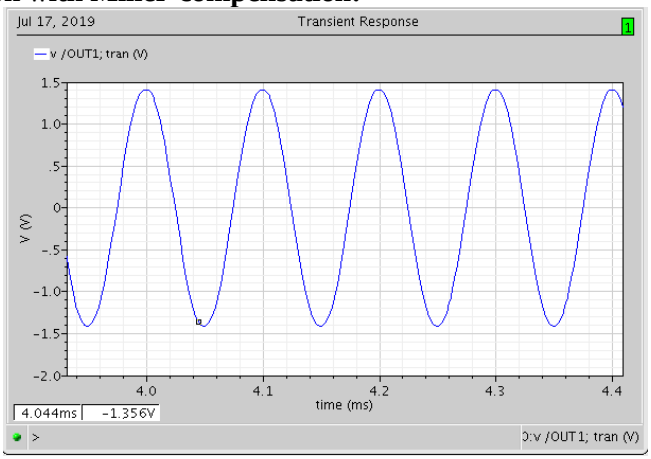

Figure 7. Transient simulation result of 2nd stage

Output voltage amplitude is about 3V (bigger than 2V) and the output voltage is not distorted.

4. Conclusion

The high-performance two-stage operation amplifier have such advantages: a high gain, a wide output voltage amplitude, and a high common mode rejection ratio. The process of the design of CMOS op-amp: First, adjust W and L to change the DC operation points, ensure all MOS working at saturation region, and meet the demand of the DC bias current. Then set proper input voltage (common mode input and differential mode output) to do AC simulation and transient simulation to check the gain and the phase margin of the op-amp.

Moreover, Miller-compensation is essential between two stages. Adjust the capacitor and the resistor to meet the demand of the phase margin and the unit gain bandwidth.

At last, common mode feedback circuit is vital because once the amplifier is at current mismatch (it is common in actual environment), some MOS will work at linear region, which will cause the op-amp malfunctioning. However, in simulation environment, the change of process corner or the change of temperature doesn't exist. Because all MOS work at saturation region without common mode feedback circuit, this paper omits design process of common mode feedback circuit and the simulation result of op-amp with common mode feedback circuit.

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