A Fast-transient NMOS Capacitor-less LDO with Spike Voltage Sampling Amplifier and Transient Enhancement

Yun Li[1], Shengming Huang[1*] and Quanzhen Duan[1*]

Tianjin University of Technology, Tianjin, 300384, China

[*]Corresponding author's e-mail: smhuang0101@163.com and qzduan@tjut.edu.cn

Abstract. A fully-integrated NMOS low dropout voltage (LDO) with spike voltage sampling amplifier is proposed in this paper to provide a stable power supply for many portable devices and artificial intelligence systems. The proposed Spike Voltage Sampling Amplifier circuit is composed of an error amplifier based on dynamic bias of output voltage and a capacitive coupling network, which is embedded in the circuit to detect fluctuations in the output voltage to increase the slew rate of the power transistor so that it turns on and off quickly. The LDO is implemented in 0.18 um CMOS process, which consumes 84uA quiescent current. It regulates output at 1.6V, with dropout voltage of 200 mV. For load current transients from light load 100 uA to heavy load 20 mA at the 100 ns edge-time, the undershoot of the LDO is 82 mV and the recovery time is 167 ns. Similarly, the load current transient from heavy load to light load produces an overshoot of 67 mV and recovery time is 156 ns.

1. Introduction

In recent years, with the rapid development of SOC, the integration of chips is getting higher and higher, and the same is true for power management. As an important part of power management, LDO provides a stable power rail for the system. The reduction or even disappearance of the output capacitor makes the area of the without off-chip capacitor LDO drastically reduced, which meet the needs of the development of SOC, and easily integrated, however, the output transient response deteriorate compared to the conventional LDO. When the load changes rapidly, its output becomes unstable, which may cause system instability and logic misjudgement, so transient optimization of the LDO without off-chip capacitance becomes critical.

This paper proposes a fast response capacitor-less LDO with transient processing optimization circuit. A simplified block diagram of the designed topology is shown in Figure 1. The spike voltage sampling amplifier (SVSA) circuit is proposed, which amplifies and transmits the ripple of the output voltage to the push-pull circuit to enhance the gate slew rate of the power transistor, so that the LDO has a settling time of less than 200 ns and the spike voltage is less than 100 mV at 100 ns edge-time. In addition, the power device chooses to replace the PMOS with NMOS. The NMOS has a smaller gate capacitance. Therefore, the dominant pole is set at the gate of the NMOS to obtain a larger unity gain bandwidth (UGB), and the loop stability is further guaranteed. The circuit structure and implementation of the transistor circuit will be described in Section 2. Section 3 describes the stability analysis of the LDO. The simulation results are shown in the section 4, and the section 5 provides the conclusions of this paper.

Content from this work may be used under the terms of the Creative Commons Attribution 3.0 licence. Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.
Published under licence by IOP Publishing Ltd

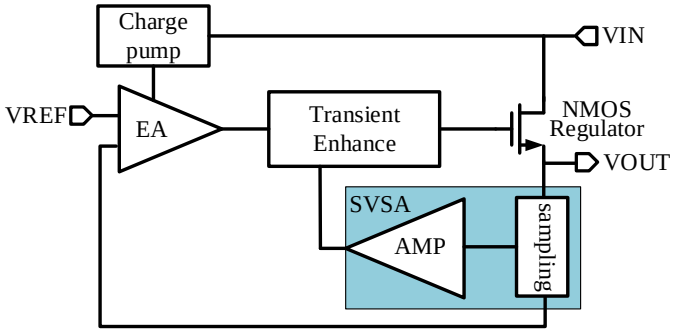

Figure 1. Simplified block diagram of the designed topology

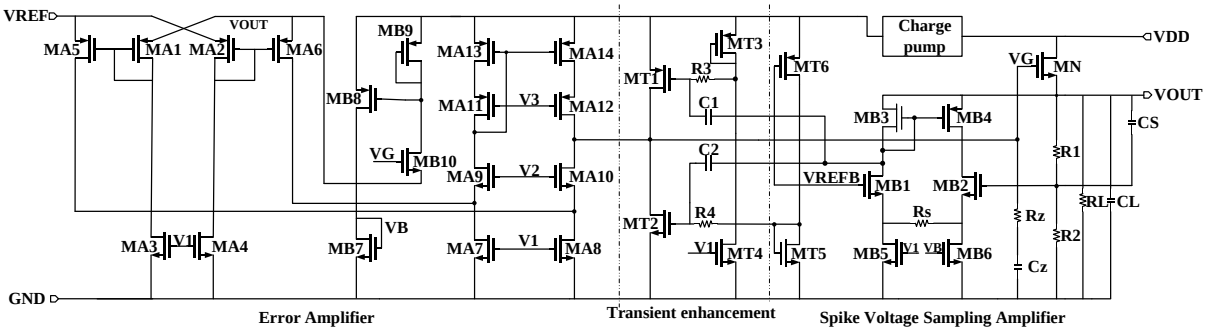

Figure 2. Schematic of the proposed LDO regulator circuit

2. Proposed LDO Architecture

The LDO proposed in this paper is shown in Figure 2. It consists of an NMOS regulator, an error amplifier (EA), a spike voltage sampling amplifier and a charge pump. The error amplifier in this paper is a common-gate folding amplifier. The input stage is a common-gate differential pair, and the folded structure is used as the output stage. Because of the common-gate input has a low input impedance, the low input impedance of the error amplifier can effectively reduce the output impedance of the LDO and improve the loop stability of the LDO. The folded output stage has a high output impedance, which is beneficial to set the output of the error amplifier as the main pole of the loop. The SVSA circuit is designed to detect output voltage fluctuations generated by load changes, and the detected ripple is coupled to the transient enhanced network through a high-pass capacitor network through an amplifier. The charge pump generates a voltage double the VDD to power the error amplifier. The purpose is to increase the output stage voltage to drive the NMOS regulator to ensure a 200 mV dropout.

2.1. Error Amplifier

The error amplifier adopts a folded common-gate amplifier. The transistors M_{A1}, M_{A2}, M_{A5}, and M_{A6} are two inputs across the stage. The M_{A5} and diode-connected M_{A1} are one input of the EA. Similarly, another consists of M_{A6} and diode-connected M_{A2}.The two transconductance stages are cross-coupled to form a differential input stage with low input impedance. The M_{A5} and M_{A6} operate in a common gate configuration, so that the input differential signal swing is further amplified, resulting in a significant increase in the overall transconductance of the EA. This amplifier has a larger unity gain bandwidth and a faster step response than the conventional cascade amplifier. The folded output provides a large output impedance that can be expressed as follow:

$$R_{oEA} = \frac{g_{mA12}g_{mA10}(r_{oA5}+r_{oA8})r_{oA10}r_{oA12}r_{oA14}}{g_{mA10}(r_{oA5}+r_{oA8})+g_{mA12}r_{oA5}r_{oA8}r_{oA12}r_{oA14}} \quad (1)$$

Where g_{mA10}, g_{mA12}, are transconductance of M_{A10}, M_{A12}; and r_{oA5}, r_{oA8}, r_{oA10}, r_{oA12}, r_{oA14}, are output resistance of M_{A5}, M_{A8}, M_{A10}, M_{A12}, M_{A14}.

2.2. Spike Voltage Sampling Amplifier

In the input terminal of the operational amplifier in the spike voltage sampling unit, resistance voltage division and capacitive coupling are used to jointly sample and detect the transient change of the output voltage. The sampled value of the resistor divider is $R_2/(R_1+R_2)\Delta V_{out}$ and the detection value on the capacitor is ΔV_{out}. The transient sampling voltage V_T obtained by the sampling circuit can be found in

$$\Delta V_T = \left(1+\frac{R_2}{R_1+R_2}\right)\Delta V_{out} A_{TR} \tag{2}$$

$$A_{TR} = \frac{g_{mB1} r_{oB1} r_{oB3}}{2R_s \| r_{o5} + [1+(g_{mB1}+g_{mbB1})(2R_S \| r_{o5})] r_{o1}} \tag{3}$$

A_{TR} is the gain of the sampling circuit operation amp. The variation is coupled to the gate of M_{T1} and M_{T2} through capacitors C_1 and C_2. When load current (I_L) suddenly increases, V_{OUT} will also drop rapidly at the same time. At this time, the amount of change is sensed by the sampling circuit and coupled to the gates of M_{T1} and M_{T2} through C_1 and C_2. Due to the influence of the coupling capacitance C_2, the voltage of gate source (V_{GS}) of M_{T2} is reduced, so the current of M_{T2} is decreased. At the same time, C_1 transmit the change to the gate of M_{T1}, which causes a sharp and instant increase for V_{GS} of M_{T1}, M_{T1} current I_{DT1} increases. Such a push-pull output stage consisting of M_{T1} and M_{T2} charges the gate capacitance of the NMOS regulator, so that the V_{GS} of the NMOS regulator increases to regulate the output. M_{T1} and M_{T2} are biased in the sub-threshold region due to the action of M_{T3} and M_{T5}, and the push-pull-level regulation circuit is formed only when the output voltage fluctuates. Similarly, when I_L suddenly decreases, the output voltage V_{OUT} increases. The amount of change in V_{OUT} is simultaneously coupled to M_{T1} and M_{T2} by C_1 and C_2, increases the V_{GS} of M_{T2} and reduce the V_{GS} of M_{T1}. Therefore, a push-pull output stage is temporarily formed, M_{T1} turns off and the drain current of M_{T2} is increased, and the gate capacitance of the NMOS regulator is discharged, so that the V_{GS} of the NMOS regulator is reduced to limit the load current, so that circuit enters the steady state eventually.

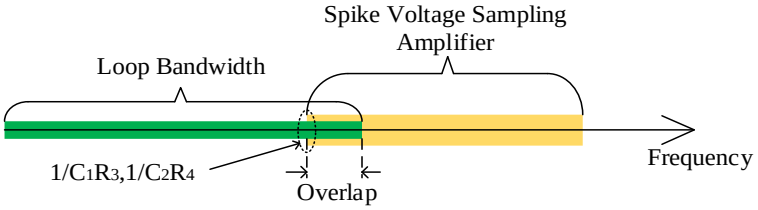

Figure 3. Loop bandwidth and frequency of proposed Spike Voltage Sampling Amplifier

In SVSA, C_1, C_2, R_3, and R_4 form a high-pass filter. C_1, C_2 as high-pass components, can provide two fast paths compared to the change voltage through the EA to the NMOS regulator. Then the choice of C_1, C_2, R_3, and R_4, needs to refer to the loop bandwidth of the LDO. The relationship between these frequencies is shown in Figure 3. The loop bandwidth of the LDO is finite and low-pass, however the frequency of the sampling circuit is $1/C_1R_3$, and $1/C_2R_4$ is high-pass. Set this frequency lower than UGB so that there is a certain overlap between these two, which can widen the bandwidth of the LDO. This makes the detection circuit and the LDO itself respond quickly to changes in the output voltage. The unity gain bandwidth of the LDO proposed in this paper is 14.5 MHz, so choose C_1=C_2=1 p, R_3=R_4=16 K.

2.3. NMOS Regulator

The NMOS regulator has a lower gate capacitance than the PMOS regulator, which pushes the dominant pole ω_{p1} to a higher frequency. Wider UGB and higher slew rate will be obtained to enhance the load transient response of the LDO. The NMOS regulator forms a source follower with a lower output impedance, further ensuring loop stability. The equivalent output impedance of LDO can be expressed as follow:

$$R_{oN} = \frac{1}{g_{mNM}+g_{mbNM}+\frac{1}{r_{oNM}}} \parallel R_{IEA} \parallel R_L \tag{4}$$

$$R_{IEA} = \frac{1}{g_{m1}+g_{m5}} \tag{5}$$

Where R_{IEA} is the input resistence of Error Amplifier.

3. Stablity Analysis

There are two low frequency poles on the loop of the LDO, one of the pole located in the gate of the NMOS regulator, and the other located in the output of the LDO. The transfer function of LDO can be expressed as [2]

$$\mathrm{H}(s) = \frac{G_{mEA}R_{oEA}\frac{G_{mN}R_{oN}}{1+(G_{mN}+G_{mbN})R_{oN}}\left(1+\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{6}$$

Where

$$\omega_Z = \frac{1}{R_Z C_Z} \tag{7}$$

$$\omega_{p1} = \frac{1}{R_{oEA}(C_{NG}+C_Z)} \tag{8}$$

$$\omega_{p2} = \frac{1}{R_{oN}(C_L+C_{par})} \tag{9}$$

C_{NG} is the gate capacitance of NMOS regulator. And C_{par} is the parasitic capacitance at the output node, only a few picofarad. For the LDO proposed in this paper, ω_{p1} is the low frequency dominant pole and ω_{p2} is the secondary pole, but its frequency is related to the load current. R_{oN} is proportional to R_L, so when the load current increases, the pole will be pushed to the high frequency. The system will probably be unstable in the case of light load. Therefore, a series R-C compensation is embedded in the gate of the NMOS to increase the phase margin under light load conditions, so that the system remains stable. The R-C value used in this design is R_Z=5 K, C_Z =5 p.

4. Simulation Results

Figure 4 shows the loop gain and phase diagram of the circuit under different load conditions. The loop phase margin is 52 degrees at 0.1 mA light load and 71.32 degrees at 20 mA heavy load. There is sufficient phase margin under both light and heavy load conditions to ensure loop stability and sufficient gain ensures linear regulation of the LDO.

The transient response of LDO is shown in Figure 5(a). Under the condition of V_{IN}=1.8 V & C_L=10 pF, the load jumps from 0.1 mA to 20 mA at the 100 ns edge-time, and the output voltage will generate a voltage of 81 mV undershoot, which will return to stability after 169ns. Similarly, when the load drops from 20 mA to 0.1 mA at the 100 ns edge-time, the output voltage has an overshoot voltage of 67 mV and a recovery time of 156 ns.

Figure 5(b) is the linear transient response result of the proposed LDO. In the case of I_L=20 mA & C_L=10 p, V_{IN} is switched between 1.8 V and 2.2 V during the rise and fall times of 100 ns, V_{OUT} appears to be overshoot and undershoot are 12 mV and 13 mV, respectively.

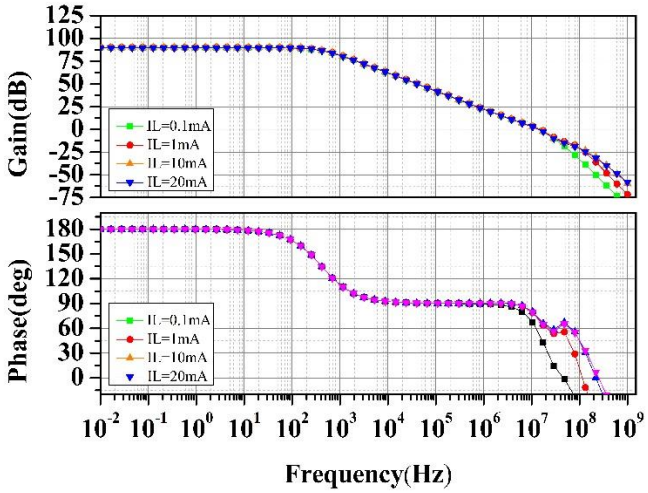

Figure 4. Loop responses of the proposed regulator at different load current

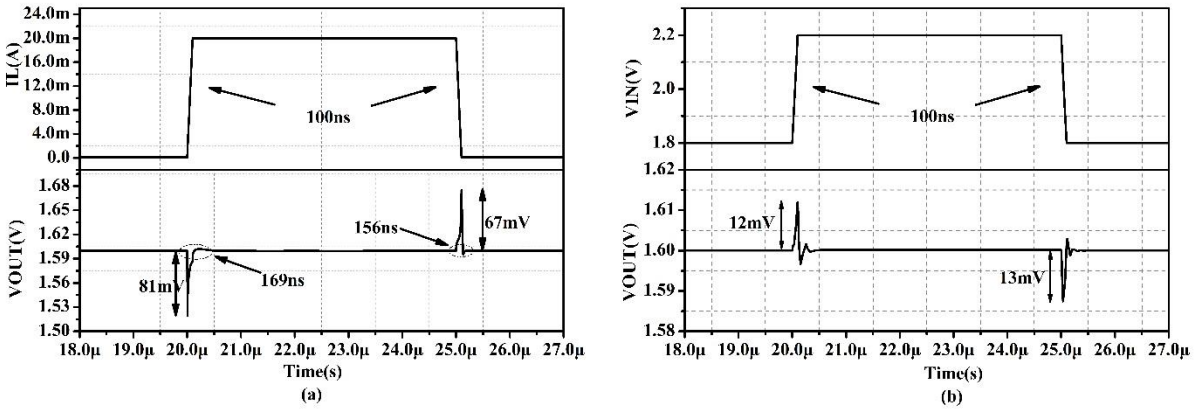

Figure 5. (a) Simulated load transient response at V_{IN} = 1.8 V & V_{OUT} = 1.6 V (b) Simulated line transient response when V_{IN} changes between 1.8 V & 2.2 V

Table 1 Performance comparison

Parameter	[7]	[8]	[4]	[9]	This work
Year	2013	2018	2018	2019	2019
Technology(um)	0.11	0.5	0.25	0.18	0.18
Regulation FET	PMOS	PMOS	NMOS	PMOS	NMOS
V_{IN}(V)	2.2	2.7	1.5-3.3	1.2	1.8-2.2
V_{OUT}(V)	2.0	2.5	1.0-3.0	1.0	1.6
Dropout(mV)	200	200	240	200	200
I_{outmax}(mA)	200	100	150	100	20
I_Q(uA)	41.5	107	1.24-100	0.4-245	84
C_L(pF)	40	N/A	1000-47000	100	0-10
ΔI_L(mA)	99.9	49.95	150	100	19.9
Undershoot(mV)	385	296	135	117	81
Overshoot(mV)	200	200	65	35	67
T_{edge} (ns)	500	10	10	300	100
T_{settle} (ns)	650	150	900	1560	160
PSR (dB) @1 kHz	N/A	-60	-43	-45	-46

5. Conclusion

In this paper, a fully integrated low dropout regulator with a spike voltage sampling circuit is proposed to achieve fast response and reduced spikes by real-time sampling feedback of the output voltage. The simulation results shows that the design possess an excellent fast response capability. The maximum settling time is only 167ns and the maximum spike voltage is 81mv, so the LDO can provide a stable output. The load regulation and line regulation are 4.08 uV/mA and 0.625 mV/V, respectively. Therefore the LDO is suitable for most SOC.

Acknowledgments

This research was supported in part by National Natural Science Foundation of China under Grant (61904124) and was supported in part by the Tianjin Municipal Science and Technology Commission under Grant(18JCQNJC70700).

References

[1] P. Y. Or and K. N. Leung. (2010) An Output-Capacitorless Low-Dropout Regulator With Direct Voltage Spike Detection. IEEE Journal of Solid-State Circuits, 45(2): 458-466.
[2] P. Y. Or and K. N. Leung. (2010) A Fast-Transient Low-Dropout Regulator With Load-Tracking Impedance Adjustment and Loop-Gain Boosting Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 57(10): 757-761.
[3] R. G. Carvajal et al. (2005) The flipped voltage follower: a useful cell for low voltage low-power circuit design. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52(7): 1276-1291.
[4] N. Liu, B. Johnson, V. Nadig and D. Chen. (2018) A Transient-Enhanced Fully-Integrated LDO Regulator for SoC Application In: 2018 IEEE International Symposium on Circuits and Systems (ISCAS). Florence pp. 1-5.
[5] P. Y. Or and K. N. Leung. (2010) A Fast-Transient Low-Dropout Regulator With Load-Tracking Impedance Adjustment and Loop-Gain Boosting Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 57(10): 757-761.
[6] J. Tang, J. Lee and J. Roh. (2019) Low-Power Fast-Transient Capacitor-Less LDO Regulator With High Slew-Rate Class-AB Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 66(3): 462-466.
[7] D. Mandal, C. Desai, B. Bakkaloglu and S. Kiaei. (2019) Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time IEEE Transactions on Circuits and Systems II: Express Briefs, 66(2): 167-171.
[8] Y. Kim and S. Lee. (2013) A Capacitorless LDO Regulator With Fast Feedback Technique and Low-Quiescent Current Error Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 60(6): 326-330.
[9] X. Ming *et al*. (2018) A Capacitor-less LDO With Fast-transient Error Amplifier and Push-pull Differentiator. In: *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, pp. 1-5.
[10] Y. Jiang, D. Wang and P. K. Chan. (2019) A Quiescent 407-nA Output-Capacitorless Low-Dropout Regulator With 100-mA Load Current Range. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 27(5): 1093-1104.
[11] P. Suriyavejwongs, B. Supmonchai and K. Opasjumruskit. (2015) Slew-rate enhanced capacitor-less low drop-out regulator with on-the-fly adjustable output voltage. In: 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, pp. 186-189.
[12] X. Tong and K. Wei. (2017) A Fully Integrated Fast-Response LDO Voltage Regulator with Adaptive Transient Current Distribution. In: 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Bochum, pp. 651-654.

[13] A. Maity and A. Patra. Tradeoffs Aware Design Procedure for an Adaptively Biased Capacitorless Low Dropout Regulator Using Nested Miller Compensation. IEEE Transactions on Power Electronics, 31(1): 369-380.