

# Design of a Broadband LNA with Multi-feedback Using 70nm GaAs MHEMT Process

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**Abstract.** This paper presents a broadband LNA using 70nm GaAs MHEMT process operating from 1.5GHz to 20GHz. The multi-feedback technique and input/output impedance match are applied to compensate the transistor gain roll-off with frequency and optimize the stability and reflection coefficients. The effect of the multi-feedback technique for stability, noise figure, gain flatness, linearity, and S-parameter performance are analyzed and discussed. Among the whole bandwidth, this LNA features gain of average 29.5dB increasing with frequency and noise figure of average 1.15dB. This LNA also achieves good reflection and isolation performance. The consuming of this LNA is blow 150mW and the chip area is less than 1.4mm\*0.8mm. The figure-of-merit (FOM) is about 362.6 (GHz/mW). This LNA could be found its application in high data rate transmission, software defined radio, 5G communication, test instrumentation, wideband radar and other wideband systems.

## 1. Introduction

The low noise amplifier (LNA) is important for receiver front-ends [1-3]. The demands of the wideband LNA are increasing because of the growing requirements of test instrumentation, high data rate transmission, millimeter wave transceiver, 5G communication and other broadband systems [4-6]. As the first stage of the receiver system, the noise figure (NF) of the LNA needs to be low enough and the gain of the LNA needs to be high enough [7]. Also, in the broadband system, the LNA needs unconditional stability, good input/output (I/O) matching, good gain flatness, acceptable linearity across wideband, small chip area and low power consumption [6,8].

Monolithic microwave integrated circuit (MMIC) technologies can easily implement high performance microwave circuits for their superior noise or power characteristics at microwave frequencies [9-10]. Several researches of LNAs with low noise and high gain performance have been carried out on different process: InP HBT (Heterojunction Bipolar Transistor) and HEMT (High Electron Mobility Transistors), GaAs PHEMT (Pseudomorphic HEMT) and MHEMT (Metamorphic HEMT), SiGe HBT, or GaN HEMT technology [8-11].

Several researches for improving performances of broadband MMIC LNA have been reported. Some reported feedback methods to improving wideband performance of LNA by eliminating the influence of Cgs or Cds of the transistors includes source degeneration [4,12], direct feedback from drain to gate formed by resistor, inductor and capacitor (RLC) with gain compensation [5-7], transformer feedback [1], and dual-feedbacks [3]. The paper [13] reported the method of incorporating



Cgs into the input match network to obtain broadband performance. Distributed amplifier (DA) is designed to get the broadband performance in the paper [14]. In the microwave DA, the Cgs and Cds are absorbed into the two sets of high impedance transmission lines, which connect the gates and drains of several transistors, to make of series of LC sections for achieving the broadband performance [14]. However, the DA is not preferable in some applications owing to its large chip size cost and high NF. Another structure to design broadband amplifier is that using multi-stages to expand bandwidth and improve the gain [1,15]. But many papers did not design the comprehensive performance of the LNA. For example, some paper have high gain ripple [15-16] or bad I/O matching [7,12] in band. Even some LNAs have relatively high NF or large chip size [14,17]. The poor I/O matching, narrow bandwidth biasing and poor gain flatness of the transistors limit many LNA's application in broadband systems [5,18]. Although the technologies are promising, it is always a challenge to design high quality wideband MMIC LNA.

In this paper, a broadband MMIC LNA has been designed with 70nm GaAs MHEMT process of OMMIC Foundry. As shown in Fig.1, this proposed LNA is designed as cascade structure with multi-feedback networks to enhance the stability and wideband I/O impedance matching. For higher integrating level, the small on-chip inductors are applied to I/O ports for compensating impedance matching. This LNA shows an NF of 1dB~1.35dB, an output 1dB compression point (P1dB) of 7dBm and a positive increasing gain of 27dB~32dB operating from 1.5GHz to 20GHz. The bond wires are also taken into account in the design and the S11 and S22 of the LNA are both below -10dB. The figure-of-merit (FOM) is about 362.6 GHz/mW, with the chip size of 1.4mm\*0.8mm. The rest of the paper is organized as follows. The MMIC LNA design flow, GaAs MHEMT technology and transistor characteristic analysis are presented in section 2. In section 3 and section 4, the LNA circuit model and characteristic analysis are described. The simulation results and discussions are included in section 5. Finally, conclusions are described in section 6.

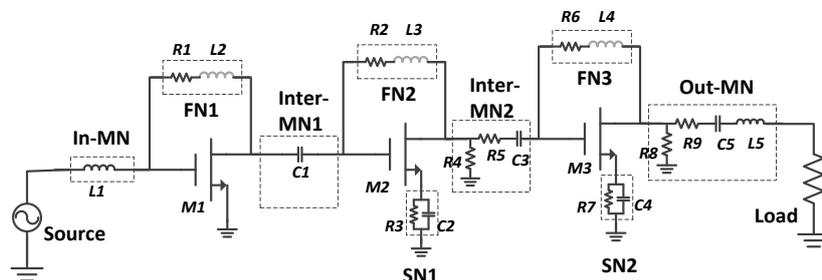


Fig.1 The schematic structure of the proposed LNA

## 2. Technology and Transistor

Generally, the performance of an LNA depends on the transistor type, transistor size, circuit structure, match network, design method, DC bias, manufacturing technology, packaging and so on [19]. The entire design and analysis procedures of the LNA MMIC are as follows. Firstly, select a proper technology, gate width (W), finger number (N) and DC bias point, depending on the characteristic of the transistors. Secondly, choose the proper amplifier architecture, DC bias networks and the matching networks. Then, design, analyze, simulate, and optimize the circuit structure and parameters carefully.

In this paper, we choose the D007IH GaAs process, whose substrate has a thickness of 100 $\mu$ m and a relative permittivity  $\epsilon_r$  of 12.9. The D007IH process is based on a high Indium content epitaxial active layer, grown on a metamorphic buffer layer with 70nm gate length [20]. This process shows extremely low noise and very high cut off frequency ( $f_T=300$ GHz) due to the multi-gates short-channel and 2DEG channel [19-20].

Selection the bias points of MHEMT depends on the transconductance  $g_m$ , maximum available gain (MAG), minimum noise figure (NFmin), NF, and stability [19]. We choose proper operating bias point of MHEMT ( $V_{ds}$  operating range at about 1V and  $V_{gs}$  operating range from -0.2V to 0V) to make a compromise between NF and MAG.

As shown in Fig.2, we do the simulation (NFmin, MAG, Zin, Zout) by changing W and N of the transistor to choose the proper transistor size. We can see that the NFmin almost does not change obviously by altering the W and N and the gm increases by increasing the W and N. The S11 and Sopt for the transistor are also plotted in Fig.2(3) over a frequency range of 0.5GHz~30GHz. Matching the source impedance with S11 and Sopt in broadband will simultaneously generate a low noise and good input match. Hence W and N are chosen in such a manner that the S11\* and Sopt for minimum noise are as close as possible [3,19]. In this paper, we prefer to choose a larger transistor size (larger W\*N) to make a compromise between lower NFmin (or NF), higher MAG and good I/O match.

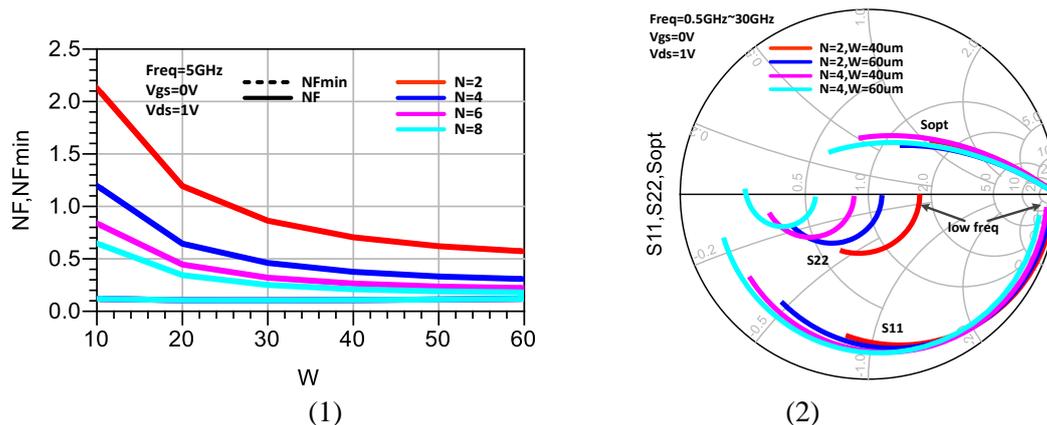


Fig.2 Simulation performance of MHEMT by changing W and N: (1)NFmin, NF vs W, N; (2)S11, S22, Sopt vs frequency

### 3. Circuit Design

As shown in Fig.1, there are three gate-drain negative feedback networks (FN), two source self-bias networks (SN) and some matching networks (MN). The three negative FNs consist of a resistor R and a parasitical transmission line (with parasitic inductor) from the drain to the gate. These FNs play an important role in I/O matching and stability with undesired noise to the LNA. The two source SNs, which make up of a source degeneration resistor R connecting parallel to a capacitor C, play an important role in gain flatten and automatic transient protection to the LNA when powered up. To extend bandwidth and achieve optimized for input matching and NFmin, an input MN composed of a series inductor L is added before the input stage. Also, an output MN composed of RLC is added to the output to achieve a good output matching response. In addition, the inter-grade MN, optimized for direct impedance transformation, will play a role to the inter-grade stability between the transistors. The FNs and MNs are realized using microstrip lines or small lumped elements all on chip. By introducing FNs, SNs and MNs, not only the I/O matching and gain can be largely extended, but also a flatter noise frequency response closer to the NFmin within wideband have been achieved. Depending on the analysis above, we choose 4 fingers and 40um gate width for the M1, and 6 fingers and 50um gate width for M2 and M3.

The DC BN is used to protect the RF signal from the circuit's DC supplied [6]. In the broadband LNA design, it is a big challenge to design broadband bias circuit to avoid RF leakage almost from dc to high frequency [19]. In this paper, in order to get better performance, the transistors sources and drains are biased from on-chip high performance spirals inductors. The SN, consisting of parallel resistor and capacitor, connects at the source to get stable DC biasing point. In this proposed LNA, for the better performance in terms of both gain and NF, we choose Vgs, Vds of the first stage as 0V and 1V. Because of the R locals at the source of the M2 and M3, the Vd is increased to 1.2V to making the Vds as 1V. Setting the Vg2 and Vg3 as 0V, the Vgs of M2 and M3 will be biased at -0.2V.

## 4. Circuit Design

### 4.1. Noise Performance

Generally, when the circuit consist the feedback networks, the performances of the LNA are strongly influenced by the feedback networks [5-7]. The PRC noise model, which is represented by Pucel's three independent noise parameters P, R, and C, has been widely used to evaluate the noise performance of the proposed LNA [3,19]. In the LNA, the FN1 not only feeds the signal back to the input and adds additional noise, but also optimizes the input impedance of the LNA [5]. The noise model can be established by analyzing the PRC model of the first stage and simplifying the circuit model with neglecting the sub-circuits [3,5]. The FN1 deteriorates the LNA's noise inevitably due to the contribution from the resistor R1. Although the value of R1 optimizes the input matching bandwidth and stability, the gain will be degraded seriously if the value is too small. However, at high frequency, the long resistor in the layout behaves as transmission lines, and these distributed effects have an influence on the resistor. Fig.3 shows the NFmin, NF,  $\Gamma_{opt}$  (optimum noise source reflection coefficient) and  $\Gamma_s$  (source reflectance coefficient) according to the frequency with difference R1 (without L1). For a good input match and NF, we also add additional matching inductor L1 at the input.

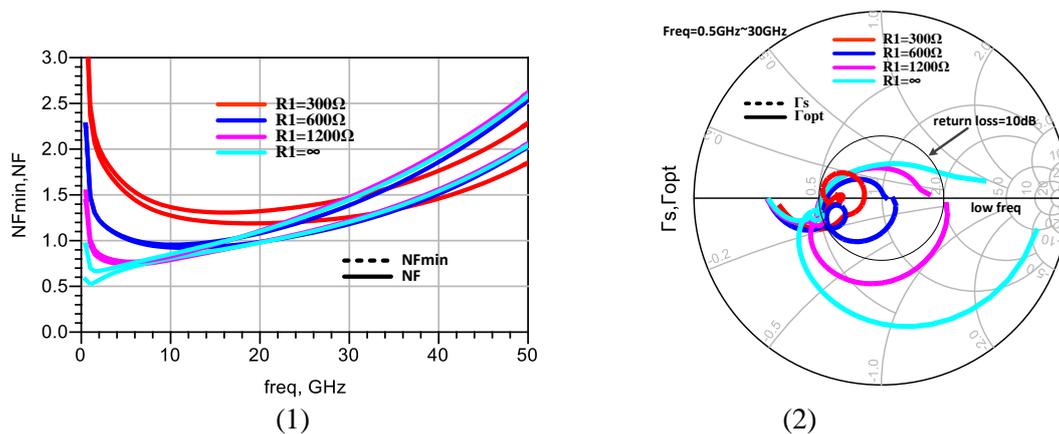


Fig.3 Performance according to the frequency with R1: (1) NFmin and NF; (2)  $\Gamma_{opt}$  and  $\Gamma_s$

### 4.2. Gain Flatten

As we know, the MAG drops when the transistor operating frequency goes higher. In this circuit, the FNs and SNs are designed to guarantee unconditionally stable and provide wideband gain flatten and I/O impedance matching. At low frequency, the source SN of M2 and M3 is equivalent to a small resistor which deteriorates the gain inevitably, and the FN is equivalent to a resistor R which deteriorates the gain too. However, at the high frequency (such as above 10GHz), the SN is shorted by the capacitor, which would not obviously decrease the gain of the LNA. Also, the FN, which is equivalent to a resistor R1 with a parasitic on-chip microstrip, decreases the gain more slightly than at low frequency.

### 4.3. Impedance Match

The input mismatch may degenerate both NF and gain performances of the LNA. We adopted on-chip small lumped elements rather than distributed elements for impedance matching. From the noise analysis above, the feedback topology in this paper, which makes the  $\Gamma_{opt}$  closer to the  $\Gamma_s^*$  in the Smith Chart, is a trade-off for noise and broad input matching. From the Fig.3 and Fig.4, it can be seen that we can control the input matching and NF by choosing an appropriate value of R1 and L1. The input matching network is simplified with acceptable NF over a wide bandwidth. To maximize the gain of the whole circuit, the last stage amplifier should optimize to achieve the highest gain. In this

paper, we adopt two resistors R8, R9, a series L5 and a blocking capacitor C5 to achieve good output match. The Fig.4 shows the S21 and S22 with different parameters of L5 and R9.

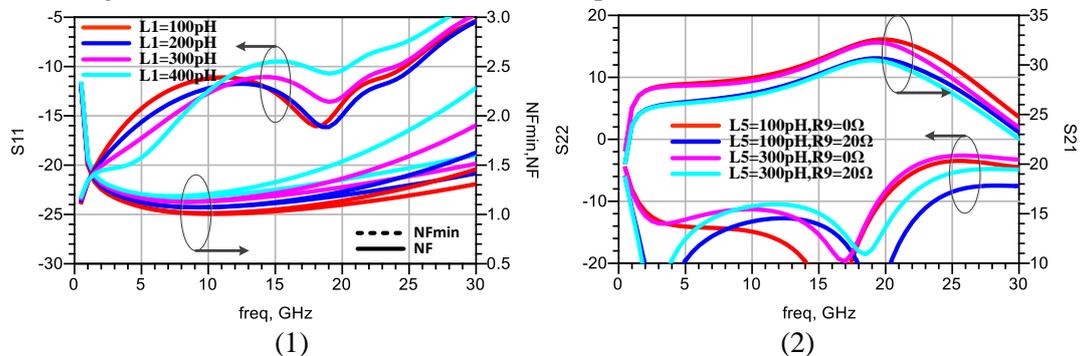


Fig.4 The impedance matching: (1) input matching with difference L1, (2) output matching according to the frequency

## 5. Simulation Results

In this paper, we choose the D007IH process from OMMIC foundry. The 70nm gate length MHEMT is built on GaAs substrate with 100um thickness. Gates and drains of transistors are biased through on-chip inductor BNs. To validate the characteristic of the LNA, this three-stages LNA circuit with multi-feedback is simulated by Advanced Design System (ADS) software including EM simulation to optimize the layout performance. Since the LNA is usually the first element in the front end, the final EM simulation analysis includes the bond wires and the RF pads. Fig.5 shows the 3D circuit layout of the MMIC with an area of 1.4mm\*0.8mm.

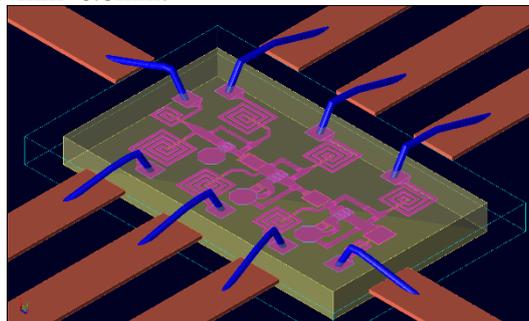
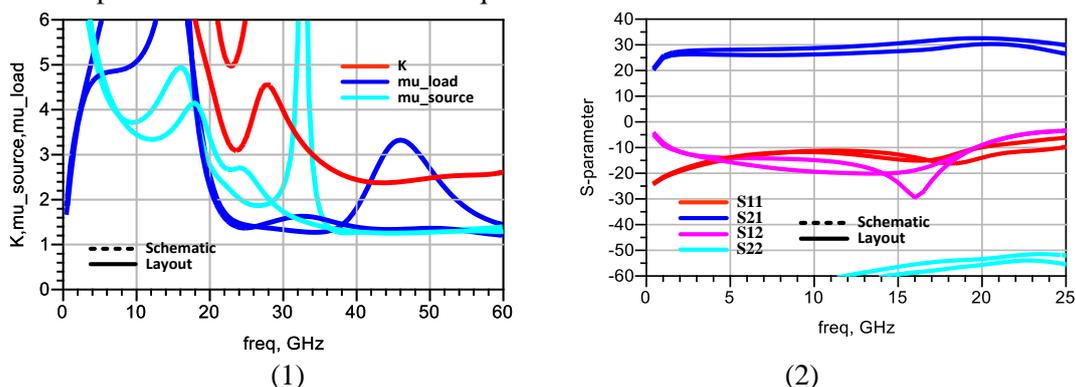


Fig.5 3D layout of the proposed LNA

From the simulation results of Fig.6(1), we can see that the LNA is unconditionally stable in a broadband. And Fig.6(2) shows I/O return loss is better than -10dB from 1.5GHz to 20GHz. The simulated LNA presents a gain about 29.5dB with the positive increase across the band. The isolation (S12) is better than 50dB and the NF is from 1dB to 1.35dB in the band. Fig.6(4) demonstrates the simulated output P1dB>7dBm at different frequencies.



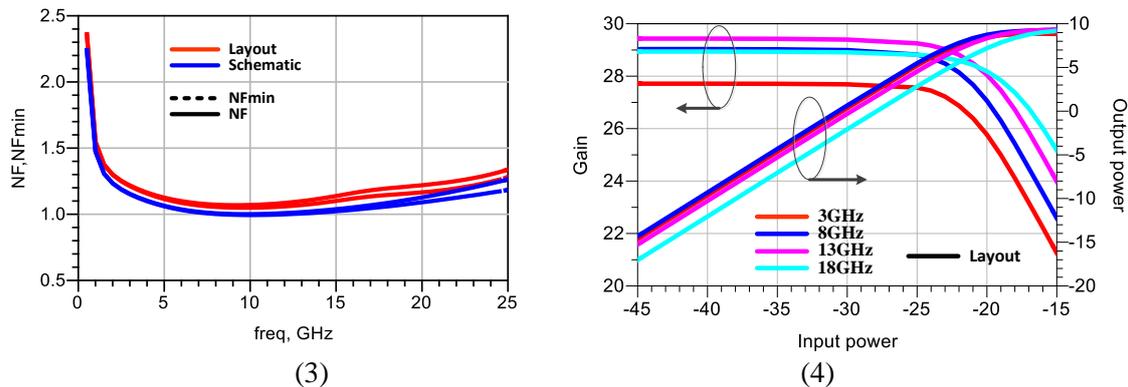


Fig.6 The simulation results of the proposed LNA: (1) Stability; (2) S-parameters (3) Noise; (4) P1dB

The FOM can be used to evaluate the performance of an LNA. The FOM relates to the gain-bandwidth product (GBP), NF and DC power consumption. The  $S_{21, mag}$  is the magnitude of the small signal gain,  $NF_{mag}$  is the magnitude of the noise figure, and  $P_{dc}$  is the dc power consumption in milli-watt [3].

$$FOM = \frac{S_{21, mag} * Bandwidth [GHz]}{(NF_{mag} - 1) * P_{dc} [mW]}$$

Tab.1 The FOM of the recent published LNA MMICs

Ref	Technology	Frequency (GHz)	Gain ** (dB)	NF** (dB)	S11 in band (dB)	Gain variation (dB)	Chip Area (mm <sup>2</sup> )	Pdc (mW)	FOM (GHz/mW)
[3] #	0.5- $\mu$ m pHEMT	0–6	16	1.5–2.2	<-10	0.4	0.26	42.5	10.9*
[7]	0.15- $\mu$ m pHEMT	3.2-14.7	34	1.3	<-5*	0.8	2.5x1.5	45	1839
[6]	0.10- $\mu$ m pHEMT	3.8-19.8	20	2	<-5*	3	1.5x1.0	40	68.4*
[18]	0.15- $\mu$ m pHEMT	0.1-20	28.6	3.1-5.8	<-10	5*	1.53	505	15.7*
[15]	0.15- $\mu$ m pHEMT	3-15	28	2*	<-7*	7*	2x1	200	64.7*
[13]	0.15- $\mu$ m pHEMT	1.6-3.1	30.5	0.67-0.85	<-10*	2*	2.5x1.5	54.5	161.47
[14]	0.1- $\mu$ m pHEMT	2-40	15.2	2.3	<-5	4*	1.88	110	16.4*
This work#	0.07- $\mu$ m mHEMT	1.5-20	29.5	1.15	<-10	5(positive increase)	1.4x0.8	150	362.6

PS: \*estimated from the data shown in the paper; \*\* average in band; \*\*\* not described in the paper; #simulation results

The Tab.1 summarizes the performance of this proposed LNA and recent published similar wideband GaAs LNA MMICs in different processes. In this paper, the high gain, low NF, small chip size performances with a FOM of 362.6GHz/mW make this proposed broadband LNA more competitive. And the performance of the positive increase gain with the frequency in-band is valuable for engineering practice.

## 6. Conclusion

In this work, we present the a multi-stages MMIC GaAs MHEMT LNA with multi-feedback operating from 1.5GHz to 20GHz for broadband applications. With a chip size about 1.4mm\*0.8mm, this LNA is unconditionally stable across the required operating frequencies. The results suggest that the proposed LNA is suited for the applications such as high data rate transmission, SDR, digital RF, test instrumentation, UWB transceiver, multi-mode transceiver, and other wideband systems.

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