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# 1.2 Mfps standalone X-ray detector for Time-Resolved Experiments

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Abstract: We present a standalone and autonomous X-ray detector capable of operation with the speed of up to1.2 Mfps. The detector utilizes UFXC32k hybrid pixel detectors for sensing X-rays, Spartan-6 LX45 FPGA placed in commercially available sbRIO 9628 controller for data acquisition and processing including a compression with zero-suppression algorithm. A Linux-RT system working on the 400 MHz Dual-Core CPU is used for FPGA control and data streaming to the higher-level system over 1 Gbps Ethernet connection. 1.2 M frames per second is achieved in so-called burst mode of operation while in zerodead-time mode 70 kfps is possible. Due to efficient data compression in FPGA there's no need of using high-speed transceivers and Frame-Grabber cards on the data server side and the detector can stream the data infinitely over standard 1 Gbps network connection. Operation modes were tested at Advanced Photon Source Synchrotron at Argonne National Laboratory.

Keywords: Data acquisition concepts; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Modular electronics; X-ray detectors

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## Contents





## 1 Introduction

Pixel X-ray detectors are very popular and used in various different fields. Nowadays single photon counting detectors become more and more popular due the noiseless imaging capabilities, where signal is separated from electronics noise with the use of discriminator blocks. This ability of noise separation makes single photon counting detector desirable in a variety of applications in different fields such as medical imaging, material science or industry [1–3]. Single photon counting pixel X-ray detectors are very often designed as hybrid detectors. In such a system the sensor material is separated from the readout integrated circuit (ROIC) allowing changing sensor material for different applications. Therefore, the design of ROIC is the main challenge and many scientific groups around the globe are working on improving the main parameters, namely the noise and offset spread influencing the energy resolution of the detector but also improving a photon-count rate allowing detector operation with higher photon flux. Table 1. presents the most popular hybrid pixel detector readout circuits and their analog front-end performance.

**Table 1**. Comparison of few recent IC designs of integrated circuits for hybrid detector readout.

| ASIC | **FRIC [4]** | **Medipix3RX [5, 6]** | **IBEX [7]** | **UFXC32k [8]** |
|---|---|---|---|---|
| Technology | 40 nm | 130 nm | 110 nm | 130 nm |
| Array size | 64 × 64 | 256 × 256 | 256 × 256 | 128 × 256 |
| Pixel size ($\mu m^2$) | 50 × 50 | 55 × 55 | 75 × 75 | 75 × 75 |
| Hardware implementation of charge sharing correction | Yes | Yes | No | No |
| Analog power / pixel (μW) | 12 | 7.5 | 7.4 | 26 |
| FWHM (keV) | 0.71 | 0.96 | 0.85 | — |
| ENC ($e^-$) | 45[1] | 80 | 89 | 123 |
| Front-End Dead time (ns) | 50 | 690 | 100 | 232 |

For the final application the performance of the analog front-end and the digital backend of the pixel and the IC periphery is of equal importance. The digital blocks define the final functionality of the ROIC and furthermore the operation of the final, standalone detector device which uses certain ROIC in the sensing part. Due to very high count-rate of the front-end and high data throughput a UFXC32k-based detector was used for the 1.2 Mfps standalone camera prototype.

This article presents the methodology, tools and methods used for building a prototype of the standalone X-ray detector using a single-photon counting ROIC and operating with very high frame rate of 70 kfps in a zero-dead and 1.2 Mfps in the burst mode. The prototype camera utilizes Spartan-6 LX45 FPGA for communication with ROIC, data processing and compression, a Dual-Core CPU for the standalone operation, state monitoring, communication with higher level control system (e.g. APS control by EPICs). Section 2 presents the details of hardware and software design of the camera. Section 3 focuses on the tests in real experiment at synchrotron and section 4 contains conclusions.

## 2 Camera design

### 2.1 Hardware design

With many possible approaches towards the design of a standalone detector including the one where the whole embedded device is designed "from scratch", we've decided to use a commercially available embedded controller and shape it's functionality by software. Among a large variety of available devices one in particular brings an attention by allowing the software design using a single software platform for each target including FPGA, Real-Time OS and Windows Target. More than that, the sbRIO 9628 [9] contains a high density connector for 96 HS DIO lines with the ability of single-ended or LVDS configuration in the software. The Spartan-6 LX45 is large enough to cover assumed functionality of 28 LVDS lines timed with up to 400 MHz clock for interfacing with UFXC32k ROIC, 4 single-ended TTL lines sampled with 200 MHz for triggering purposes, in FPGA data processing and compression and streaming the zero-suppressed result to the CPU with direct memory access. Interfacing to the embedded system is possible with the use of 1 Gbps, which is utilized for streaming the measurement data to the higher level system, which in our case is the control system at APS in Argonne National Laboratory.

The only components necessary to be placed on the designed PCB containing the UFXC32k chips are the power supply blocks and the communication lines interfacing with sbRIO9628 thru high density mezzanine card (RMC). The designed system is shown in figure 1. The sensor is on the opposite side of the power-supply blocks.

Utilizing the sbRIO 9628 interfacing capabilities, the designed detector can interface with higher level system with up to two Ethernet cables, USB, it can stream the data to the SD card or the USB drive.

### 2.2 Software design

The biggest advantage of the commercially available controller is that the most time-consuming part, namely the design of the FPGA, CPU and memory related blocks together with separate sections of power supply are already done, tested and verified for operation in well-defined conditions. The functionality of the controller is defined by software.



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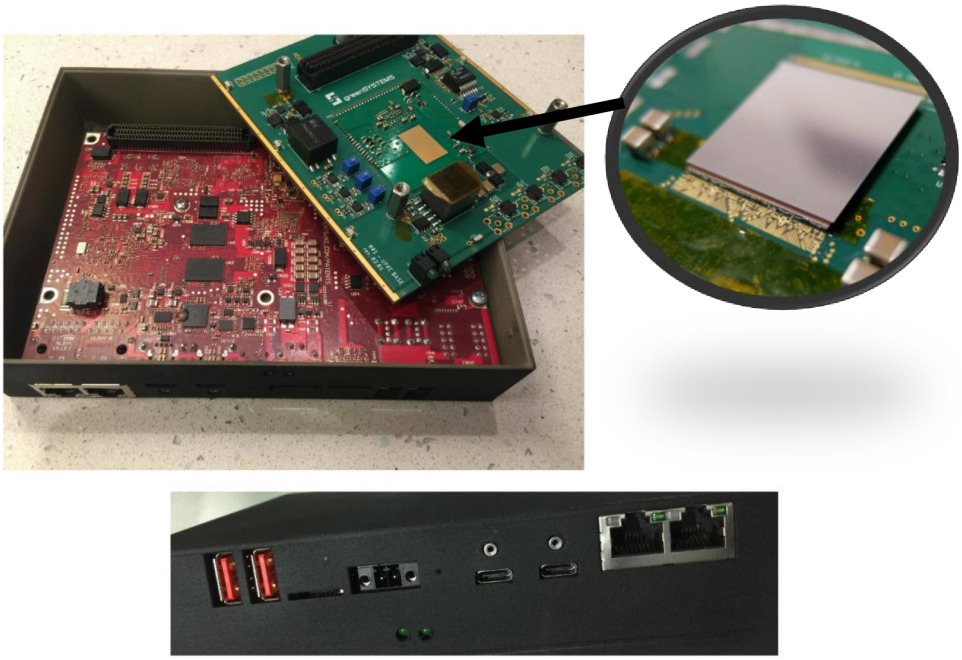

**Figure 1**. Hardware components of the detector.

In the presented device three different targets are used, namely FPGA, CPU with Linux Real-Time OS and higher level operating system (here it is Windows OS). The FPGA is responsible for majority of low-level operations, like interfacing with UFXC32k ROICs using 28 lines timed with up to 400 MHz, acquisition of the ROICs bit-stream and the bit by bit pixels' value reconstruction, data zero-suppression with pixel address assigning and sending the data to the RAM via DMA. The simplified scheme of the FPGA software is shown in figure 2. All the desired functionality necessary for the camera operation is possible to write without significant limitations in LabVIEW, a high abstraction level, graphical system design platform. Different modes of operation are supported with separate FPGA code which can be loaded by the program working on the CPU and RT OS. For time-resolved experiments the important modes are the continuous zero dead-time mode and a burst mode described in detail in [10]. In both zero dead-time and a burst modes the data dynamic range is set to be only 2-bit, which is sufficient for XPCS experiments conducted at APS, but may not be enough for other experiments. The ability of using FPGA I/O transceivers with the speed exceeding 200 MHz is realized with VHDL definition in the form of component level IP (CLIP). This CLIP definition allows using FPGA ser-des blocks with the output clock speed up to 800 MHz.

The FPGA software architecture allow for operation with different speeds and different modes and the change between 1.2 Mfps burst mode and 70 kfps zero dead-time mode is just the parameter of a program. In a standard small angle scattering XPCS the number of photons scattered from the sample is very small reaching up to 1% of the detector occupancy/frame even for a very high photon flux from synchrotron beam. This is one of the reasons the data streaming via 1 Gbps Ethernet link is possible. Continuous and endless data streaming is possible if the detector occupancy is lower than 1% (up to around 40 MB/s). If the photon flux is high, the data can be streamed continuously up to the amount of the RAM available in real-time OS, which is only about 400 MB, then the



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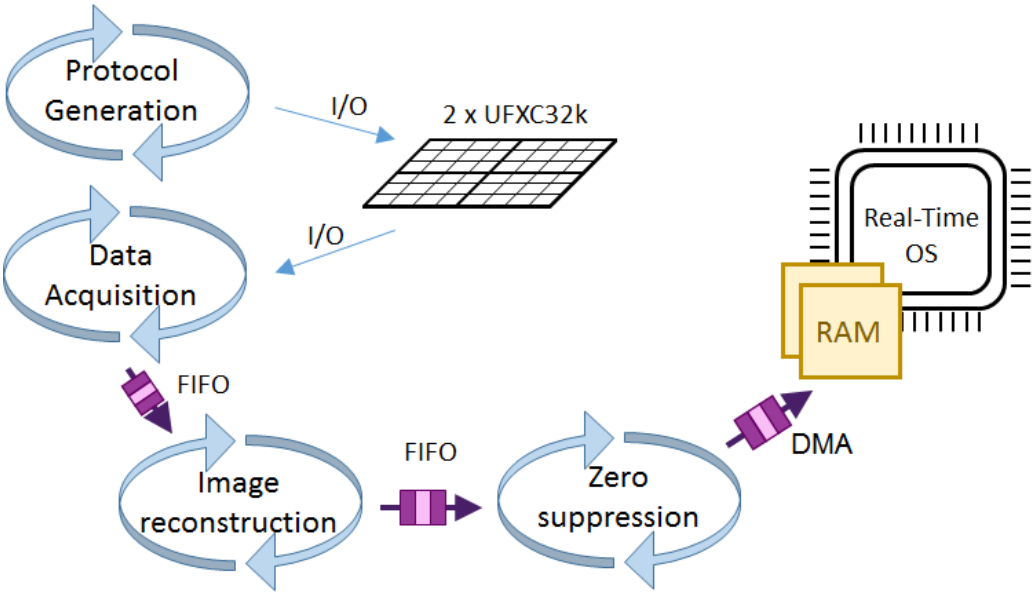


**Figure 2**. FPGA software architecture.

events will be lost and certain notification will be shown. One way to recover from this situation is to add attenuation of the photon flux arriving to the sample.

## 3 Verification of detector operation

The UFXC32k-based detector is tested for high frame-rate operation and used in XPCS experiments since 2016 [11] producing few scientific results published e.g. in Physics Review Letters and The Journal of Chemical Physics. First systems were built with the use of high-end controllers with standard PC systems allowing for fast implementations and changes of the desired functionality. Those systems are fairly robust and reliable, they need an occasional rebooting and are difficult to move from one station to the other. There was a need for a standalone detector that could work within extended time frame and this work is the first attempt to build a high-frame rate, X-ray standalone detector capable of operating with up to 70 kfps in the zero dead-time mode and the burst mode is possible with up to 1.2 Mfps. First results taken with the UFXC32k based device and the speed of 70 kfps are shown in figure 3. This is an X-ray photon correlation spectroscopy experiment showing x-axis scaled in seconds with five decades range.

## 4 Conclusions

The presented tools and methods used for design a prototype device proof that a very high performance embedded device can be designed with the use of a commercially available controller allowing for functionality change by software. Using the sbRIO 9628 allow the utilization of LabVIEW, a high abstraction level graphical system design platform to write an efficient FPGA code overcoming various limitations and allowing continuous data acquisition with the speed of 70 kfps with zero-dead time mode and 1.2 Mfps in a burst mode. The detector behaviour is defined by the



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software working on Linux RT OS and written in the very same tool and the very same project window allowing for enormous acceleration of the design and debugging process. More than that — the communication with the higher level system is defined in the very same way.

The camera will be updated with new functionalities allowing triggering and memorizing single frame from 70 kfps stream for the purpose of particle tracking experiments.

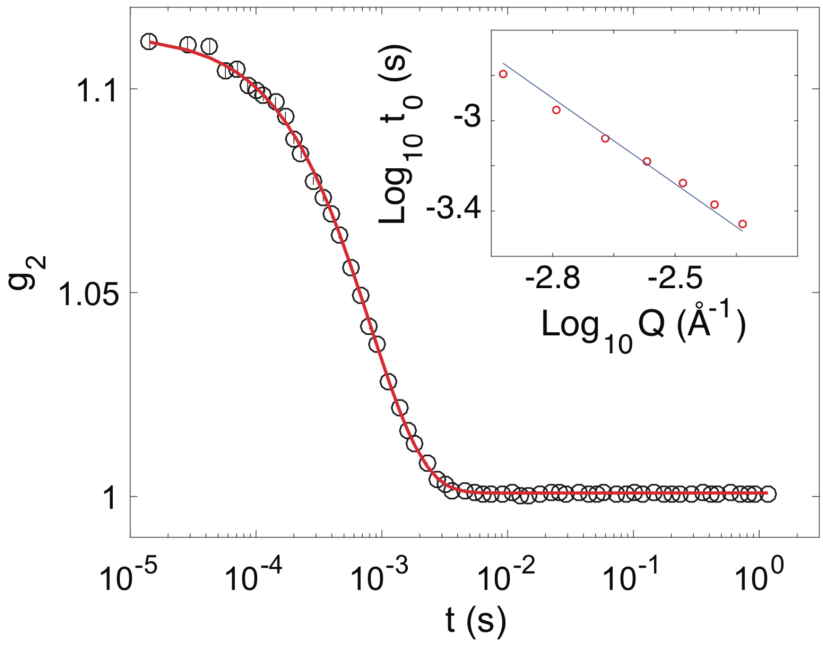


**Figure 3**. XPCS time autocorrelation ($g_2$) determined from Brownian motion of 100 nm diameter silica nanoparticles suspended in water. The solid red line is a fit to an exponential function $\exp(-2t/t_0)$ and the inset plots $t_0$ determined at different momentum transfer $Q$. The solid blue line indicates the $Q^{-2}$ scaling which is expected for Brownian motion.

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