Upgrade of the CMS electromagnetic calorimeter for precision timing and energy measurements at the High Luminosity LHC

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ABSTRACT: The high luminosity upgrade of the LHC (HL-LHC) at CERN will provide unprecedented instantaneous and integrated luminosities of around 5×10^{34} cm^{-2} s^{-1} and up to 4500 fb^{-1}, respectively, from 2027 to 2035. We predict an average of 140 to 200 concurrent interactions per bunch crossing (pile-up). This poses a major challenge to the event reconstruction. The Compact Muon Solenoid (CMS) detector is therefore undergoing an extensive Phase II upgrade program to prepare for these challenging conditions. The upgrade of the barrel part of the CMS electromagnetic calorimeter (ECAL) for HL-LHC will extend the detector performance to be able to cope with these harsh conditions, particularly the increased trigger and latency requirements at the HL-LHC. The lead tungstate crystals in the ECAL barrel sub-detector will still perform well. The avalanche photodiodes which detect the scintillation light will also continue to be operational with some increase in noise due to radiation-induced dark currents. However the entire readout electronics will need to be replaced. The upgraded detector will have a 25 fold improved trigger granularity and a sampling rate increase by a factor of four. In addition, the upgraded detector will have the new capability to provide precision timing measurements for photons and electrons with energies greater than 10 GeV. This will significantly improve the performance under the predicted pile-up conditions. High precision time resolution will be exploited for pileup mitigation and to permit the assignment of physics objects to their correct vertices. In this report the status of the ongoing R&D activities for the ECAL barrel upgrade will be presented.

KEYWORDS: Calorimeters; Front-end electronics for detector readout

Contents

1 Introduction

The electromagnetic calorimeter (ECAL) is a key tool for the identification and reconstruction of photons and electrons, and is important for the measurement of jets and missing transverse momentum. It is composed of a barrel (EB), cylindrical in shape, covering the central rapidity region (up to $|\eta| = 1.48$) of and two disks called endcaps (EE), which detect incident particles up to $|\eta| = 3.0$. The detector was designed having in mind the search for the Higgs decay to two photons, for which excellent energy resolution and efficient identification for photons are required. A precise measurement of energy and momentum of electrons is important for the Higgs decay into two Z bosons and many other research topics within and beyond the Standard Model.

The ECAL has indeed fulfilled its performance goals with remarkable success. However, it was designed to meet these performance requirements up to an integrated luminosity of $500\,\mathrm{fb}^{-1}$. In order to maintain the current performances up to the integrated luminosity of $4500\,\mathrm{fb}^{-1}$ foreseen at the end of the HL-LHC program, an upgrade of the EB readout electronics, which we describe in this report, is needed. The transparency loss in EE will be so significant that the detector will be completely replaced before the start of HL-LHC [1].

2 The CMS ECAL detector

The CMS ECAL is a homogeneous calorimeter made of 75 848 lead tungstate ($PbWO_4$) scintillating crystals, located inside the CMS superconducting solenoid magnet. The photodetectors are avalanche photo-diodes (APD) in the barrel and vacuum phototriodes (VPT) in the endcaps. The barrel region is made of 36 identical supermodules (SM), each containing the crystals, APDs, and readout electronics. The latter includes very front-end (VFE) cards, which provide pulse amplification, shaping, and digitisation functions, and front-end (FE) cards which provide data pipeline, data transmission, and trigger primitive formation functions. Electrons and photons are typically reconstructed up to $|\eta| < 2.5$, the region covered by the tracker, while jets are reconstructed up to $|\eta| = 3.0$. The ECAL energy resolution achieved during 2010 and 2011 ranges from 1.1 to 2.6% in the barrel and 2.2 to 5% in the endcaps for photons from Higgs boson decays.

3 HL-LHC ECAL upgrade scope

Two of the challenges that the ECAL detector will have to face for the HL-LHC program are ageing effects and harsher data-taking conditions. Ageing will cause a loss of transparency and an increase in the APD leakage current and therefore noise. To mitigate both effects, the operating temperature will be reduced from the current 18°C to 9°C. On the other hand, the number of average concurrent interactions per bunch crossing will increase to 200 from the 40 that corresponded to the normal running condition in the first phase of LHC. An improved time resolution will be needed in order to be able to distinguish the primary vertex from the other vertices in the same bunch crossing. To meet this goal, a faster front-end electronics is being designed. This improvement will also result in a better discriminating power between scintillation light generated by electromagnetic showers from the faster anomalous signals caused by particles hitting the APD directly. The back-end, off-detector electronics is also being redesigned, in order to obtain greater flexibility in the trigger and cope with the increased CMS-wide level-1 (L1) trigger latency (from 3.5 µs to 12 µs) and rates (from 100 KHz to 750 KHz) [2].

4 The upgraded ECAL front-end electronics

In the upgrade program, the crystals, APDs and motherboards of the EB will remain the same. The APD output will be sampled and each sample shipped out to the off-detector electronics using high-speed optical links. The front-end will comprise a new, faster analog electronics and the sampling rate will increase from 40 to 160 MHz, with 12-bit resolution, to obtain better time resolution and anomalous signal discrimination. The cost of this improvement is the increase in data rate, for which a loss-less data compression mechanism is envisaged.
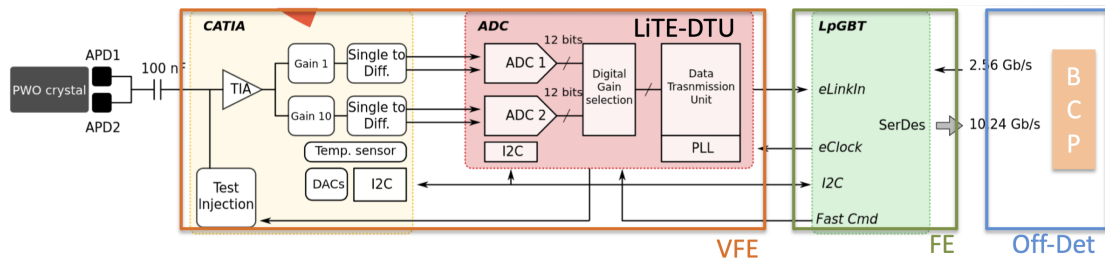

Figure 1. Block representation of the EB readout electronics for HL-LHC.

Figure 1 shows a block diagram of the new readout electronics. The upgraded VFE comprises an analog ASIC called CATIA, which implements two transimpedence amplifiers (TIAs) with 35 MHz bandwidth, and a digital ASIC called LiTE-DTU, comprising two 12-bit ADCs sampling at 160 MHz, data transmission with gain selection and compression. Each VFE reads five APDs and carries five channels, each channel consisting of a CATIA and a LiTE-DTU. Five VFEs are connected to a single FE card that collects data from the VFEs and transmits to the off-detector electronics using the lpGBT [3] optical transmission system. Also connected to the FE is a low voltage regulator board (LVR), a radiation-hard voltage regulator card based on the Feast DC-DC converter. Off-detector, the Barrel Calorimeter Processor (BCP) card will use powerful FPGAs to form the L1 trigger decision and read out the detector.
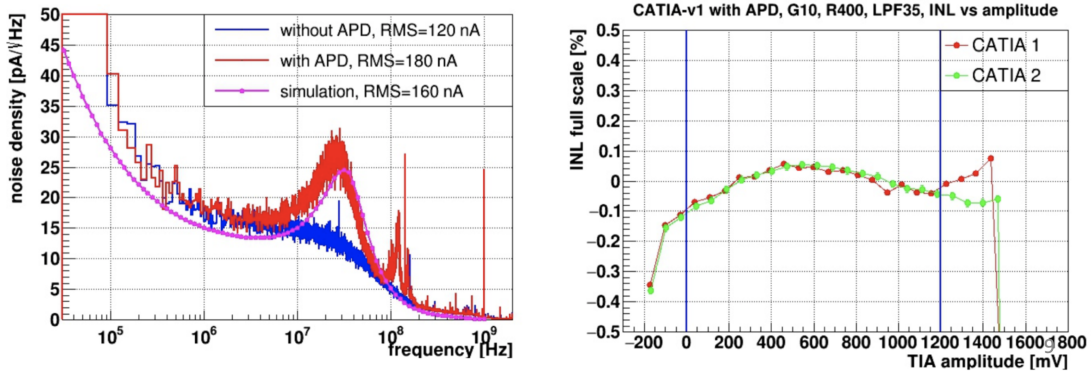
Figure 2. Left: noise performance of the CATIA ASIC as a function of frequency, connected and not connected to the APD, compared to simulations. Right: integral non-linearity measurements of the first and second CATIA prototype, as a function of input signal amplitude.
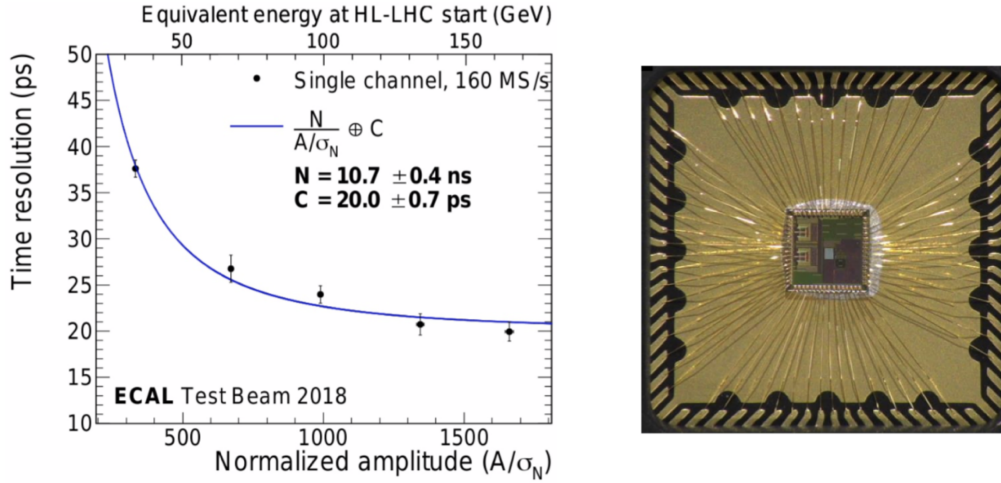

Figure 3. Left: time resolution as a function of normalized amplitude and energy obtained in a test beam campaign with the CATIA ASIC connected to a commercial ADC. Right: the first prototype of the LiTE-DTU ASIC.

The CATIA ASIC is built in 130 nm CMOS technology. It comprises a high-gain and a low-gain amplification channel of the APD output, to cope with the dynamic range requirements, and it features test pulse injection. The performances of the CATIA prototype have been tested in test beam campaigns and shown to be very good in term of noise, linearity, and time resolution. The results are presented in figures 2 and 3. Figure 2, left, shows the measured noise density spectrum of the CATIA, with and without connection to the APD, compared to simulation. Figure 2, right, shows a measurement of the integral non-linearity (INL) of two samples of the CATIA (v1) as a function of the amplitude of an injected test pulse. In the range of interest (0 to 1200 mV) the INL is below 0.1%. Figure 3, left, shows the timing resolution obtained with electrons from a Test Beam at Cern as a function of signal amplitude and energy. A resolution of better than 30 ps is obtained for electrons of energy greater than 50 GeV.

The LiTE-DTU ASIC is built in 65 nm CMOS technology. It includes two 12-bit ADCs running at 160 MHz, designed by a commercial company and specified for a ENOB (equivalent

number of bits) of better than 10.2 at 50 MHz. The data transmission unit selects the highest non-saturated gain channel and takes care of data transmission and compression. It includes a PLL circuit for clock generation, it's designed to be TID (total irradiation dose) tolerant up to 2 kGy and it features SEU-tolerant logic. The loss-less data compression mechanism exploits the fact that the spectrum of the hits in each ECAL crystal falls very rapidly with energy. Consequently, the signal is above 2.5 GeV only in a small fraction of events. The compression algorithm was designed to use 6 bits to encode signals below 2.5 GeV, and 12 bits for signals above 2.5 GeV. This allows the reduction of the expected bandwidth occupancy to 1.08 Gb/s, to be compared with the 2.08 Gb/s needed in absence of compression. The first prototype of the LiTE-DTU chip was under test in late 2019. An image of the packaged prototype is visible in figure 3 (right).

The function of the FE card is the streaming of digitized data generated on the VFE to the CMS ECAL back-end electronics, system initialization and control of all VFE components, and precise distribution of the clock to VFE cards. It includes four lpGBT downlinks at 10.24 Gb/s and one downlink at 2.56 Gb/s. A demonstrator was built using GBTx, and a prototype with lpGBT is expected in early 2020.

The off-detector BCP card will be common for ECAL and HCAL, the barrel section of the hadron calorimeter. Its purpose is trigger primitive formation, clock distribution, control, and data readout. It will be implemented as an ATCA blade and will rely on FPGA technology.

5 Summary

HL-LHC poses challenging demands on detectors, with a 4–5 fold increase in occupancy with resoect to LHC conditions. To maintain adequate performances, the ECAL barrel readout must be improved with better time resolution and trigger flexibility. For HL-LHC the readout electronics will be completely replaced, while keeping the crystals and photosensors. The upgrade will encompass faster analog electronics, higher sampling rate, and full granularity off-detector trigger primitive formation. The upgrade project is well defined and prototypes have been extensively tested or are currently under test.

References

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