IOP Publishing Superconductor Science and Technology
Supercond. Sci. Technol. 33 (2020) 035010 (8pp) https://doi.org/10.1088/1361-6668/ab6feb

# A compact AQFP logic cell design using an 8-metal layer superconductor process

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Received 14 November 2019, revised 14 January 2020
Accepted for publication 24 January 2020
Published 12 February 2020

**Abstract**

Adiabatic quantum-flux-parametron (AQFP) is an adiabatic logic based on the quantum-flux-parametron. It has extremely low switching energy, as well as high signal gain and high robustness. In this work, we present the development of an AQFP cell library using the MIT LL 100 $\mu$A $\mu$m$^{-2}$ superconductor electronics fabrication process, SFQ5ee. Four types of basic sub-cells, i.e. buffer, inverter, constant, and branch, are designed as the building blocks for combinational AQFP logic cells. Taking advantage of the 8 metal layers, we place the dc superconducting quantum interference device (SQUID) part of a buffer above the ground plane and the signal transformer part below the ground plane to mitigate unwanted couplings. In addition, by vertically overlapping the signal transformer and the dc SQUID, the dimension of a buffer is reduced to 15 $\mu$m $\times$ 20 $\mu$m, which is only 30% of that of the conventional design. More complex AQFP logic cells, such as the majority gate, AND gate, and OR gate, are designed by arraying the sub-cells together. Correct operations and wide excitation current margins are confirmed for the established AQFP logic cells by both simulation and experiments.

Keywords: adiabatic logic, qfp, cell library, superconducting integrated circuits

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Superconductor logic is considered promising for realizing extremely energy-efficient supercomputing systems; and its advantages as well as challenges have been widely discussed in several projects [1–3]. To this end, extensive efforts have been spent on the development of superconductor digital circuits based on rapid single flux quantum (RSFQ) logic [4, 5]. With the reduction of static power consumption, energy-efficient RSFQ logic families can operate with a bit energy below 1 aJ [6–9].

In the last few years, we have been investigating an alternative superconductor logic family known as adiabatic quantum-flux-parametron (AQFP) logic [10, 11]. As both dynamic and static power consumption are significantly reduced due to adiabatic switching operations [12, 13], AQFP can achieve a bit-energy even below $k_BT$ ($k_B$ denotes the Boltzmann constant and $T$ represents temperature) [14, 15], which is more than three orders of magnitude lower than the energy-efficient variants of RSFQ logic. We established two sets of AQFP cell libraries in [16, 17] using the 2.5 kA cm$^{-2}$ Nb standard process (STP2) [18] and the 10 kA cm$^{-2}$ Nb high-speed standard process (HSTP) [17]. Both include four metal layers and are provided by the National Institute of Advanced Industrial Science and Technology. Based on these cell libraries, several large AQFP circuits comprised of over 20k Josephson junctions (JJs) have been designed and demonstrated [19].

The development of a more advanced superconducting integrated-circuit fabrication process known as SFQ5ee [20], provided by MIT Lincoln Laboratory (MIT LL), has raised new opportunities to realize superconductor logic circuits. It

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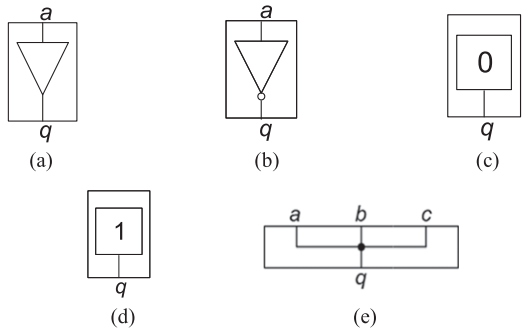



**Figure 1.** Symbol view of sub-cells. (a) Buffer ($q = a$). (b) Inverter ($q = \bar{a}$). (c) Const0 ($q = 0$), (d) Const1 ($q = 1$). (e) 1-to-3 branch when driven from $q$ or 3-to-1 confluence when driven from $a/b/c$.

is an eight-metal-layer fully-planarized process based on $Nb/Al–AlO_x/Nb$ JJs with a critical current density of 100 $\mu A\ \mu m^{-2}$. Since more metal layers are available compared to the four metal layers of HSTP and STP2, the AQFP cell design is expected to be miniaturized if we properly utilize the additional layers.

In this work, we establish an AQFP cell library with compact cell dimensions using the MIT LL SFQ5ee process. By implementing the dc SQUID part and the output signal transformer on separate layers, the physical dimension of a buffer cell is reduced by 70% when compared to the designs for STP2 and HSTP. In the following, basic design principles and layouts of the proposed AQFP cell library is given in section 2. Numerical simulations of a 9-stage buffer chain, including data propagation, operation margin, and energy dissipation, are provided in section 3. For the experimental validation, a class of AQFP cells and appropriate test circuits have been designed, fabricated, and measured at 4.2 K. Both the simulation and tested results reveal desired functionalities as well as wide operating margins.

## 2. AQFP cell library

### 2.1. Design principle

Based on the minimalist design concept [16], establishment of an AQFP cell library involves four types of fundamental sub-cells, i.e. buffer, inverter, constant, and branch, whose symbol views are illustrated in figure 1. Because the buffer, inverter, and constant sub-cells are similar to each other with only slight differences, we can focus on optimizing the buffer design and in turn those optimizations are likely applicable to also the inverter and constant sub-cell. Furthermore, with only a total of four sub-cells to work with, our optimization efforts overall are kept to a minimum. By using only this small collection of sub-cells, we can construct an expressively rich set of Boolean logic cells including majority, AND, OR, and splitter gates. We can mix-and-match buffers and inverters to create logic cells that intrinsically operate with positive or negative input without any additional overhead in logical depth. Some examples of Boolean logic cells (MAJ3_ppn, AND2_np, OR2_pn, SPL3) and how they are constructed from the sub-cells are shown in figure 2. Note that the

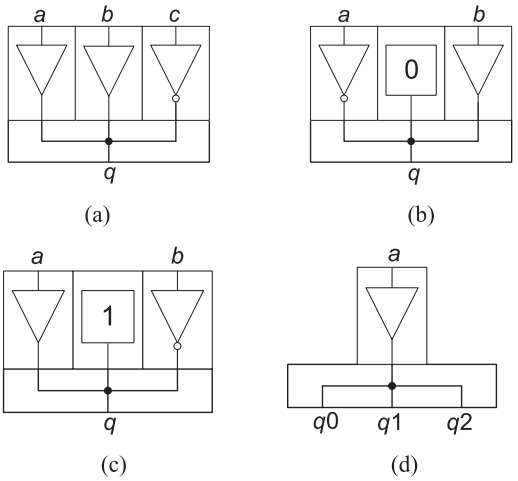



**Figure 2.** Symbol views of Boolean logic cells. (a) MAJ3_ppn ($q = \mathrm{MAJ}(a, b, \bar{c})$). (b) AND2_np ($q = \bar{a} \cdot b$). (c) OR2_pn ($q = a + \bar{b}$). (d) SPL3 ($q_0, q_1, q_2 = a$).

Boolean logic cells in this work are named using the following convention: ⟨cell name⟩ ⟨number of logic inputs⟩_ ⟨polarity of input $a$⟩ ⟨polarity of input $b$⟩…⟨polarity of input $k$⟩, where positive (not inverted) and negative (inverted) polarities are denoted by $p$ and $n$ respectively. For instance, MAJ3_ppn in figure 2(a) denotes a 3-input majority gate with positive input $a$, positive input $b$, and negative input $c$; thus, $q = \mathrm{MAJ}(a, b, \bar{c}) = ab + b\bar{c} + \bar{c}a$. Complex and large-scale AQFP circuits can be realized by organically arranging the logic cells together, as it is done in [19, 21].

### 2.2. Design of logic cells

The layout of an AQFP buffer cell for SFQ5ee is presented in figure 3(a), and its corresponding schematic is given in figure 3(b). The dc superconducting quantum interference device (SQUID) part ($J_1$–$L_1$–$L_2$–$J_2$) is placed above the ground plane (M4 of the MIT LL SFQ5ee process), whereas the output signal transformer part ($L_q$ and $L_{out}$) is placed below the ground plane. This mitigates unwanted couplings between the dc SQUID and the output signal transformer, even without magnetic shields [22]. As a result, the signal transformer can be designed in an asymmetric way to reduce the footprint area; note that conventional design uses symmetrical structures to mitigate unwanted couplings [16, 17], which results in a somewhat large cell dimension. By overlapping the dc SQUID and the signal transformer parts in the vertical direction, the whole size of a buffer cell is only 15 $\mu$m × 20 $\mu$m, occupying only 30% area of the design for HSTP (25 $\mu$m × 40 $\mu$m) [17], and 25% area of the design for STP2 (30 $\mu$m × 40 $\mu$m) [16].

The relevant parameters, as listed in the caption of figure 3, are extracted using a 3D inductance extractor InductEx (v 5.06) [23]. $L_{in}$ is the input signal inductor of the AQFP; $L_1$ and $L_2$ are the coupling inductors of the dc SQUID of the AQFP to the excitation line inductor $L_x$ and the dc offset line inductor $L_d$; $L_q$ is the output inductor of the AQFP which is coupled to $L_{out}$ to create the output signal transformer; $k_{x1}$ and $k_{x2}$ are the coupling factors of $L_x$–$L_1$ and $L_x$–$L_2$ respectively; $k_{d1}$ and $k_{d2}$ are the coupling factors of $L_d$–$L_1$ and

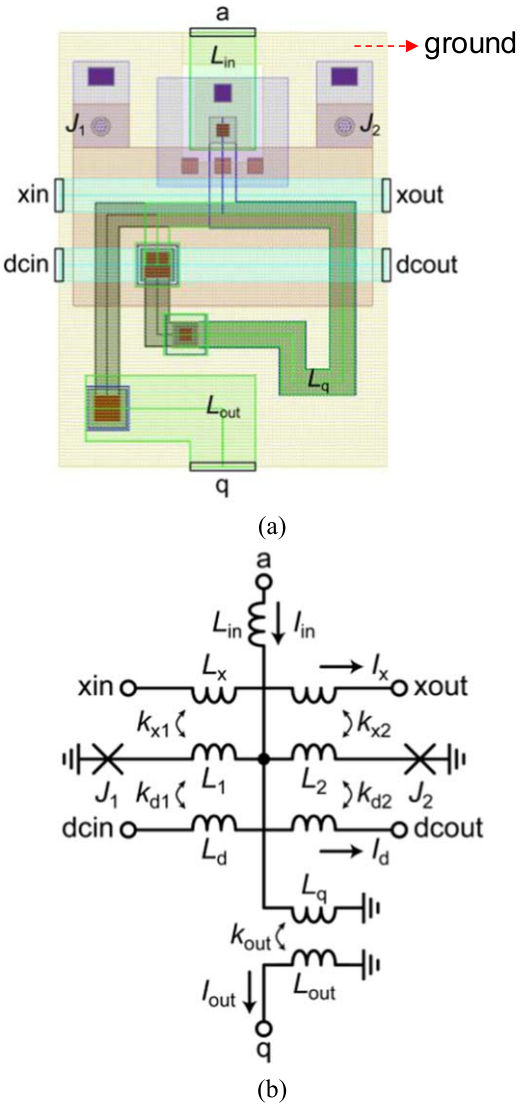



**Figure 3.** Buffer cell with underdamped JJs for MIT LL SFQ5ee process. (a) Layout, with whole size 15 $\mu$m × 20 $\mu$m. (b) Corresponding schematic. $L_{in}$ = 1.22 pH, $L_1$ = 1.42 pH, $L_2$ = 1.42 pH, $L_x$ = 5.19 pH, $L_d$ = 5.17 pH, $L_q$ = 8.27 pH, $L_{out}$ = 28.4 pH, $k_{x1} = k_{x2} = -0.22$, $k_{d1} = k_{d2} = -0.14$, $k_{out} = -0.472$, and the critical current of $J_1$ and $J_2$ is 50 $\mu$A. The parasitic couplings are: $k_{xq} = 0.0005\,34$, $k_{dq} = 0.00005\,46$, $k_{xout} = -0.002\,21$, and $k_{dout} = -0.001\,33$.

$L_d$–$L_2$ respectively; $k_{out}$ is the coupling factor of $L_{out}$-$L_q$; $k_{xq}$, $k_{dq}$, $k_{xout}$, and $k_{dout}$ are the parasitic couplings of $L_x$–$L_q$, $L_d$–$L_q$, $L_x$–$L_{out}$, and $L_d$–$L_{out}$ respectively. Ports $a$ and $q$ are respectively the signal input and output of the AQFP. Ports xin and xout are bidirectional ports of the ac excitation clock. Ports dcin and dcout are bidirectional ports of the dc offset. The principle operation of the AQFP is described in detail in [11, 17, 22]. Due to relatively strong intrinsic damping of the SFQ5ee process [20], the junctions $J_1$ and $J_2$ are underdamped without shunt resistors to achieve extremely low energy consumption [14]. It is observed that the coupling coefficient $k_{out}$ between $L_q$ and $L_{out}$ reaches −0.472 in this

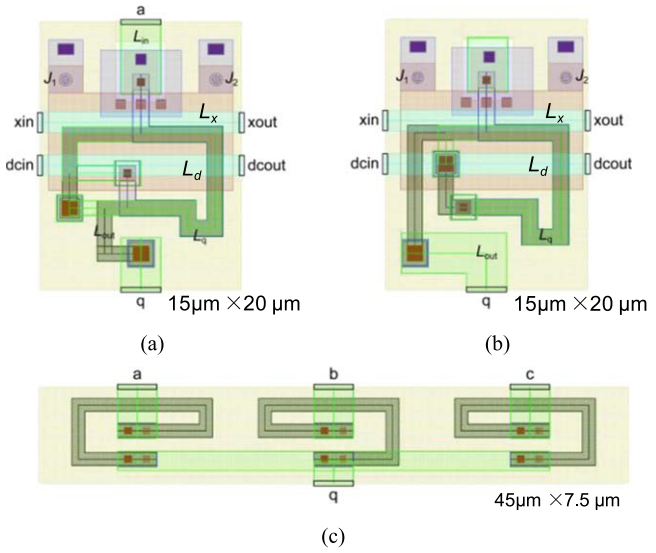



**Figure 4.** Layout of sub-cells. (a) Inverter. (b) Constant. (c) 1-to-3 branch. Inverter and constant are designed based on buffer, with the same size of 15 $\mu$m × 20 $\mu$m. Branch is a branch of inductors with a size of 45 $\mu$m × 7.5 $\mu$m.

work, which is an improvement over [16]. This implies a

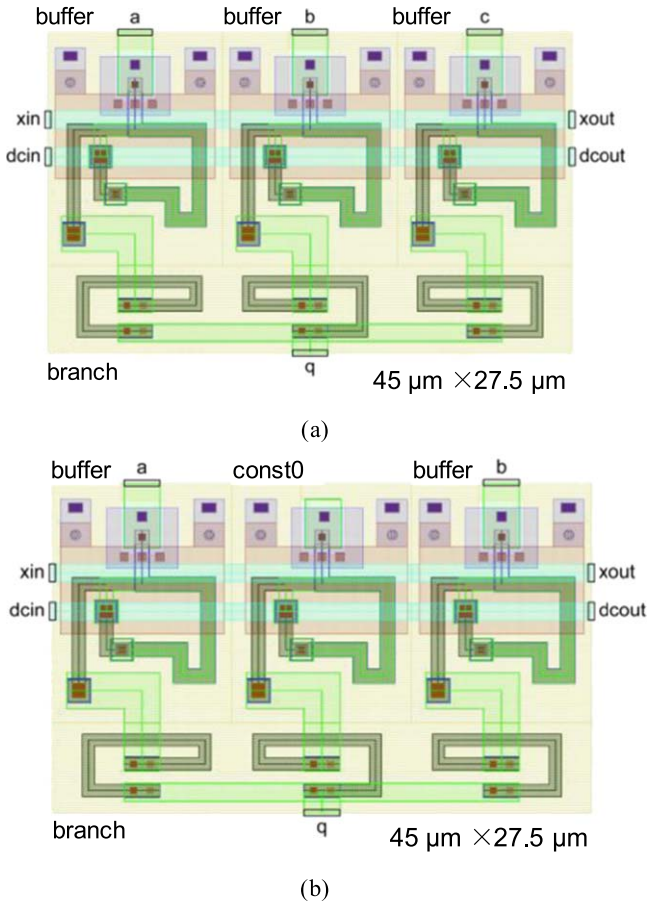



**Figure 5.** Layout of some Boolean logic cells. (a) MAJ3_ppp. (b) AND2_pp. Both gates occupy a size of 45 $\mu$m × 27.5 $\mu$m. The other majority, AND, OR, and splitter gates can be designed by re-arranging the sub-cells appropriately.

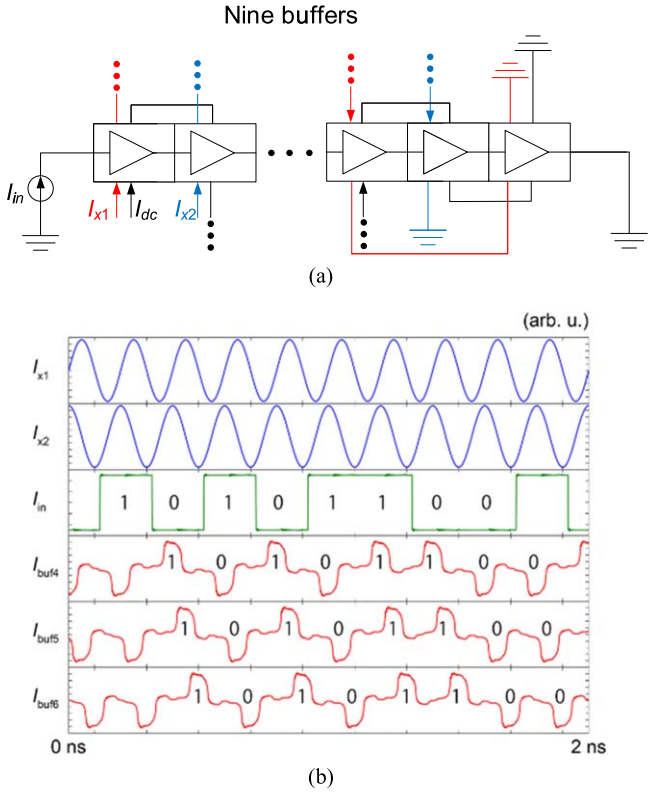



**Figure 6.** Simulation of a buffer chain. (a) Schematic. Nine AQFP buffers are connected in series. (b) Transient analysis at 5 GHz operating frequency.

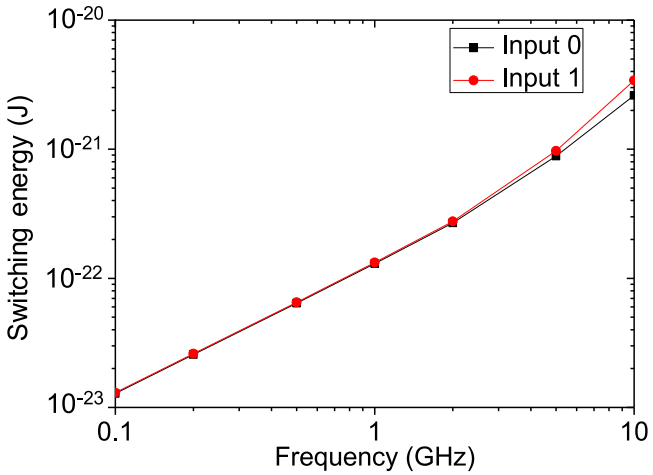



**Figure 7.** Simulation results of the energy dissipation of an AQFP buffer for the MIT LL SFQ5ee process.

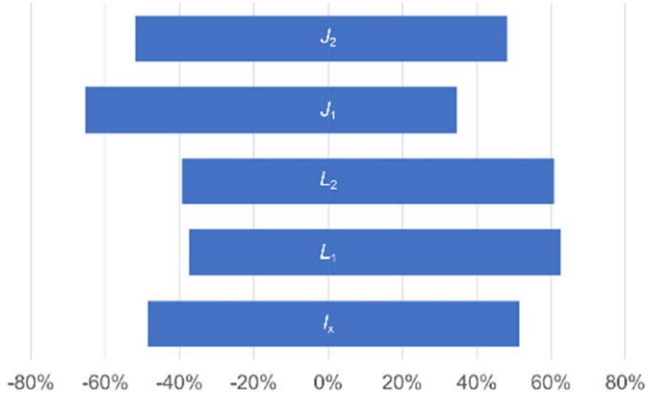



**Figure 8.** Simulation results of the parameter margins of an AQFP buffer for the MIT LL SFQ5ee process.

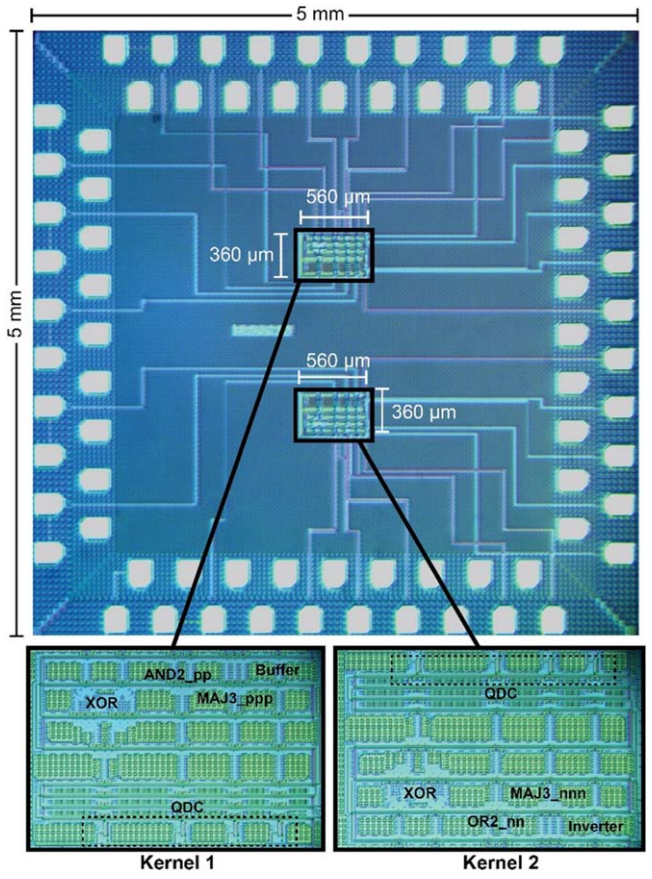



**Figure 9.** Micrographs of the 5 mm × 5 mm chip fabricated using SFQ5ee at MIT LL. Kernel 1 (left inset) and kernel 2 (right inset) both have an area of 560 $\mu$m × 360 $\mu$m (length × width).

higher output signal current amplitude between AQFP gates and thus a larger maximum wiring length under the SFQ5ee process. The values of the parasitic couplings between excitation current and the signal transformer are also provided in the caption. These parasitic couplings appear because of the aforementioned asymmetrical construction of the signal transformer. However, the values of parasitic couplings are quite small since a ground plane [20] is implemented between the dc SQUID and the signal transformer. The influence of the parasitic couplings will be considered by numerical simulations, including the estimation of operating margins and energy dissipation in the next section.

According to the minimalist design approach [16], other sub-cells such as inverter, constant, and branch are prepared based on the buffer cell, as shown in figure 4. Note that all these sub-cells occupy a significantly reduced area when compared with [16, 17]. Thereafter, Boolean logic cells are obtained by arraying the sub-cells together, some of which are shown in figure 5.

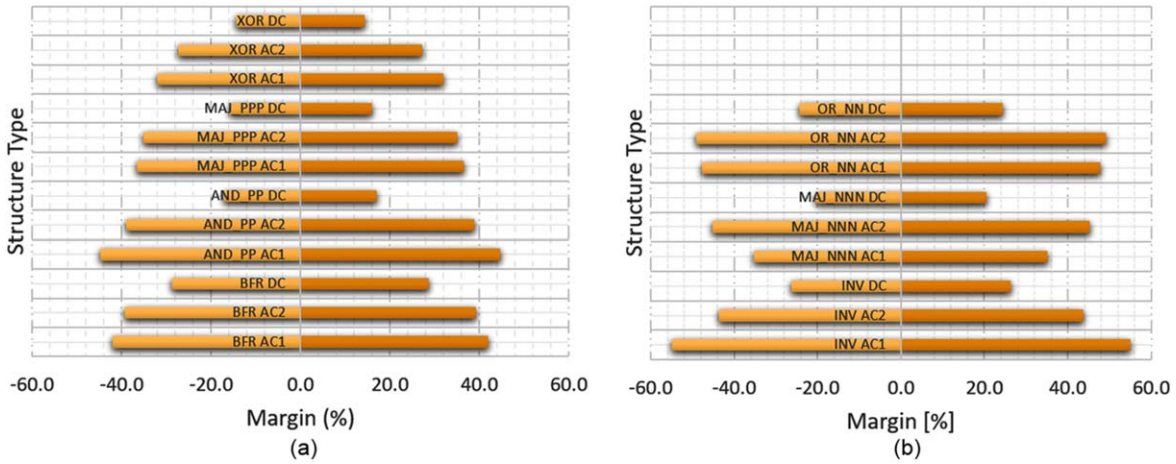



**Figure 10.** Measured excitation margins for ac biases AC1/AC2 and dc offset for kernel 1 (a) and kernel 2 (b). The margins shown here are averaged across all working test structures as indicated in table 1. Non-working test structures are not included in the average. The XOR of kernel 2 was not connected on-chip due to a lack of available pads.

**Table 1.** Summary of the measurement results of all the circuits-under-test (CUTs) on each of the six copies of the chip shown in figure 9. The status of 'working' indicates that the correct output pattern was obtained. A 'non-working' status indicates that the CUT failed to correctly operate after three defluxing attempts.

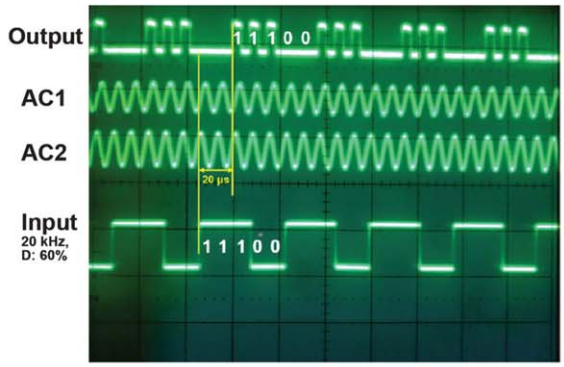
| | Kernel 1 | | | | Kernel 2 | | | |
|---|---|---|---|---|---|---|---|---|
| CUT | BFR | AND2_pp | MAJ3_ppp | XOR | INV | MAJ3_nnn | OR2_nn | Total working CUTs per chip |
| Chip 1 (B7) | Working | Non-working | Working | Non-working | Working | Working | Working | 5/7 |
| Chip 2 (D7) | Working | Working | Working | Working | Working | Working | Working | 7/7 |
| Chip 3 (C7) | Working | Working | Non-working | Working | Working | Working | Working | 6/7 |
| Chip 4 (C4) | Working | Working | Working | Working | Working | Working | Working | 7/7 |
| Chip 5 (C5) | Working | Non-working | Non-working | Non-working | Non-working | Non-working | Working | 2/7 |
| Chip 6 (D5) | Working | Working | Working | Working | Working | Working | Working | 7/7 |
| No. of chips where CUT worked | 6/6 | 4/6 | 4/6 | 4/6 | 5/6 | 5/6 | 6/6 | |

## 3. Numerical simulation

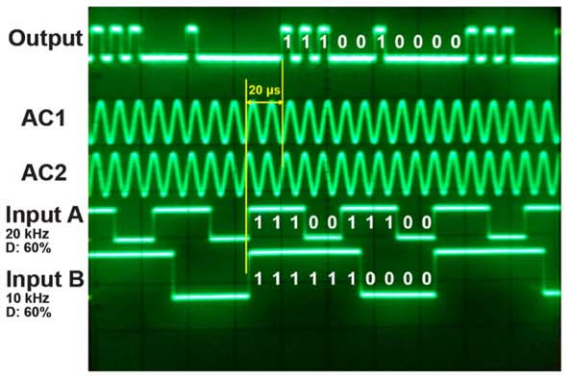
To evaluate the established cell library, we first simulate a 9-stage buffer chain using JSIM [24] to show that the proposed AQFP buffer can work correctly at GHz-range operating frequencies. Figure 6(a) shows the schematic for the simulation: nine AQFP buffers are connected in series, where each buffer has the circuit parameters shown in the caption of figure 3. The transient analysis results of the buffer chain are then given in figure 6(b), where $I_{x1}$ and $I_{x2}$ are the excitation currents, $I_{in}$ is the input current, and $I_{buf4}$, $I_{buf5}$, $I_{buf6}$ are the output currents of the fourth, fifth, and sixth buffers, respectively. Note that the input sequence 10101100 generated by $I_{in}$ propagates correctly in the buffer chain, which indicates that the proposed AQFP buffer can operate even with small parasitic couplings.

The energy dissipation of the buffer, given by integrating the product of excitation current $I_x$ and the voltage across $L_x$ over time [25], is then verified using JSIM as well. In figure 7, the simulation results of switching energy (energy dissipation per excitation cycle) of an AQFP buffer are shown for an input of 0 and 1, respectively, as a function of operating frequencies (frequencies of $I_{x1}$ and $I_{x2}$). It is noteworthy that the switching energy for an input of 0 is slightly different from that for an input of 1 because the parasitic couplings, such as $k_{xq}$ and $k_{dq}$, brings a subtle asymmetry in the operation of an AQFP buffer. However, in both cases the switching energy decreases linearly as the operating frequency decreases, indicating adiabatic operation of the AQFP buffer. Due to a large McCumber parameter [26], i.e. $\beta_C$, provided by the SFQ5ee process [20], the simulated switching energy at a 5 GHz operating frequency in this work is only 0.774 zJ (here we present the average value for input 0 and 1), giving an energy delay product of 0.155 zJ ns.

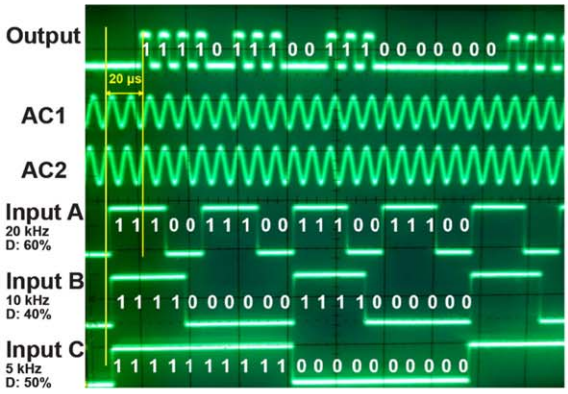
In addition, figure 8 shows the simulation results of the parameter margins of the AQFP buffer (using JSIM). The excitation current margin is approximately ±50%, which is wide enough for large-scale circuit design. The other circuit



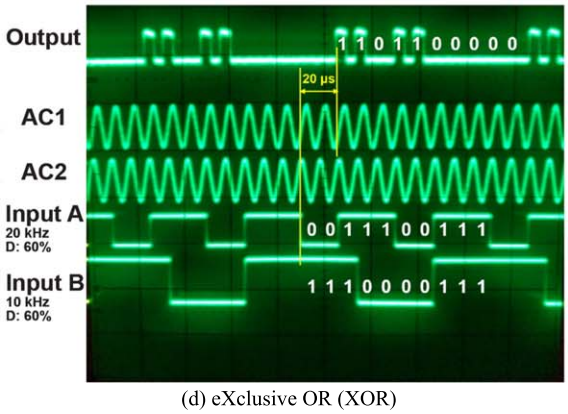

(a) Buffer (BFR)



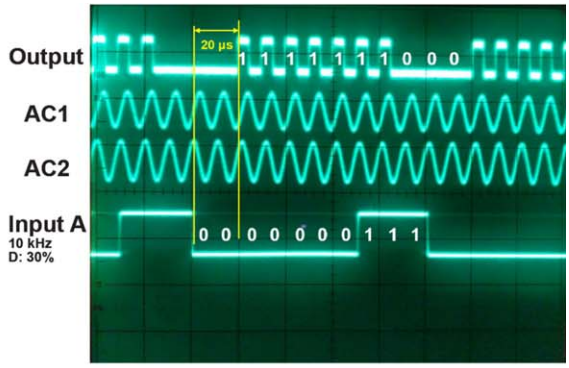

(b) AND (AND2_pp)



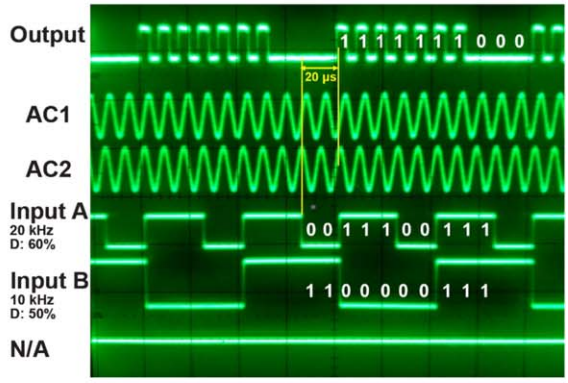

(c) Majority-3 (MAJ3_ppp)



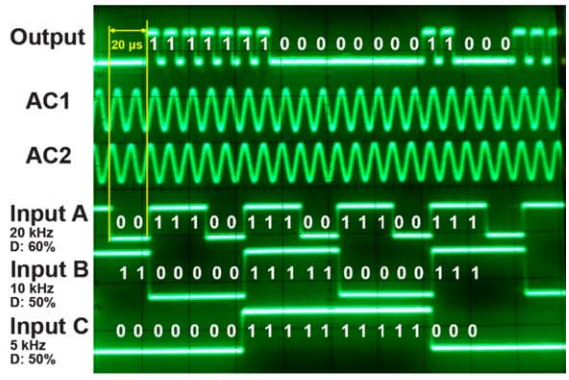

(d) eXclusive OR (XOR)




(e) Inverter (INV)




(f) NAND (OR2_nn)




(g) Minority-3 (MAJ3_nnn)

**Figure 11.** Measured waveforms for kernel 1 (a)–(d), and kernel 2 (e)–(g). AC1 and AC2 are ac-sinusoidal waveforms at 100 kHz separated by a 90° phase shift. Inputs are pulse waves at various low frequencies (5, 10, 20 kHz) and duty cycles ($D$: 30%, 40%, 50%, 60%). The output is a unipolar return-to-zero signal generated from a dc SQUID read-out. All waveforms show correct operation. The test circuits are all designed to have a 2-cycle latency on chip (20 $\mu$s at a clock frequency of 100 kHz).

parameters are also very wide, which ensures that the designed AQFP buffer works robustly even with small parasitic couplings.

## 4. Experimental results

For experimental validation, we designed a set of circuit-under-test (CUT) structures and placed them into two equal size (360 $\mu$m $\times$ 560 $\mu$m) kernels for tape-out. As shown in the micrograph of figure 9, kernel 1 encompasses the following CUTs:

- Buffer (BFR)
- 2-input AND gate (AND2_pp)
- 3-input majority gate (MAJ3_ppp)
- 2-input eXclusive OR gate (XOR), composed of two splitters, two AND2_pn cells, and one OR2_pp cell internally

Kernel 2 includes the following CUTs:

- Inverter (INV)
- 2-input NAND gate (OR2_nn)
- 3-input minority gate (MAJ3_nnn)
- 2-input XOR (left unconnected due to lack of pads)

Although most of the logic cells being tested have a latency of one clock phase (1/4 of the clock cycle in 4-phase clocking), all the designed CUTs have additional data buffering and an output dc SQUID for off-chip readout (QFP/DC converter: QDC). This resulted in a 2-cycle latency that we should expect in our experimental results for all the designed CUTs.

The test setup involves the use of a 2-channel arbitrary function generator to generate AC1 ($I_{x1}$) and AC2 ($I_{x2}$) sinusoidal excitation clocks with 100 kHz frequency and 1000 $mV_{pp}$ with a 20 dB 50 $\Omega$ attenuator before entering the chip. With a 100 kHz excitation clock, we expect a 20 $\mu$s latency for each CUT. One dc current source provides ~1.5 mA dc offset for the excitation clock, and another provides a dc bias of 1.20 mA (0.120 mA after a 20 dB attenuator) for the dc SQUID readout interface. The readout interface generates unipolar return-to-zero output signals. Another arbitrary function generator is used to create pulse waves for the data inputs at various low frequencies (5, 10, 20 kHz), and duty cycles ($D$: 30%, 40%, 50%, 60%) with an amplitude of 8 $mV_{pp}$ (16 $\mu A_{pp}$ after a 20 dB 50 $\Omega$ attenuator). The output signal is captured by an analog differential oscilloscope. All equipment is synced by a master trigger.

We first measured two chips using an immersion probe lowered into a liquid He Dewar inside an RF shielded room. This gave us a controlled testing environment while we debug the experimental setup. After confirming the successful operation of the CUTs and performing preliminary measurement of cell excitation margins, we moved on to testing several chips using an integrated cryogenic electronic test-bed (ICE-T) [27]. Two inserts, each housing three individually wired chips, were cooled simultaneously in the ICE-T. A summary of the multi-chip test result is shown in table 1 with excitation margins shown in figure 10. Furthermore, an example of the measured waveforms of correctly operating CUTs for both kernels are shown in figure 11 with the expected 2-cycle latency.

We have successfully demonstrated all CUTs working on multiple chips (3 out of 6). CUTs denoted as non-working failed to show the correct output after three defluxing attempts. In our preliminary setup in immersed liquid He, we occasionally encountered disconnects between the probe and the chip pads which required re-seating the chip. This could be one reason why some CUTs failed to work on some chips and worked on other chips.

With respect to the excitation margins, we measured the average margins of AC1, AC2, and the dc offset across all working test structures in figure 10. Non-working CUTs were not included in this average. The margins are measured by varying the amplitudes of AC1, AC2, and the dc offset until the output waveforms become unstable. AC1/AC2 are fixed to 1000 $mV_{pp}$ when they are not being varied, whereas the dc offset is fixed to 1.5 mA when it is not being varied. The dc bias of the dc SQUID is always fixed to 1.20 mA (0.120 mA after 20 dB attenuation). The excitation margins are sufficiently wide for large-scale circuit design ranging from $\pm$30% to $\pm$55% for the ac excitation clocks.

## 5. Conclusion

In conclusion, we have developed the first AQFP cell library that exploits the use of an advanced 8-metal layer 100 $\mu A\,\mu m^{-2}$ SFQ5ee superconductor electronics process provided by MIT LL to achieve approximately a 70% area reduction when compared with current AQFP cell designs. This is done by separating the dc SQUID of the AQFP and the signal transformer into different layers separated by the ground plane so that the two structures can safely overlap vertically. We built up the library by focusing on the optimization of AQFP sub-cells which are then used to easily create a rich set of Boolean logic gates. We confirmed the operation of the cell library numerically and we demonstrated fully operational circuits including three full chips. These chips consisted of test structures composed of all the sub-cells used throughout the AQFP cell library. The measured excitation margins were also wide indicating their suitability for large-scale circuit implementation.

Moving forward we plan to assess how the reduced area at the cell level affects the overall area of larger circuits. Furthermore, AQFP-RSFQ interfaces implemented in the SFQ5ee process are under development to interface with high-speed RSFQ logic and RSFQ-based output interfacing circuits for high-frequency testing and novel hybrid-logic systems.

## Acknowledgments

This research is supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research

Projects Activity (IARPA) via the US Army Research Office grant W911NF-17-9-00001. Chips have been fabricated by the MIT Lincoln Laboratory via the SFQ5ee process.

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