Performance Analyses of Planar Schottky Barrier MOSFETs with Dual Silicide Layers at Source/Drain on Bulk Substrates and Material Studies of $ErSi_x/CoSi_2/Si$ Stack Interface *

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A dual silicide layer structure is proposed for Schottky barrier metal-oxide-semiconductor field effect transistors (MOSFETs) on bulk substrates. The source/drain regions are designed to be composed with dual stacked silicide layers, forming different barrier heights to silicon channel. Performance comparisons between the dual barrier structure and the single barrier structure are carried out with numerical simulations. It is found that the dual barrier structure has significant advantages over the single barrier structure because the drive current and leakage current of the dual barrier structure can be modulated. Furthermore, the dual barrier structure's performance is nearly insensitive to the total silicide thickness, which can relax the fabrication requirements and even make an SOI substrate unnecessary for planar device design. The formation of $ErSi_x/CoSi_2$ stacked multilayers has been proved by experiments.

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With the scaling down of device feature size, we are facing serious performance problems, such as short channel effects (SCEs) and quantum size effects. Plenty of devices have been designed to overcome such problems. Among them, Schottky-barrier metal-oxide-semiconductor field effect transistors (SB-MOSFETs) are considered as alternative structures.[1−5] SB-MOSFETs can be applied for different channel structures, such as ultra-thin-body (UTB) channel for planar devices,[6−8] fin-like channel for multiple-gate devices,[9−11] nanowire channel for gate-all-around devices.[12,13] Planar SB-MOSFETs always exhibit the simplest structure design and fabrication process. Previously, we proposed the dual barrier SB-MOSFETs (DBFETs) on silicon-on-insulator (SOI) substrates for the planar cases,[14] also discussed on their possible applications in Ge-based devices.[15] In this Letter, we expand the application of DBFETs on bulk substrates, which plays an important role for heating radiation. The working mechanisms and electrical properties of DBFETs on bulk substrates are focused firstly, the impact factors of physical parameters on performance are analyzed in detail. Furthermore, we also conduct the material experiment to demonstrate the feasibility of double silicide layers. The material analysis of the dual silicide layers is carried out by x-ray diffraction (XRD), transmission electron microscopy (TEM) and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) measurements.

Schematic structures of the conventional single barrier SB-MOSFETs (SBFETs) on a UTB substrate and DBFETs on a bulk substrate are illustrated in Figs. 1(a) and 1(b) respectively. In our design of DBFETs, source/drain regions are composed of dual stacked heterogeneous silicide layers, and the channel body is tied to the bulk substrate directly. The performance comparisons between SBFETs and DBFETs have first been carried out by numerical simulations. This simulation mainly focuses on n-type channel DBFETs on bulk substrates. The major parameters and their default values for the simulations are listed in Table 1. For both SBFETs and DBFETs, the physical gate length $L_g = 16$ nm, and the equivalent gate oxide thickness $d_{ox} = 1$ nm. We use abrupt source/drain profiles in the simulation, so the gate length always equals the channel length. We apply low barrier height for the top contact, $SBH_t = 0.2$ eV, (e.g., $ErSi_{1.7}$ with 0.28 eV for electron),[16,17] and high barrier for the bottom contact, $SBH_b = 0.6$ eV, (e.g., $CoSi_2$ with 0.64 eV for electron).[18] For SBFETs, the silicon channel thickness d_{si} is much thinner than d_{tot}, and the barrier height at source/drain contact equals SBH_t. The supply voltage V_{dd} is set to be 0.5 V. The default gate work function is 4.18 eV, and work function engineering is also used for studying the influence of barrier height.[19]

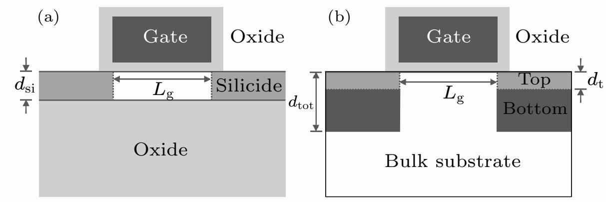

Fig. 1. Schematic structures of (a) UTB SBFETs and (b) DBFETs on a bulk substrate.

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Table 1. Major parameter range and value. SBH_t: barrier height for the top layer, SBH_b: barrier height for the bottom layer, SBH: Barrier height for SBFETs, d_{ox}: equivalent gate oxide thickness.

Parameter description	Data range	Default value
Gate length L_g	16 nm	16 nm
d_{ox}	1 nm	1 nm
Total silicide thickness d_{tot}	10 to 60 nm	40 nm
Top silicide thickness d_t	3 to 15 nm	3 nm
SBH_t	0.2 to 0.6 eV	0.2 eV
SBH_b	0.3 to 0.8 eV	0.6 eV
SBH	0.2 to 0.6 eV	0.2 eV
Si thickness for SBFETs, d_{si}	5 to 10 nm	

We employ the Synopsys Sentaurus TCAD tools to carry out the numerical simulation. The tools are used to solve Poisson's equation coupled with the electron/hole current continuity equation to obtain the device electrical characteristics, and to calculate the tunneling current based on the non-local WKB approximation model,[20] with the effective tunneling mass for electrons and holes being $m_{te} = 0.19m_0$ (light electrons) and $m_{th} = 0.16m_0$ (light holes), respectively.[21] The hydrodynamic model, Fermi distribution and density gradient quantization model[22,23] are also used to improve the simulation accuracy. The models and parameters applied in the TCAD tools have been clarified in Refs.[15,22].

From Fig. 2, we can see the benefits brought by the dual barrier structure. Firstly, we analyze the case of SBFETs. As shown in Fig. 2(a), the electron leakage current exists in the whole channel region of SBFETs due to thermal emission at the OFF state. As a result of quantum confinement effect, the current occurs with a distance from channel top surface. Such a phenomenon can also be seen in Fig. 2(b). At the ON state, the thickness of Schottky barrier on the source side is reduced by gate voltage, causes a large amount of electrons to tunnel through the source contact and to form the tunneling current. The tunneling current is considerably larger than the thermionic current, and becomes the main portion of the electron current. Figure 2(c) shows that the tunneling current is larger near the top region of the source-side contact (about 2 nm from the silicon surface), because the barrier is much thinner than that in the deep vertical portion of the contact. In the case of DBFETs, the leakage current mainly exists in the top region (within 3 nm from surface). The current flowing through the bottom region is significantly suppressed by the mid-gap barrier SBH_b, as if the current is limited to the top region. At ON state, electrons also tunnel from the source-side surface, as show in Fig. 2(d). Hence, the drive current of DBFETs is determined by the low SBH_t. Therefore, we can expect that the ON state current of DBFETs can reach the same level with SBFETs, considering the rather thinner channel body of SBFETs. For SBFETs, the whole drain-side contact region collects electrons, while for DBFETs, the collection region is limited to the top part due to the barrier height difference between the dual contacts. This means that the current is hardly related to the thickness of silicon, so the fabrication processing can be simplified.

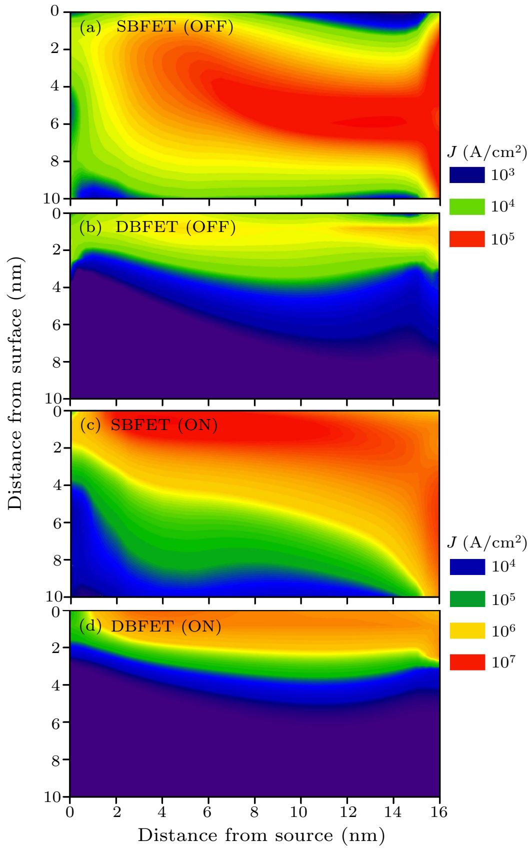

Fig. 2. Electron current density distributions along channel at the OFF state: (a) SBFETs and (b) DBFETs, and at the ON state: (c) SBFETs and (d) DBFETs.

Next, we study the influence of SBH_t and SBH_b on the performance of DBFETs. In Fig. 3(a), the relationships of I_{on} and I_{min} with SBH_t are illustrated. This valley value on the I–V curve, I_{min}, can be used to evaluate the controllability of the leakage current. The drain current is normalized for comparison, and the drain voltage $V_{ds} = V_{dd}$. We adjust the gate work function until the I_{off} equals 100 nA/µm when $V_g = 0$ V, and I_{on} is extracted when $V_{on} = V_{off} + V_{dd}$. It is found that lowering SBH_t results in a larger current because it helps to increase the tunneling current. It is also observed that I_{min} keeps almost constant when SBH_t changes, which means that I_{min} is mostly determined by SBH_b (considering the vertical depth of top contact is much thinner than that of bottom contact). As shown in Fig. 3(b), the device gets the lowest I_{min} when $SBH_b = 0.6$ eV, which can be explained by the two-type carriers conducting the mechanism in SB-MOSFETs.[24] Near mid-gap barrier height, which is half the silicon band gap (1.12 eV) at room temperature, can sufficiently suppress both electron and hole leakage current, and lead to the lowest I_{min}. It can also be seen that the normalized I_{on} (with fixed

$I_{off} = 100\,nA/\mu m$) increases with SBH_b, because the increase of SBH_b offers better subthreshold slope (SS). Thus, we can make a conclusion that I_{on} is mainly determined by SBH_t, and SBH_b exerts more effect on $I_{min}(I_{off})$ rather than I_{on}. After that, in Fig. 3(c), we show the typical I–V curves for both DBFETs and SBFETs with different SBH_t and SBH_b. Then the DBFET with $SBH_t = 0.2\,eV$ and SBH_b=0.6 eV has shown the best performance according to the above comparisons.

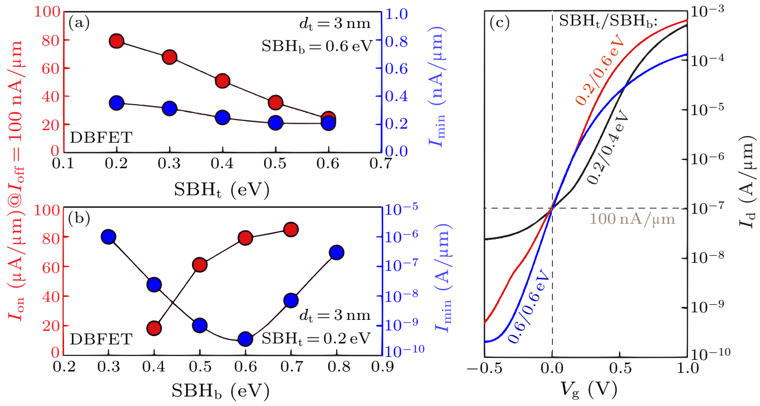

Fig. 3. (a) I_{on} (red symbols) and I_{min} (blue symbols) versus SBH_t for DBFETs with $SBH_b = 0.6\,eV$. (b) I_{on} (red symbols) and I_{min} (blue symbols) versus SBH_b for DBFETs with $SBH_t = 0.2\,eV$. (c) Typical I–V curves after work function tuning.

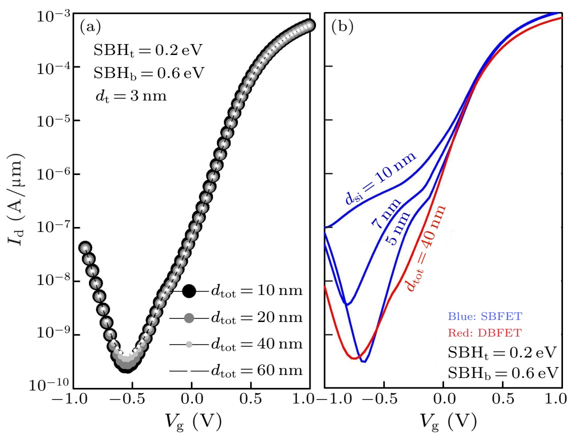

Fig. 4. (a) Transfer curves of DBFETs with d_{tot} changing from 10 to 60 nm. (b) Transfer curves of SBFETs (blue lines) and DBFETs (red lines).

In Fig. 4(a), it is found that the DBFETs' current stays almost unchanged when d_{tot} is increased, which means that the increase of the bottom region thickness will not induce too much leakage current. Thus d_{tot} as well as the channel thickness can be as large as what the manufacturing process requires. I–V comparisons between UTB SBFETs and DBFETs on bulk substrates are shown in Fig. 4(b). Here the gate work function of DBFETs is tuned to be 3.98 eV to make I_{on} of DBFETs reach the same level as those of SBFETs. For SBFETs, we can find that the OFF-state current is significantly influenced by d_{si}. To achieve $I_{off} < 100\,nA/\mu m$, d_{si} must thinner than 10 nm, which is in accordance with the necessity of the UTB substrate for SBFETs. As a control, DBFETs with channel body tied to the bulk substrate can even exhibit almost the same I_{min} as that of the SBFETs with $d_{si} = 5\,nm$, while I_{on} is still close to those of SBFETs.

Considering the significant difference between SBH_t and SBH_b, which is required for DBFETs, it is important to confirm the morphology between the grown $ErSi_x$ and the buried $CoSi_2$ layers. Herein, a verification experiment has been conducted. We use an n-type Si (100) substrate as the starting material. After removing the native oxide layer with buffered HF, 8 nm/30 nm thick Ti/Co layers were deposited subsequently by sputtering. A diffusion using rapid thermal annealing (RTA) was performed at 540℃ for 60 s followed by the removal of residual Ti and Co layers. The formation of disilicide was carried out by RTA at 850℃ for 60 s, and the resulting $CoSi_2$ layer was 80 nm thick (corresponding to sample O). Then, a 20-nm-thick poly silicon layer was deposited by LPCVD at 610℃ to prepare for the formation of $ErSi_x$. After cleaning the poly silicon surface, 8 nm/50 nm thick Ti/Er layers were deposited to ensure that the deposited poly Si can be fully consumed during the silicidation of $ErSi_x$. Lastly, RTAs at 500℃ for 5 min (corresponding to sample A) and 10 min (corresponding to sample B) were conducted for $ErSi_x$ formation respectively, and the experiment was completed by selective removal of unreacted Ti and Er.

The material structure of the grown film stacks is analyzed with x-ray diffraction measurement (Rigaku DMAX-2400). In Fig. 5, we show the XRD spectra of the three samples for comparison. The existence of $CoSi_2$ and $ErSi_x$ layer has been confirmed by the XRD spectra. For samples A and B, we can only see the peaks related to $CoSi_2$ (JCPDS No. 74-1371) and ErSi (ICSD No. 106-621), and there is no evidence showing the presence of Co–Er–Si intermixture or Co–Er mixture material. It is reported that, during the formation of $ErSi_x$, the silicon atoms are the dominant diffusing species, while the erbium atoms are even immobile.[16,25] This means that the silicon atoms diffuse into metal erbium to form $ErSi_x$ layer by layer, not vice versa. In the present experiment, the erbium layer will not connect to the $CoSi_2$ layer until silicon is exhausted. Furthermore, no titanium silicide will be formed until the erbium layer is thoroughly transformed to silicide.

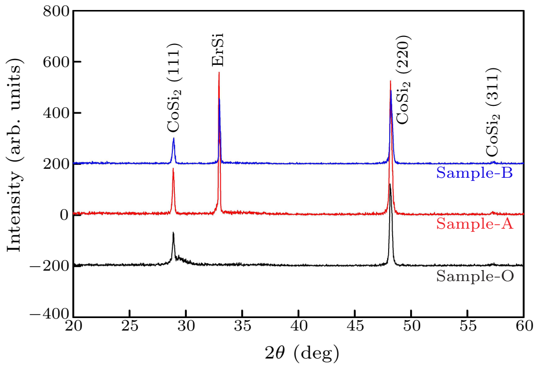

Fig. 5. XRD results of samples O, A and B. The peaks of each sample are marked with materials and orientations.

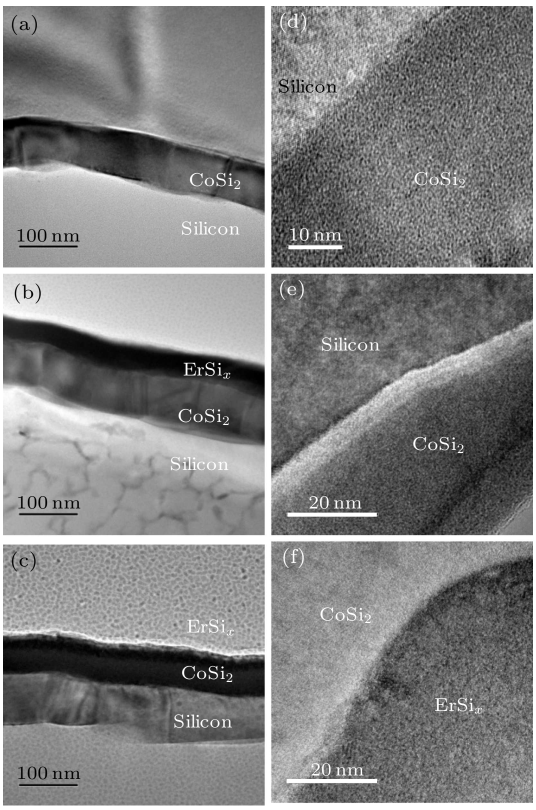

Fig. 6. TEM cross-sectional photographs of (a) sample O, (b) sample A and (c) sample B. HRTEM cross-sectional photographs of (d) sample O, (e) sample A and (f) sample B.

The cross section of grown samples' surface region is measured by TEM (Hitachi H-9000NAR) and illustrated in Fig. 6, in which we can confirm the formation of $Si/CoSi_2/ErSi_x$ stack. In Figs. 6(a) and 6(b), we show the TEM photographs of the cross sections of $Si/CoSi_2$ interfaces before and after the growth of $ErSi_x$, respectively. Comparing with the interface details in Fig. 6(a), we can see that the morphology of $CoSi_2$ in Fig. 6(b) has not changed much after the annealing for the growth of $ErSi_x$. We can also observe the significant interface between the silicon substrate and the $CoSi_2$ layer in HRTEM photographs, as shown in Figs. 6(d) and 6(e). In Figs. 6(c) and 6(f), we show the TEM and HRTEM photographs of sample B, which sustained a long time annealing. The interfaces in Fig. 6(c) are still clear and the details of the $CoSi_2/ErSi_x$ interface in Fig. 6(f) can also be identified by the textile of the $CoSi_2$ and $ErSi_x$ grains.

After that, HAADF-STEMs with EDX line-scan measurements (Philips-FEI Tecnai F30) were carried out. In Fig. 7, we show the line-scan profiles of the three samples. Figure 7(a) shows the line-scan profiles at the interface between the silicon substrate and the as-grown $CoSi_2$ monolayer in sample O. For samples A and B, the profiles of cobalt in Figs. 7(b) and 7(c) shows a monotonic degressive region for cobalt at the interface sites (a monotonic incremental region for erbium correspondingly). If there is any secondary phase or intermixing layer present at $CoSi_2/ErSi_x$ interface, the monotonic changing tendency will be changed. Considering that sample O exhibits clear interface between $CoSi_2$ and Si substrate, we have also proved the thermal stability of the $CoSi_2$. The previously reported experiment has also shown the stability of $CoSi_2$ after high temperature treatment.[16] It is reported that, with the annealing at 1000℃ and the processing time over 30 min, the thickness of $CoSi_2$ still shows little change, which implies that the $CoSi_2$ formation has weak correlation with annealing conditions.

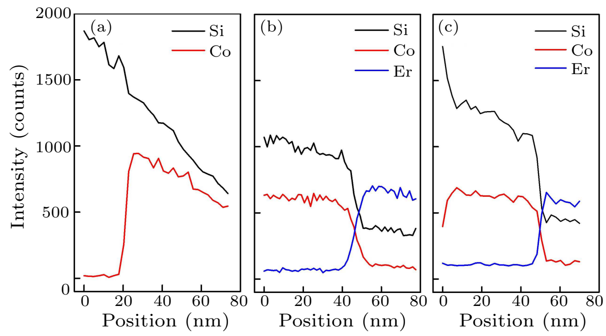

Fig. 7. HAADF-EDX line-scan profiles of (a) sample O, (b) sample A, and (c) sample B.

In summary, we have studied the dual barrier structure for SB-MOSFETs, and demonstrated the performance advantages through simulation and verified the manufacturing feasibility of the dual silicide layer formation. The results show that the dual barrier structure can exhibit better electrical properties than the single barrier structure. The use of low top barrier height improves the ON-state current, and near mid-gap bottom barrier height reduces the leakage. The minimal current of the dual barrier structure is almost insensitive to the total silicide thickness. Considering that the dual barrier structure is designed on the bulk substrate, the benefits brought by the bulk substrate can be comprehensively inherited.

References

[1] Larson J M and Snyder J P 2006 *IEEE Trans. Electron Devices* **53** 1048
[2] Larrieu G and Dubois E 2004 *IEEE Electron Device Lett.* **25** 801
[3] Connelly D et al 2006 *Appl. Phys. Lett.* **88** 012105
[4] Zhu S et al 2004 *IEEE Electron Device Lett.* **25** 565
[5] Vega R A and Liu T J K 2008 *IEEE Trans. Electron Devices* **55** 2665
[6] Knoch J and Appenzeller J 2002 *Appl. Phys. Lett.* **81** 3082
[7] Zhang Z et al 2008 *IEEE Electron Device Lett.* **29** 125
[8] Knoch J et al 2006 *IEEE Trans. Electron Devices* **53** 1669
[9] Tsui B Y and Lin C P 2004 *IEEE Electron Device Lett.* **25** 430
[10] Lee T P et al 2007 *IEEE Electron Device Lett.* **28** 164
[11] Tsui B Y and Lin C P 2005 *IEEE Trans. Electron Devices* **52** 2455
[12] Tan E J et al 2008 *IEEE Electron Device Lett.* **29** 902
[13] Peng J W et al 2008 *Appl. Phys. Lett.* **93** 073503
[14] Li D et al 2007 *Chin. Phys. B* **16** 240
[15] Xu H et al 2015 *Jpn. J. Appl. Phys.* **54** 04DC13
[16] Choi J et al 2013 *ACS Appl. Mater. & Interfaces* **5** 12744
[17] Tan E J et al 2008 *IEEE Electron Device Lett.* **29** 1167
[18] Zhao Q T et al 2006 *Semicond. Sci. Technol.* **21** 157
[19] Hou Y T et al 2004 *IEEE Trans. Electron Devices* **51** 1783
[20] Matsuzawa K, Uchida K and Nishiyama A 2000 *IEEE Trans. Electron Devices* **47** 103
[21] Xiong S Y, King T J and Bokor J 2005 *IEEE Trans. Electron Devices* **52** 1859
[22] Kang Z Y et al 2009 *Semicond. Sci. Technol.* **24** 105001
[23] Wettstein A, Schenk A and Fichtner W 2001 *IEEE Trans. Electron Devices* **48** 279
[24] Zhang Y H et al 2002 *IEEE Electron Device Lett.* **23** 419
[25] Tang X et al 2003 *Solid-State Electron.* **47** 2105