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TIPS-pentacene based MIS structure using a polymer insulator: role of interface traps studied using HMDS treatment, frequency and light intensity

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Abstract

Though it is well known that the characteristics of solution-processed polymer based organic thin film transistors depend crucially on the semiconductor/polymer interface. The mechanisms of charge processes are not understood well. We show that the nature of the interface charge processes is best studied using metal-insulator-semiconductor (MIS) structure. We choose to study the model material system of TIPS-pentacene based MIS capacitor with poly-4-vinylphenol (PVP) as the gate dielectric. We investigate the nature of the interface traps through the effect of frequency, and white light on the capacitance-voltage (C-V) characteristics with and without hexamethyldisilazane (HMDS) treatment of the PVP surface. The lower threshold voltage in bare PVP devices is due to gate field enhancement with electron traps which get suppressed with HMDS treatment. The capacitance-frequency (C-f) measurements show a single slope in case of HMDS treated PVP surface while two distinct slopes are observed for the case of bare PVP surface confirming the presence of two traps in bare PVP organic semiconductor interface. The effect of white light intensities on the threshold of both treated and untreated interfaces confirm the presence of electron traps which on being trapped modify the net gate field. The observed effects are attributed to the large number of ions, such as oxygen (O_2^-) and hydroxyl ions (OH^-) which give rise to electron traps of approximate concentration $\sim 2.1 \times 10^{11}$ cm^{-2}, which can be neutralized by HMDS treatment.

Keywords: traps, MIS structure, photoresponse, capacitance-voltage measurement, TIPS-pentacene

(Some figures may appear in colour only in the online journal)

1. Introduction

Organic semiconducting materials in the form of small molecules or polymers are leading to potential applications in emerging large area electronics through devices such as organic light emitting diode (OLED), solar cell, organic thin film transistors (OTFTs) and various chemical and biological sensors [1–5]. Pentacene is one of the most studied model organic semiconductor for OTFTs as an active material due to its good air stability [6, 7] and high field-effect mobility (2 cm^2 V^{-1} s^{-1}) [8]. In order to be compatible with flexible electronics it is necessary to develop low-cost solution-process organic semiconductors so that they can be spin-coated, inkjet-printed and roll-to-roll processed over flexible substrates [9, 10]. The chemically tuned 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) is highly soluble in various solvents have attracted considerable attention due to the face-to-face stacking in crystalline form attributed for

π-orbital overlap [11, 12]. However, mechanisms of charge trapping at the semiconductor-dielectric interface is not as well-understood, and hence has been an impediment in realizing reproducible and controllable devices.

To study the mechanisms of charge process at the interface such as accumulation and depletion in organic semiconductors in various regions of applied bias, MIS structure is one the simplest and easy structure to implement and interpret [13]. Lu *et al* studied charge carrier trapping phenomena in pentacene based OTFT and MIS structure by using Si/SiO_2 as an substrate/insulator combination [14]. Jeong *et al* compare the interface trap densities in a-IGZO TFTs with SiO_X and SiN_X dielectrics using high-frequency C-V measurements [15]. Tseng *et al* illustrated the importance of overlap capacitance effect in high speed application of fully printed TIPS-pentacene OTFT [16]. Okura *et al* calculated the dielectric/semiconductor interfacial density by using C-V technique in $Si|SiO_2|$Pentacene|Gold OTFT structure [17]. Pingel *et al* have studied the hole density, conductivity, and mobility of F4TCNQ doped poly(3-hexylthiophene) by using admittance spectroscopy in a MIS sandwich structure [18]. Leong *et al* shows the memory effect in gold nanoparticles doped pentacene thin film by taking C-V and C-f measurements which confirmed that charge trapping/detrapping occurs in Au nanoparticles [19]. Therefore, MIS structure has been proven to be a reliable way of studying charge processes, though it has not been applied to polymer/organic semiconductor systems. Instead of using OTFTs, we choose to study the effect of interface traps in solution-processed polymeric MIS device. This has the advantage of avoiding complications due to charge transport and variable band-bending in the channel of an OTFT.

In this study, the nature of interface traps at semiconductor/polymer interface is investigated using threshold voltage (V_{Th}) shift of MIS C-V characteristics with signal frequency and illumination intensity. The frequency as well as light response has been demonstrated on MIS capacitor and OTFT by using solution-processed PVP as dielectric material and TIPS-pentacene as a p-type semiconductor. In order to ensure a good interface formation between dielectric and organic semiconductor, the PVP surface was treated with HMDS and compared with the bare one. We carried out capacitance-voltage (C-V) and capacitance-frequency (C-f) measurements for MIS capacitor in both HMDS treated and bare PVP surfaces. For HMDS treated PVP surface, the role of interface traps has been elucidated by HMDS treatment and change in threshold voltage due to frequency and illumination intensity.

2. Experimental details

C-V experiments have been carried out on TIPS-pentacene based MIS capacitors fabricated on ITO coated glass substrates. The ITO layer of width 1.5 mm was patterned using standard photo-lithography techniques for the gate electrode. The ITO coated glass substrate is cleaned by UV-ozone treatment for 20 min to make it hydrophilic. We used 10 wt% PVP and 5 wt% poly melamine-co-formaldehyde as a cross-linking agent (CLA) for dielectric in propylene glycol methyl ether acetate (PGMEA) as a solvent. The solution was spin coated at 3000 rpm to get 592 ± 5 nm thickness. The dielectric layer was cured at 200 °C for 1h in a vacuum of 5×10^{-6} mbar for cross linking the PVP and CLA to reduce the leakage current [20, 21]. HMDS solution is coated at 4000 rpm for 1 min on PVP surface and annealed at 100 °C for 10 min on the top of hot plate. TIPS-pentacene with 1.5 wt% solution in 1,2,3,4-tetrahydronaphthalene (tetralin) was spin coated at 1000 rpm for 1 min and cured on hot plate at 100 °C for 15 min to get 40 ± 3 nm thick as an active semiconductor layer for MIS and OTFT structures. Finally, cross gold electrode of 1.5 mm width, and 80 nm-thick was thermally deposited on top to achieve the MIS device area of 2.25 mm^2. Figure 1 shows the cross-sectional view of the MIS device structure, and chemical structures of dielectric, and active semiconductor materials. The characterization of MIS and OTFT devices were carried out using a semiconductor parameter analysis system consisting of automated source-measure unit (Keithley 2602A) for both steady-state I-V, and transient measurements. For C-V and C-f measurements we used impedance analyzer, Agilent 4294A with the capability of frequencies ranging from 40 Hz to 110 MHz. The signal amplitude was 100 mV in all cases. All devices were fabricated in clean-room environment and characterized in a vacuum ($\sim 10^{-2}$ mbar).

3. Results and discussion

Figure 2 shows the C-V characteristics of the MIS device at various frequencies. We observe that in a p-type TIPS-pentacene semiconductor (hole transport layer), capacitance decreases with increasing the applied voltage from −40 V to +25 V. The high and low capacitance values are correlated with hole accumulation and depletion at negative and positive applied bias, respectively.

In this layered structure, the total capacitance (C_T) is given by the series combination of the dielectric capacitance (C_i) and semiconductor capacitance (C_s) [22, 23]:

$$\frac{1}{C_T} = \frac{1}{C_i} + \frac{1}{C_s} \tag{1}$$

Or

$$C_T = \frac{C_i C_s}{C_i + C_s} \tag{2}$$

By fabricating MIM (ITO|PVP|Gold) structure we have shown that dielectric capacitance and leakage current for various thicknesses of PVP and optimized for the fabrication of MIS structure and OTFT devices [20]. For the fabricated MIM and MIS (ITO|PVP|TIPS-pentacene|Gold) structures, we measured $C_i = 15.44$ nF cm^{-2}, and $C_T = 13.28$ nF cm^{-2} at 10 KHz. With the help of equation (1), the semiconductor (TIPS-pentacene) capacitance is calculated as $C_s = 94.85$ nF cm^{-2}. The dielectric and semiconductor capacitance for typical devices are calculated from the following

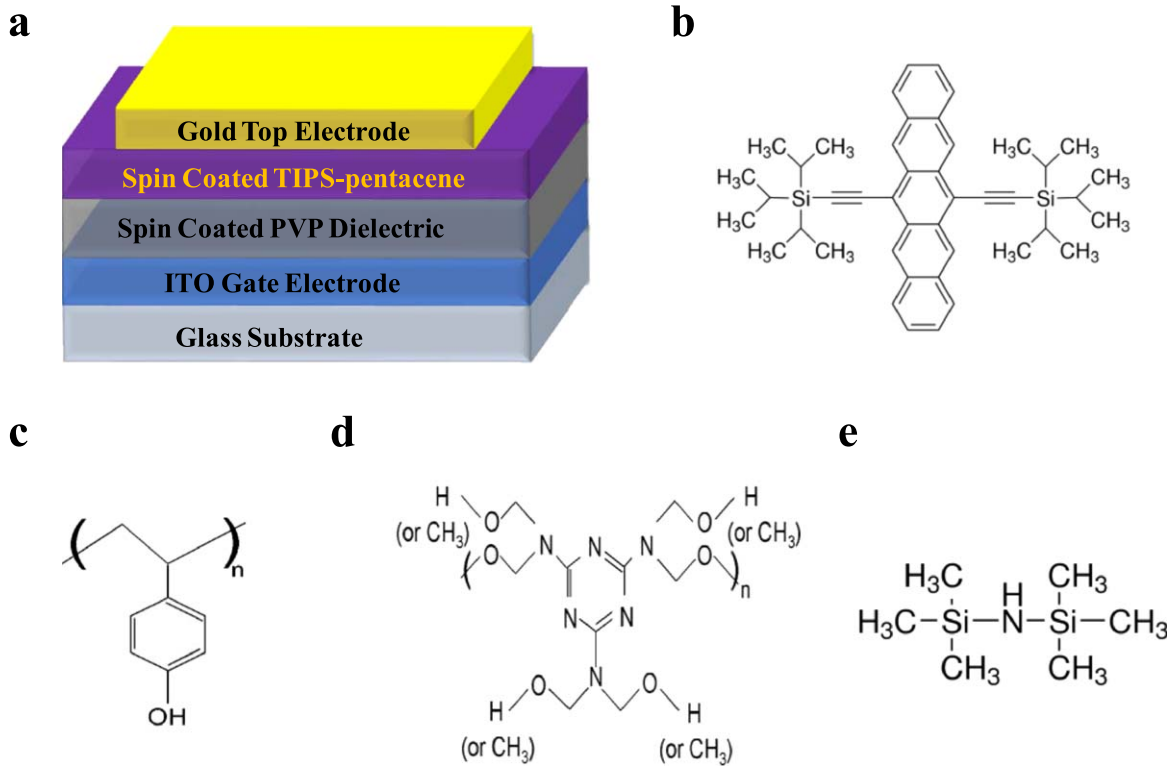

Figure 1. (a) Cross-sectional view of the MIS structure. Chemical structure of materials used in MIS device fabrication: (b) TIPS-pentacene, (c) PVP, (d) Poly melamine-co-formaldehyde (CLA), and (e) Hexamethyldisilazane (HMDS).

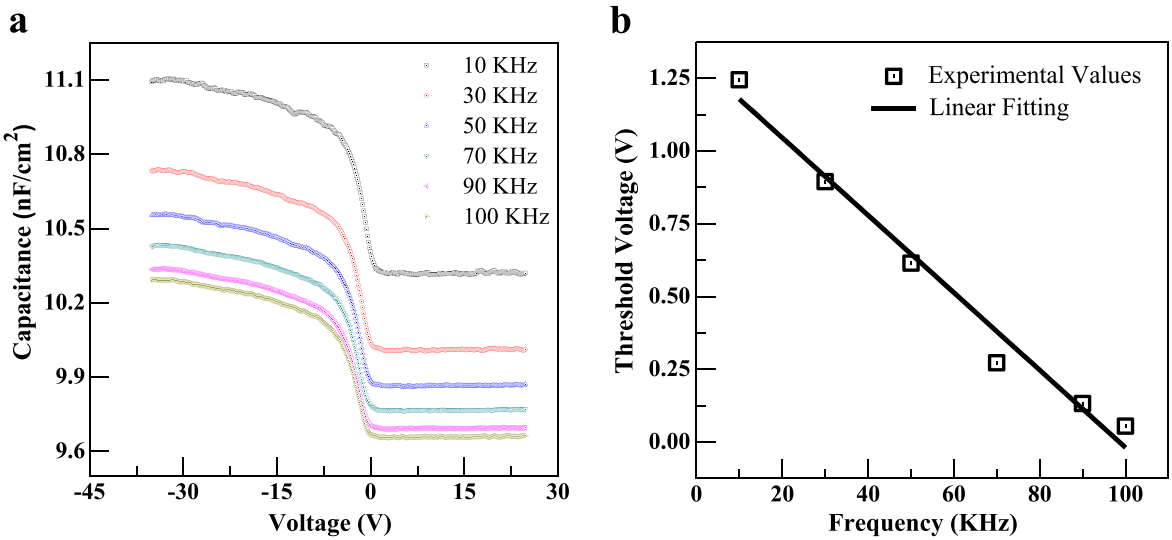

Figure 2. (a) Capacitance-voltage (C-V) characteristics of TIPS-pentacene based MIS structure (HMDS treated) at various frequencies, and (b) change in V_{Th} with frequency.

equations:

$$C_i = \varepsilon_i \frac{A_i}{d} \tag{3}$$

$$C_s = \varepsilon_s \frac{A_s}{W} \tag{4}$$

where ε_i and ε_s are the permittivity of the dielectric and semiconductor respectively, d is the dielectric thickness and w is the depletion width. A_i and A_s are overlap area for dielectric and semiconductor materials, respectively, and in our case $A_i = A_s = 2.25$ mm^2.

In figure 2(a) we observe that capacitance has high values for negative gate voltage (V_{GS}) and decreases with increasing V_{GS}. For negative V_{GS}, the accumulation of holes occurs at semiconductor surface and hence depletion width minimizes to zero in accumulation regime. As a result, the total capacitance (C_T) is close to the dielectric capacitance (C_i). On the other hand, for positive V_{GS}, the semiconductor (p-type) surface depleted and the net capacitance is given by

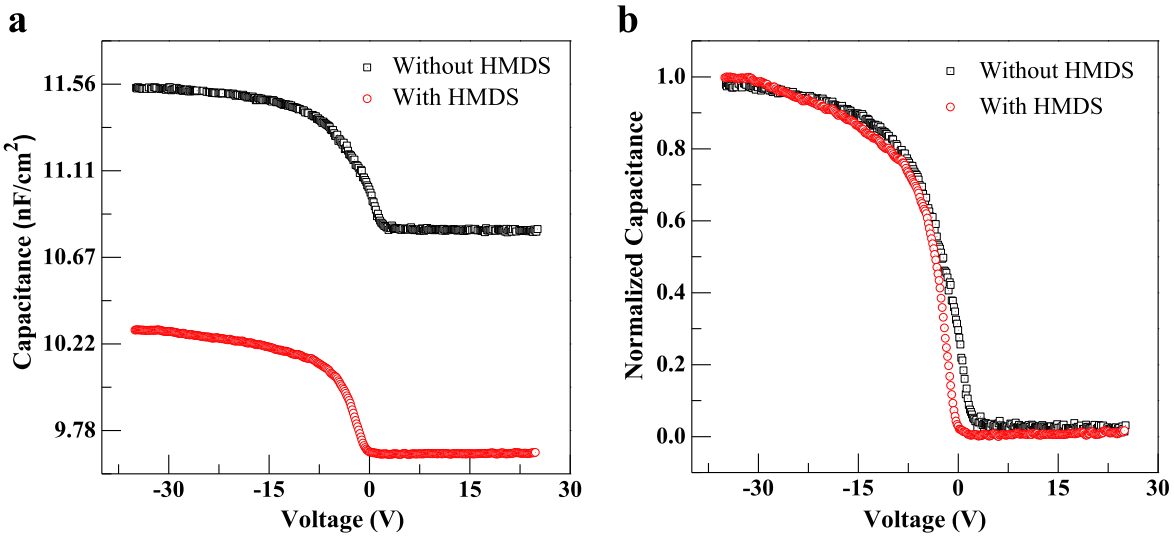

Figure 3. (a) C-V characteristics of MIS device with and without HMDS treated PVP surface at 100 KHz, and (b) normalized C-V curve corresponding to figure (a) to show the change in V_{Th}.

equation (2). Figure 2(b) shows the change in threshold voltage (V_{Th}) with different frequencies, where V_{Th} is defined as the onset voltage for charge accumulation. It linearly decreases with increasing frequency clearly implying participation of reduced concentration of interface traps with increasing frequency. At very high frequencies the charge carriers cannot change in response with V_{GS} while at lower frequencies when V_{GS} is changed very slowly, the minority charge carriers (electrons in this case) have sufficient time for trapping at dielectric-semiconductor interface. The field due to trapped electrons enhances the gate field and cause charge accumulation at lower voltage (i.e. positive V_{GS}) as compared to higher frequencies. The linear dependence is expected since threshold voltage is proportional to logarithmic of charged trap density, and the occupation density at the Fermi level is also similarly proportional to the response frequency [22].

Figure 3 shows the comparison of MIS structures in terms of C-V measurements between HMDS treated PVP surface and bare PVP surface without any treatment. High capacitance (both C_{Max} and C_{Min}) values have been observed for bare PVP surface fabricated MIS devices than HMDS treated surface without changing the net capacitance ΔC ($=C_{Max} - C_{Min}$). The higher capacitance in MIS devices for bare PVP surface is attributed to large number of electron traps at PVP/TIPS-pentacene interface due to the presence of ions such as oxygen (O_2^-) and hydroxyl ions (OH^-) created during UV-ozone treatment, which was necessary to be able to coat a uniform semiconductor film over it. A sheet of negative electron charges at the interface control the field in the channel in the entire range from depletion to accumulation region and is responsible for a proportional shift in C_{Max} and C_{Min}. The UV-ozone treatment for HMDS treated PVP surface is not required because of close matching of surface energy between HMDS and TIPS-pentacene solution. The V_{Th}, calculated from figure 3(b), for bare PVP surface (2.93 V) is larger than HMDS treated surface (0.86 V) because

Table 1. Change in physical parameters in two cases i.e. with and without HMDS treated PVP surface.

Physical Quantity	Without HMDS (Bare PVP surface)	With HMDS treatment
V_{Th} (V)	2.93	0.86
C_{Min} (nF cm^{-2}) at 100 KHz	10.81	9.66
C_{Max} (nF cm^{-2}) at 100 KHz	11.53	10.28

trapped electrons at PVP/TIPS-pentacene interface enhance the gate field while sweeping V_{GS} from positive to negative values and hence starts hole accumulation earlier than HMDS treated PVP surface fabricated MIS devices. In other words, the shift in V_{Th} can be consider as stretch-out of the C-V curve due to electron traps. The difference in threshold value (ΔV_{Th}) between treated and untreated interface would amount an interface charge concentration $\sim 2.1 \times 10^{11}$ cm^{-2}. This total trap density (N_{Trap}) for MIS structure can be calculated using the following relation [24]:

$$N_{Trap} = \frac{C_i|\Delta V_{Th}|}{q} \quad (5)$$

where C_i is dielectric capacitance and q is electronic charge. Table 1 summarizes the V_{Th}, C_{Min} and C_{Max} values for a comparison of with and without HMDS treated PVP surface at 100 KHz.

Interface electron traps are responsible for giving rise to hysteresis effect in I-V and C-V characteristics of MIS capacitor as well as OTFTs [25]. figure 4 shows the comparison in hysteresis behavior of bare and HMDS treated PVP surface for MIS capacitor. The voltage sweep direction (anticlockwise) is shown in figure 4. Voltage sweep started from accumulation (−40 V) to depletion (+20 V) in forward direction and then +20 V to −40 V in reverse direction. In the

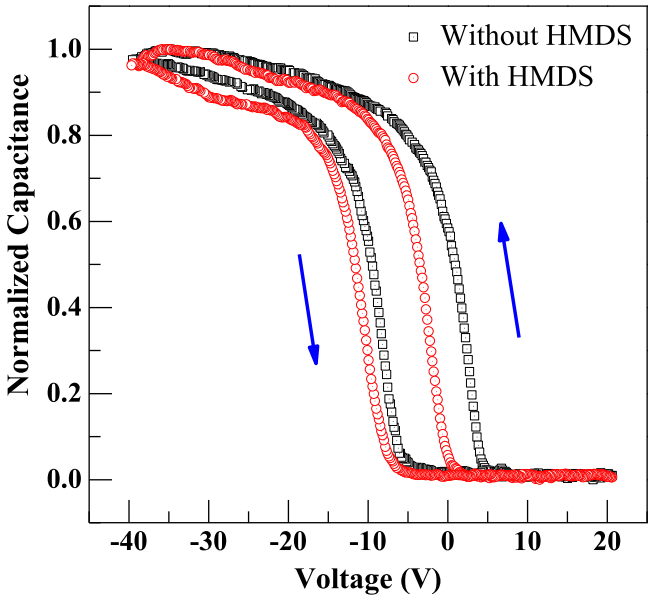

Figure 4. C-V characteristics (anti-clockwise hysteresis) in TIPS-pentacene based MIS capacitor at 100 KHz. Comparison between bare and HMDS treated PVP surfaces.

off-state (+20 V) large number of electrons get trapped at dielectric/semiconductor interface and increase the capacitance. We observe a clear shift in threshold voltage in both cases. For bare PVP surface, $\Delta V_{Th} = 10.40$ V give rise trap density of the order of 1×10^{12} cm^{-2} while for HMDS treated PVP surface, $\Delta V_{Th} = 7.58$ V correspond to trap density of the order of 7.32×10^{11} cm^{-2} using equation (5). HMDS treatment of the PVP surface help to reduce a large amount of interfacial electron trap states ($\sim 2.1 \times 10^{11}$ cm^{-2}) by suppressing the oxygen (O_2^-) and hydroxyl ions (OH^-) over bare PVP surface [26, 27]. Watson *et al* studied the photo-capacitance measurements on P3HT based MIS capacitor and achieved similar order of interface trap density [28, 29]. Wang *et al* compare OTS-treated and untreated Ta_2O_5 films for pentacene MIS capacitor and obtain a decrease in interfacial states due to OTS treatment [30].

The comparison between bare and HMDS treated PVP surface has been investigated more carefully with C-f measurements as shown in figure 5. Kim *et al* also studied, similar HMDS treatment for PVP surface [31]. High cut-off frequency in MHz range shows a good quality interface formation between HMDS and TIPS-pentacene, and suitable for all frequency applications in various electronics circuits as depicted in figure 5(a). A single slope in C-f curve in figure 5(a) is indicative of a single trap present in the bulk of the TIPS-pentacene while an additional slope in figure 5(b) with PVP/TIPS-pentacene structure confirms the presence of two traps in PVP/TIPS-pentacene MIS structure: one in the bulk of TIPS-pentacene material, and other at the PVP surface as an electron trap. These traps are corresponding to the traps identified using dynamic measurements in our previous work [32].

Another effective way of showing involvement of interface states and their study is by using light intensity as a probe. This has earlier been shown in fully OTFT structure [33]. However, MIS structure is more suited for straight forward conclusions and quantitative estimation since it avoids complications of a three terminals structure. In this series of C-V experiments, to understand the trap kinetics at various stages inside such solution-processed MIS (ITO|PVP|HMDS|TIPS-Pentacene|Gold) structures, we have shown the effect of white light by varying the intensity from dark to 275 mW cm^{-2}. It is illustrated in figure 6(a), where we observe that the capacitance for positive voltage (C_{Min}) is strongly affected with light intensity and decreases linearly with increasing light intensity as depicted in figure 6(b). The capacitance in accumulation region (C_{Max}) first increases and then saturates for higher light intensities. Since C_{Max} is corresponding to dielectric capacitance (C_i) and C_{Min} is affected with semiconductor contribution in the net capacitance as given by equation (2). C_{Min} decreases with increasing light intensity indicating recombination of charge carriers on semiconductor side of the MIS device, while C_{Max} saturated with light intensity confirmed that dielectric side has relatively less participation in charge carrier dynamics with light. The positive shift in V_{Th} with light intensity is due to electron traps at dielectric-semiconductor interface which enhances the gate field during negative sweep before recombination occurs. The linear variation of V_{Th} with light intensity is shown in figure 6(b). This feature can indeed be used as a method of light detection when suitably optimized and calibrated.

The OTFTs fabrication, I-V characteristics and white light photoresponse for OTFTs has been shown elsewhere [33]. For OTFT fabrication we used the same dielectric and semiconductor material as for MIS structure and white light photoresponse has been studied with the same white light emitting diode (LED) in a wide range of intensity varying from dark to 385 mW cm^{-2}. In OTFT structure, due to additional field with drain-source voltage (V_{DS}) the phenomenon is dominated with field emission instead of the recombination like in MIS devices.

4. Concluding remarks

In summary, we have studied the C-V and C-f measurements for MIS structure (ITO|PVP|TIPS-pentacene|Gold) with and without HMDS treatment of the PVP surface. Higher capacitance values have been observed in bare PVP surface due to large number of electron traps present at PVP/TIPS-pentacene interface attributed to oxygen (O_2^-) and hydroxyl ions (OH^-). The C-f measurements confirmed the presence of additional traps present in bare PVP surface apart from one present in the bulk of the semiconductor depicted in C-f curve of the HMDS treated MIS structure. HMDS treatment of the PVP surface help to reduce a large amount of interfacial electron trap states ($\sim 2.1 \times 10^{11}$ cm^{-2}) by suppressing the oxygen (O_2^-) and hydroxyl ions (OH^-) over bare PVP surface. The role of the interface traps is also clearly observed through variation of white light intensity which changes the threshold voltage of the C-V curve linearly, and hence can be used as a

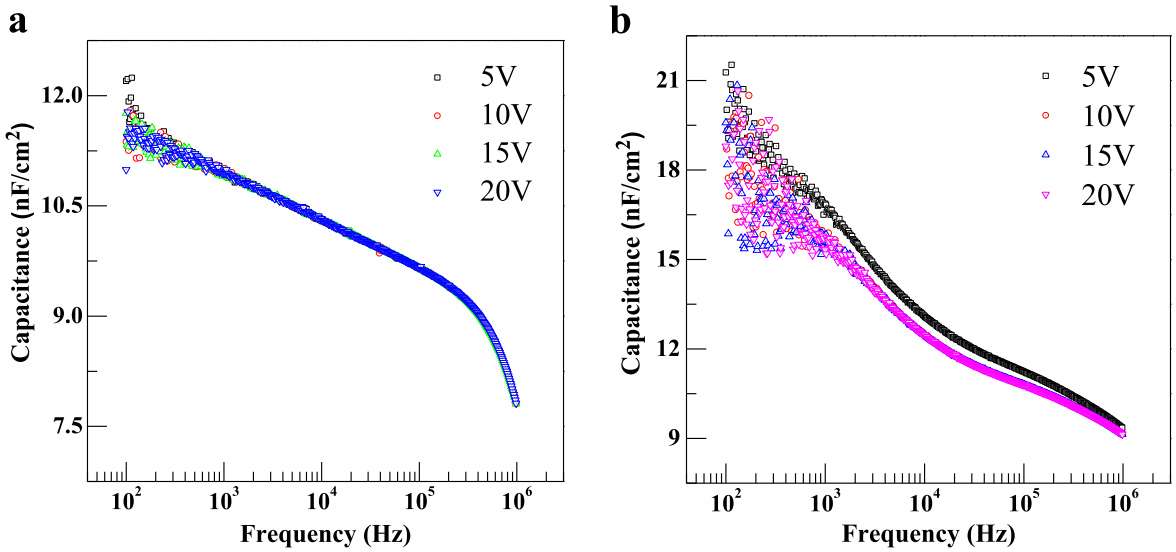

Figure 5. Capacitance-frequency (C-f) characteristics of MIS structure at different voltages, (a) with HMDS treated PVP surface, and (b) without HMDS treated PVP surface.

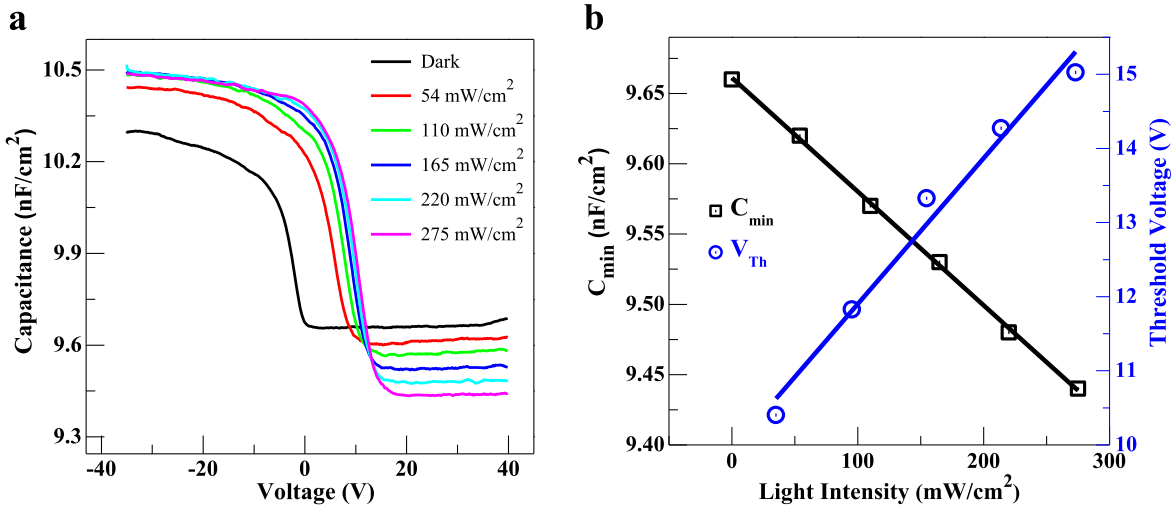

Figure 6. (a) C-V characteristics of the MIS device (HMDS treated) in dark and various white light intensities at constant 100 KHz frequency, (b) plot of C_{min}, and change in V_{Th} with light intensity.

simple method of photodetection when suitably optimized and calibrated.

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