Effect of overdrive voltage on PBTI trapping behavior in GaN MIS-HEMT with LPCVD SiN_x gate dielectric*

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The effect of high overdrive voltage on the positive bias temperature instability (PBTI) trapping behavior is investigated for GaN metal–insulator–semiconductor high electron mobility transistor (MIS-HEMT) with LPCVD-SiN_x gate dielectric. A higher overdrive voltage is more effective to accelerate the electrons trapping process, resulting in a unique trapping behavior, *i.e.*, a larger threshold voltage shift with a weaker time dependence and a weaker temperature dependence. Combining the degradation of electrical parameters with the frequency–conductance measurements, the unique trapping behavior is ascribed to the defect energy profile inside the gate dielectric changing with stress time, new interface/border traps with a broad distribution above the channel Fermi level are introduced by high overdrive voltage.

Keywords: gallium nitride, LPCVD-SiN_x MIS-HEMTs, overdrive voltage, trapping behavior

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1. Introduction

AlGaN/GaN-based metal–insulator–semiconductor high electron mobility transistor (MIS-HEMT), presenting a lower gate leakage and a larger gate bias swing than the Schottky HEMT,[1] is an excellent candidate for power switching application due to the advantages of high speed and high breakdown voltage.[2,3] However, the non-native gate dielectric will bring bulk defects and interface-states, which will lead to severe reliability issues during the fast switching. Bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), and stress-induced leakage current (SILC) are hot issues for evaluating the quality of gate dielectric.[4–6] Positive bias is often necessary to realize the fully turn-on of a MIS-HEMT. However, the long term degradation of electrical parameters during positive gate voltage stress will influence the operation condition. Therefore, an extensive investigation on the positive bias temperature instability (PBTI) is necessary.

To date, some investigations have been performed concerning the gate insulator material, the deposition method of insulator, the AlGaN barrier thickness, *etc*. Lagger *et al.* evaluated the threshold voltage (V_{th}) shift and interface trap density by adjusting the dielectric material and thickness. The capacitance–voltage (C–V) analysis revealed that the density of trapped electron depends on the dielectric capacitance and the gate bias.[7] He *et al.* compared the V_{th} instability of the fully recessed MIS-FET with that of the partially recessed MIS-HEMT. Similar PBTI behaviors were observed for both devices under the positive gate bias stress ($V_{gstress}$), but the MIS-FET presents enhanced pulse-mode stability because the fully recessed structure conduces to merging the dielectric/nitride interface with the GaN channel.[8] Generally, the channel electrons are captured by the interface traps at the dielectric/nitride interface when a positive gate bias is applied, resulting in the PBTI behavior occurring. However, the overdrive gate bias ($V_{overdrive} = V_{gstress} - V_{th}$) is relatively small in previous studies (below 10 V).[9,10] Unlike the single dielectric/GaN interface structure in MIS-FET, MIS-HEMT has multiple interfaces below gate dielectric. Therefore, a high overdrive gate bias is necessary to isolate the dielectric/nitride interface for better understanding the PBTI kinetics in GaN MIS-HEMTs.

2. Device structure and experimental details

In this work, PBTI behavior of GaN MIS-HEMT with LPCVD-SiN_x gate dielectric was evaluated under $V_{overdrive}$ = 18.5 V–25.5 V. The degradation of g_{max} and SS as a function of ΔV_{th} are used to evaluate the effect of the overdrive voltage. Besides, the interface state density before and after stress were measured by frequency dependent conductance method. The corresponding degradation kinetics of PBTI reflected by energy band diagram was exhibited based on the experimental and simulation results.

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Figure 1 shows the optical photo and the cross-section sketch of the device, which was manufactured on the standard CMOS (complementary metal–oxide–semiconductor) production line. The GaN epitaxial layer was grown by metal organic chemical vapor deposition on a 6-inch (111) Si substrate (1 inch = 2.54 cm), which consists of a 4-μm GaN buffer, a 300-nm/25-nm AlGaN/GaN heterojunction and a 2-nm GaN cap. Sandwiched between the AlGaN/GaN heterojunction is a 0.7-nm AlN interlayer.

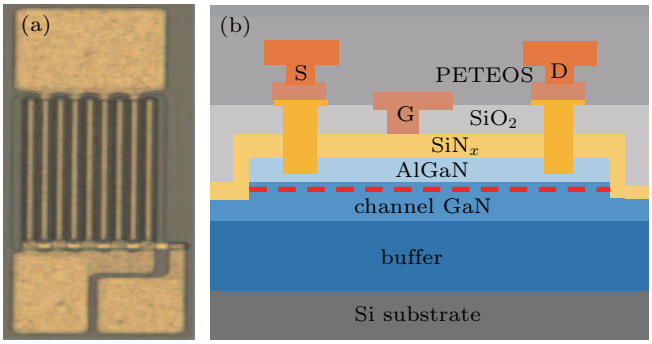

Fig. 1. (a) Micro-photograph and (b) schematic cross-section of GaN MIS-HEMT with LPCVD SiN_x dielectric.

The device process started with a 300-nm mesa etching, then a 35-nm SiN_x was deposited by low pressure chemical vapor deposition (LPCVD) as the first passivation layer as well as the gate dielectric on the top GaN, followed by a second passivation layer of 500-nm SiO_2 obtained by plasma enhanced chemical vapor deposition. Then, two 560-nm depth windows were opened by a combination of inductivity coupled plasma (ICP) dry etching and wet etching method for source and drain ohmic contact, and a 20-nm/120-nm/70-nm/60-nm Ti/Al/Ti/TiN metal was deposited by physical vapor deposition, then a rapid thermal annealing process was performed under 850 °C at N_2 environment for 45 s. Followed closely was the gate window opened and gate metal deposition process by using the TiN/Ti/Al with the thickness of 20 nm/30 nm/100 nm. The device used in this work features a dimension of $L_g/L_{gs}/L_{gd}/W_g$ at 3 μm/3.5 μm/6.5 μm/100 μm.

Before stress tests, all devices were initialized by a negative gate bias ($V_g = -1.5$ V) pre-treatment, with the source and drain grounded ($V_s = V_d = 0$ V) for 1000 s. Then the initial electrical parameters, such as threshold voltage $V_{th0} = -10.5$ V (defined at $I_d = 1$ mA/mm), maximum transconductance (g_{max0}) of 5.46 mS/mm, and subthreshold swing (SS_0) of 80 mV/dec were extracted as reference values for subsequent stress experiments (Fig. 2(a)). The aim of pretreatment is to release the electrons from the pre-existing trapping sites to realize initial stabilization. Based on the time dependent dielectric breakdown (TDDB) tests, the gate voltage for lifetime of 10 years is about 15 V as shown on the curve of the scale factor (η) of 63.2% (Fig. 2(b)). This value is regarded as a maximum gate voltage stress in the following PBTI tests.

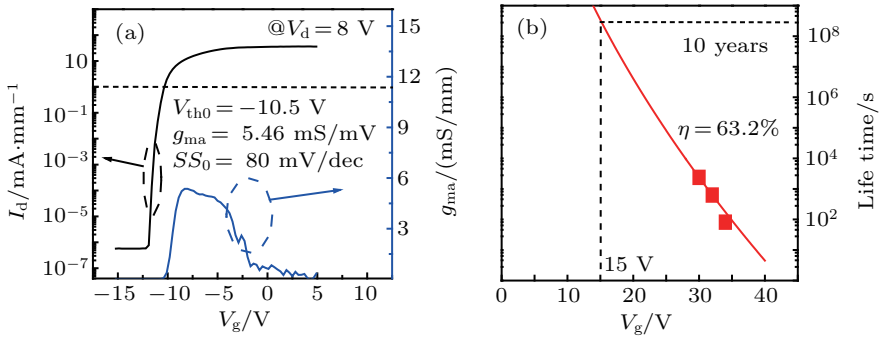

Fig. 2. (a) Transfer characteristics after a pretretment under $V_g = -1.5$ V, $V_s = V_d = 0$ V, 1000 s. (b) Before PBTI tests, an extrapolated lifetime of TDDB *versus* gate bias shows that the gate voltage on the curve of TDDB scale factor (η) of 63.2% at 10 years is about 15 V.

The PBTI test (including two segments of stress phase and recovery phase) is a static measure/stress/measure test under different values of constant gate voltage and temperature stressed. In the stress phase, devices were biased under a constant static positive gate voltage stress ($V_{gstress}$) and $V_s = V_d = 0$ V for different stress times. After every stress phase, a gate recovery voltage of −1.5 V was given immediately also with $V_s = V_d = 0$ V. During all stress phases and recovery phases, fast I_d–V_g sweeps (about 1 s–2 s) were obtained for monitoring the evolution of V_{th}, g_{max}, and SS at 10 s, 30 s, 60 s, 100 s, 300 s, 600 s, 1000 s, respectively. The gate leakage current was also recorded at each measurement, showing no obvious variation even with the maximum stress voltage $V_{gstress} = 15$ V and highest temperature of 125 °C for 1000 s (not shown).

3. Results and discussion

3.1. Influence of positive voltage stress at room temperature

This subsection focuses on the influence of positive $V_{gstress}$ on PBTI trapping behavior at room temperature. Figure 3(a) shows the semi-log curves of threshold voltage shift

($\Delta V_{\rm th}$) *versus* stress period ($t_{\rm stress}$) at $V_{\rm gstress} = 8$ V, 10 V, 12 V, and 15 V, respectively. We observe that $\Delta V_{\rm th}$ increases with $V_{\rm gstress}$ and $t_{\rm stress}$ increasing. After being stressed for 1000 s, $\Delta V_{\rm th}$ exhibits 1.3 V and 4.75 V for $V_{\rm gstress} = 8$ V and 15 V, respectively. After stress phase, all devices are immediately biased at $V_{\rm recovery} = -1.5$ V to record the $V_{\rm th}$ recovery at room temperature (Fig. 3(b)), it is difficult to recover completely even biased at $V_{\rm recovery} = -1.5$ V. Furthermore, for $V_{\rm recovery} = 0$ V, the $V_{\rm th}$ only recovers slightly after being stressed under $V_{\rm gstress} = 15$ V ($\Delta V_{\rm th} = 3.25$ V after 1000-s recovery, which is not shown here), indicating that a higher density of trap states may be introduced by high overdrive voltage.

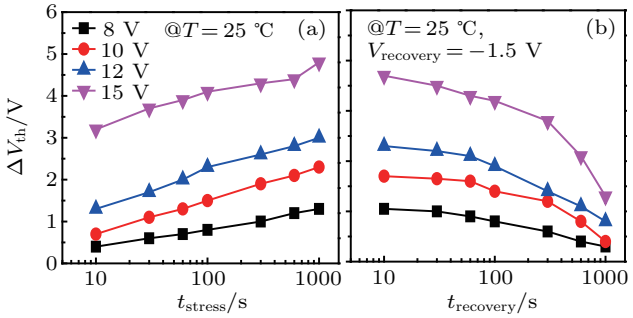

Fig. 3. Semi-log curves of (a) $\Delta V_{\rm th}$ *versus* $t_{\rm stress}$ under different gate voltage stresses at room temperature, and (b) $\Delta V_{\rm th}$ recovery at $V_{\rm recovery} = -1.5$ V.

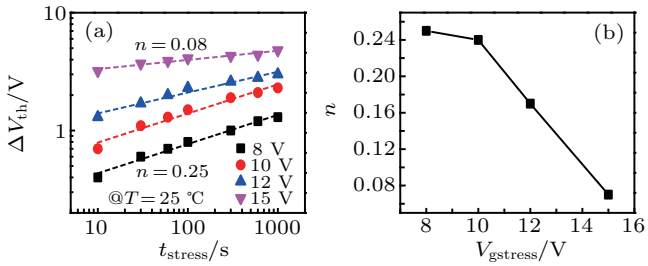

Fig. 4. (a) Log–log curve of $\Delta V_{\rm th}$ *versus* $t_{\rm stress}$ under different gate voltage stress values at room temperature, and (b) trend of time exponent n *versus* $V_{\rm gstress}$.

Further analysis of log–log curves reveals a strong power law relationship between $\Delta V_{\rm th}$ and $t_{\rm stress}$ under different overdrive voltages (Fig. 4(a)), which is consistent with the results observed in Si technology.[10] The power law semi-empirical equation of $\Delta V_{\rm th}$ can be described as[11,12]

$$\Delta V_{\rm th} = A \exp\left(\frac{E_{\rm d}}{kT}\right)\left(\frac{|V_{\rm gstress} - V_{\rm th0}|}{t_{\rm ox}}\right)^{\gamma} t_{\rm stress}^{n}, \qquad (1)$$

where A is a prefactor constant, $E_{\rm a}$ is the activation energy, k is the Boltzmann constant, T is the temperature stress, $t_{\rm ox}$ is the thickness of gate dielectric, n is the time exponent, γ is the power-law field acceleration factor. The time exponent n deduced from the slope of log–log curve decreases from 0.247 to 0.077 (Fig. 4(b)). Three sets of experiments are repeated, and thus confirming the accuracy of this trend (not shown here). The range of n values are in agreement with the typical range for GaN MIS-HEMTs by using the LPCVD-SiN_x as a gate dielectric, but the drastic decrease trend is different from the low overdrive ($V_{\rm overdrive} = 0.76$ V–4.76 V) conditions.[10] Generally, the $V_{\rm th}$ evolution is caused by the electrons trapping in the pre-existing dielectric defects. A smaller exponent n for larger overdrive voltage stress means that more accessible defects near or in the SiN_x/AlGaN interface with small trapping constant are occupied by electrons in a shorter time, thus causing a larger $\Delta V_{\rm th}$.

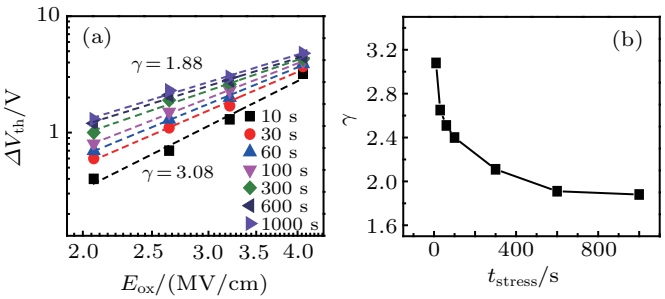

Fig. 5. (a) Power-law field acceleration γ obtained by fitting the log–log curve of $\Delta V_{\rm th}$ *versus* $E_{\rm ox}$, and (b) γ decreases from 3.08 to 1.88 with time going by.

The power-law field acceleration factor γ reflects the energy distribution and concentration of empty dielectric traps (*i.e.*, the defect energy profile) close to the Fermi level of channel,[11,13] and can be obtained by fitting the log–log curve of $\Delta V_{\rm th}$ *versus* gate dielectric field ($E_{\rm ox}$) (Fig. 5(a)). In general, $E_{\rm ox}$ is calculated by $(V_{\rm gstress} - V_{\rm th0})/t_{\rm ox}$ for the E-mode device. Whereas for the D-mode devices used in this paper, the generation of channel in the dielectric/AlGaN interface induces the second rising slope with a turn-on voltage of approximately 0.75 V in capacitance–voltage (C–V) curve (not shown here). Therefore, the $E_{\rm ox}$ is calculated by $(V_{\rm gstress} - 0.75\ {\rm V})/t_{\rm ox}$. It is found that γ exhibits a downward trend from 3.08 to 1.88 with time going by (Fig. 5(b)), which is different from low overdrive conditions in other works.[10] The decreasing of γ suggests the energy distribution of empty dielectric traps above the channel Fermi level will become wider, and the concentration of traps will become closer to the channel Fermi level. A possible reason is that the high overdrive voltage stress will introduce new accessible defects in or near the dielectric/AlGaN interface. This can be reflected by the degradation of $g_{\rm max}$ and SS, as well as the linear correlation between them and $\Delta V_{\rm th}$ as shown in Fig. 6. The function between $\Delta g_{\rm max}$ and $\Delta V_{\rm th}$ is given by[14,15]

$$g_{\rm max} = \max\left(\frac{\partial I_{\rm d,lin}}{\partial V_{\rm g}}\right) = W\mu_0 C_{\rm ox}(V_{\rm g} - V_{\rm th0})/L, \qquad (2)$$

where $I_{\rm d,lin}$ is the drain current in linear region, W/L is the ratio between channel width and length, μ_0 is the carrier mobility not affected by electrical field, and $C_{\rm ox}$ is the capacitance of gate dielectric. The decrease of $g_{\rm max}$ and the increase of SS are related to the increasing of trap density during stress.[16,17]

Electrons trapped by the pre-existing and new created interface/border traps during high overdrive voltage will enhance the Coulumb scattering, and then weaken the mobility of channel carriers. Although the linear correlation is similar, the degradation percentage is relatively small compared with the previous reports.[16,17] One possible reason is that the 25-nm-thick AlGaN barrier in our structure acts as an isolation layer between SiN_x dielectric and GaN channel.

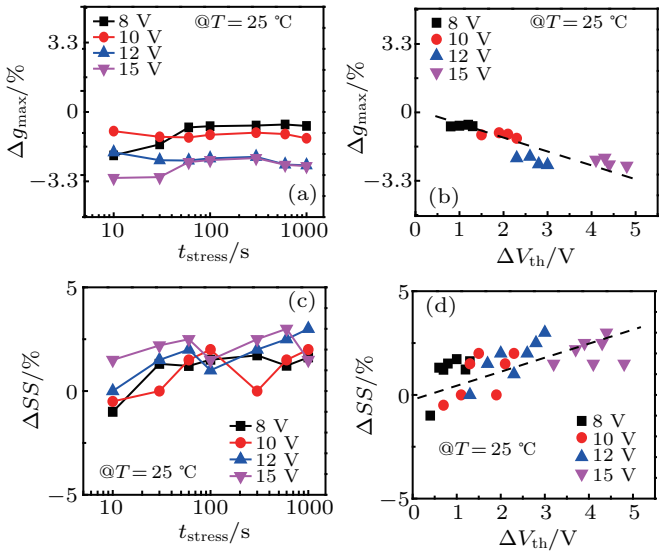

Fig. 6. (a) Plots of weak g_{max} degradation *versus* t_{stress}, observed under different values of $V_{gstress}$ and room temperature, (b) linear correlation between Δg_{max} and ΔV_{th}, (c) plots of *SS* degradation *versus* t_{stress}, and (d) correlation between ΔSS and ΔV_{th}.

3.2. Influence of temperature during high overdrive gate voltage stress

Temperature stress is another important factor which will influence the electron trapping/detrapping behavior. The influence of temperature stress under relatively moderate (8 V) and harsh gate voltage stress (15 V) are shown in Fig. 7. The threshold voltage shifts positively and increases with temperature increasing (ΔV_{th} = 1.85 V and 4.8 V for $V_{gstress}$ = 8 V and 15 V, respectively, after being stressed at 125 °C for 1000 s). Besides, the recovery rate of ΔV_{th} is also speeded up by temperature. However, ΔV_{th} becomes much smaller with temperature increasing for high gate voltage stress than that for moderate stress, indicating that temperature stress has a weaker influence on trapping process when overdrive voltage stress is higher.

Further analysis shows that under different stresses at temperature of 25 °C, 50 °C, 75 °C, and 125 °C, *n* value decreases from 0.25 to 0.07 for $V_{gstress}$ = 8 V while from 0.07 to 0.04 for $V_{gstress}$ = 15 V (Fig. 8), which is rarely observed in other reports. In this paper, ΔV_{th} = 1.2 V and 4.5 V, respectively, for $V_{gstress}$ = 8 V and 15 V are selected to extract the activation energy (E_a) *versus* corresponding t_{stress}. The values of E_a extracted by fitting the log–log Arrhenius plots (Fig. 9) are approximately 0.347 eV and 0.115 eV for $V_{gstress}$ = 8 V and 15 V, respectively. The obvious difference in E_a value between moderate and high gate voltage stress may reflect the different influences of defect energy profile inside the gate dielectric as explained in the following.

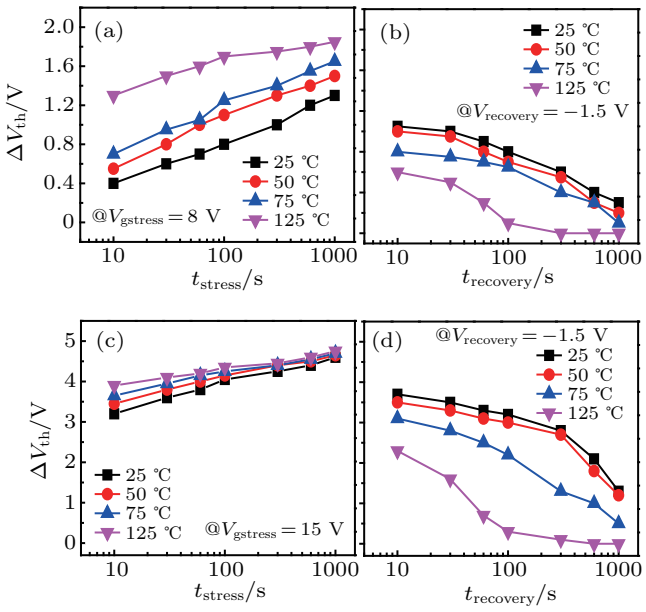

Fig. 7. (a) Shift of V_{th} at $V_{gstress}$ = 8 V, (b) recovery of V_{th} after $V_{gstress}$ = 8 V for 1000 s, (c) shift V_{th} at $V_{gstress}$ = 15 V for 1000 s, and (d) recovery of V_{th} after $V_{gstress}$ = 15 V for 1000 s.

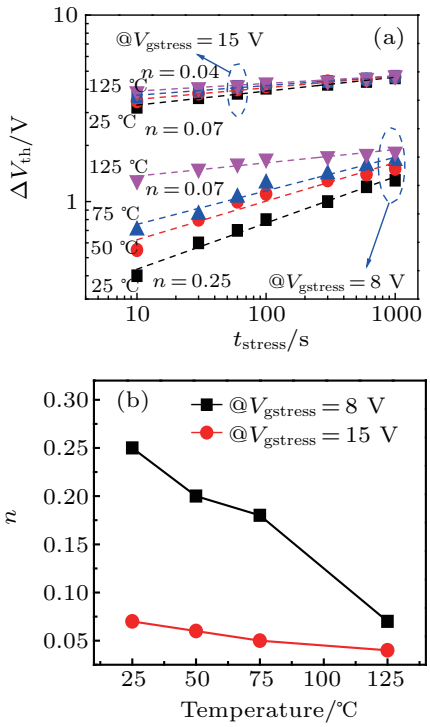

Fig. 8. (a) Log–log curves of ΔV_{th} *versus* t_{stress} at different values of temperature and $V_{gstress}$, and (b) plots of fitted *n* *versus* temperature for both $V_{gstress}$ values.

After 1000-s stress test under $V_{gstress}$ = 15 V at 25 °C, the peak value of conductance (G_p/ω) increases and is about 1.8 times higher than the initial value (Fig. 10). The density of

interface-states (Fig. 11) increases about 0.2 orders of magnitude. The frequency-dependent conductance[18] method to evaluate interface-states for D-mode MIS-HEMTs may not accurate, but the increase of G_p/ω and interface-states, induced by high overdrive voltage stress, can reflect the change of defect energy profile close to the channel Fermi level.

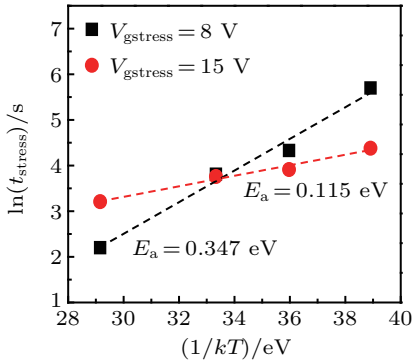

Fig. 9. Arrhenius plot of stress time needed for a fixed ΔV_{th} value for $V_{gstress}=8$ V and 15 V.

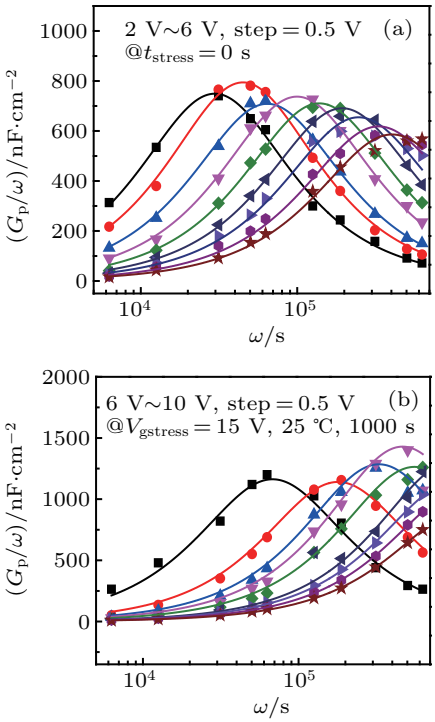

Fig. 10. Plots of G_p/ω *versus* frequency in a range from 1 kHz–100 kHZ of GaN MIS diode before (a) and after (b) 1000-s stress test under $V_{gstress}=15$ V at 25 °C.

Finally, a degradation model is proposed to illustrate the trapping behavior induced by high overdrive voltage stress. Simulation results show that the SiN_x gate dielectric becomes a main area to withstand the positive electric field from gate, AlGaN barrier close to SiN_x dielectric will form obvious electron accumulation layer (a second channel, named spill-over condition) for $V_{spill-over}=V_{gstress}>5$ V, and more obvious electron accumulation layer for higher $V_{gstress}$ (Fig. 12(a)). As proved by Lagger *et al.*, the AlGaN barrier height acts as an electron trapping rate-limiter for $V_{gstress}<V_{spill-over}$, while the density of trapped electrons scales with the number of free electrons at the insulator/dielectric interface when $V_{gstress}>V_{spill-over}$. In this work, the gate overdrive voltage (18.5 V–25.5 V) is selected under the strong spill-over condition. Therefore, the new trap states created by stress are mainly located at the insulator/barrier interface.[19] The defect energy profile changes with time, *i.e.*, the spread of empty dielectric traps above the channel Fermi level will become wider, and the concentration of which will become closer to that above the channel Fermi level (from ΔE_1 to ΔE_2), resulting in a higher trapping probability, a lower activation energy and a weaker time-dependent stress.

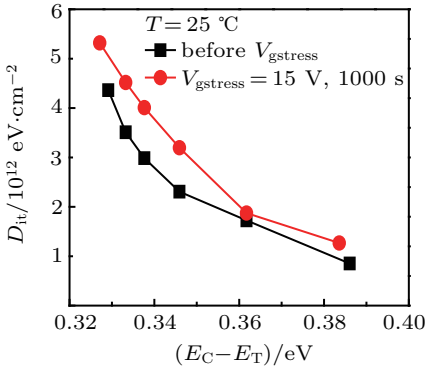

Fig. 11. Interface-states generation after 1000-s stress test under $V_{gstress}=15$ V at 25 °C.

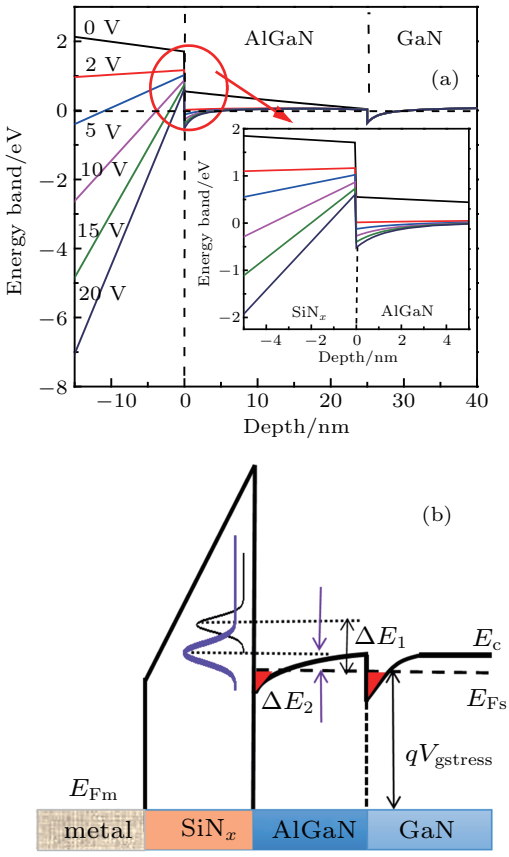

Fig. 12. (a) Simulation energy band diagram of SiN_x/AlGaN/GaN during different gate voltage stresses, and (b) variation of defect energy profile during high overdrive gate voltage stress.

4. Conclusions

In summary, a comprehensive investigation of high overdrive voltage on PBTI ctrapping behavior is presented for D-Mode GaN MIS-HEMTs with LPCVD-SiN_x gate dielectric. A higher overdrive voltage is more effective to accelerate the electron trapping process, and introduces new interface/border defects in the dielectric, thus the spread of empty dielectric traps above the channel Fermi level will become wider, and the concentration of traps will become closer to the channel Fermi level, resulting in a higher trapping probability, hence a larger $\Delta V_{\rm th}$ with a weaker time dependence and a weaker temperature dependence are observed.

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