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Micro-trench free 4H-SiC etching with improved SiC/SiO_2 selectivity using inductively coupled $SF_6/O_2/Ar$ plasma

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Abstract

SiC dry etching process for formation of a trenched-gate structure in trench metal-oxide-semiconductor field-effect-transistors employing bottom protection p-well (BPW) has been investigated. $SF_6/O_2/Ar$ based inductively-coupled-plasma reactive-ion-etching were utilized with various variations in process parameters, such as bias power, ICP power, kind of gas species, working pressure and temperature. The effects of process parameters on trench profiles were analyzed by a cross-sectional scanning electron microscope and profilometer to suppress micro trenches at a bottom corner of the trench and improve SiC/SiO_2 etch selectivity. We successfully demonstrated the micro-trench free SiC trench structure with high SiC/SiO_2 etch selectivity of 3.7 at bias power of 1 kW, ICP power of 4 kW, $SF_6/O_2/Ar$ flows of 6/6/8 sccm, working pressure of 15 mTorr and temperature of 20 °C.

Keywords: SiC, trench, etching, ICP-RIE, MOSFET

(Some figures may appear in colour only in the online journal)

1. Introduction

4H-SiC trench metal-oxide-semiconductor field-effect-transistors (TMOSFETs) have received a considerable amount of attention for next-generation high-power applications due to their wide bandgap properties, such as high critical electric-field ($E_C = 3\ MV\ cm^{-1}$) and low intrinsic carrier concentration ($n_i = 6 \times 10^{-7}\ cm^{-3}$) [1–3]. Also, absence of JFET regions and small cell-pitch of the SiC TMOSFETs make availability to reduce specific on-resistance ($R_{on,sp}$) effectively so that low static- and dynamic-loss are achievable [4–6].

Gate oxide on the JFET regions in SiC planar MOSFETs can be shielded by the depletion expanded laterally from retro-graded p-base under off-state blocking mode. Unfortunately, gate oxide at a bottom center and bottom corner of trench gate in conventional SiC TMOSFETs is not sufficiently shielded by the depletion expanded vertically from box-profile p-base so that high electric-field is crowded at gate oxide under off-state blocking mode. This electric field crowding at gate oxide may occur dielectric breakdown prior to avalanche breakdown at p-base/drift interface at active regions or edge termination regions.

During dry etching process for SiC to form the trench-gate structure, micro trenches can be created by the higher ions concentration and higher etch rate at the bottom corner of trench than those at trench center [7–10]. The micro trenches may cause reduction in breakdown voltage of SiC TMOSFETs owing to high electric-field crowding at the gate oxide near micro trenches. Although micro trenches are successfully removed by optimized etching conditions, additional structures to protect gate oxide, such as bottom protection p-well (BPW) and bottom thick-oxide, should be utilized to shield gate oxide of SiC TMOSFETs [11–15].

BPW structure has highly doped p^+ regions under trench gate so that it prevents bottom of trench gate from depletion and electric-field crowding. To form BPW under trench gate, etching mask for trench is typically used as implantation mask as well so that enough thickness of etching mask should remain after SiC etching. Forthemore, a relatively deep SiC trench is required for BPW structure to suppress the JFET

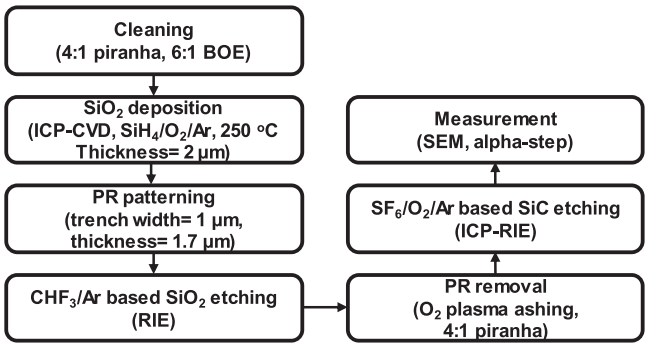

Figure 1. A schemiatic diagram of the experimental procedure.

effects caused by expansion of depletion from each p-base and BPW so that a high SiC etch selectivity over the mask layer is desirable [15].

SiC typically has a low etch-rate and a low etch selectivity over photoresist due to its strong bonding energy [10, 16, 17]. Various metalic mask materials, such as Ni, Ti/Ni, Ti/Cr, Al, ITO and SnO_2, etc, have been studied for improvement of SiC/ mask etch selectivity [7, 16–21]. However, metalic masks may raise metal-contamination concerns during the fabication processes. Besides, it is known that a few metalic masks, such as Al, bring about formation of non-volatile by-product during etching [18]. These by-product may affect SiC trench profiles.

In this paper, we used a SiO_2 etching mask for SiC etching. The SiO_2 mask makes availability to form SiO_2 spacer on the trench sidewall before removal of SiO_2 etching mask so that p^+ regions for BPW can be selectively formed on trench bottom by ion implantation. Also, we controlled various etching process parameters, such as bias power, ICP power, kind of gas species, working pressure and temperature, and analyzed their effects on the SiC trench profile. We successfully achieved micro-trench free SiC trench structures with the sufficiently high SiC/SiO_2 etching selectivity for SiC trench etching and BPW formation.

2. Fabrication procedure

A schematic diagram of the experimental procedure is shown in figure 1. We used a 100 mm n-type 4H-SiC substrate with 4°-off orienatation. After 4:1 piranha and 6:1 buffered oxide etchant (BOE) cleaning, the 2 μm thick SiO_2 etching mask was deposited at 250 °C by $SiH_4/O_2/Ar$ based inductively-coupled-plasma chemical-vapor-depositon (ICP-CVD). Then, photoresist patterns having 1 μm-width trench and thickness of 1.7 μm were formed on the SiO_2 layer. SiO_2 mask was etched by CHF_3/Ar based reactive ion etching (RIE) with high SiO_2/photoresist etch selectivity (>10) and SiO_2/SiC etch selectivity (>10) conditions. An O_2 plasma ashing process and 4:1 piranha cleaning were carried out to remove photoresist for the etched samples. Finally, SiC etching was performed by $SF_6/O_2/Ar$ based inductively-coupled-plasma reactive-ion etching (ICP-RIE). The etched depth, SiC/SiO_2 etch selectivity and SiC trench profiles were evaluated by profilometer (Alpha step) and scanning electron microscopes (SEM).

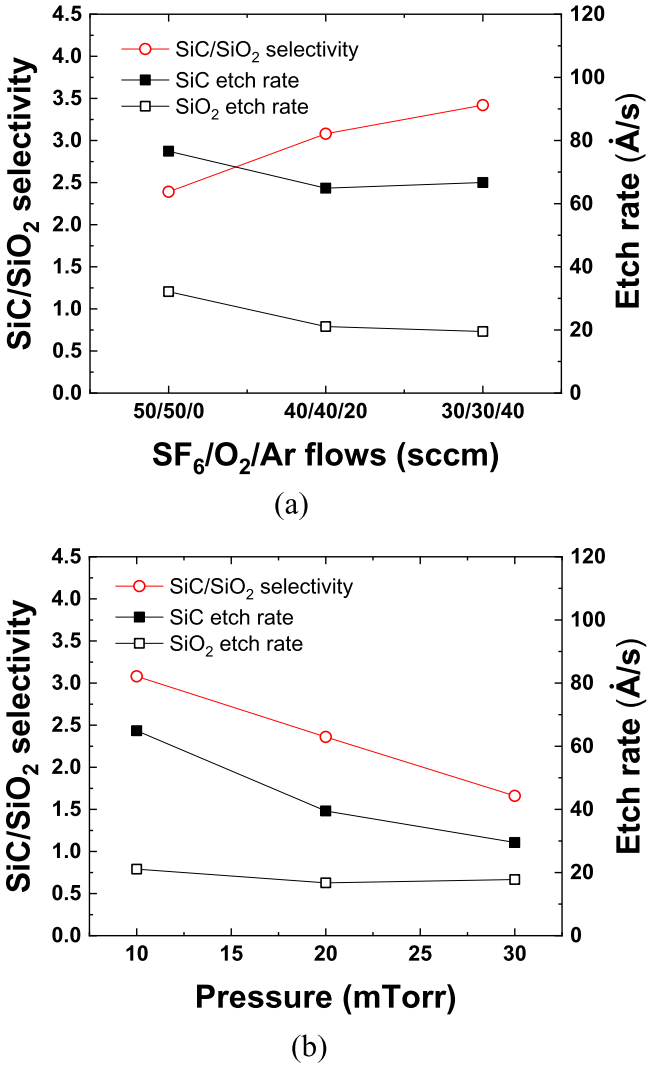

Figure 2. SiC/SiO_2 etch selectivity and each etch rate according to (a) $SF_6/O_2/Ar$ flows and (b) working pressure.

Diameter of an bottom electrode in our equipment is 340 mm and the 100 mm wide etching windows opens with donut-type quartz clamp. The temperature on bottom electrode was controlled by water circulation on the backside of the electrode. The working pressure was controlled by auto-pressure-control (APC) system and throttle valve.

3. Results and discussion

It is well known that 20 %-O_2 fraction in SF_6/O_2 mixture is typically used for etching of Si and SiC because of high etching speed [17, 18, 20–23]. However, non-volatile by-products, such as CF and CF_2 bonds, are produced on the etched surface during SiC etching with low O_2-fraction so that low angle or V-shape SiC trench profiles are created [8, 16, 22, 24]. We used identical O_2 flow to SF_6 for the efficient reaction for generation of a volatile CO by-product during the SiC etching [18, 20, 24].

Figure 2(a) shows the SiC/SiO_2 etch selectivity and each etch rates of SiC and SiO_2 according to $SF_6/O_2/Ar$ flow

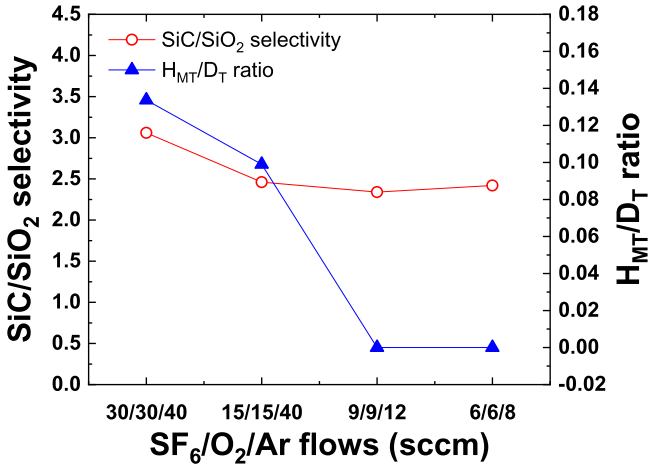

Figure 3. SiC/SiO_2 etch selectivity and H_{MT}/D_T ratio according to $SF_6/O_2/Ar$ flows.

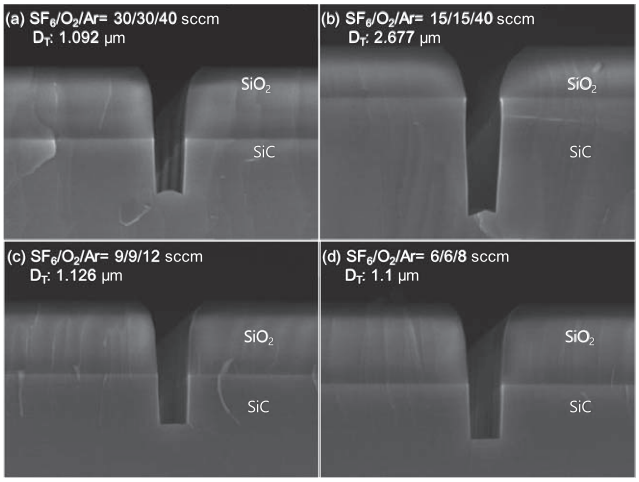

Figure 4. SEM images according to $SF_6/O_2/Ar$ flows of (a) 30/30/40 sccm, (b) 15/15/40 sccm, (c) 9/9/12 sccm and (d) 6/6/8 sccm.

conditions with working pressure of 10 mTorr, bais power of 0.5 kW, ICP power of 2 kW and temperature of 5 °C. For all conditions, total gas flow was fixed to 100 sccm. With higher Ar-fraction in $SF_6/O_2/Ar$ flows, higher SiC/SiO_2 etch selectivity was observed. The experiment with $SF_6/O_2/Ar$ flows of 30/30/40 sccm showed the high SiC/SiO_2 etch selectivity of 3.41 while those with 50/50/0 sccm and 40/40/20 sccm were 2.39 and 3.08, respectively. Addition of Ar flow to SF_6/O_2 chemistries results in increase of SiC etching rate because Si–C bonding is weaken by physical bombardment by Ar on the surface [8, 18, 25]. For $SF_6/O_2/Ar$ flows of 40/40/20 sccm, the SiC/SiO_2 etch selectivity is decreased as increasing working pressure as shown in figure 2(b). At the high working pressure condition, a mean free path of the ions is shorten and a directionality of ion is decreased so that SiC etch rate is reduced [7, 8, 21, 22]. When we increased temeperature from 5 °C to 20 °C with $SF_6/O_2/Ar$ flows of 40/40/20 sccm, working pressure of 20 mTorr, bias power of 0.5 kW and ICP power of 2 kW, the SiC/SiO_2 etch selecitivity was increased to from 2.36 to 4.13 due to the decreased SiO_2 etch rate.

$SF_6/O_2/Ar$ flows were additionally optimized to remove micro trenches at bottom corner of the SiC trench structure. Figure 3 shows the SiC/SiO_2 etch selectivity and H_{MT} (micro-trench height) over D_T (trench depth) for the etching conditions with bias power of 1 kW, ICP power of 2 kW, working pressure of 10 mTorr and temperature of 20 °C. Both H_{MT} and D_T have dependent on etching time so that we evaluated micro-trench shape by H_{MT}/D_T ratio. We believe that the H_{MT}/D_T ratio can be decreased by reduction in total gas flow because large amount of ion flux on the trench corner affects creation of micro-trench structures. When the $SF_6/O_2/Ar$ flows were changed from 30/30/40 to 15/15/40 sccm, the H_{MT}/D_T ratio was slightly reduced. In addition, when total gas flow was reduced to equal to or less than 30 sccm with identical gas proportion to the 30/30/40 sccm condition, the micro trenches were successfully removed as shown in figure 4. However, SiC/SiO_2 etch selelctivity showed trade-off replationship with the H_{MT}/D_T ratio so that

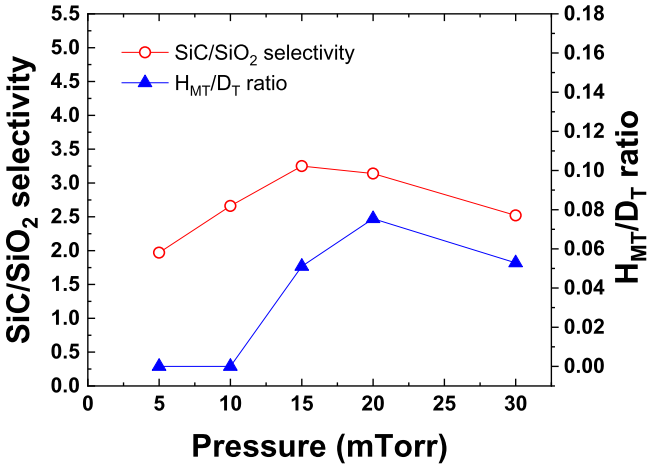

Figure 5. SiC/SiO_2 etch selectivity and H_{MT}/D_T ratio according to working pressure.

the lower total gas flow induced the lower SiC/SiO_2 etch selectivity.

For SiC TMOSFETs using the BPW structure, longer distance than 1 μm between p-base/drift interface and trench bottom is deriable to suppress JFET effects. In our design, the junction depth of p-base is 1 μm from the surface so that the target D_T is set to 2 μm. During the SiC etching process, top corner of SiO_2 mask is etched faster than a planar side. In those reasons, sufficiently high SiC/SiO_2 etch selectivity is required to form 2 μm deep SiC trench and prevent Al implantation on the trench sidewall during BPW formation. Figure 5 shows the effects of working pressure with range from 5 to 30 mTorr on the SiC/SiO_2 etch selectivity and the H_{MT}/D_T ratio for the conditions with bias power of 1 kW, ICP power of 2 kW, $SF_6/O_2/Ar$ flows of 9/9/12 sccm and temperature of 20 °C. It is noted that the SiC/SiO_2 etch selectivity and the H_{MT}/D_T ratio showed trade-off replationship for the working pressure variation as similar as gas flow variation described above. SEM images for each etching conditions are shown in figure 6. No micro trenches were observed at 5 and 10 mTorr. However, the trench width were broaden at 5 mTorr because of the low

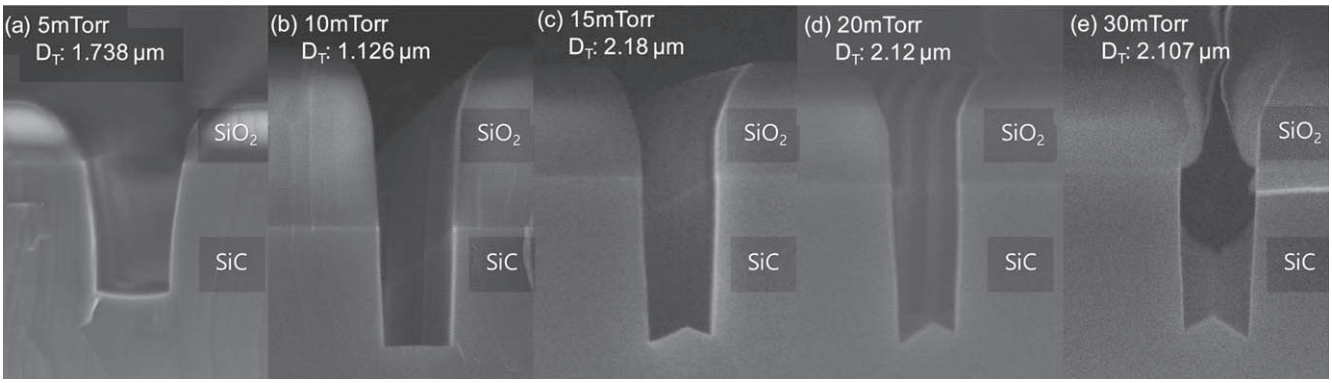

Figure 6. SEM images according to working pressure of (a) 5 mTorr, (b) 10 mTorr, (c) 15 mTorr, (d) 20 mTorr and (e) 30 mTorr.

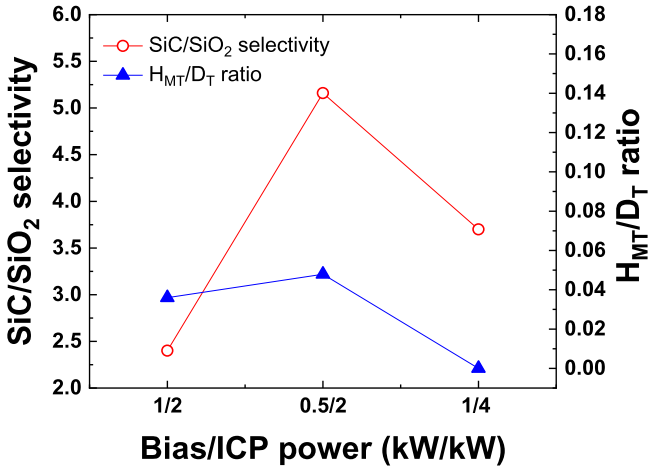

Figure 7. SiC/SiO_2 etch selectivity and H_{MT}/D_T ratio according to bias and ICP powers.

SiC/SiO_2 etch selectivity, meaning that serious Al implantation problems on the trench sidewall occur. Implantation of Al into trench sidewall affects electrons flow through channel and accumulation regions in the SiC TMOSFETs under on-state conduction mode. Also, threshold voltage can be undesirably increased. Even the 15 mTorr condition induced micro trenches, the SiC/SiO_2 etch selectivity was the highest among all working pressures. Thus, we chose the working pressure of 15 mTorr for the futher optimization including the SiC/SiO_2 etch selectivity and the H_{MT}/D_T ratio.

In figure 7, we compared the SiC/SiO_2 etch selectivity and the H_{TM}/D_T ratio for three-different bias/ICP power conditions with the fixed working pressure of 15 mTorr and temperature 20 °C. Also, SEM images for each etch condition are shown in figure 8. For this experiment, the $SF_6/O_2/Ar$ flows of 6/6/8 sccm were chosen to suppress micro trenches effectively. When bias power of 1 kW and ICP power of 2 kW were used with $SF_6/O_2/Ar$ flows of 6/6/8 sccm, the H_{MT}/D_T ratio was 0.036, while that with $SF_6/O_2/Ar$ flows of 9/9/12 sccm was 0.051 as shown in figure 5. However, the relatively low SiC/SiO_2 etch selectivity of 2.4 was shown at

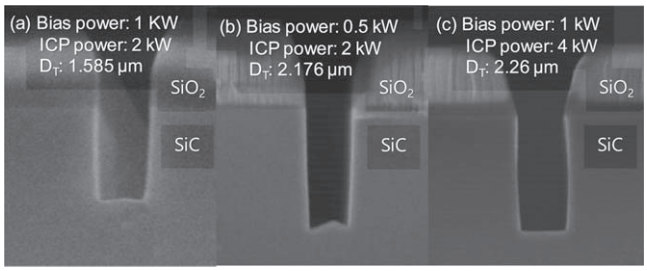

Figure 8. SEM images according to bias/ICP power of (a) 1 kW/2 kW, (b) 0.5 kW/2 kW and (c) 1 kW/4 kW.

$SF_6/O_2/Ar$ flows of 6/6/8 sccm compared to 3.25 with $SF_6/O_2/Ar$ flows of 9/9/12 sccm.

With lower bias power of 0.5 kW, the SiC/SiO_2 etch selectivity was considerably improved to 5.16 at $SF_6/O_2/Ar$ flows of 6/6/8 sccm due to the reduced SiO_2 etch rate, but the H_{MT}/D_T ratio was increased to 0.048. For bias power of 1 kW, ICP power of 4 kW and $SF_6/O_2/Ar$ flows of 6/6/8 sccm, the micro trenches were successfully removed by higher bias power and improved straightness of radicals. Also, it is believed that SiC etch rate is slightly increased at higher ICP power condition resulting in the suppression of micro trenches [7, 8, 10, 17]. Also, the higher SiC/SiO_2 etch selectivity of 3.7 and high SiC etch rate of 110 Å s^{-1} were achieved at bias/ICP power of 1 kW/4 kW compared to the conditions with bias/ICP power of 1 kW/2 kW and 0.5 kW/2 kW.

4. Conclusion

We successfully demonstrated the micro-trench free SiC trench structure by $SF_6/O_2/Ar$ based ICP-RIE. Also, the effects of various process parameters on SiC trench profiles were analyzed. High SiC/SiO_2 etch selectivity of 3.7 without micro trenches were achieved bias power of 1 kW, ICP power of 4 kW, working pressure of 15 mTorr, temperature of 20 °C and $SF_6/O_2/Ar$ flows of 6/6/8 sccm. The SiC trench profiles with the optimized etching condition are suitable for fabrication processes and design of SiC TMOSFETs using the BPW structure.

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