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FRIC — a 50 µm pixel-pitch single photon counting ASIC with Pattern Recognition algorithm in 40 nm CMOS technology

P. Otfinowski,[a,1] **G.W. Deptuch**[a,b] **and P. Maj**[a]

[a] *Department of Measurement and Electronics, AGH University of Science and Technology, Cracow, Poland*
[b] *Fermilab, Batavia, IL, U.S.A.*

E-mail: potfin@agh.edu.pl

Abstract: This work presents design and measurement results of FRIC — a prototype ROIC for fine resolution hybrid pixel detectors. The chip was manufactured in 40 nm CMOS process and contains an array of 64 × 64 pixels with 50 µm pixel pitch. It implements a very versatile analog front-end, capable of energy resolution of 0.71 keV FWHM and an estimated dead-time of 50 ns. The chip also features a Pattern Recognition algorithm together with signal summing for charge sharing correction. Low power consumption makes this circuit applicable in large-area detectors.

Keywords: Data reduction methods; Digital electronic circuits; Electronic detector readout concepts (solid-state); Pattern recognition, cluster finding, calibration and fitting methods

[1] Corresponding author.

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1 Motivation

The aim of this paper is to present design details and measurement results of a high granularity hybrid single photon counting pixel detector for operation with monochromatic radiation (e.g. synchrotron radiation) [1–3]. Decreasing pixel pitch increases the power density of the ASIC, which requires an optimization of the analog front-end for low power [4]. In addition, the charge sharing effect becomes more prominent and implementation of a charge-sharing compensation algorithm becomes a necessity [5]. However, existing solutions indicate that such an algorithm tends to degrade system performance in terms of count rate and electronic noise [6, 7]. A compromise solution, which could compensate some of the charge sharing effects without these penalties is also desired.

2 Circuit architecture

The prototype circuit was designed in 40 nm CMOS technology. It consists of an array of 64 by 64 pixels and peripheral circuits, such as reference and readout/control block. The chip has two 8-bit threshold DACs and an external exposure control signal for short, precise exposure times. All control signals are LVDS.

Diagram of a single readout channel is presented in figure 2. It consists of two amplifier stages, a pair of discriminators, digital algorithm and two 16-bit counters.

The first stage — the Charge Sensitive Amplifier (CSA) — is built of an amplifier based on the CMOS inverter circuit. It has fixed feedback capacitance C_{F1}, while the feedback resistance can be regulated globally with an on-chip DAC, which affects pulse amplitude and duration. To facilitate testing and characterization of the ASIC, a capacitor connected to the calibration circuit is added to the input.

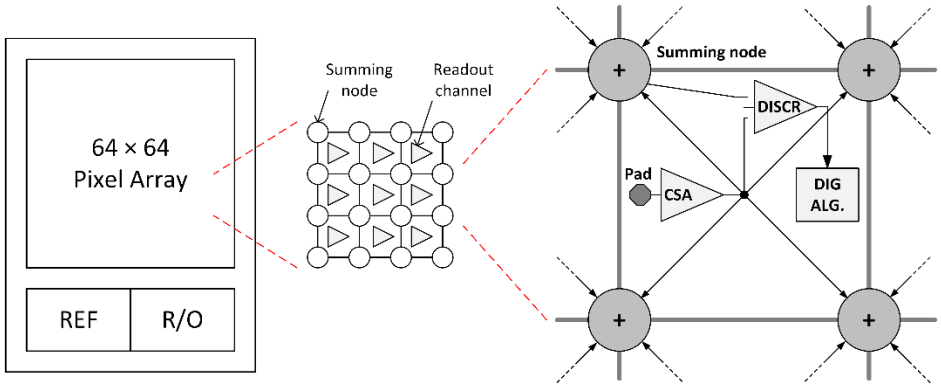

Figure 1. Chip architecture block diagram.

The second stage — the Shaper — is AC-coupled to the preceding stage. It is built of the same amplifier and it also has a fixed feedback capacitance C_{F2}. The time constant of the second stage is set to be much larger the first stage, so it operates as a voltage amplifier. The second stage also realizes charge summing, which is realized in the charge domain — signals from the first stages of three neighboring pixels can be also be AC-coupled to the input of the amplifier.

The output signal of the second stage is then AC-coupled to a set of two high-speed discriminators with independent thresholds. Each discriminator has a 5-bit trimming DAC to correct threshold dispersion.

Finally, outputs from the discriminators are fed to the pixel logic, which realizes the Pattern Recognition algorithms and controls two counters. The counters can be configured as two independent, one 32-bit long counter or one 16-bit counter with interleaved readout (zero dead-time). Data from the counters is read-out serially.

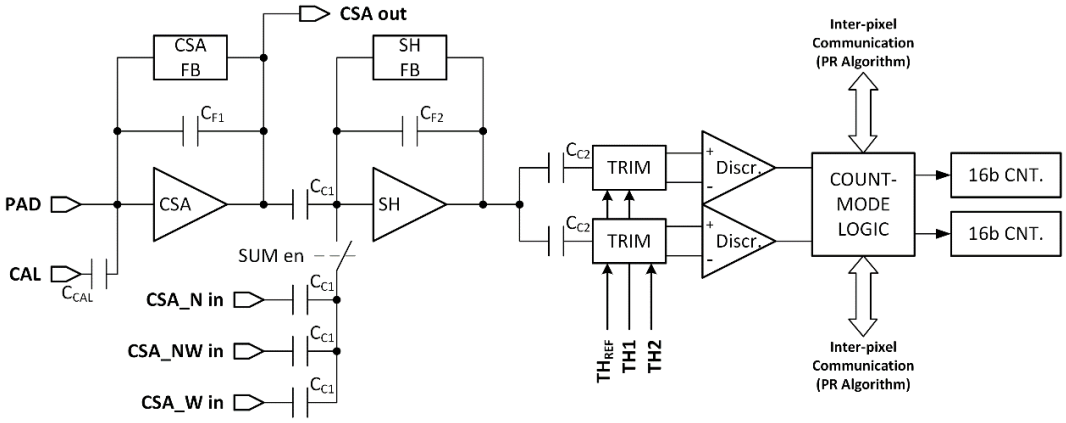

Figure 2. Readout channel functional diagram.

3 On-chip calibration results

The chip was bonded to a 64 × 64 pixel 0.32 mm thick silicon detector. Figure 3 show a photograph of the chip with a detector bonded to the test PCB. The chip was biased with 1.05 V (digital and

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analog blocks) and 2.5 V (LVDS drivers/receivers). The results were measured for two different analog front-end gain settings — achieved by adjusting CSA feedback resistance and discriminator bias current — and are referred as high-gain and low-gain.

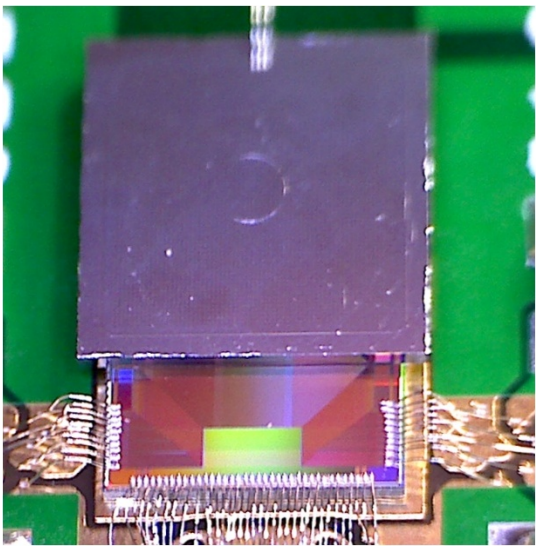

Figure 3. Test chip with a detector wire-bonded to the PCB.

3.1 Discriminator offset voltage

The discriminator offset voltage was measured by means of threshold-scan and gaussian-fitting noise counts. It was independent of the analog front-end gain setting. The results obtained are presented in figure 4, expressed in global threshold DAC units.

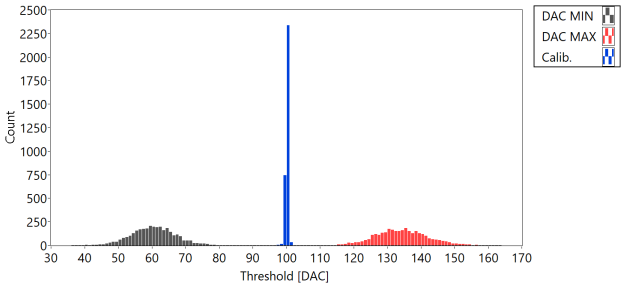

Figure 4. Discriminator offset voltage calibration results.

Three different trim-DAC settings were used — all DACs to minimum value, all DACs to maximum value and after calibration. The standard deviation of the uncalibrated thresholds is equal to 6.4 and 7.5 DAC unit for the minimum and maximum trim-DAC value, respectively, and 0.34 DAC unit after calibration, yielding an improvement of approximately 19.

3.2 Charge-to-amplitude transfer characteristic and signal-to-noise ratio

Pulse amplitude and signal-to-noise ratio measurements were done using the on-chip calibration circuit. A threshold scan was taken for a known amount of charge injected to the input, 400

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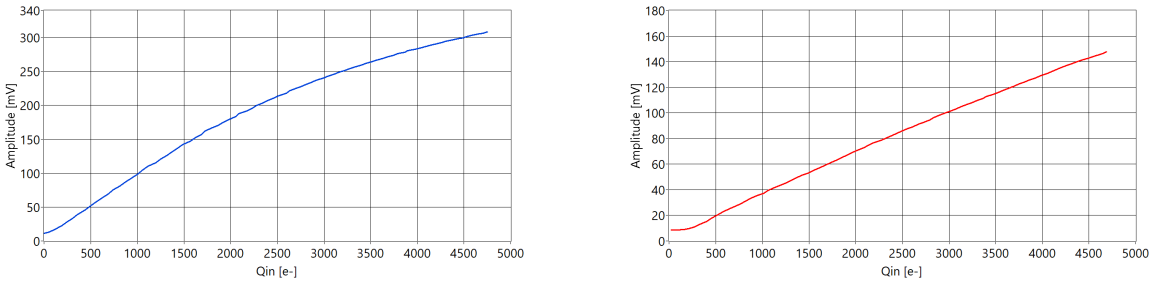
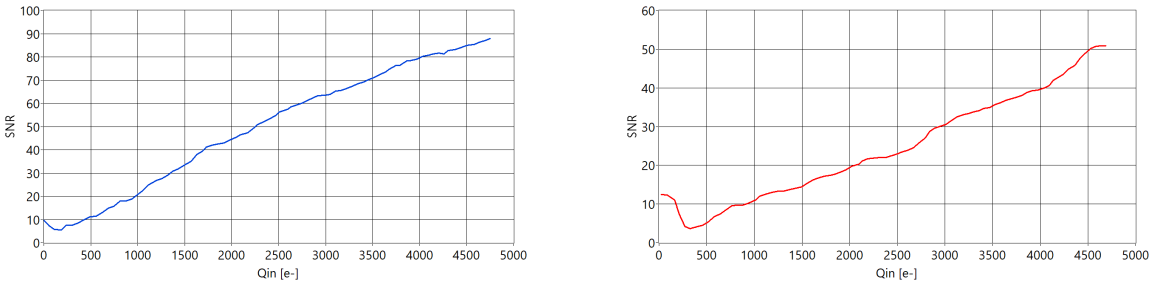
calibration pulses per threshold step. After s-curve fitting, signal amplitude and noise were extracted. The procedure was repeated for an increasing value of injected charge to obtain complete analog front-end transfer characteristics. Measured pulse amplitude and signal-to-noise ratio versus the input charge characteristic are plotted in figure 5 and figure 6, respectively.



(a) **(b)**

Figure 5. Pulse amplitude vs. input charge: a) high-gain, b) low-gain.

In high-gain setting the transfer characteristic shows non-linear behavior, while the average gain is on the order of 66 $\mu V/e^-$. For the low-gain setting the linearity is improved significantly and the average gain is equal to 32 $\mu V/e^-$.



(a) **(b)**

Figure 6. Signal-to-noise ratio vs. input charge: a) high-gain, b) low-gain.

Signal-to-noise was measured as the ratio of a pulse amplitude to the noise, extracted from an s-curve. For input charge of about 2200 e^-, corresponding to the photon energy of 8 keV, the SNR is equal to approximately 49 and 22 for the high- and low-gain setting, respectively, which translates to an ENC of 45 e^- and 100 e^-.

3.3 Front-end dead time

During chip verification process we did not have access to a high-intensity X-ray source for high count rate tests, which is the most common method to measure dead-time of analog front-end. Therefore, we have estimated it by directly estimating comparator pulse length. It was possible, because the chip has a dedicated external control signal for precise exposure timing. In our test setup the exposure timing could be controlled with a resolution of 12,5 ns (f_{CLK} = 80 MHz).

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The procedure to reconstruct the discriminator output signal was as follows (figure 7):

1. Send a calibration pulse.
2. Wait a predetermined delay time.
3. Send a short exposure signal strobe. Depending on discriminator output, the counter is incremented or not.
4. Repeat steps 1–3 and readout the counter data.
5. Increment the delay time and repeat steps 1–4.

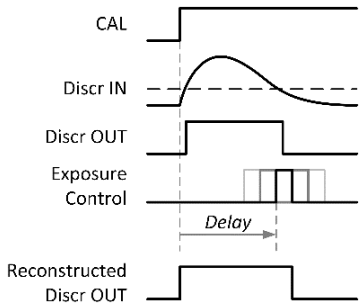
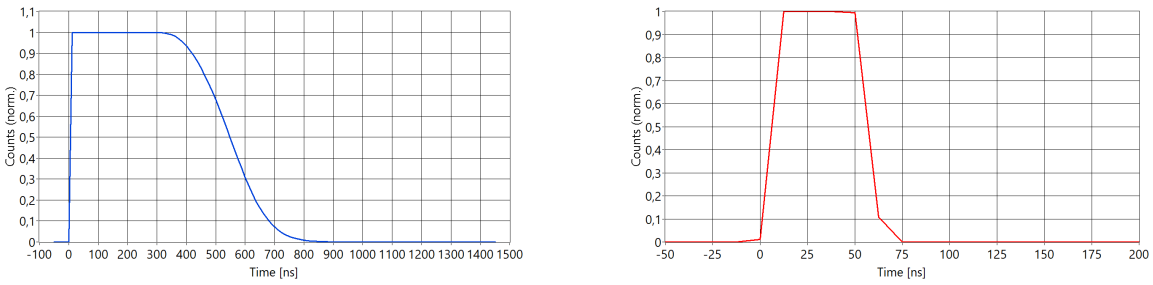


Figure 7. Front-end dead-time measurement procedure.

The reconstructed discriminators' signals are presented in figure 8. The pulse width varied across different pixels because of mismatch, thus the plot shows averaged and normalized response from all pixels. The measured full-width half-maximum of averaged pulse's times for high-gain setting is equal to 550 ns, with threshold set at 10% of pulse amplitude. For the low-gain setting the obtained FWHM time is 50 ns, with threshold set at 24% of pulse amplitude (the absolute threshold value was the same as in high-gain setting, but the pulse amplitude was lower).



(a) **(b)**

Figure 8. Averaged and normalized discriminator output signal: a) high-gain (TH=10%), b) low-gain (TH=24%).

It is important to note, that the discriminator's output is sampled by the exposure control signal level, not its edge. Therefore, the measured comparator pulse length will always be longer than an actual one.

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4 X-ray measurements

The ROIC was exposed to 8 keV X-rays (Cu target). All channels were uniformly illuminated. The exposure time was 10 s/frame. During all measurements only on-chip DACs were used for bias setting and no forced cooling was used. The detector was biased to 180 V.

4.1 Charge sharing compensation

Figure 9 presents a threshold scan registered by a single pixel for three different operating modes: conventional single photon counting (SPC), Pattern Recognition algorithm enabled (PR only) and PR algorithm with signal summing enabled (SUM+PR).

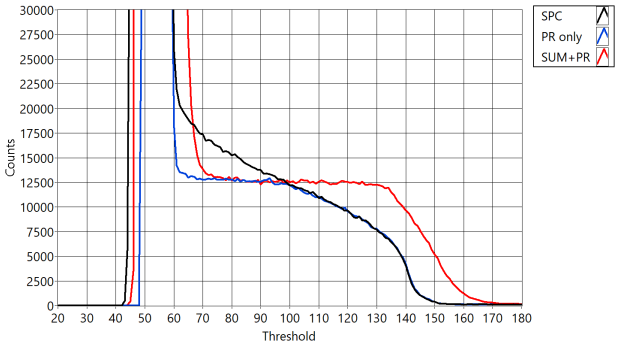

Figure 9. Comparison of a threshold scans registered by a single pixel without and with different charge sharing compensation modes.

In the conventional SPC mode number of counts is heavily affected by the set threshold. Enabling the pattern recognition algorithm results in significant reduction of excess counts caused by charge sharing — number of counts is nearly constant up to about half of signal energy. For thresholds over half of signal energy, the curve follows the one of SPC mode. The baseline noise is not affected.

When Pattern Recognition algorithm is used together with signal summing, the number of counts is constant across almost all signal range. It can be noted however, that signal summing resulted in an increase of baseline noise. Additionally, the perceived signal energy is composed of four s-curves from neighboring channels — because of gain dispersion, the information about signal energy is blurred.

4.2 Energy spectrum

To measure the energy resolution, the chip operated in a conventional single photon counting mode, without charge sharing compensation algorithms. First, a threshold scan was taken. Secondly an off-chip gain and offset correction were performed. Then, the results were averaged and the differential energy spectrum was computed. Normalized results are presented in figure 10.

For the high-gain setting, the FWHM energy resolution is equal to 0.71 keV and the corresponding ENC is equal to 84 e^-. The k-alpha and k-beta peaks of Copper are clearly visible. For the low-gain setting the FWHM is equal to 1.13 keV, which corresponds to ENC of 132e^-.

The results presented here are different than in section 3.2. However, one has to keep in mind, that the presented results are severely affected by charge sharing. Additionally, because of

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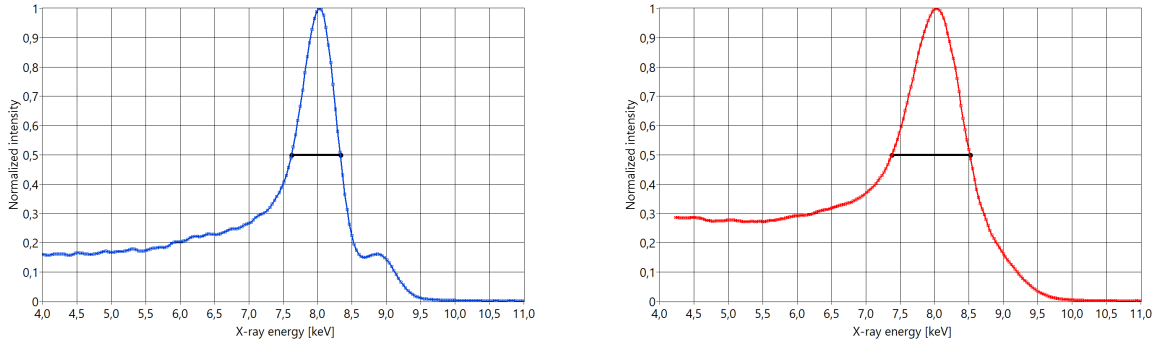

(a) **(b)**

Figure 10. Normalized differential energy spectrum: a) high-gain, b) low-gain.

nonlinearity of the charge-amplitude transfer characteristic in high-gain setting, the actual gain at the measured energy is lower, which also affects the final energy resolution.

5 Summary

This work presented measurement results of FRIC — a ROIC prototype for fine resolution hybrid pixel detectors. The chip was manufactured in 40 nm CMOS process as an array of 64×64 pixels with 50 µm pixel pitch. It implements a very versatile analog front-end, achieving energy resolution of 0.71 keV FWHM at high-gain setting and an estimated dead-time of 50 ns in low-gain setting. Power consumption in the range of 12 µW–18 µW per pixel makes this circuit applicable in large-area detectors, even considering the very small pixel pitch.

The chip features a Pattern Recognition algorithm for charge sharing correction. When used together with signal summing it allows to reconstruct the signal amplitude and makes the imaging system less dependent on the set threshold. The PR algorithm alone is an interesting alternative, as it still makes the system less susceptible to charge sharing without increasing noise and FE dead-time due to signal summing.

The comparison of the presented work with current state-of-art circuits is presented in table 1. It presents results for high- and low-gain setting or comparable, when the data is available.

Acknowledgments

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Table 1. ASICs with implementation of hardware algorithms for dealing with charge sharing.

ASIC	**FRIC**		Medipix3RX [1, 6]		IBEX [2]		UFXC32k [3]	
Technology	**40 nm**		130 nm		110 nm		130 nm	
Array size	**64 × 64**		256 × 256		256 × 256		128 × 256	
Pixel size (μm^2)	**50 × 50**		55 × 55		75 × 75		75 × 75	
CS correction	**Yes**		Yes		No		No	
Analog power/ pixel (μW)	**12**	**18**	7.5		7.4		26	
FWHM (keV)	**0.71**	**1.13**	0.96,[2]	—	0.85	—	—	—
ENC (e^-)	**45**,[1]	**100**,[1]	80	—	89,[3]	—	123	235
FE Dead time (ns)	**(550)**	**(50)**	690	400	—	100,[4]	232	85

[1]Measured with calibration pulses.
[2]Measured at 12 keV, without off-chip data alignment.
[3]Corrected for charge sharing.
[3]4Retrigger feature disabled.

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