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Implementation of the interpolator for signal peak detection in read-out ASIC

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Abstract: A prototype interpolator for signal peak detection in read-out ASIC is presented. It uses interpolation algorithm for finding additional points between ADC samples. This allows to increase an accuracy for signal peak detection. Behavioral models of interpolator for Spline and Lagrange algorithm were realized and compared. Interpolator was designed in 180 nm UMC MMRF CMOS process. It is based on a 6th order Lagrange interpolation polynomial. The interpolator ensures the accuracy of signal peak finding is less than 1.5 LSB of ADC at sampling frequency of 25 MHz and 200 ns peaking time of 2nd order shaper.

Keywords: Digital electronic circuits; Digital signal processing (DSP); Front-end electronics for detector readout

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1 Introduction

One of the trends in the development of front-end electronics is a digitization of analog signals at the earliest stage, followed by their application specific processing in digital domain. The digital processing allows to filter data, remove uninformative or spoiled data, detect overlays and calculate of signal peak. The processing functions are usually assigned to the remote data acquisition system. The stream of digital data coming from read-out ASIC can easily reach a few Gb/s.

In order to reduce the output data flow, it is usually required a selective digital signal processing being built-in the ASIC. For asynchronous peak detection inside the read-out ASIC at a high resolution (e.g. 10 bit) for fast signals (e.g. ones coming from shaper having peaking time of 200 ns) the sampling rate must be very high — at least 100 Msps. That is because for peak detection with a fixed error (e.g. less than 1 LSB) it is necessary to have change in amplitude for each sampling interval less than the required error. The maximum peak determination error as function of ADC sampling rate for different shaper peaking times and filter orders is shown in figure 1. The data are obtained from behavioural simulation in MATLAB for 10-bit resolution ADC. The maximum error in determining the signal amplitude at this figure is defined as the maximum deviation of the signal function value at points tpeak − ts/2 or tpeak + ts/2 from the maximum signal amplitude (the full scale of the ADC), where tpeak is the shaper peaking time, ts is the ADC sampling period.

The implementation of high-speed ADC as a bulding block of readout ASICs in CMOS processes of technology nodes 130–180 nm results in high power consumption and large chip area. For known ADCs working with sampling rate more than 100 MHz the power consumption still reaches tens of mW [1–4] despite of the application of new architectural solutions [5]. That is inappropriate application for a low-power design of multichannel read-out ASICs.

To determine the signal maximum (peak) at the required accuracy (amplitude resolution), it is proposed to use an interpolation technique. The interpolation allows to find the fit function of a curve that passes through a given set of points. Knowing the equation of the curve, it is possible to calculate the values of the function at intermediate points in the area of the desired maximum of the signal. It will allow to find the peak at a necessary accuracy, to reduce the required sampling

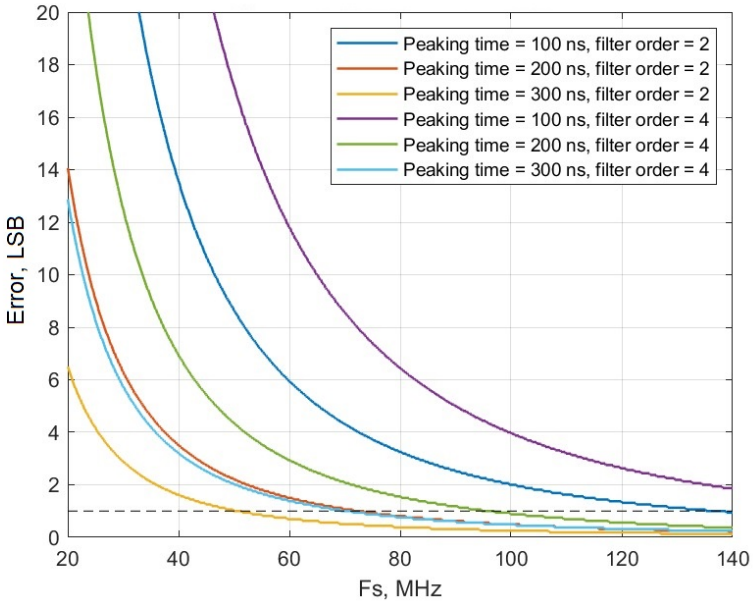

Figure 1. Maximum error of peak determining vs. ADC sampling frequency.

rate of the ADC and finally to minimize the output data volume. The paper describes a comparison of different interpolation algorithms, choice of interpolator parameters and implementation of the interpolator as building block for read-out ASIC in UMC 180 nm MMRF CMOS process.

2 Interpolator algorithm

To choose of the interpolation technique two well-known algorithms were compared: interpolation of polynomials in the Lagrange form and cubic spline interpolation [6]. The behavioral model of the read-out channel with ADC was developed in MATLAB and the generated data were processed by the mathematical model of the interpolator. The restored interpolation curve for these interpolation algorithms is shown in figure 2. The curves were restored from a set of 6 points. Both interpolation algorithms provide acceptable accuracy, but Lagrange interpolation is easier to implement in hardware. This is due to the simplification of the algorithm when working with points evenly distributed over time axis.

Knowing equation of interpolation curve, it is possible to calculate the value of the function at intermediate points. By calculating the values at these points and comparing them with the desired signal peak, it is possible to find the required interpolator parameters, which will provide the required accuracy of the maximum determination. The main parameters that affect the accuracy are the number of points selected for reconstruction of the interpolation function, the resolution and sampling frequency of the ADC, the shape of the input signal determined by the peaking time and integration order and the number of intermediate (upsampling) points. The values of the upsampling points are calculated in the interpolator. The number of intermediate points can be calculated from figure 1. For example, for a 4th order shaper having peaking time 200 ns, in order to achieve an accuracy on a peak determining of 1 LSB for a 10-bit ADC, a sampling frequency of about 100 MHz

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is required. For an ADC at sampling frequency of 25 MHz, it is necessary to add a minimum of 3 intermediate points in order to increase the sampling frequency by 4 times. Figure 3 shows the maximum error in the signal peak determination using the Lagrange algorithm for a different number of interpolation points depending on the sampling frequency of a 10-bit ADC getting the signals from a 200 ns peaking time 4th order shaper. The best result is obtained at using 6 interpolation points.

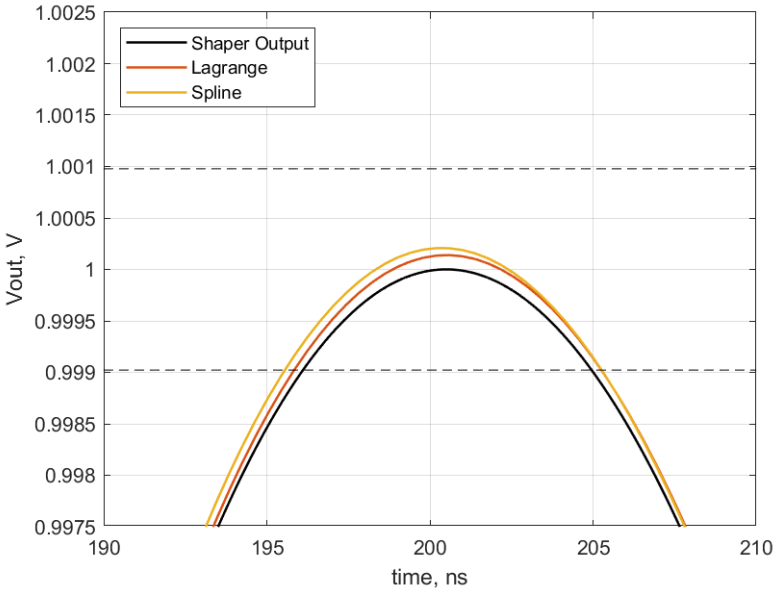

Figure 2. Interpolation curve fit near peak.

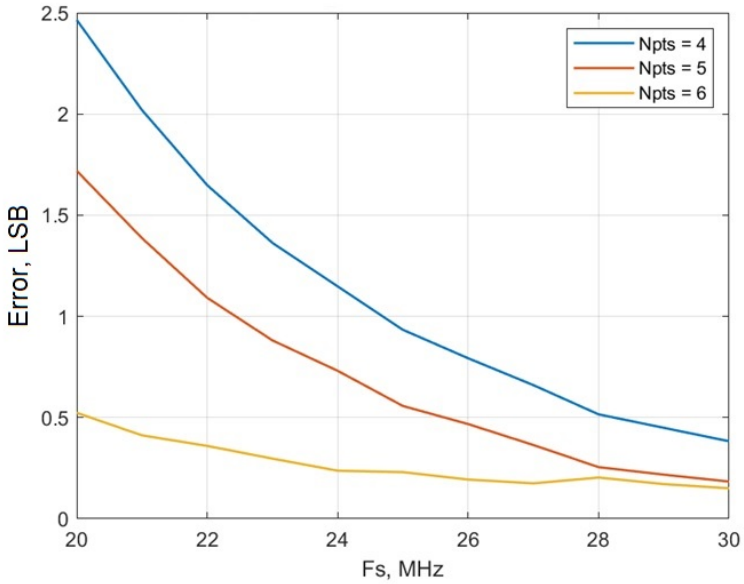

Figure 3. Lagrange interpolation error vs. sampling frequency.

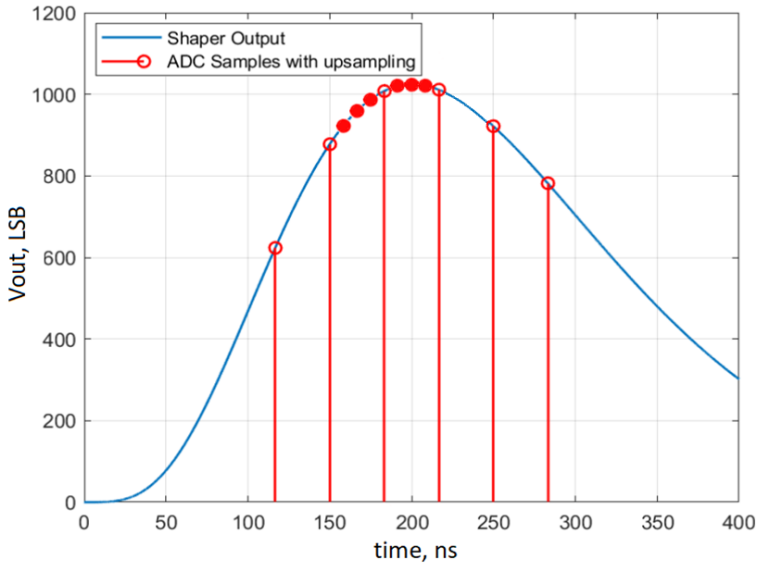

Figure 4. Samples for calculation.

The interpolator working with a Lagrange algorithm for a set of 6 points with 3 upsampling points was chosen for the implementation. An example of the selected points are shown in figure 4. A comparison on the errors of digital peak detector versus interpolator (behavioral model) is shown in figure 5. Horizontal axis is the input signal delay between the signal peak and the neighbor with peak ADC sample. The maximum error for the digital peak detector is 13 LSB, whereas for the interpolator model it is 1 LSB.

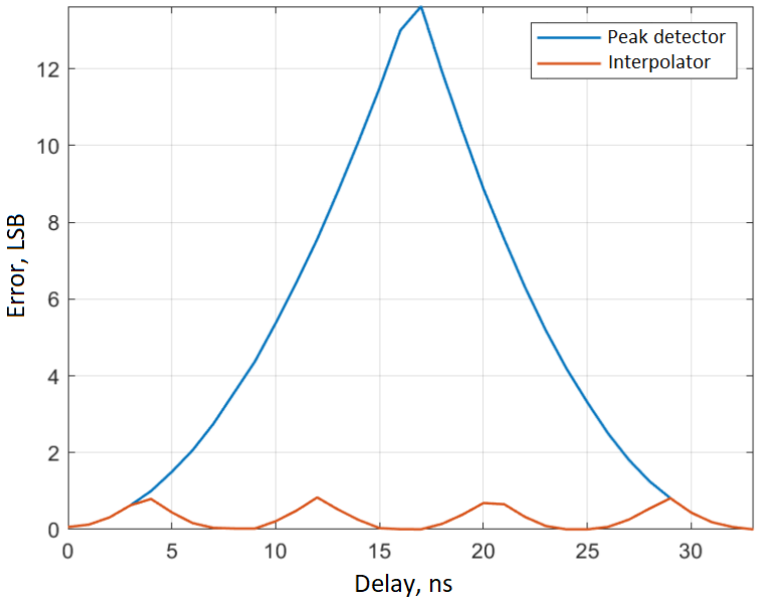

Figure 5. Error vs input signal delay (MATLAB).

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3 Implementation of the interpolator

The interpolator was described in Verilog HDL and implemented in the UMC 180 nm MMRF CMOS process. The interpolator structure is shown in figure 6. It consists of a data synchronization unit (sync), a data search unit (finder), a data processing unit (process) and a signal arrival time determination unit (tstamp). ADC data are fed to the input of the data synchronizer block. The block synchronizes the received data and transfer them to the input of the finder block. The finder saves the incoming data in a ring buffer of 6 words length and analyzes the sequence of saved words to match one of the possible patterns of the ratio of signal amplitudes: PTS[0] < PTS[1] < PTS[2] ≥ PTS[3] > PTS[4] > PTS[5], where PTS[i] are the ADC samples. At analyzing words, the requirement of exceeding the noise threshold by the data is taken into account. The coincidence of the input sequence of words with the pattern indicates the presence of a useful data. The found sequence of words is stored in a special register and transferred to the process block to calculate the signal peak using the Lagrange interpolation algorithm. According to the sampling condition, the maximum value is in the range from PTS[1] to PTS[3]. The PTS[1] value is taken as the initial maximum value. Further in the cycle, the intermediate points are sequentially calculated using the Lagrange interpolation algorithm and their values are compared with the maximum. If the calculated value at the point is greater than the maximum, then the current calculated value will be assigned to the maximum value. If the value at the point is less than the maximum, then it is concluded that the point is on the decline of the curve and the maximum has already been found and the maximum search cycle ends.

The interpolator block receives a 12-bit timestamp code from the tstamp block and determines the timestamp code corresponding to the found signal peak. In this case, the determined code has an extended bit depth of 14 bits: 12 bits from the tstamp block and additional 2 bits of expansion due to the calculation of intermediate points of the interpolation curve. These 2 bits increase the effective frequency of the timestamp counter by 4 times. The counter operates at a frequency equal to the ADC sampling frequency.

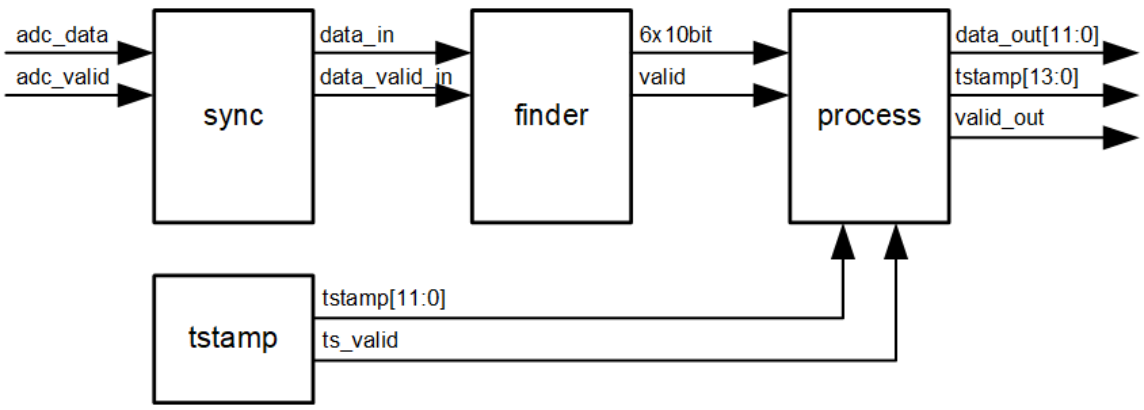

Figure 6. Interpolator structure.

Key features of the implementation of the interpolator block are a pipeline data processing and optimization of mathematical operations. Real mathematics was reduced to operations on integers. The weighting coefficients of the Lagrange polynomial were recalculated in order to replace the

integer division by the shift. Input values are 10-bit, output values are 12-bit. The calculations are performed under 14-bit numbers. In this case, the two additional minor bits reduce the rounding error of the intermediate results. Two of the most significant additional bits protect against overflow during addition/subtraction operations. Real values of weighting coefficients were also converted to 14-bit integers.

The pipelining is characterized by a high degree of utilization of gates. When the interpolator is fully loaded in the pipeline, the multiplication unit is fully busy, and the adder is idle for one clock cycle during the calculation of the point. Figure 7 shows the operational stages of the computing pipeline. One cycle for calculating an intermediate point is highlighted in gray. A dash indicates an idle cycle.

For signal peak calculation the interpolator needs to 39 clock period at 80 MHz frequency and all process take 487.5 ns.

MUL0	MUL1	MUL2	MUL3	MUL4	MUL5	MUL0	MUL1	MUL2
ADD4	-	ADD0	ADD1	ADD2	ADD3	ADD4	-	ADD0

Figure 7. Operational stages of computing pipeline.

Interpolator unit occupies a silicon area of $1100 \times 140\,\mu m^2$ and consumes a power of about 4 mW. Thus the power consumption of the interpolator is small in comparison with the one of high-speed ADC. Transferring out all ADC samples in order to calculate the peak in the external processing system also requires additional power to be spent by high-speed transmitters. For example, the LVDS transmitter has an output current of about 4 mA.

4 Simulation results

The peak determination error was measured for the interpolator unit versus the digital peak detector for an arbitrary input signal delay from 0 to Ts and for a signal amplitude equal to full ADC input range. An arbitrary signal delay value allows to analyse all possible peak positions relative to the ADC samples. The signal delay expresses the shift of the signal peak relative to the ADC samples in asynchronous system. For a 2nd and a 4th order shaper with 200 ns peaking time and sampling frequency (Fs) equal to 25 and 30 MHz, the maximum digital peak detector error is equal to 10 and 13 LSB respectively, whereas the interpolator unit has a maximum error of 0.75 LSB (figure 8). The interpolator has a 12-bit output and the data were presented in 10-bit format for the convenience of comparing the results obtained by the peak detector and the interpolator.

The peak determination error is also dependent on the input signal amplitude. The error as a function of the input amplitude expressed as a percentage of the ADC full scale is shown in figure 9. The maximum error equals 1.25 LSB for the 4th order shaper at Fs = 30 MHz and 1.5 LSB for the 2nd order shaper at Fs = 25 MHz for 200 ns peaking time.

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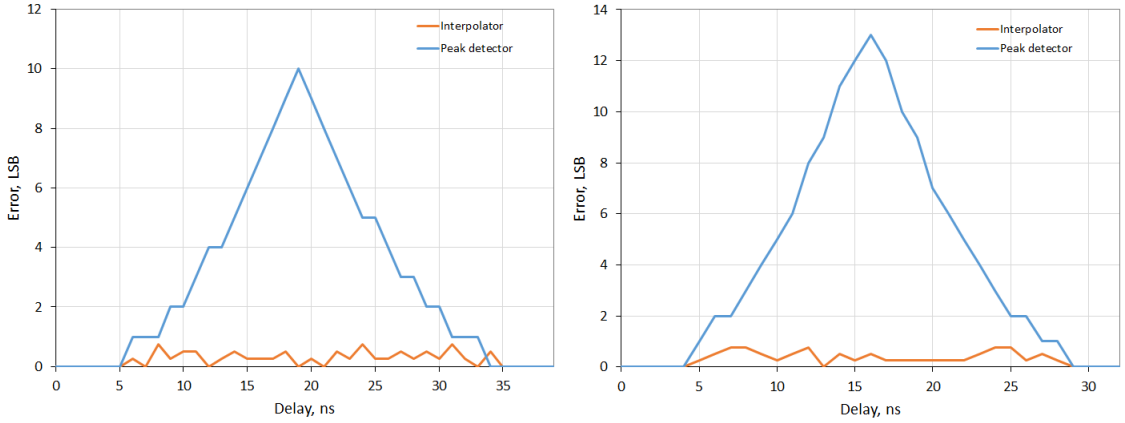

Figure 8. Error vs. delay for 25 MHz sampling and 2nd order 200 ns shaper (left) and 30 MHz and 4th order 200 ns shaper (right).

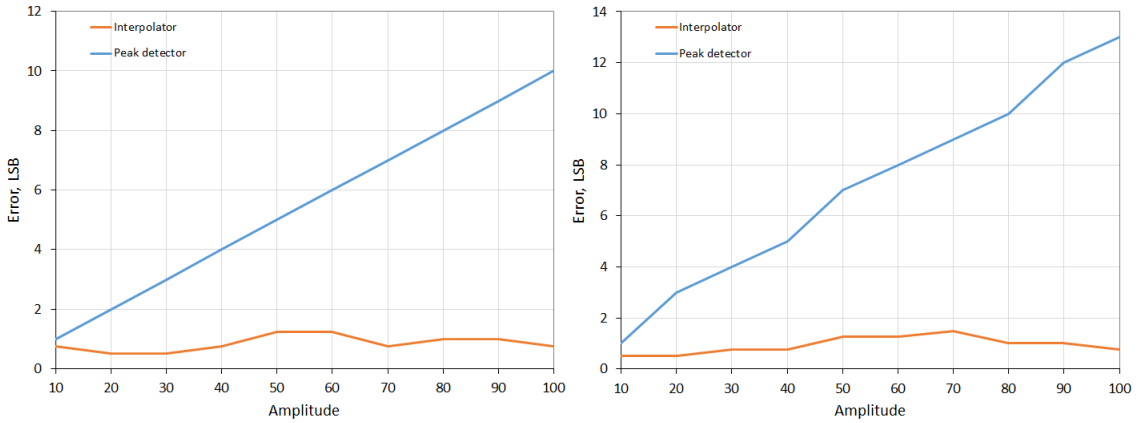

Figure 9. Error vs. amplitude for 25 MHz sampling and 2nd order 200 ns shaper (left) and 30 MHz and 4th order 200 ns shaper (right).

5 Conclusion

The interpolator for signal peak detection in the read-out ASIC was presented. Simulation results have showed that the interpolator usage allows to achieve the accuracy of peak determination of about 1 LSB for 10 bit ADC at both 25 and 30 MHz sampling rate and at shaper peaking time of 200 ns for 2nd and 4th integration order. The implemented interpolator has polynomial of 6th degree and uses 3 upsampling points, that increases the sampling rate in 4 times.

The interpolator was designed as a building block for the read-out ASIC to be prototyped in UMC CMOS 180 nm MMRF process. Power consumption of the interpolator is equal to 4 mW.

Acknowledgments

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References

[1] B. Murmann, *ADC performance survey 1997–2019*, http://web.stanford.edu/~murmann/adcsurvey.html (2019).

[2] K. Honda, M. Furuta and S. Kawahito, *A low-power low-voltage 10-bit 100-MSample/s pipeline A/D converter using capacitance coupling techniques*, *IEEE J. Solid-State Circuits* **42** (2007) 757.

[3] J. Li and U.-K. Moon, *A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique*, *IEEE J. Solid-State Circuits* **39** (2004) 1468.

[4] C. Gamauf, A. Nemecek, F.P. Leisenberger and G. Promitzer, *Design and characterization of a 10 bit pipeline- ADC for 100 MSps in 0.18µm CMOS*, in *22nd Austrian Workshop on Microelectronics (Austrochip)*, Graz, Austria, 9 October 2014, pp. 1–5.

[5] D. Osipov and S. Paul, *Low power SAR ADC switching without the need of precise second reference*, *Analog Integr. Circ. S.* **97** (2018) 417.

[6] R.W. Hamming, *Numerical Methods for Scientists and Engineers*, Dover Publications, Inc., New York (1973).

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