Research on A New Type Topology of 4-Quadrant Converters

Dawei Pan

School of Mechanical and Control Engineering, Shengli College, China University of Petroleum, Shandong Dongying, 257061, China
Email: pandawei@slcupc.edu.cn

Abstract. In consideration of the demerits of the traditional four-quadrant converter whose operating voltage of the dc side is very high, a new type topology converter is proposed whose topology belongs to quasi-buck topology and the voltage of the dc side is reduced by about 50%. Therefore this kind of four-quadrant can be used in the lower voltage filed. The modelling of the converter is described in this paper. The validity of the converter topology and the model along with the theory is proved by MATLAB simulation and the experiment result.

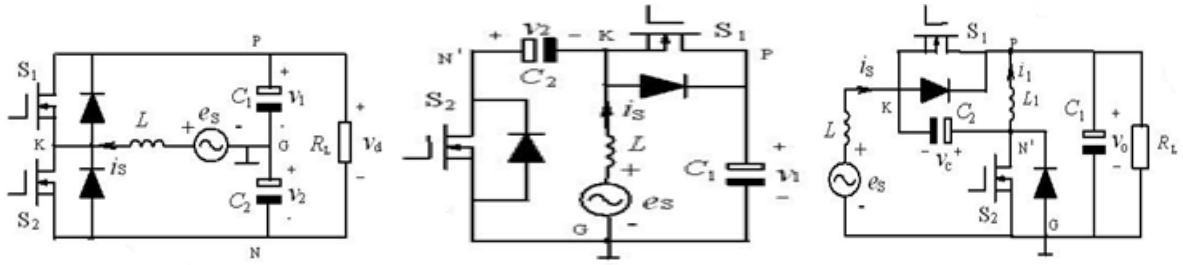
1. Introduction

Four-quadrant converters (4QC) are widely used in many fields, such as wind power technology, reversible PWM rectifier and active power filter. For the moment, most of the four-quadrant topologies belong to bridge voltage circuits, and the dc-side voltage of this kind of the topology is very high, which depends on the boost work mechanism. The demerit mentioned above limits the range application to a large extent. In this paper a new type topology converter is proposed whose topology belongs to quasi-buck topology and the voltage of the dc side is reduced by about 50%. Therefore this kind of four-quadrant can be used in the lower voltage filed. The modelling of the converter is described in this paper. The feasibility of the converter topology, the model and the theoretical analysis is proved by MATLAB numerical simulation and the hardware experiment result.

2. Topology Conversion and Principle Analysis

Both of the traditional one-phase and three-phase bridge four-quadrant converter can be considered to be composed of the half-bridge units, which are shown in figure 1(a). The kind of the half-bridge topology is extensively used, but it has the demit that the voltage U_d of the dc-side must be higher than the ac-side peak-peak voltage, which is determined by the boost work mechanism. This kind of topology can't meet the need of dc-side low voltage load if the ac-side voltage isn't reduced. To meet the need of the low voltage, the load can be transferred from the positive and negative bus u_d of the dc-side to its upper half terminal u_1, and the mode is called dc-side unsymmetrical output. But in this mode, shapes of u1 and u_2 are of distortion seriously, and the circuit can't work normally. This is because the direct component of the load at u_1 flows through the source e_S inevitably to form one single dc path, which makes the average value of i_S not to be zero, and it doesn't conform to the fundamental role of the hypostasis of four-quadrant converter. It won't work well unless the identical load is connected to the side of u_2 to form another dc circuit to balance the direct component of i_S. In order to solve the problem, the load R_1 is considered to connected to the capacitor C_1 in parallel, and at the same time the capacitor C_2 and the power switch S_2 exchange places according to the original polarity to keep the mean value of the ac-side current zero, and the topology is shown is figure 1(b). Compared with figure 1(a), the work mechanism of figure 1(a) doesn't change essentially, but the half-bridge circuit has passed out of existence, and the previous u_d has been split in half, set at each side, whereas u_1 and u_2 still exist. If U_1 and U_2, the dc mean value of u_1 and u_2, keep equal to each

other and S_1 and S_2 are applied with the PWM control similar to the half-bridge circuit, the PWM waveform of the point *K* of the two topologies will be of the same. Comparing with the half-bridge circuit, this topology has the advantage to avoid and protect the positive and negative short circuit easier, and point *P* and point *N*' are of the same potential to dc side. In order to keep point *P* and point *N*' equipotential to dc side to reach the dc balance, one inductance *L*1 is set between point *K* and point *N*' according to the Principle of steady-state voltage-second balance of inductance, which is shown in figure 1(c). Accordingly, in the unsymmetrical case that only the capacitor *C*1 is connected to the dc side load, on one hand that the dc side voltage of U_C and U_O are of balance, on the other hand that a new dc circuit is formed along *K-L-G-N'-L*1*-P-K*, which makes it become possible to remove the dc component of is in the circuit of *K-P-R*L*-G-L* and remove the dc component and that i_S will not contain the dc component because of the unbalance of the load. The dc side output voltage of the four-quadrant converter can be reduced about 50% by the topology conversion, and the topology can be called Quasi-Buck 4-Quadrant Converter (QBC).



(a) (b) (c)

Figure 1. Topology Conversion

3. The State Space Average Modelling

To the Quasi-Buck 4-Quadrant Converter shown in figure 1(c), it is assumed that the conducting time of switches of S_1 and S_2 are *dT* and *d'T*=(1-*d*)*T*, where *T* is PWM switching period and d is the duty cycle. When S_1 is on and S_2 is off, the sate space equations of the linear circuit can be obtained, which is in the form of matrix:

$$\begin{bmatrix} L\dot{i}_S \\ L_1\dot{i}_1 \\ C_2\dot{u}_C \\ C_1\dot{u}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & -1/R_L \end{bmatrix} \begin{bmatrix} i_S \\ i_1 \\ u_C \\ u_O \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} e_S \tag{1}$$

With S_1 off and S_2 on, we have

$$\begin{bmatrix} L\dot{i}_S \\ L_1\dot{i}_1 \\ C_2\dot{u}_C \\ C_1\dot{u}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1/R_L \end{bmatrix} \begin{bmatrix} i_S \\ i_1 \\ u_C \\ u_O \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} e_S \tag{2}$$

It is assumed that the system matrix and input matrix of equation (1) and equation (2) are A_1, B_1 and A_2, B_2 respectively. On the basis of reference [1] and reference [2], equation(1) and equation (2) can be synthetically transformed into the state space average (SSA) model of the converter with $A = dA_1 + (1-d)A_2$ and $B = dB_1 + (1-d)B_2$.

$$\begin{bmatrix} Li_S \\ L_1 i_1 \\ C_2 u_C \\ C_1 u_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1-d & -d \\ 0 & 0 & d & -(1-d) \\ -(1-d) & -d & 0 & 0 \\ d & 1-d & 0 & -1/R_L \end{bmatrix} \begin{bmatrix} i_S \\ i_1 \\ u_C \\ u_O \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} e_S \tag{3}$$

Left Multiplying equation (3) with $\begin{bmatrix} i_S & i_1 & u_C & u_O \end{bmatrix}$, we can get

$$Li_S i_S + L_1 i_1 i_1 + C_2 u_C u_C + C_1 u_O u_O =$$

$$= -d' u_C i_S + d u_O i_S - d u_C i_1 + d' u_O i_1 + d' u_C i_S + d u_C i_1 - d u_O i_S - d' u_O i_1 - \frac{u_O^2}{R_L} + e_S i_S = e_S i_S - \frac{u_O^2}{R_L}$$

Since $Li_S i_S = \frac{d}{dt}(\frac{1}{2} Li_S^2)$ means the instantaneous power of the inductance L and other items can be analogized, so the equation above proves that the power balance can be satisfied at any instance and the power from the source equals to the sum of output power and the power absorbed by all the reactive power components.

4. The Simulation and Experiment Results

The system control structure designed for the QBC simulation and experiment is shown in figure 2. Parameters of the converter are shown below: L=20mH, L_1=100mH, C_1=C_2=2200uF, R_L=50Ω, E_S= $\sqrt{2}$ *110V, U_O=180V. In this system equation (3) is regarded as the QBC simulation model, and the calculation of the model control variable-duty cycle d and the current closed-loop control are realized with a small inertia current tracking control algorithm [3, 4]. The MTALAB numerical simulation waveform is shown in figure 3. In the simulation result it can be found that u_O and u_C both contain the fundamental wave and second harmonic and the current i_1 barely contains the second harmonic just as the steady state analysis. The above is more obvious in the FFT spectral analysis of MATLAB shown in figure 4.

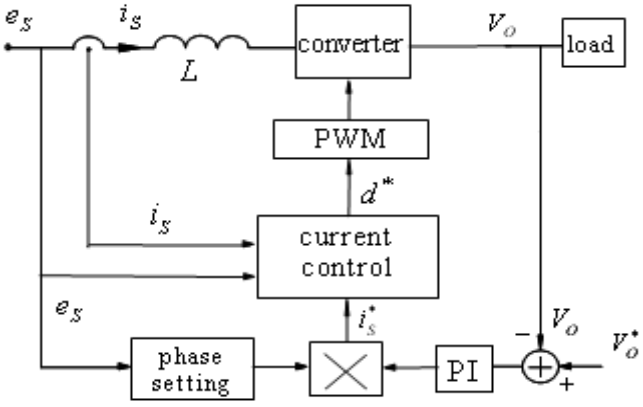


Figure 2. 4QC System Control Configuration

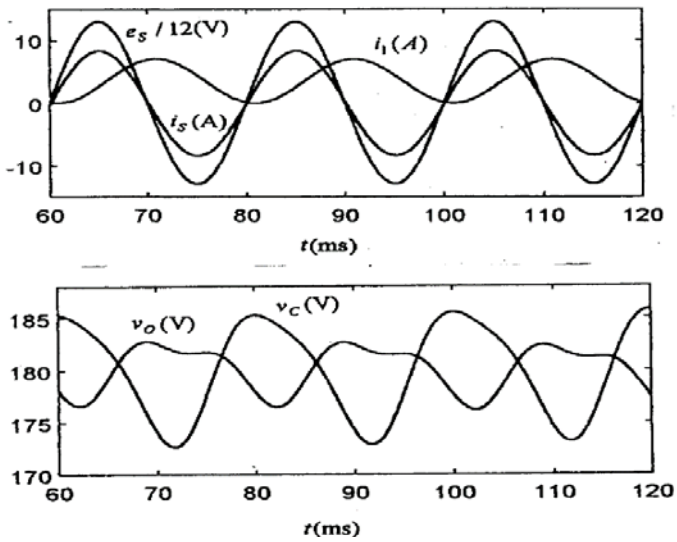


Figure 3. QBC Simulation Waveforms

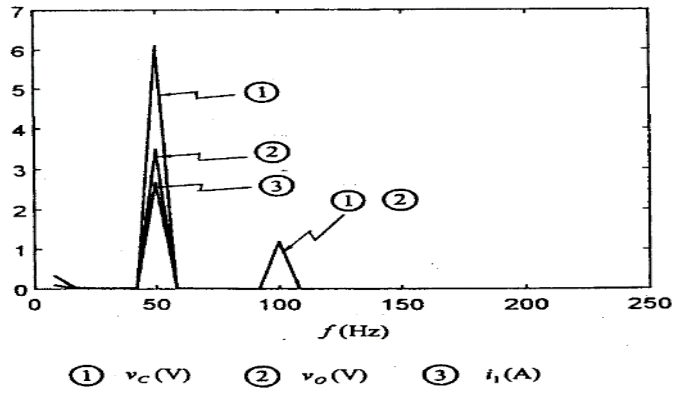
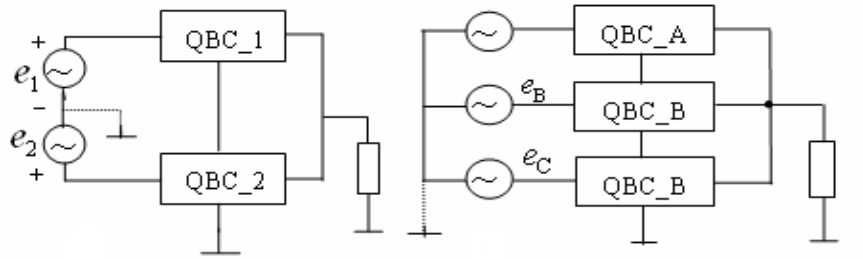


Figure 4. QBC FFT Spectrum

The current-hysteresis-loop tracking control technique is applied to compare the feedback current and the given current i_S^* to form the switch signals in the experiment system. The ac-side input current is forced to track i_S^* and the deviation is limited in a desired hysteresis band by on-off action of the power switch. The measured experiment waveform is shown in figure 5 according to the converter parameter same as the simulation system. It can be found that the current is almost a sinusoidal waveform and the power factor pf≈1, which agrees with the simulation and theoretical analysis basically. The only difference is that the simulation waveform doesn't reflect the switching frequency ripples, which is decided by the "averaging" character of the SSA model.

5. The Formation of the Single Phase and 3-Phase Converter

As the half-bridge topology shown in figure 1(a) can be the component unit of one-phase and tree-phase four-quadrant converter, the QBC unit shown in figure 1(c) can also form one-phase and three-phase four-quadrant converter, which is shown in figure 5. The dc-side output port of each QBC unit is connected in parallel, and one filter capacitor is used by the units together. In figure 5(a), the ac-side input voltage e_1 and e_2 is required to have the same amplitude and the reverse phase. In practice, an ac power e=2e_1 is connected between two input terminals to form a one-phase converter, and the two filter inductances of the input circuits can also be combined into one. A symmetrical three-phase source at the ac-side is required in the three-phase structure shown in figure 5(b).



(a) (b)

Figure 5. Configurations of Single-phase and 3-pahse Buck 4QC

As the lower limit value of the QBC dc-side voltage is reduced about 50% compared with the half-bridge unit, the dc-side voltage lower limit value of one-phase and three-phase combined by QBC is reduced greatly. It is assumed that the peak value of each unit dc-side input voltage is E_S, and the compare of the dc-side voltage lower limit value between QBC and bridge structure is shown in table 1, which shows that the dc-side voltage lower limit value of QBC is reduced about 45% compared with the bridge structure. The dc-side output voltage of three-phase QBC doesn't contain fundamental wave and the second harmonic because of the three-phase symmetry of the three units output ripple. The one-phase QBC doesn't contain the fundamental wave because the fundamental waveforms of the two units are of reversal phase. However, the second harmonic still exits like the one-phase bridge structure.

Table 1. Comparison Of the Dc-side Voltage Lower Limit

Configurations	Unit Circuit	Single-phase Circuit	3-phase Circuit
Bridge Configuration	$2E_S$	$2E_S$	$\sqrt{3}\,E_S$
QBC Configuration	E_S	E_S	E_S

6. Conclusion

In this paper a new type quasi-buck four-quadrant topology is described in detail on the basis of the analysis to the traditional half-bridge four-quadrant, and the dc-side voltage of the topology can be reduced by about 50%. The MATLAB simulation and experiment results show:

(1) The quasi-buck four-quadrant topology is correct, reasonable and feasible. Though one more inductor L1 is employed in this topology, the lower limit value of the dc-side output voltage can be reduced by about 50%, and the lower limit of one-phase and three-phase converters composed of QBC unit can be reduced by 45% compared with the traditional bridge structure. Thus this topology is especially appropriate for the application of lower dc-side voltage.

(2)The SSA model of QBC unit is correct, and it stands for the practical operating characteristic of the high switching frequency basically.

(3) The analysis results of QBC unit model match up with the MATLAB numerical simulation and experiment waves, and the results describe the relationship between each state variable and circuit parameters quantitatively to supply the important theoretical basis for the QBC system parameter design.

7. References

[1] Jiasheng Zhang, Rongtai Hao. A New Type PWM Reversible Rectifier [J]. *Transactions of China Electrotechnical Society*, 1998, 13(5):37-41

[2] Jiasheng Zhang, Rongtai Hao. State Space Averaging Model and Simulation of the 4-Quadrant Converter[J]. *Joural of Northern Jiaotong University*,1998, 22(1):67-72

[3] Jiasheng Zhang, Rongtai Hao. A New Type 4-quadrant Converter-Topology, Modeling and Simulation[J]. *Electric Drive for Locomotive*, 1997(6):15-17

[4] Jiasheng Zhang, Rongtai Hao. A New Type Topology of 4-Quadrant Converters-Modeling. Analysis and Simulation [J]. *Acta Electronica Sinica*, 1998, 26(11):73-76+72
[5] Wei Li. Improvement of Single-phase Four-quadrant Converter Dual-loop Control [J]. *Electrical Drive for Locomotives*, 2017(5):22-25+34
[6] Yijie Shi, Xiao Li and Jianxin Guo. Research on a New Type of SVPWM Control Strategy in Four-Quadrant Converter [J]. *Journal of North University of China (Natural Science Edition)*, 2016, 37(6):601-605
[7] Minyao Huang, Wenhuan Yang and Tiantian Hou. Three-Phase Double Pwm Four Quadrant AC Power Transmission System [J]. *Electronic Sci. & Tech.*, 2016, 29(5):183-186