

Flexible and Printed Electronics



PAPER

Solution-processed flexible metal-oxide thin-film transistors operating beyond 20 MHz

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Abstract

Complementary metal-oxide-semiconductor, an elementary building block, allows for a high degree of implementation of logic circuits with relatively low power consumption and low manufacturing cost, which plays a vital role not only in current Si electronics, but also in printed flexible devices. To meet the looming challenges of the Internet of Things, p-channel thin-film transistors (TFTs) with an excellent mobility and processability have been increasingly developed using organic semiconductors. However, owing to the inherent electron-donating nature of organic compounds, the high performance of n-channel organic TFTs has yet to be demonstrated. Here, in this paper, we developed state-of-the-art solution-processed indium-zinc-oxide (IZO) TFTs with high electron mobility, sharp turn-on characteristics at 0 V, and excellent atmospheric stability and compatibility with wet patterning processes. With the damage-free lithography process in conjunction with the ultimate optimization of entire device processes, IZO-based TFT arrays were successfully fabricated via a solution process on flexible polyimide substrates. A cutoff frequency of 23 MHz in air was achieved, which is almost twice as fast as the frequency used in a near-field communication band. Furthermore, the as-fabricated IZO-based TFTs even function well under bending stress. Therefore, the current concept and technique is expected to open up opportunities to develop practical flexible devices with high-speed operation.

1. Introduction

The Internet of Things (IoT) demands trillions of advanced electronic devices, including radio-frequency identification (RFID) tags and various sensors, etc, with low manufacturing cost. In this context, printing technologies, particularly those using a semiconductor ink, i.e., printed electronics, have been studied a lot due to their potentially scalable and low-cost mass production. In addition, it is beneficial that such devices operate with extremely low power consumption because their potential power source is likely to be limited by implementable energy harvesters that generally feed a low electricity, such as a small battery, solar cell, thermoelectric power generator, and wireless power transmitter. All these trends are addressing the importance of integrated logic circuits

based on a complementary metal-oxide-semiconductor (CMOS), since CMOS-based circuits, in principle, exhibit very low standby power consumption, compared to unipolar logic circuits.

CMOS-based devices require high-performance and balanced p- and n-channel thin-film transistors (TFTs). In particular, high carrier mobility is indispensable for fast responses. From the printed electronics viewpoint, solution-processable organic semiconductors have been investigated for years, and recently, a hole mobility of $>10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ has been reported [1–4]. Indeed, various groups in the organic electronics community have developed semiconductor materials and device fabrication methods, making organic semiconductor-based high-speed circuits more and more realistic. For instance, the state-of-the-art p-type organic single-crystalline transistor

has a cutoff frequency, approaching 30 MHz, twice as fast the frequency used in near-field communications (13.56 MHz) [5]. Unfortunately, organic TFTs hardly exhibit high electron mobility because of the inherent, electron-donative nature of organic compounds. In contrast, some amorphous metal-oxide semiconductors (MOs), represented by indium gallium zinc oxides, show high electron mobility and satisfactory device stability, are the most likely candidate for an n-channel TFT [6–8]. However, the device implementation technology of solution-processed MOs still lies behind vacuum-based ones in terms of intrinsic device performances and chemical compatibility during device fabrication [9, 10].

Most present solution-processed MOS TFT-based practical electronic applications, such as display panels and sensors [11–15], only require low operation frequencies (hundreds of hertz). Thus, fine-patterning processes with high spatial resolution and a high degree of integration concomitantly with ultimate compatibility to solution processability has not been developed yet. For more advanced electronic devices, such as rectifiers, frequency dividers, clock generators (a component of RFID tags), analog-to-digital converters, amplifiers, and advanced sensors, a single component of TFT should operate at higher cutoff frequencies. To achieve this, TFTs with high carrier mobility and short channel lengths in the range of less than a few micrometers are required, because the cutoff frequency is governed predominantly by the channel length, the overlapping area between the gate and the source/drain (S/D) electrodes, and the carrier mobility. It should be noted that the bottom-gate and top-contact TFT structure is commonly employed for MOS-based TFTs; therefore, a critical technique to finely pattern the S/D electrodes directly onto the surface of MOS thin films is a key engineering technique. Although some patterning methods, such as inkjet printing [16, 17], microscale soft patterning [18], reverse offset printing [19], and nano-rheology printing [20] have been developed for MOs and S/D electrodes, none of these can simultaneously yield high spatial resolution, good registration, and high-performance requirements.

Photolithography, which is often used in the silicon industry, is not only a reliable patterning technique, but it is also one of the most promising ways to realize fine patterning. However, in contrast to the silicon industry, the fabrication of S/D electrodes on MOS layers is very challenging due to chemical compatibility issues, which are likely to be more serious in solution-processed MOs than in vacuum-deposited ones [10]. For instance, acid etchants or plasma used in etching processes could damage the MOS layer, and the strong alkaline developer of the photoresist for lift-off processing can deteriorate MOS layers and dissolve aluminum (Al), which is often used for the S/D electrodes in solution-processed MOS-based TFTs. Some new photolithography methods have been reported to

form a fine pattern for fragile systems, such as using wool keratin as a resist [21], or use of a passivation layer to protect the active semiconductor layer [22]. However, questions still remain regarding the reproducible, large-scale fabrication requirement of the IoT devices in such growing methods.

In this work, we demonstrated an effective photolithography process using a mild photoresist developer, aqueous Na_2CO_3 , which enabled damage-free and high-resolution patterning of both solution-processed MOs and Al S/D layers. Indium zinc oxide (IZO) was used in this study for a proof-of-concept demonstration [23–26]. Solution-processed IZO-based TFTs were fabricated on a $6 \times 6 \text{ cm}^2$ flexible polyimide (PI) substrate, and were then examined with respect to the reliability of the patterning process, including the carrier mobility, threshold voltage, contact resistance, high-frequency transistor response, and the mechanical flexibility. Notably, a cutoff frequency of 23 MHz, which is almost twice as fast as the frequency used in the near-field communication band, in air was achieved in a high-resolution patterned short-channel IZO-based TFT. Therefore, it can be expected that the state-of-the-art CMOS circuits with low power consumption and high operational speed will be realized by combining them with existing p-type organic semiconductors, which constitutes a step forward toward the implementation of flexible, printed logic circuits and sensors.

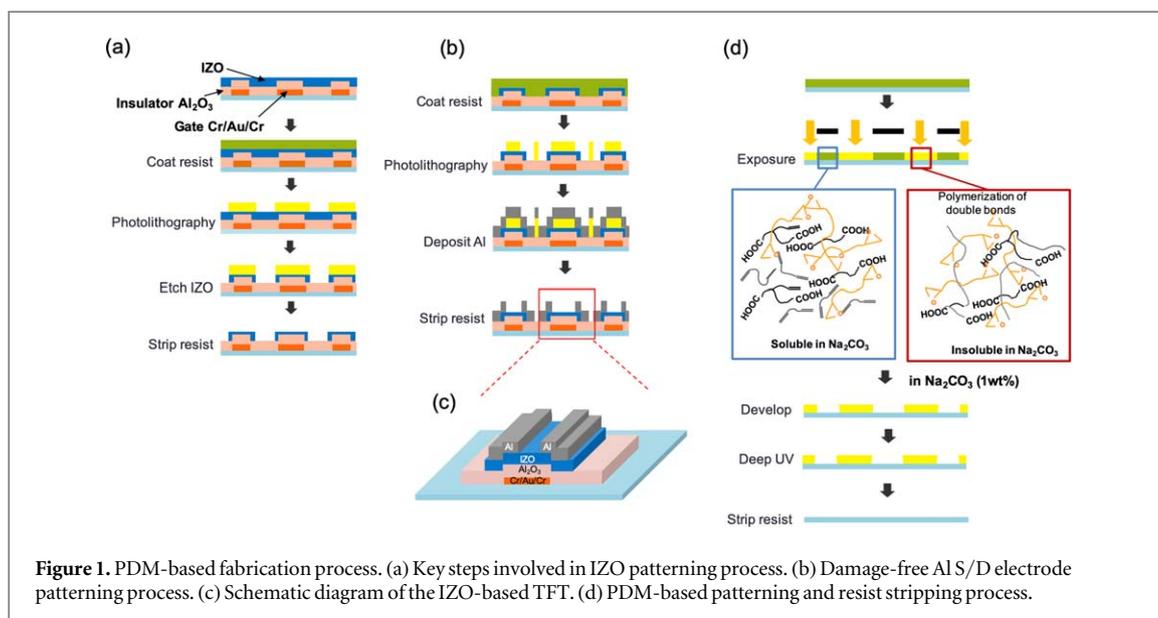
2. Methods

2.1. IZO precursor solution

IZO thin films were prepared by a conventional sol-gel method. All procedures were conducted in air. As shown in figure S1 available online at stacks.iop.org/FPE/5/015003/mmedia, indium nitrate hydrate ($\text{In}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}$) (Aldrich) and zinc nitrate hexahydrate ($\text{Zn}(\text{NO}_3)_2 \cdot 6\text{H}_2\text{O}$) (Aldrich) were separately dissolved in 2-methoxyethanol with a concentration of 0.1 M. Both solutions were stirred at room temperature for at least 6 h to achieve homogeneous solutions. The solutions were then mixed at an In-to-Zn ratio of 3:2, followed by stirring at room temperature for at least 6 h before use. Although structural and elemental analyses of the present IZO thin films were not performed in this study, it was assumed that typical ternary metal oxides are formed homogeneously with a minimum amount of residues and defects, which was evidenced by the observation of ideal transistor characteristics.

2.2. PI substrate preparation

A PI film was used as a post-delaminable substrate. To form a $10 \mu\text{m}$ thick PI film, polyamic acid (Ube Industries, Ltd) was spin coated on a glass substrate ($6 \times 6 \text{ cm}$) at a speed of 2000 rpm for 3 min, and then heated in ambient atmosphere on a hot plate at $110 \text{ }^\circ\text{C}$



for 60 min, 150 °C for 30 min, 200 °C for 10 min, 250 °C for 10 min, and 430 °C for 10 min in a step-by-step manner.

2.3. Device fabrication

Conventional photolithography was used to prepare the gate electrodes, as shown in figure S2. First, the PI substrate was subjected to deep ultraviolet (DUV) irradiation to clean the surface and improve the adhesion between the PI and gate electrode. The photoresist (TLOR, Tokyo Ohka Kogyo Co., Ltd) was then spin coated and subjected to gentle heating at 90 °C for 2 min. The photoresist was then subjected to photographic exposure at 300 mJ cm⁻² using a digital exposure device (MLA150, Heidelberg Instruments) and post-heating at 110 °C for 90 s, with subsequent development with a developer (NMD-3, Tokyo Ohka Kogyo Co., Ltd) and rinsing with water. Layers of 5 nm thick Cr, 25 nm thick Au, and 5 nm thick Cr were sequentially evaporated as a gate electrode. After removal of the remaining resist, a 75 nm thick Al₂O₃ layer was formed by atomic layer deposition as the gate dielectric layer.

The procedure for the formation and patterning of the IZO layer is shown in figure 1(a). First, the substrate was cleaned by DUV, and the precursor solution was then spin coated at 500 rpm for 5 s and at 5000 rpm for 30 s. Thermal annealing was then performed on a hot plate at 150 °C for 5 min and 370 °C for 1 h to yield an IZO layer with a thickness of *ca.* 10 nm. For IZO patterning, a photosensitive dielectric material (PDM; Taiyo Ink Mfg. Co., Ltd) was spin coated at 5000 rpm for 120 s, followed by gentle heating at 75 °C for 30 min. Fine PDM patterns were formed under the following conditions: exposure at 1000 mJ cm⁻², development with aqueous Na₂CO₃ (1 wt%) at room temperature for 150 s and rinsing with water. After this, the unprotected IZO was etched

by immersion in oxalic acid (1.75 wt%) for 3 s and rinsed with water. DUV irradiation under an oxygen atmosphere for 20 min was then performed, followed by treatment with *N*-methylpyrrolidone to remove most of the resist. Finally, the substrate was again exposed to DUV in an oxygen atmosphere for 30 min and sintered at 370 °C for 1 h in air to further remove the residual resist and solvent.

To complete the device fabrication, a conventional Nd:YAG laser was used to make through-holes for the bottom-gate electrodes. An Al layer (60 nm) as S/D electrodes was then thermally evaporated and patterned via the lift-off process based on the photoresist PDM (figure 1(b)). The patterning and stripping processes were performed under the same conditions as the IZO etching process. A schematic diagram of as-fabricated IZO-based TFT is shown in figure 1(c).

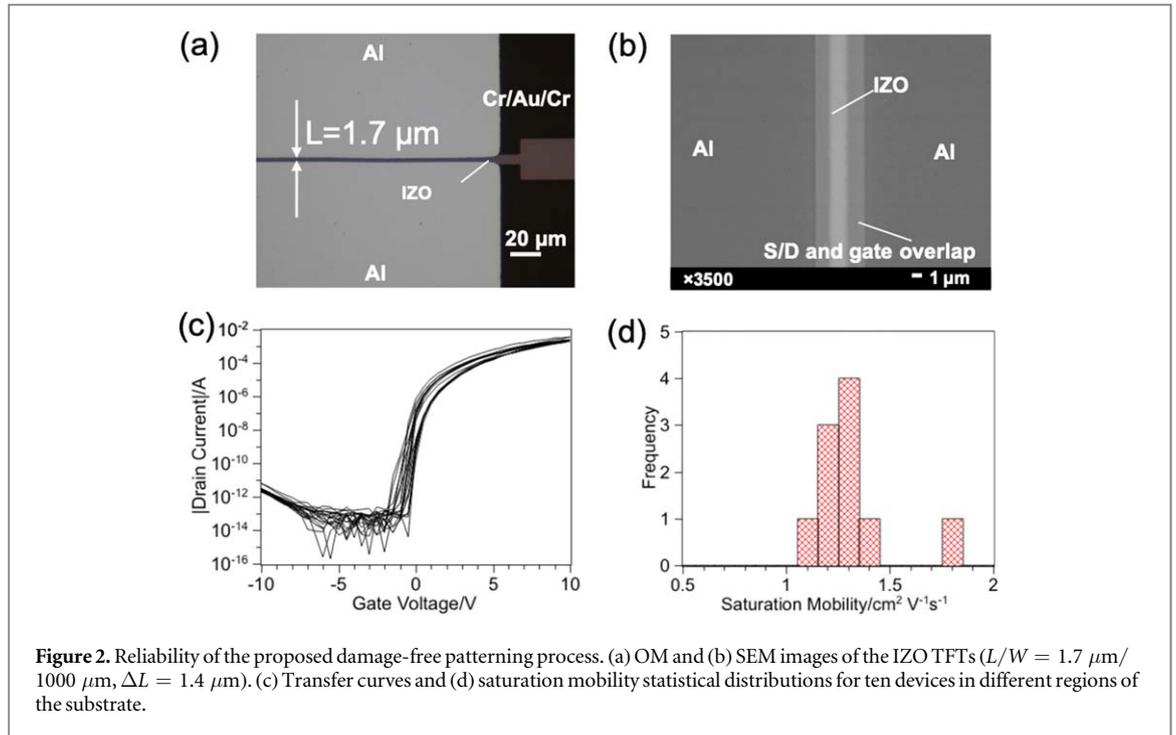
2.4. Device characterization

All electrical measurements were conducted under ambient air and dark conditions. TFT properties were evaluated using a semiconductor parameter analyzer (Keithley 4200-SCS). Dynamic measurements for the evaluation of the cutoff frequency were conducted with the same setup as reported in our previous work [5], the details of which are given in the supporting information (section 1). Images of the IZO TFTs were acquired using optical microscopy (OM) and scanning electron microscope (SEM; JEOL JSM-7600F). The thickness of the IZO layer was measured with a stylus profiler (Bruker Dektak XT).

3. Results and discussion

3.1. Fabrication and process reliability

The critical point in the present study is the utilization of a PDM composed of epoxy resins, carboxylic acid resins, and photosensitive monomers for patterning of



the IZO layer and Al S/D electrodes. Figure 1(d) shows the detailed process scheme and chemical reactions of the resist. During the exposure process, irradiation with UV light causes polymerization of photosensitive monomers, making the exposed photoresist insoluble in aqueous Na_2CO_3 , while the unexposed parts are still soluble. DUV was employed to sever the chemical bonds of the polymerized resist to make it readily removable. Further details on PDM can be found in the literature [27, 28]. Thus, the IZO layer and S/D electrodes in this study were prepared by employing the PDM. For the IZO patterning process, after fabrication of the IZO layer, PDM was spin coated on the as-fabricated substrate and patterned by UV exposure and developed with aqueous Na_2CO_3 . The unprotected area of the IZO was then etched with oxalic acid. For the Al S/D electrode fabrication process, PDM was patterned first and used as a mask for Al deposition. The patterned Al S/D electrodes were then obtained by a lift-off technique.

To demonstrate the viability of the current process for large-scale integrated circuits, TFT arrays were fabricated on a $6 \times 6 \text{ cm}$ PI substrate. OM (figure 2(a)) and SEM (figure 2(b)) images of a short-channel TFT [channel length/channel width (L/W) = $1.7 \mu\text{m}/1000 \mu\text{m}$, and the overlap between gate and S/D electrodes of $1.4 \mu\text{m}$] confirmed well-defined patterns. Hence, the optimized feature size of this process was estimated to be *ca.* $1.5 \mu\text{m}$. To discuss the scalability and homogeneity, the TFT properties having the same dimensions were evaluated by ten devices in different regions of the substrate. To obtain the curves of the transfer characteristics, the gate voltage (V_G) dependence of the drain current (I_D) was fitted using the following equations:

in the linear region,

$$I_D = \frac{W\mu_{\text{lin}}C_i}{L}(V_G - V_{\text{th}})V_D, \quad (1)$$

and in the saturation region,

$$I_D = \frac{W\mu_{\text{sat}}C_i}{2L}(V_G - V_{\text{th}})^2, \quad (2)$$

where μ_{lin} and μ_{sat} are the carrier mobilities in the linear and saturation regions, respectively. C_i is the gate capacitance per unit area and V_{th} is the threshold voltage.

The overlaid transfer curves (figure 2(c)) and the statistical distributions of μ_{sat} (figure 2(d)) indicate homogeneity over the substrate with $\mu_{\text{sat}} > 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The transfer characteristics and μ_{sat} statistical distributions of the device with $L/W = 1.7 \mu\text{m}/1000 \mu\text{m}$, $L/W = 5 \mu\text{m}/1000 \mu\text{m}$ and $L/W = 20 \mu\text{m}/1000 \mu\text{m}$ (overlap between gate and S/D electrodes of $2 \mu\text{m}$) can be found in the supporting information (figure S4). The good overlaps of the transfer curves of different devices imply that this process can be used for large-scale integrated circuits based on solution-processed MOSs.

3.2. Transistor characterization

With a decrease in the TFT channel length, the heterointerface between the S/D electrodes and the semiconductor, i.e., the contact resistance, plays an increasingly dominant role in TFT performance. Therefore, transistor characterization was conducted with varied L of 1.7, 2.5, 5, and $20 \mu\text{m}$. Figure 3(a) shows OM images of TFTs with various L . Transfer curves in the saturation ($V_D = 10 \text{ V}$, figure 3(b)) and linear regions ($V_D = 3 \text{ V}$, figure 3(c)), and output curves (figure 3(d)) for the corresponding TFTs

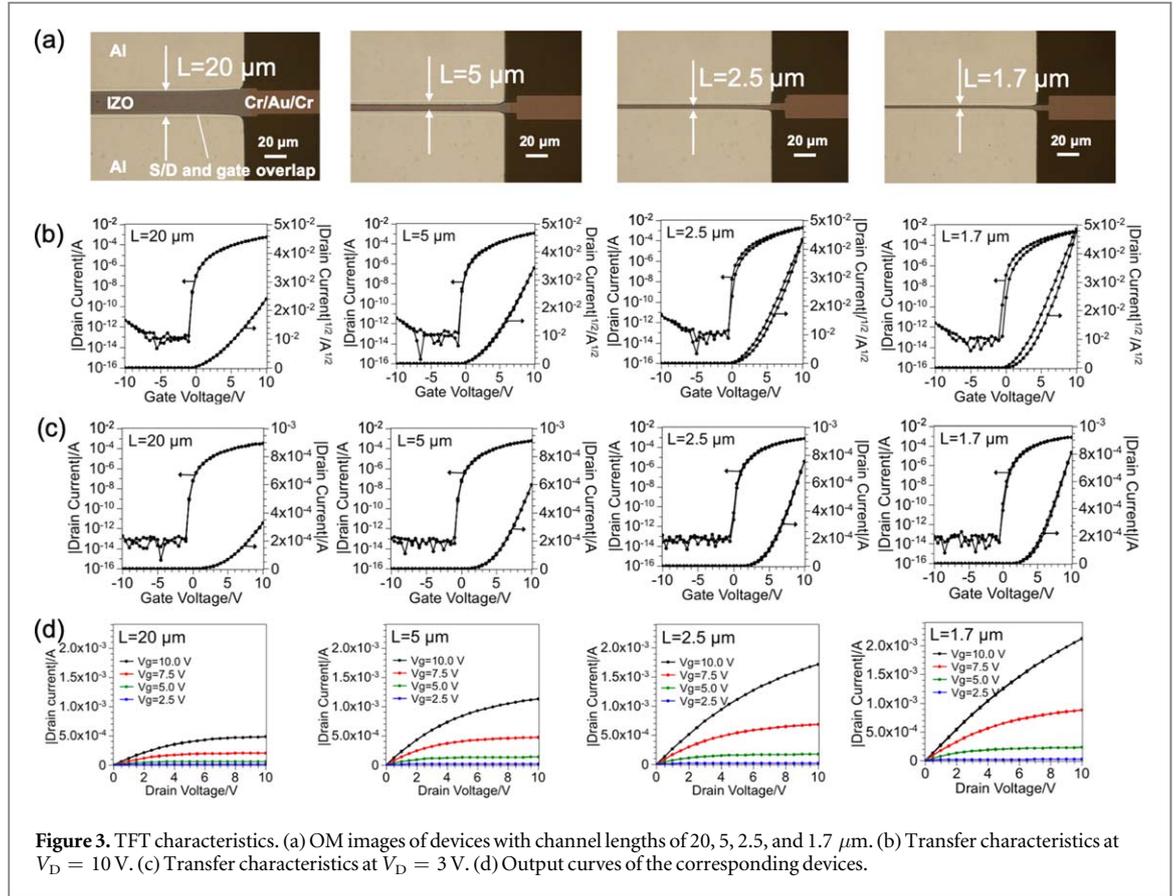


Figure 3. TFT characteristics. (a) OM images of devices with channel lengths of 20, 5, 2.5, and 1.7 μm . (b) Transfer characteristics at $V_D = 10$ V. (c) Transfer characteristics at $V_D = 3$ V. (d) Output curves of the corresponding devices.

revealed that all devices exhibited negligible hysteresis, a turn-on voltage (V_{on}) of *ca.* 0 V, an off current (I_{off}) as low as 10^{-13} A, and an on-off current ($I_{\text{on}}/I_{\text{off}}$) ratio as high as 10^{10} . We suspect that slight hysteresis of the device with $L = 1.7 \mu\text{m}$ is caused by the contact resistance, since compared with the long channel device, contact resistance play a more important role in determining device performance; this will be discussed more detail in sections 3.3 and 3.4. In addition, μ_{sat} were 1.5, 1.8, 2.5, and $4.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for devices with $L = 1.7, 2.5, 5.0,$ and $20.0 \mu\text{m}$, respectively. V_{th} at $V_D = 10$ V was 1.8 V for the TFT with $L = 1.7 \mu\text{m}$, and 2.4 V for the other TFTs with larger L . The μ value increased significantly with an increase of V_G , as typically found for highly disordered systems. For instance, as the operation voltage was increased from 10–15 V, μ_{sat} increased from 4.2 – $7.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the TFT with $L = 20 \mu\text{m}$, as shown in figure S5.

The good TFT performance can be attributed to the high-performance IZO active layer [26], which is shown in figure S6, obtained via methods 2.1, and the damage-free process with the use of a resist that can be processed with a mild developer (1 wt% aqueous Na_2CO_3) for patterning of the IZO layer and S/D electrodes. In contrast, with conventional photolithography processes that typically employ a strong alkaline solution as the developer, such as aqueous TMAH, the resultant TFTs have large hysteresis and a high off current (figure S7(a)). Similar phenomena

have also been reported by Lee and co-workers [18]. In addition to the Al S/D electrodes losing their metallic luster (figure S7(b)), it has also been suggested that serious chemical damage results from conventional photolithography. Besides, a comparison of the effects of different developers is shown in figure S8, and almost no performance deterioration was detected for the TFT with immersion in Na_2CO_3 (1 wt%) for 150 s. In contrast, TFTs after immersion in TMAH (2.38 wt%) for the same time, showed lower performance.

3.3. Contact resistance

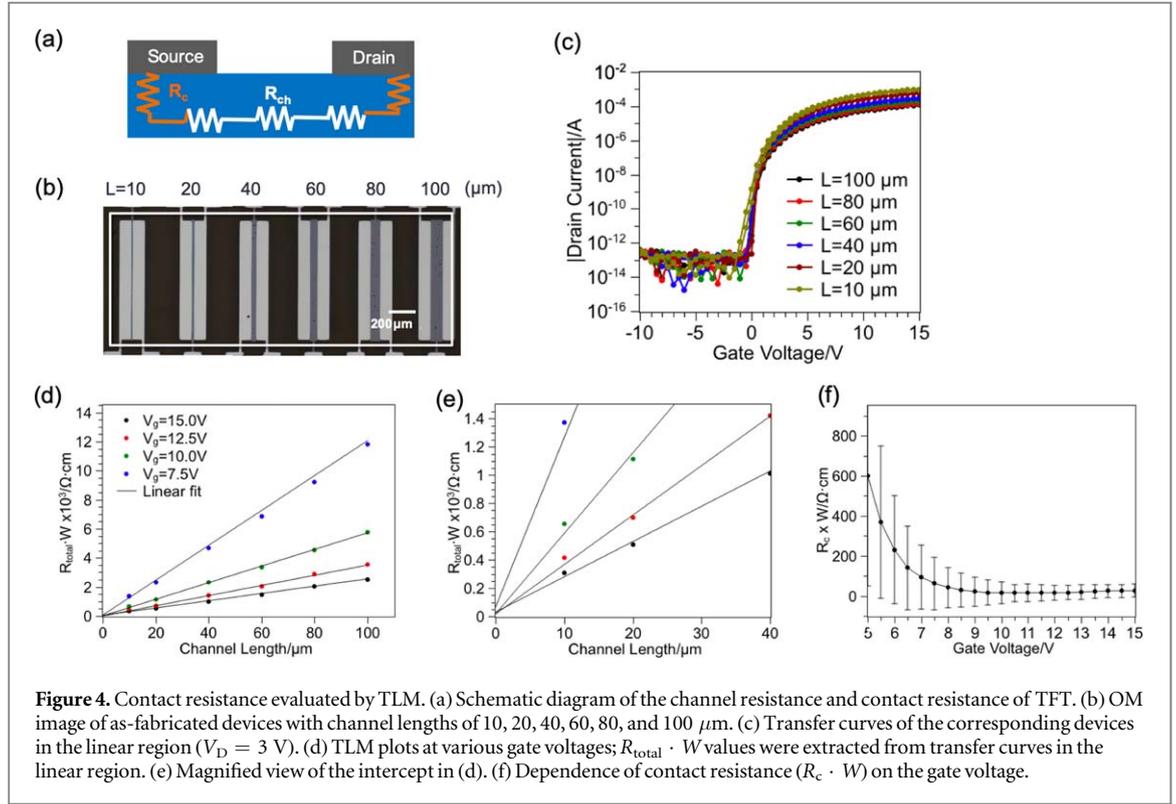
The contact resistance of the IZO-based TFT prepared using the proposed damage-free process was estimated by the transmission line method (TLM) [29–31]. As shown in figure 4(a), the total resistance (R_{total}) of a TFT is the sum of the channel resistance (R_{ch}) and the contact resistance (R_c). In the linear region, R_{ch} can be approximated to be uniform and is thus expressed as:

$$R_{\text{ch}} = \frac{L}{W\mu_{\text{lin}}C_i(V_G - V_{\text{th}})}. \quad (3)$$

R_{total} normalized by W can be expressed as:

$$R_{\text{total}} \cdot W = \frac{L}{\mu_{\text{lin}}C_i(V_G - V_{\text{th}})} + R_c \cdot W. \quad (4)$$

By plotting $R_{\text{total}} \cdot W$ as a function of L and subsequent linear fitting, $R_c \cdot W$ can be calculated from the intercept with the y -axis.



TFTs with various L of 10, 20, 40, 60, 80, and 100 μm were prepared to study the R_c embedded in the current process (figure 4(b)). The transfer curves of corresponding devices in the linear region ($V_D = 3\text{ V}$, figure 4(c)) suggested these TFTs have reasonable TFT performance, with V_{th} of ca. 6 V and μ_{lin} of 3.7, 4.5, 4.6, 4.9, 4.5, and 4.7 $\text{cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for L of 10, 20, 40, 60, 80, and 100 μm , respectively. As shown in figures 4(d) and (e), $R_{\text{total}} \cdot W$ and L have good linear correlations at every V_G featured, and thus $R_c \cdot W$ was fairly estimated to be dependent on V_G (figure 4(f)). It should be noted that at $V_G > 8.5\text{ V}$, $R_c \cdot W$ is no longer independent of V_G , being ca. 29 $\Omega\text{ cm}$, which is categorized into a class of the lowest contact resistance reported to date for organic and solution-processed MOS-based TFTs [5, 16, 32], and indicates the potential for high-frequency operation. In addition, the low contact resistance can be attributed to the uniformity of the solution-processed IZO, and the clean interface between IZO and the Al S/D electrodes, the latter of which is due to the extra DUV treatment to remove the resist residue after the IZO etching process. In contrast, a larger contact resistance was implied in other TFTs fabricated without the extra DUV treatment, as shown in figure S9.

3.4. Cutoff frequency

The current-gain cutoff frequency (f_T), which has been used to qualify the operation speed of the devices [9], was assessed to estimate the intrinsic frequency response of the present IZO-based TFTs. In principle, when the operation frequency reaches the cutoff frequency, the output current (i_{out}) becomes equal to

the input current (i_{in}), so that the power gain (gain-dB) becomes 0 dB in response to the applied AC gate voltages (v_g). Considering a TFT that is operated in the saturation region with v_g , i_{in} due to gate capacitance (C_G) can be described as

$$i_{\text{in}} = v_g j C_G, \quad (5)$$

and i_{out} due to transistor effect can be defined as:

$$i_{\text{out}} = -v_g g_m, \quad (6)$$

where j is the imaginary unit and g_m is the device transconductance ($g_m = \frac{\Delta I_D}{\Delta V_G}$), calculated in the saturation region [$g_m = \frac{C_i \mu_{\text{eff}} (V_g - V_{\text{th}})}{L}$]]. Thus, f_T and gain-dB can be expressed as:

$$f_T = \frac{g_m}{2\pi C_G} = \frac{\mu_{\text{eff}} (V_G - V_{\text{th}})}{2\pi L (L + 2\Delta L)}, \quad (7)$$

$$\begin{aligned} \text{gain-dB} &= 20 \log \left(\frac{i_{\text{out}}}{i_{\text{in}}} \right) = 20 \log \left(-\frac{g_m}{j\omega C_G} \right) \\ &= 20 \log \left[\frac{\mu_{\text{eff}} (V_G - V_{\text{th}})}{2\pi f L (L + 2\Delta L)} \right], \end{aligned} \quad (8)$$

where ΔL is the overlap between the gate and S/D electrodes, as shown in figure 5(a), and μ_{eff} is the effective mobility, which can be derived by taking into account the contact resistance as shown in the equation (9):

$$\mu_{\text{eff}} = \frac{\mu_{\text{int}}}{1 + \frac{R_c W}{L} \mu_{\text{int}} + C_i (V_g - V_{\text{th}})}, \quad (9)$$

where μ_{int} is the intrinsic mobility.

From equation (9), we can also see that contact resistance is dominant in the short-channel device

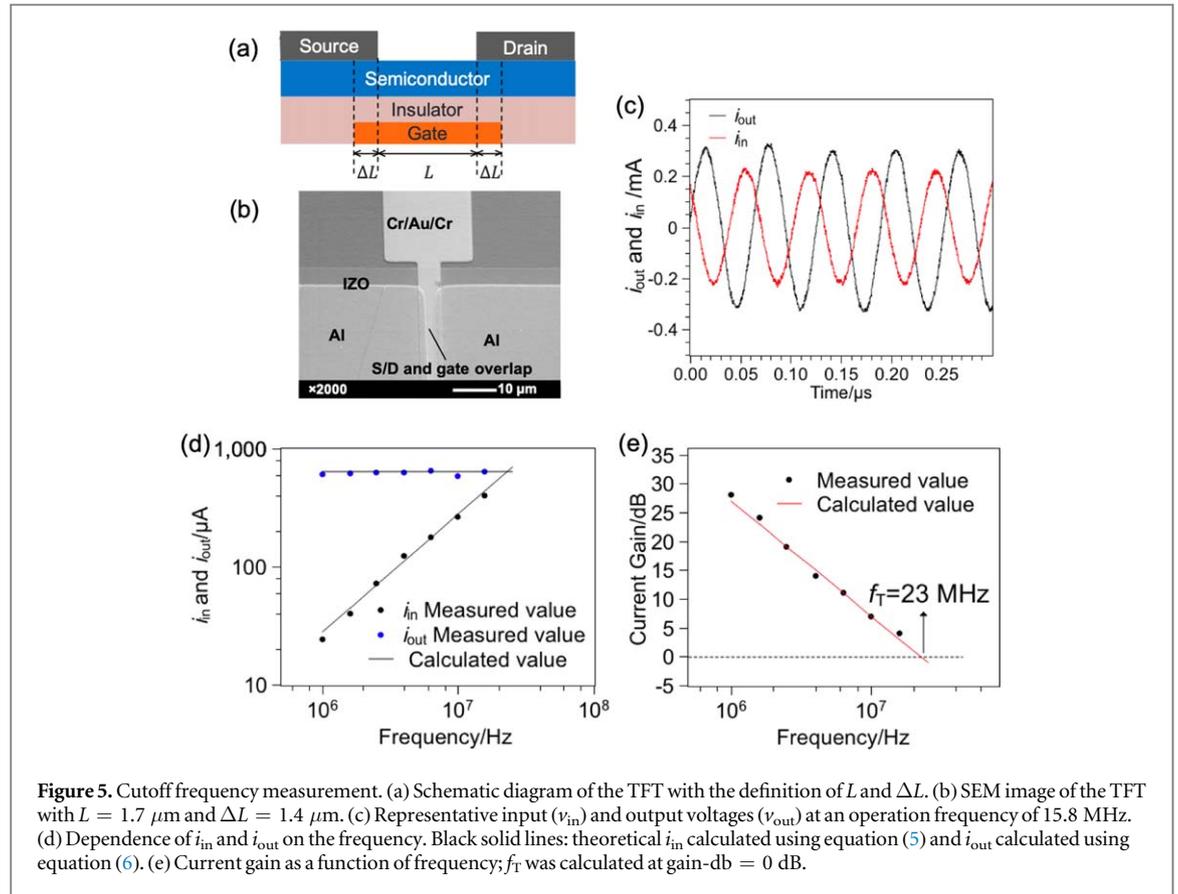


Table 1. Comparison of V_G -normalized f_T for solution-processed TFTs.

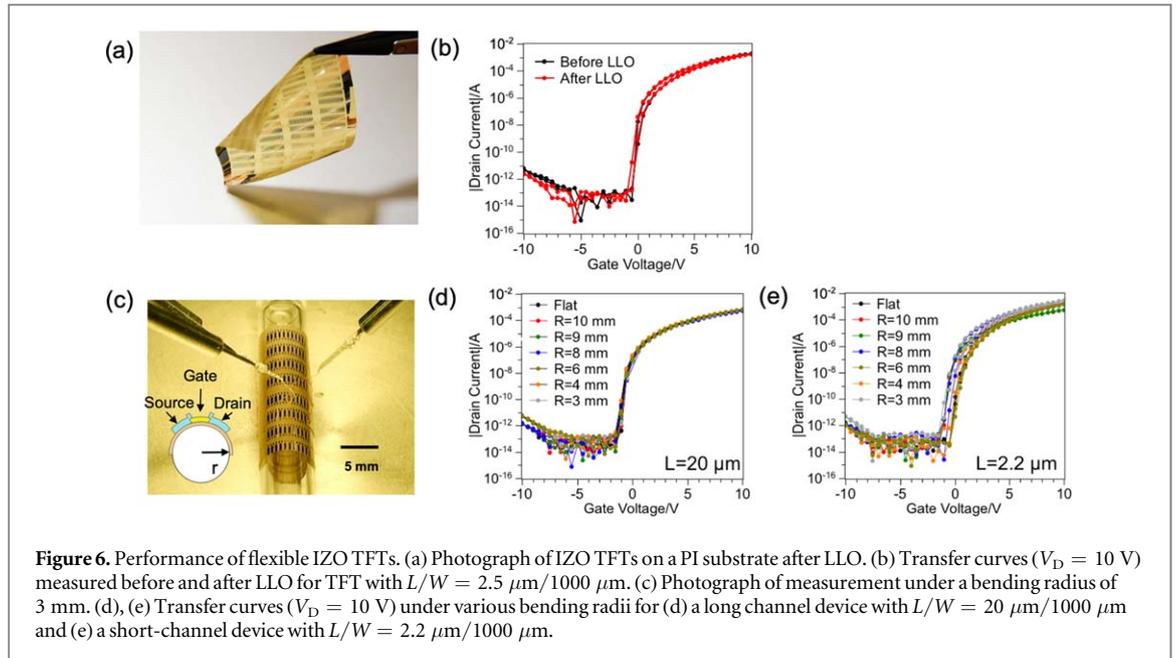
Semiconductor	Process	Mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	V_G (V)	f_T (MHz)	f_T/V_G (MHz V^{-1})	References
IZO	Spin coating	1.4	10	23	2.3	This work
C_{60}	Evaporated	2.22	25	27.7	1.1	[33]
Rubrene	PVT	4.0	15	25	1.7	[34]
C_8 -DNBDT-NW	Continuous edge casting	2.7	10	20	2	[5]
$\text{P}(\text{NDI}_2\text{OD-T}_2)$	Bar coating	0.9	30	20	0.67	[35]
C_{10} -DNNT	Evaporated	No data	20	20	1	[36]
DNTT	Evaporated	0.44	15	20	1.3	[37]
C_{10} -DNNT	Evaporated	2.5	10	19	1.9	[38]
C_{10} -DNNT	Edge casting	No data	20	10	0.5	[39]
$\text{P}(\text{NDI}_2\text{OD-T}_2)$	Bar coating	No data	7	14.4	2.06	[40]
IGZO	Spin coating	12.9	15	4.7 ^a	0.312 ^a	[41]

^a Estimated from the result of decay time obtained for the ring oscillator.

with a channel length of a few micrometers, and this result is consistent with the result in section 3.2.

To demonstrate the usefulness of the present TFTs for high-speed operation, the dynamic response of the device was investigated and the results are shown in figure 5 ($L/W = 1.7 \mu\text{m}/1000 \mu\text{m}$, $\Delta L = 1.4 \mu\text{m}$; SEM image in figure 5(b)). The static TFT properties ($\mu_{\text{sat}} = 1.4 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $V_{\text{th}} = 2 \text{V}$) were characterized prior to the dynamic measurement. For the dynamic measurement, DC signals of V_G and V_D were set to 10 V. A small AC signal (v_g) of 1 V was also applied to the gate terminal. Figure 5(c) shows the waveforms of i_{in} and i_{out} in response to v_g at a frequency of 15.8 MHz. The phase difference between

the input and output signals was $\pi/2$, which is consistent with the theory. The measured and calculated values of i_{in} and i_{out} are plotted as a function of frequency in figure 5(d). The calculated i_{in} was obtained from equation (5), where the gate capacitance C_G , measured from the capacitance–voltage characteristics (details given in the supporting information, section 2) was 4.6 pF for the device in question. In addition, i_{out} was calculated using equation (6). As shown in figure 5(d), the calculated i_{in} and i_{out} were consistent with the measured values. These were also converted to the power gain as a function of frequency (figure 5(e)), where an extrapolation of the linear fit crossing 0 dB at 23 MHz was regarded as f_T . For



reasonable comparison, f_T was normalized by the DC voltage applied, i.e., V_G , since f_T is a function of V_G as described in equation (7). The V_G -normalized f_T ; f_T/V_G is shown in table 1, along with some related reports. Since research on solution-processed metal-oxide semiconductor are still focusing on single device, cutoff frequency related reports are very rare. So here we listed TFTs based on the concept of organic or printed electronics. It should be noted that f_T/V_G in the present IZO-based device is the highest reported to date among TFTs of organic or printed electronics.

3.5. Flexibility

After completing all the procedures, the PI substrate was delaminated from the glass support by a laser lift-off (LLO) technique to evaluate the TFT properties under bending stress [42]. Figure 6(a) shows a photograph of the free-standing PI film with TFT arrays. After delamination, it was confirmed that the TFTs exhibited negligible performance degradation (figure 6(b)). The TFT performance under bending stress with different bending radii of 10, 9, 8, 6, 4, and 3 mm was evaluated by winding the film around cylinders with the respective radii. A photograph of measurement under a bending radius (r) of 3 mm is shown in figure 6(c). Figure 6(d) compares the transfer curves of a TFT with $L = 20 \mu\text{m}$ under various bending radii, where no deterioration was observed, even under the maximum bending stress attempted. In addition, figure 6(e), which shows the TFT properties with a shorter L of $2.2 \mu\text{m}$, revealed almost negligible effects of bending, although V_{on} was shifted negatively (*ca.* 1 V). This negative V_{on} shift can probably be attributed to the bias stress effect because the bias stress in a short channel ($L \leq ca. 2 \mu\text{m}$) device was found to be more significant than that with longer L , as can be found in the supporting information

(section 3). Since the transfer performances under different bending radii were not measured by the order of radii, the transfer curves shown in figure 6(e) did not show a rule with different bending radii. Notice that the one measured later suffered more bias stress. Atmospheric oxygen or moisture are typically considered an origin of bias stress. Therefore, a sealing process is expected to improve the resistance to bias stress, and further investigation on such improvements is ongoing.

We suspect that probably owing to the low thickness of inorganic materials (Al_2O_3 insulation layer of 75 nm, IZO active layer of about 10 nm), even for the brittle inorganic materials, no degradation, such as cracks, has been detected in this study (figure S12) [43].

4. Conclusion

Based on the concept of printed/flexible electronics, high-performance n-channel TFTs based on solution-processed IZO were demonstrated on a flexible PI substrate. In this work, an effective, damage-free patterning process was established to produce finely patterned IZO-based TFT arrays, and a short channel length down to $1.7 \mu\text{m}$ was realized. The crucial point of this new method is the utilization of a mild resist developer (aqueous Na_2CO_3) instead of conventional resist developers such as aqueous TMAH, which suppresses chemical damage to the IZO and Al S/D layers. The TFTs exhibited carrier mobilities of $>1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in air, accompanied by negligible hysteresis and high on-off current ratios up to 10^{10} under operation at 10 V. In addition, a potential application to high-speed electronic circuits was demonstrated by cutoff frequency measurements to realize $f_T = 23 \text{ MHz}$ with an operation voltage of

10 V. It is noteworthy that the voltage-normalized f_T value of 2.3 MHz V^{-1} is the highest among organic or printed electronics reported to date. Taking into account the stability of the TFT performance under bending stress, the proposed damage-free patterning process is expected to open opportunities for MOS-based flexible integrated circuits and wearable applications.

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