IOP Conf. Series: Journal of Physics: Conf. Series **1455** (2020) 012023 doi:10.1088/1742-6596/1455/1/012023

Solution-Processed Amorphous Zinc Oxide Thin Film Transistor Based NAND Gate

Omprakash S S and Naveen Kumar S K
Department of Electronics, Mangalore University, Mangalore 574199, India
Email-id: ompaks@gmail.com

Abstract —Herein, we discuss the synthesis and deposition of thin films amorphous zinc oxide (a: ZnO) by custom-designed spray pyrolysis unit for Thin Film Transistor (TFT) application towards NAND gate fabrication. Top gate top contact TFT was fabricated on a glass substrate, a: ZnO as the channel layer, PVA as gate dielectrics material and Al as electrodes. Electrical properties of a: ZnO TFT (W/L= 500/200µm) were probed. The individual transistor with a threshold voltage (V_{th}=2.1 V), off and on current (I_{off} = order of 10^{-8}A; I_{on}= 10^{-3}) and Ion /I_{off} ratio (order of 10^{5}). The linear mobility is calculated and obtained as 3 cm^{-2}/Vs. NAND gate is one of the universal and basic building blocks of a digital circuit. The fabricated NAND gate is subjected to the logic operation in the range of 0 to 10V was tested. The result implies that it can be utilized for logical circuit operation.

Keywords—NAND gate, spray pyrolysis unit, TFT, ZnO.

1. INTRODUCTION

Thin Film Transistor (TFT) is a special kind of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) which is built by layering thin films of an active semiconductor layer, dielectric layer and metallic layers over a supporting substrate as shown in Fig 1. TFT is classified into four types as organic [1], inorganic, silicon-based [2], and hybrid [3] kind (a combination of organic and inorganic). Oxide semiconductors (OS) based TFT come under the inorganic TFT which have attracted present researcher. Oxide semiconductor used for fabrication of TFT is IGZO, SnO_2, IZO, GZO and ZnO. The oxide semiconductor has gained attention due to numerous merits like transparency [4], low temperature [5], excellent chemical stability, higher mobility and process versatility [6]. OS-TFT is the promising technology for the next generation of transparent, wearable and flexible [7] consumer electronics [8].

Although OS-TFT [9] [10] has gained a lot of attention and demonstrated higher performance than the Silicon-based TFT, this TFT is fabricated in vacuum-based process. In the vacuum-based process, there still exists bottleneck concerning fabrication onto larger areas, use of the non-vacuum compatible substrate and cost reductions of manufacturing. These led to the emergence of the solution-processed technique [11] [6] which includes Spin coating [12], spray coating [7], doctor blade coating and dip coating. Among solution-processed the spray pyrolysis has gained more consideration due to its economical process, masking capability and is a large area coating process.

Among these Oxide semiconductors, ZnO [13] has gained much attention due to its nature of stability, nontoxic and ease of solubility in all the solvents [10]. However, most of the ZnO-based TFT have used mostly SiO_2 as dielectrics. The others use metal oxides such as Al_2O_3[14], Y_2O_3[15], TiO_2[16]and ZrO_2[17]. Since these dielectric materials use a higher temperature for their deposition, polymers such as cellulose acetate [18], PDMS, PVA [19] and PVP [20] are deposited at low temperature hence they gained great attention.

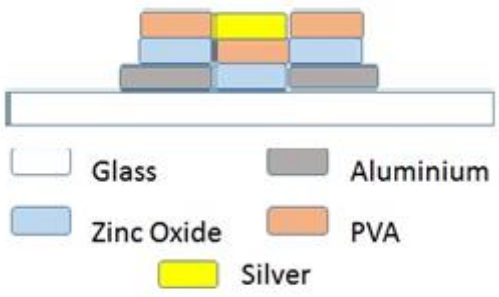

Fig 1 Schematic of TFT

In this paper, we discuss the synthesis of ZnO and PVA solutions. The fabrication of thin films of ZnO, Al and PVA were carried out a bare glass substrate using custom designed and fabricated mask. These were integrated to fabricate of ZnO TFT. The input and output characteristics of the TFT were studied. The TFT were interconnected to form a digital circuit i.e., NAND gate and the operations of the NAND gate was studied.

2. MATERIALS AND METHODS:

2.1. Materials

Zinc acetate dehydrated, acetic acid and methanol were purchased from Finar Limited. PVA (cold water soluble) is procured by Himedia. Conductive Pen Micro Tip (sliver pen) was purchased from Chemtronics. Electrical properties such as input and output characteristics of the TFT were carried out at MIT Manipal probe station with Keithley Instruments. The output characteristics of the NAND gate was performed at Mangalore University electronics laboratory.

2.2. Synthesis

ZnO solution: Zinc acetate dehydrated precursor is dissolved in a mixture of methanol and deionized water in a proportion of 2:1 to form a solution of 0.3M. While stirring the solution, a few drops of acetic acid are added to form a transparent solution.
PVA Solution: The PVA granules of 0.5g were dissolved in 10ml of double distilled water and stirred for 30 minutes to form a homogenous solution. The solution is kept for ageing for one day to make it more viscous.

2.3. TFT Fabrication

The aluminium as the source and a drain electrode (100nm) that were thermally evaporated on to an ultrasonically cleaned glass substrate with a customized shadow mask with the parameter is shown in Table I and Fig 2(a).

Table I
Parameter for Al deposition for electrodes

Source material	Aluminium
Base vacuum	5×10^{-5} mbar
Rate of deposition	5-6 Å
Substrate rotation	On
Substrate temperature	70 °C

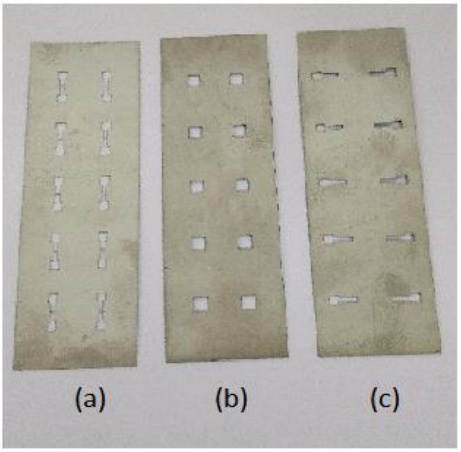

Fig 2 Image of the mask used for a) source and drain electrode b) channel layer c) gate electrode

The synthesized ZnO solution is spray-coated with custom design spin spray unit onto preheated aluminium-coated glass and plain glass substrates with a shadow mask aligned with respect to the gate and

source. The parameter for the deposition of ZnO film is shown in Table II and Fig 2(c).

Table II
Parameter for deposition of ZnO thin film.

Nozzle	Glass
Solution concentration	0.3 M
Solvent	Method and DI water (2:1)
Nozzle–substrate distance	25 cm
Flow rate and volume	3-4 ml/min and12ml
Compress air pressure	1bar
Substrate temperature	275 ^{o}C
Substrate rotation	ON

PVA insulator is coated by drop cast method onto preheated ZnO/Aluminum coated glass and FTO coated glass substrates at a temperature of 55℃. The drop cast is performed in ambient air.

Top Gate-Top contact transistor is fabricated by employing aluminium as a gate electrode by thermal evaporation on glass pre-coated with layers, aluminium, zinc oxide and PVA with parameter and masks as shown Table I and *Fig 2* (b). The zinc oxide acts as an active layer and PVA acts as a gate dielectric for the fabricated TFT. The front and rare view of fabricated TFT is shown in Fig 3(a) and (b) respectively.

Fig 3 Image of TFT fabricated a) front view b) rare view

3. RESULT AND DISCUSSIONS

Fig 4 shows the drain-to-source current verses the drain-to-source voltage (I_d–V_{ds}) characteristics of a ZnO TFT measured in the air; the gate voltage (V_G) was varied from 0V to 10 V, in 2 V increments. The output characteristics of this device are indicative of typical n-channel operation. The curves reveal reasonable linear and saturation regions V_{ds} scans. In addition, a clear pinch-off and a high saturation current, of approximately 4.08X10^{-4}A for V_{DS} = 16.8 V and V_G = 10 V, are achieved.

The transfer characteristic of the device, measured in air, is shown in Fig *5*. The drain-to-source voltage was fixed at 4V, and V_G was swept reversibly from -2V to 5 V. On the application of a positive gate bias, I_d increases sharply; a small amount of hysteresis is observed when the scan direction was reversed. The value of linear mobility (**μ_{lin}**) can be extracted from transfer characteristics using the formula shown in equation (1).

$$\mu_{lin} = \frac{L}{C_G W V_D}\left(\frac{\partial I_{dlin}}{\partial V_G}\right) \quad (1)$$

Where C_G is the capacitance of the insulator layer, L length of the channel, W is the width of the channel, $\frac{\partial I_{dlin}}{\partial V_G}$ is the slope of the channel above the value of V_{th}, $V_D >> V_{GS} - V_{th}$ the transfer characteristics. The value of the linear mobility (μ_{lin}) is found to be 5 cm^2/Vs. The sub-threshold swing was calculated using formula as shown in equation (2).

$$S = \frac{\partial V_G}{\partial (log_{10} I_d)} \quad (2)$$

The values μ_{lin} and S is calculated using the transfer characteristics. The threshold voltage (V_{th}), sub-threshold slope, and on/off ratio, are 2.1 V, 0.5 V/decade, and 10^5. The linear field-effect mobility, which was derived from the slope of the plot of $I_{DS}^{1/2}{}_{sat}$ against V_G, was 3 cm^2/Vs. The same TFTs is used for fabrication of NAND Gate circuit construction.

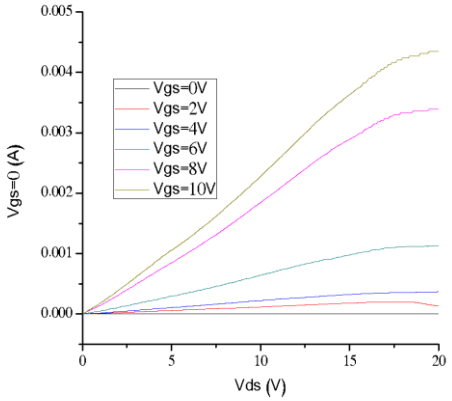

Fig 4 The output characteristics of the TFT

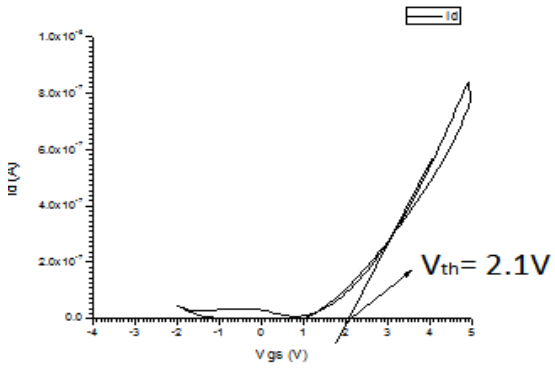

Fig 5 Transfer characteristics of TFT

The OFF-state current is less than 10^{-8} A, limited by gate leakage. The TFT transfer characteristics show enhancement mode operation allowing the realization of simple circuits without the necessity of level shifting. The low threshold voltage value, as well as the small value of sub-threshold swing, allows the device to operate at 5 V, indicating potential low-power applications, and significant future progress in energy efficiency. Devices also operated from 1 to 10 V, compatible with different current integrated-circuit technologies. NAND gates are the fundamental building block for implementing larger-scale digital circuits. The NAND gate was realized by a series connection of two drive transistors and a load transistor. Using ZnO Thin Film Transistor, one of the logic gate i.e., NAND gate was designed, constructed and tested for its output voltage. The circuit is as shown in Fig 6.

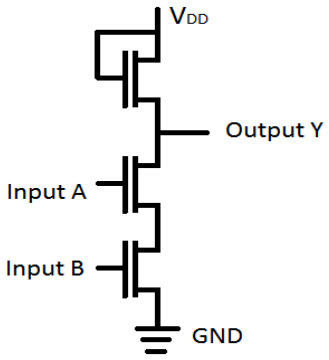

Fig 6 Circuit of a NAND gate

An n-type logic circuit for the NAND gate is fabricated and as shown in Fig 7. The fabricated NAND gate is a logic circuit which is constructed using TFT. The output voltage is noted down and compared with its logical output as shown in Table III.

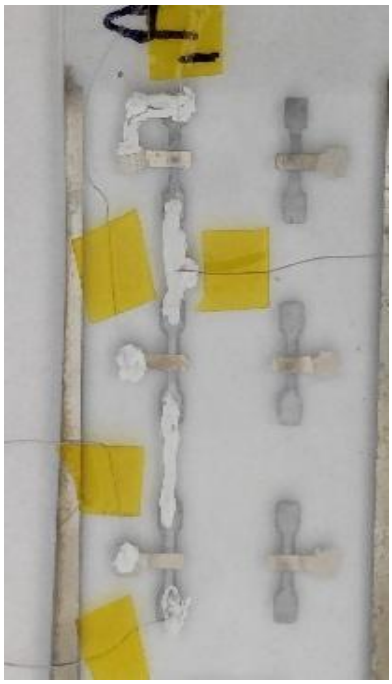

Fig 7 Fabricated of the NAND gate on the glass substrate.

Table III
The output voltage of the NAND gate as observed.

Input A	Input B	Output Y	Output Voltage
0	0	1	7.7
0	1	1	7.6
1	0	1	7.9
1	1	0	1.9

4.CONCLUSION

This work presents the synthesis and deposition of ZnO and PVA solution with a detailed process condition. The fabrication of the ZnO Thin Film Transistor with W/L ratio of 2.5 was maintained using a custom-designed mask. The distinct TFT were probed in ambient condition. The characteristics of the distinct

transistor with a threshold voltage of V_{th}=2.1 V, I_{on} /I_{off} ratio order of 10^5, linear mobility of 3 cm^{-2}/Vs and sub-threshold of 0.5 V/decade. The transistor further interconnected to form a digital NAND circuit. The NAND gate is probed for the output characteristics and the result satisfies the actual truth table.

ACKNOWLEDGEMENTS

Authors S S Omprakash and Naveen Kumar S K are grateful to the CENSE Department IISc., Bangalore, Manipal Institute of Technology, Manipal, DST-PURSE laboratory Mangalore University, Mangalore.

REFERENCES

[1] F. Yakuphanoglu, E. Basaran, B.F. Senkal, and E. Sezer, "Electrical and optical properties of an organic semiconductor based on polyaniline prepared by emulsion polymerization and fabrication of Ag/polyaniline/n-Si Schottky diode.," *The journal of physical chemistry. B*. vol. 110, no. 34, pp. 16908–13, 2006.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors.," *Nature*. vol. 432, no. 7016, pp. 488–492, 2004.

[3] S.S. Omprakash and S.K. Naveen Kumar, "PANI/ZnO hybrid nanocomposites TFT for NAND gate application.," *Materials Today: Proceedings*. vol. 5, no. 4, pp. 10827–10832, 2018.

[4] J. Liu, D.B. Buchholz, R.P.H. Chang, A. Facchetti, and T.J. Marks, "High-performance flexible transparent thin-film transistors using a hybrid gate dielectric and an amorphous zinc indium tin oxide channel.," *Advanced Materials*. vol. 22, pp. 2333–2337, 2010.

[5] K.K. Banger, Y. Yamashita, K. Mori, et al., "Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol-gel on-chip' process.,." *Nature materials*. vol. 10, no. 1, pp. 45–50, 2011.

[6] D. Wan, X. Liu, L. Xu, et al., "The Study for Solution-Processed Alkali Metal-Doped Indium-Zinc Oxide Thin-Film Transistors.," *IEEE Electron Device Letters*. vol. 37, no. 1, pp. 50–52, 2016.

[7] M.A. Dominguez-Jimenez, F. Flores-Garcia, A. Luna-Flores, J. Martinez-Juarez, and J.A. Luna-Lopez, "Thin-film transistors based on zinc oxide films by ultrasonic spray pyrolysis.," *Revista Mexicana de F´ısica*. vol. 61, no. April, pp. 123–126, 2015.

[8] J. Meyer, S. Hamwi, M. Kröger, W. Kowalsky, T. Riedl, and A. Kahn, "Transition metal oxides for organic electronics: Energetics, device physics and applications.," *Advanced Materials*. vol. 24, no. 40, pp. 5408–5427, 2012.

[9] W. Xu, H. Li, J. Bin Xu, and L. Wang, "Recent Advances of Solution-Processed Metal-Oxide Thin-Film Transistors.," *ACS Applied Materials and Interfaces*. vol. 10, no. 31, pp. 25878–25901, 2018.

[10] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances.," *Advanced Materials*. vol. 24, no. 22, pp. 2945–2986, 2012.

[11] S. Park, C.H. Kim, W.J. Lee, S. Sung, and M.H. Yoon, "Sol-gel metal oxide dielectrics for all-solution-processed electronics.," *Materials Science and Engineering R: Reports*. vol. 114, pp. 1–22, 2017.

[12] Y.-J. Chang, D.-H. Lee, G.S. Herman, and C.-H. Chang, "High-Performance, Spin-Coated Zinc Tin Oxide Thin-Film Transistors.," *Electrochemical and Solid-State Letters*. vol. 10, no. 5, p. H135, 2007.

[13] M. Esro, G. Vourlias, C. Somerton, W.I. Milne, and G. Adamopoulos, "High-mobility ZnO thin-film transistors based on solution-processed hafnium oxide gate dielectrics.," *Advanced Functional Materials*. vol. 25, no. 1, pp. 134–141, 2015.

[14] K.S. Shamala, L.C.S. Murthy, and K. Narasimha Rao, "Studies on optical and dielectric properties of Al2O3 thin films prepared by electron beam evaporation and spray pyrolysis method.," *Materials Science and Engineering: B*. vol. 106, no. 3, pp. 269–274, 2004.

[15] G. Adamopoulos, S. Thomas, D.D. C Bradley, M.A. McLachlan, and T.D. Anthopoulos, "Low-voltage ZnO thin-film transistors based on Y 2 O 3 and Al 2 O 3 high-k dielectrics deposited by spray pyrolysis in air.," *APPLIED PHYSICS LETTERS*. vol. 98, p. 2011.

[16] D. Afouxenidis, R. Mazzocco, G. Vourlias, et al., "ZnO-based thin-film transistors employing aluminium titanate gate dielectrics deposited by spray pyrolysis at ambient air.," *ACS Applied Materials and Interfaces*. vol. 7, pp. 7334–7341, 2015.

[17] G. Adamopoulos, S. Thomas, P.H. Wöbkenberg, D.D.C. Bradley, M.A. McLachlan, and T.D. Anthopoulos, "High-mobility low-voltage ZnO and Li-doped ZnO transistors based on ZrO2 high-k dielectric grown by spray pyrolysis in ambient air.," *Advanced Materials*. vol. 23, no. 16, pp. 1894–1898, 2011.

[18] S.S. Omprakash and N.K.S. K, "PANI / ZnO Hybrid Nanocomposites TFT for NAND Gate.," *Materials Today: Proceedings*. vol. 5, no. 4, pp. 10827–10832, 2018.

[19] S. Omprakash and S.K. Naveen Kumar, "Fabrication of Flexible Metal Oxide Thin Film Transistor by Indigenously Developed Spray Pyrolysis Unit.," *Transactions, E C S Society, The Electrochemical*. vol. 88, no. 1, pp. 129–138, 2019.

[20] K. Kim, E. Lee, J. Kim, et al., "Interface engineering for suppression of flat-band voltage shift in a solution-processed ZnO/polymer dielectric thin film transistor.," *Journal of Materials Chemistry C*. vol. 1, no. 46, pp. 7742–7747, 2013.

Mr. Omprakash S. S. received M.Sc. degree from Bangalore University, Bangalore, India in 2010. He worked in Oxford Independent Pre University College, Ullal, Bangalore, as a lecturer in Department of Electronic Science from 2010 -2012. He was Junior Research Fellow at R.V. College of Engineering, Bangalore on the project titled "Development of Nano Material and Optically Enabled, Front Surface and Back Contact Tailored, Enhanced Efficiency Amorphous Silicon Solar cells" from 2012 to Jan 2015. He is currently working toward the PhD degree in the field of fabrication Thin Film Transistor for microelectronic circuit design in Mangalore University, Mangalore, India. He has presented 10 international and 1 national research papers and published 5 international journals and 1 meeting abstract on his ongoing work.

Dr. Naveen Kumar S K is a Professor and Chairman of the Department of Electronics at Mangalore University. He received his PhD in Electronics (2001) from University of Mysore, Mysore, India. His research interests are in the areas of Nano sensor, nanoelectronics devices, Image inscription on FPGA, Microwave Electronics and Medical Electronics. He was working as an assistant professor (Sr) at the Department of Electronics, University of Mysore from 2002 to 2013. He has completed 2 projects and been working on 1 project. He has been working as a professor at the department of electronics, Mangalore University, Mangalore, India since 2013. He is currently working as a professor and chairman of the department. He has authored over 150 journal articles and conference publicationS.