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Improvement of column-parallel sampling for a monolithic pixel detector

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Abstract: Monolithic pixel detectors often use an on-chip analog to digital converter (ADC) with successive approximation register (SAR) to digitize the signal amplitude of the pixels. This paper solves the challenges of column-parallel sampling with respect to the layout, power consumption, process variability, speed, and the integration of fully differential ADC architecture with ADC driver. To save power and area, a single column ADC digitizes the signals from two columns. A fully differential amplifier (ADC driver) is used to convert a single-ended signal from a pixel to the differential signal for driving the fully differential SAR ADC inputs. An implemented prototype occupies $445 \times 115\,\mu m^2$ and achieves 4 MHz sampling frequency. The overall power consumption is 200 µW from a 1.8 V power supply at 10 frames per second readout frequency.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics

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1 Introduction

Pixel detectors have been used in imaging systems during the last three decades. Radiation-tolerant pixel detectors are, for example, used for space applications, X-ray detectors, avionics, and high energy physics (HEP) experiments. A monolithic pixel detector combines the sensor part of the detector with the readout electronics [1, 2]. The monolithic detector provides a cheaper and more compact solution in comparison with a hybrid detector [3]. In the monolithic pixel detector, analog signals from a pixel are often digitized by a column analog to digital converter (ADC) with successive approximation (SAR). The digitized signals are then read out serially by a fast digital interface.

A differential asynchronous architecture is popular in the SAR ADC design. The differential architecture, in comparison with a single-ended design, provides higher immunity to process variability, better noise immunity, and higher radiation tolerance. One of the most notable papers dedicated to SAR ADC has been published by Liu et al. [4]. Liu first presented a customized Metal-oxide-Metal (MoM) capacitor for capacitive digital to analog converter (CDAC), which they called a cage capacitor. In this paper, a new cage capacitor layout is proposed. The disadvantage of the Liu design [4] is the variable common mode at the comparator input, which makes comparator design more difficult. Another excellent design published by Harpe et al. [5] has all the advantages of [4] and solves the variable common mode problem. The voltage at the comparator input converges to the middle of the voltage reference. It simplifies the comparator design and improves linearity. The proposed SAR ADC design is a combination [4] and [5] with added new modifications that are explained in the following sections.

A single-ended to differential voltage converter is needed to drive the fully differential ADC inputs. This circuit is often implemented using a fully differential amplifier with a common mode feedback [6]. The converter has to be fast enough and have a large voltage output swing with low power consumption.

The problem is to integrate the fully differential SAR ADC with the ADC driver and maintain low nonlinearities, high speed, a small area, and low power consumption. A comprehensive solution for the combination of differential ADC with a single-ended input signal is missing in the existing literature. This paper brings together the integration of the ADC driver and asynchronous, fully differential SAR ADC on the same substrate. This integration allows us to digitize the single-ended signal from a pixel and exploit the advantages of the differential SAR ADC approach. Another advantage of the proposed solution is in sharing a single ADC with two columns. A simple asynchronous state machine controls the conversion of odd and even columns and stores data into the output registers. The operation is asynchronously initiated by a signal that performs row shifting. This new approach saves power and the layout area.

This paper is organized as follows: section 2 discusses novelties in the proposed circuits. Simulation and measured results are discussed in section 3. Section 4 concludes this paper.

2 Proposed circuit description

The proposed asynchronous column SAR ADC is used in a pixel detector with 32 rows and 64 columns. Each ADC converts signals from two columns, odd and even. Data from the ADC is moved to a row shift register (RSR) and then read out serially from the chip with a fast digital interface. An illustration of the pixel detector is depicted in figure 1.

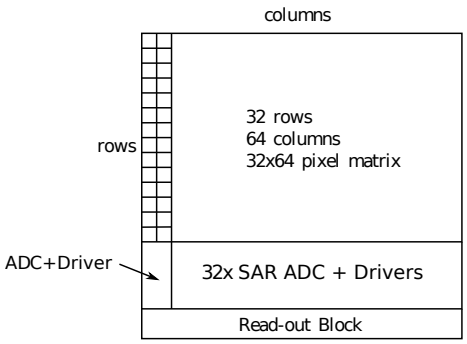

Figure 1. Pixel detector illustration.

A simplified block diagram of the proposed 8-bit column ADC is shown in figure 2. Input signals from odd and even columns are connected to VIN<0> and VIN<1>. These inputs are fed through the input demultiplexers where the signal ADC_PIN_EN selects VIN<1:0> or the external pin ADC_PIN. This external pin serves for testing purposes. The buffer block is used to increase input impedance of column ADC. In the proposed design, the buffer was realized by a standard two-stage operational transconductance amplifier (OTA).

Two bootstrap switches [7] serve as a multiplexer controlled by the finite state machine (FSM). The output of the bootstrap switches is connected to the ADC driver. The FSM selects one of the

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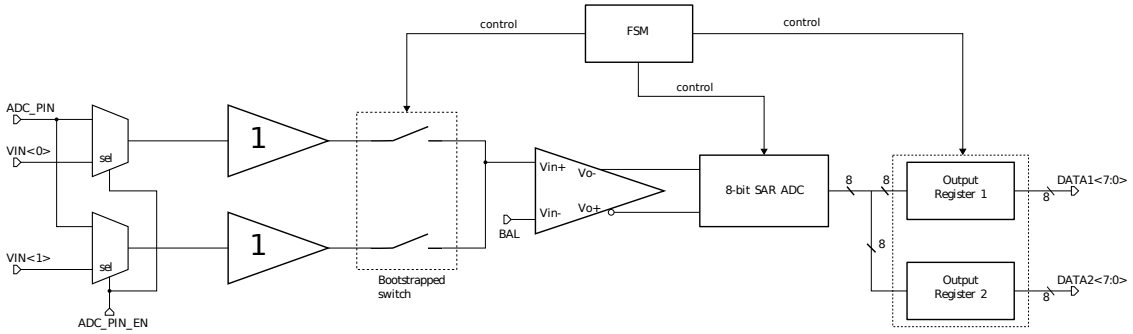

Figure 2. Duplex Asynchronous 8-bit ADC.

inputs for analog to digital conversion using bootstrapped switches. The bootstrap switch design is used in order to maintain good linearity resulting in low distortion.

The ADC driver block is a fully differential amplifier which drives the differential SAR ADC inputs. The main task of this block is to convert a single-ended signal to a differential signal. The BAL signal sets the common mode. The ADC driver is described in detail in section 2.2.

The 8-bit asynchronous SAR ADC with charge redistribution is described in section 2.3. The output data from the ADC is latched to one of the output registers. The SAR ADC and output registers are controlled by the FSM.

The FSM was implemented by standard digital cells and is described in section 2.4. In the initial state, the FSM turn on the bootstrap switch at input VIN<0>. A conversion cycle is initiated at the falling edge of an external signal that performs row shifting, described in detail in section 2.4. An analog value of the signal VIN<0> are digitized and latched to the output register 1. Immediately after conversion VIN<0>, the FSM switch off VIN<0> and turns on VIN<1>, waits some time to settle the ADC driver output and initiate the second conversion which is latched to the output register 2. Novelties of individual circuits are described in the following subsections.

2.1 Bootstrapped switch

The bootstrapped switch uses a standard circuit from reference [7]. The modified design is shown in figure 3. The used technology, 180 nm silicon on insulator (SoI) process, provides NMOS and PMOS transistors with break down voltage of 1.98 V and 5 V. The node X in figure 3 reaches a voltage level of up to 2.8 V. Therefore there are used transistors with thicker gate oxides with a breakdown voltage of up to 5 V.

2.2 ADC driver

The proposed fully differential operation amplifier (FDOA) in figure 4 design is based on reference [8]. The input stage forms the PMOS transistors M0, M1, cascodes M6, M7, current source M8 and current mirrors stabilized by a common mode feedback M2, M3. The common mode feedback is composed of transistors M15, M16, M11, M13, which set a common mode level and the resistors R2, R3, capacitors C6, C7 senses the output voltage and cancel differential signals.

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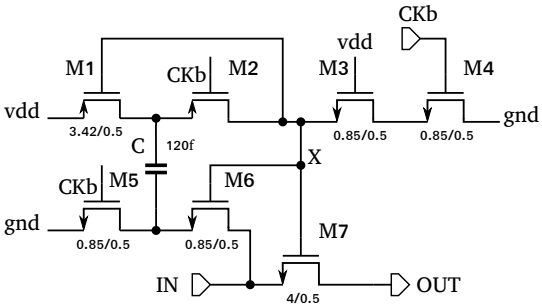

Figure 3. Bootstrapped switch.

The transistors M12, M13, M26, and M30 are class AB output stage at output Vo+. Vo- is identical to Vo+. Resistors R7, R6, R8, R9 and capacitors C0, C5, C8, C9 form a frequency compensation. The remaining transistors are for biasing purposes. Advantage of this circuit is a large output swing of class AB stage, fast settling time, and low output impedance. The usage of a fully differential amplifier with common mode feedback for single-ended to differential signal conversion have also advantage of small sensitivity to process variations.

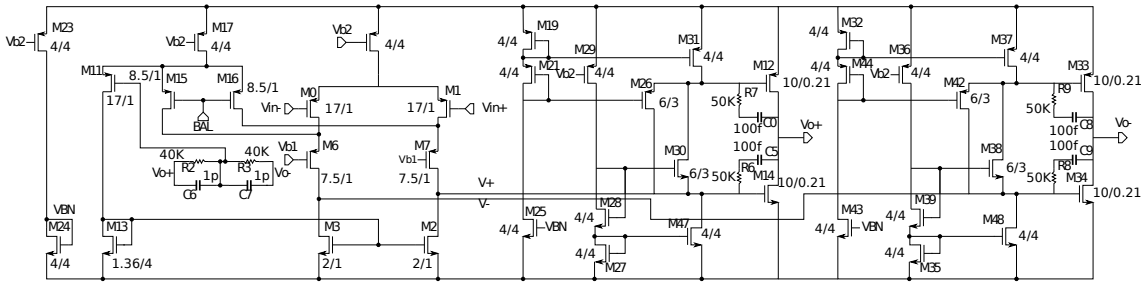

Figure 4. Proposed ADC driver.

Voltage Vb1 is connected to the ground and the BAL voltage sets the common mode. The output voltage versus input voltage is depicted in figure 5. Note that the output voltage is equal to -1.024 V for the zero input voltage and +1.024 V for the maximum reference input voltage, which is also 1.024 V. The Output settling time is less than 100 ns. Power consumption is 160 µW. The Layout area is $50 \times 115\ \mu m^2$.

2.3 8-bit SAR ADC

A block diagram of the proposed asynchronous 8-bit SAR ADC is depicted in figure 6. The basic switching principle is the same as in [5]. CDAC has a different design in comparison with [5] explained below. A new pulse generator is added in order to generate an MCLK signal at the falling edge of the SAMPLE signal. The MCLK signal is used to sample the input analog voltage to CDACs through bootstrapped switches. A new reset circuit is added to generate a SYNC signal that is needed for the duplex asynchronous conversion. The individual blocks different in comparison with [5] are explained below.

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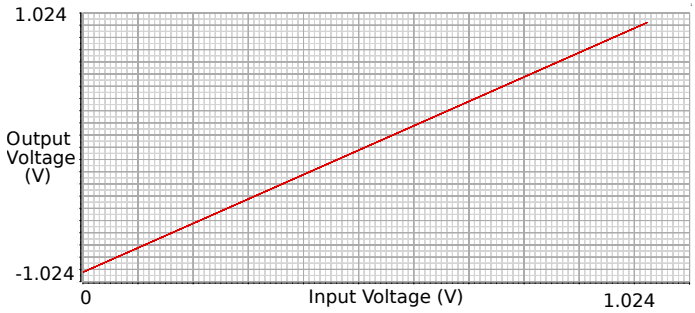

Figure 5. Input Voltage vs Ouput Voltage of the proposed ADC driver.

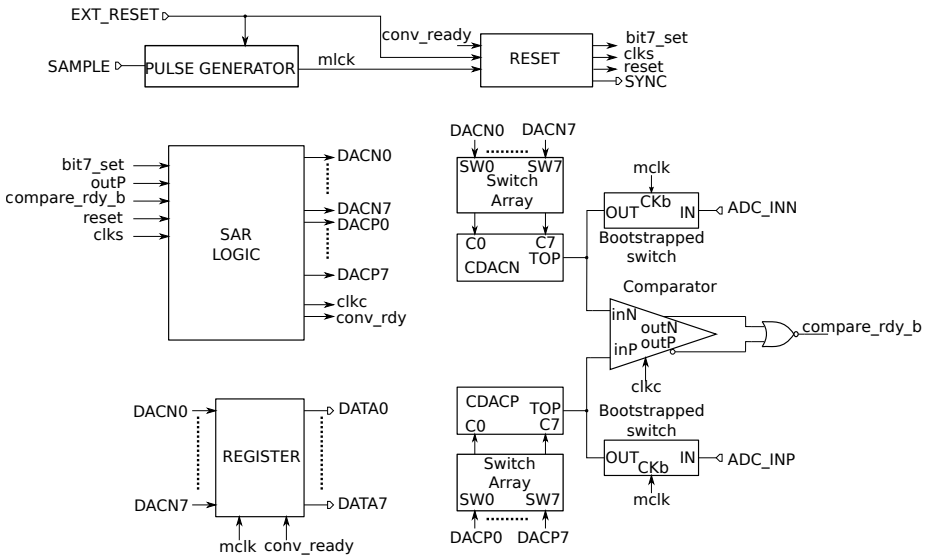

Figure 6. 8-bit SAR ADC block diagram.

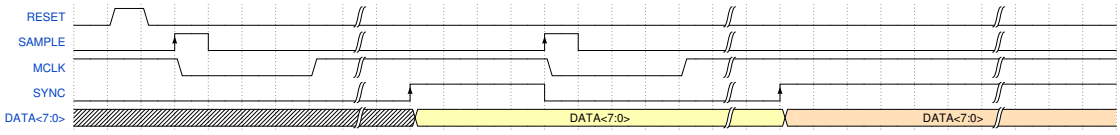

Figure 7. SAR ADC Timing diagram (not to scale).

The asynchronous operation is depicted in figure 7. Before a conversion cycle takes place, the RESET signal goes high to set all D-circuits to the low initial state and reset the SAR logic to its initial state. The ADC converter is in standby mode after reset. Another reset signal is generated internally by the signal CONV_READY when a conversion cycle has been completed. The converter goes on standby mode after every conversion. The pulse generator is a monostable circuit that generates a pulse MCLK at the rising edge of the signal SAMPLE. An input differential signal is sampled to the CDACs when MCLK is low. The SAR logic begins successive approximation when the MCLK goes high. The SYNC signal goes high when the ADC finishes a conversion cycle. DATA

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is latched to the output register at the rising edge of SYNC. The SYNC signal goes low when the next conversion is required by the SAMPLE signal.

2.3.1 Capacitive DAC

The Proposed CDAC contains 256 customized MoM capacitors. Each unit capacitor has the dimensions $4.24 \times 4.24\,\mu m^2$, with capacitance 4.5 fF. Details of the unit capacitor is shown in figure 8. The metal 3 forms one pole and metals 1 or 4, the second pole of the capacitor. All metals including vias, excepting gaps for the metal 3 pole, forms a box structure which highly decreases parasitic capacitances. The CDAC layout area is $195 \times 57.5\,\mu m^2$, overall capacitance is 1.174 pF.

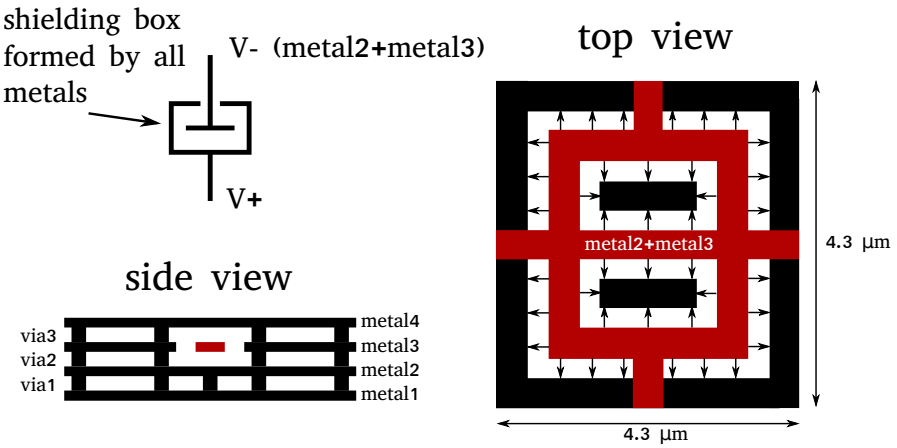

Figure 8. The proposed MoM capacitor.

2.3.2 Reset circuit

The reset circuit is an additional part of the SAR logic. The RESET signal is generated if the EXT_RESET or CONV_READY signal is received. This circuit also generates the signal BIT7_SET on the MCLK rising edge and SYNC when the conversion is finished. The signal SYNC is needed for the asynchronous double column conversion. The reset circuit is shown in figure 9 and a timing diagram in figure 10.

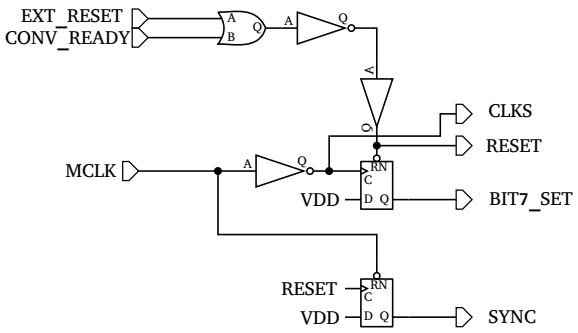

Figure 9. Reset circuit.

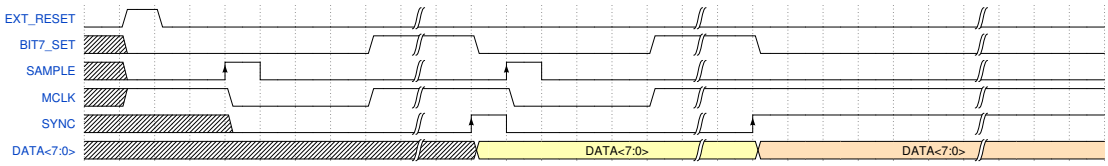

Figure 10. Reset circuit timing (not to scale).

2.3.3 Pulse generator

The pulse generator is a monostable circuit that generates an MCLK pulse of defined length. The MCLK signal is active low, used for sampling analog voltage to CDAC. The proposed pulse generator is illustrated in figure 11.

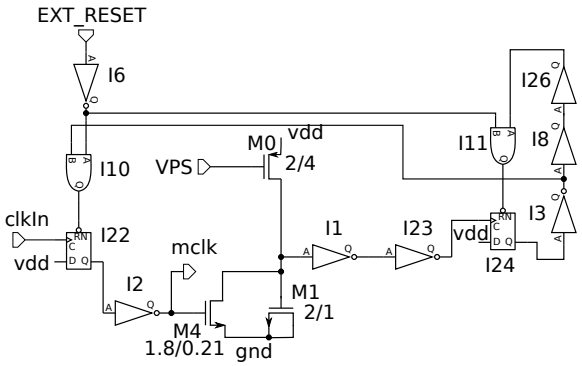

Figure 11. Pulse generator.

First of all, the MCLK signal has to be initiated by EXT_RESET. It turns on the transistor M4 to discharge MOS capacitor M1. M1 is charged by a constant current from current source M0 when the MCLK is low at CLKIN rising edge (CLKIN is SAMPLE signal). The M0 current is adjusted by VPS voltage. I1 output goes low when the voltage at the M1 capacitor reaches a threshold voltage of the inverter. In this time, I24 Q output goes high and the short reset signal is generated by a delay line I8, I26 in order to reset I22, I24. MCLK is low and circuit waits for next CLKIN rising edge. The timing diagram is shown in figure 12.

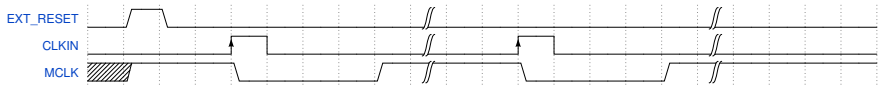

Figure 12. Pulse generator timing (not to scale).

2.4 Finite state mashine (FSM)

The simple finite state machine (FSM) drives the bootstrapped switches at the FDOA input, latches output data into registers and also drives the SAMPLE signal of the SAR ADC. The circuit diagram is shown in figure 13 and the time diagram in figure 14. At first, the EXT_RESET goes low to initiate the D-circuit outputs into a low state. The REG_SET signal is low and turns on the even column connected by the bootstrapped switch. The first row of the pixel detector is selected at

ROW_SHIFT rising edge. The ROW_SHIFT signal is held high until a voltage level is steady at the output of the input buffers. The first conversion cycle is initiated at ROW_SHIFT falling edge by SAMPLE signal, generated by I8. The delay loop, composed of I12-I14, reset I8 when the SAMPLE signal goes low. I12 and I13 are delay buffers. The SYNC signal goes high when the first (odd column) conversion has finished. The ADC data is latched to both registers at the rising edge of SYNC and REG_SET. At the same time, the second SAMPLE signal is generated and the second (even) bootstrapped switch is turned on (the odd bootstrapped switch is turned off) by the REG_SET signal. At SYNC rising edge, the second (even) conversion cycle is initiated. The ADC data (even) is latched to one register by the rising edge of the SYNC when the second conversion cycle is finished. Data latched in both registers are moved to a shift register and are ready to be read out. The next conversion cycle can be initiated by ROW_SHIFT when the data is moved into the shift register.

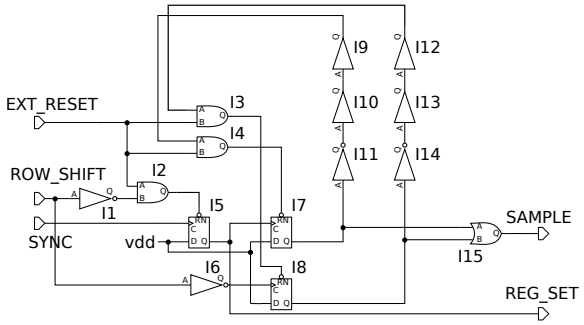

Figure 13. FSM circuit diagram.

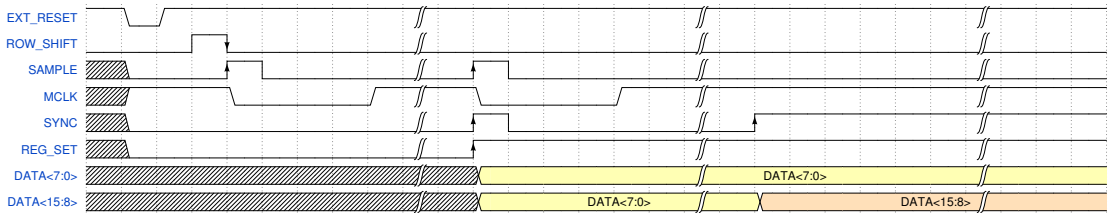

Figure 14. FSM timing diagram (not to scale).

2.5 Layout

The layout is shown in figure 15. A common centroid technique is used for transistors in the comparator circuit of the SAR ADC and for transistors in the ADC driver. The common centroid technique helps to improve matching properties and increases radiation hardness. The layout is kept as symmetrical as possible. At the bottom of the layout the output registers are placed for a simple connection of the readout circuits. A free place in the symmetrical structures are filled with decoupling capacitors. Driving signals, bias and power are connected on top of the layout by top metal in the used technology. The dimensions of the layout are $445 \times 115\,\mu m^2$. All 32 column ADC's are placed side by side.

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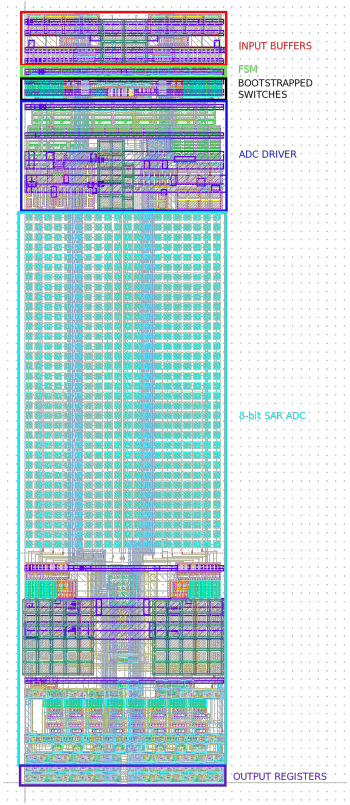

Figure 15. Layout.

3 Results

In this section, the simulated and measured results of the implemented prototype are provided. Simulated integral and differential nonlinearities (INL, DNL) for all corners of 180 nm SOI CMOS technology are shown in figure 16 and figure 17. These nonlinearities have been extracted from the transfer function with a gradually increased step of 1 mV (0.25 LSB) at the buffer input. The worse case DNL is held within 1 LSB and -0.5 LSB and INL between 1 LSB and -2 LSB.

The fabricated monolithic pixel detector has an external ADC_IN input where it is possible to connect the external signal to the input buffer of the column ADC. It allows us to test the input buffer, ADC driver, SAR ADC, and the double column conversion. The same measurement method as in the circuit simulations is used. The input signal from a programmable generator was set to ramp with 1 mV increment per frame. The frame rate has been set to 10 frames per second. 1024 frames have been collected.

The measurements of the implemented prototype in 180 nm SoI CMOS technology have revealed a problem with the limited range of the ADC. The problem is caused by the incorrect layout of the PMOS voltage divider which sets 512 mV from the ADC voltage reference for BAL input of the fully differential amplifier. The BAL signal is lower than 512 mV resulting in the limited output voltage range. However, the problem occurs outside of the presented design, therefore, it does not influence the presented solution. The problem was understood and will be eliminated in future circuit re-designs. The limited range is shown in figure 20. Measured and calculated DNL

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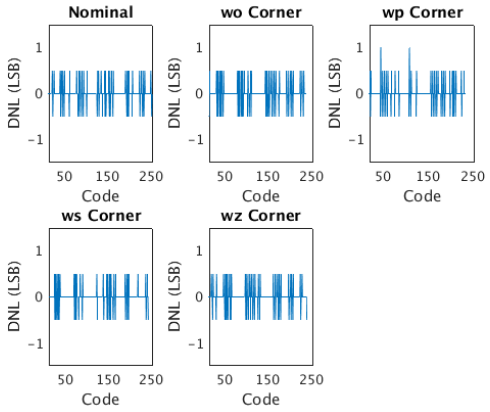

Figure 16. Simulated DNL.

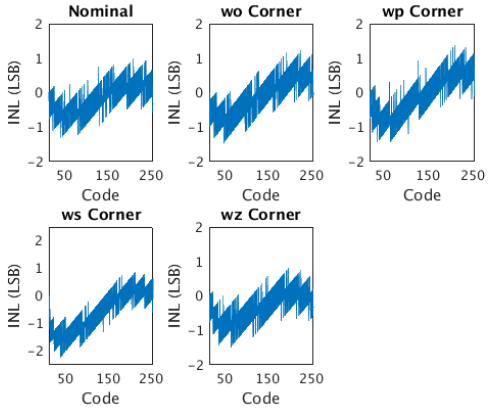

Figure 17. Simulated INL.

and INL are shown in figure 18 and figure 19 respectively. They are calculated from the transfer function shown in figure 20 at the range in which the implemented prototype is working. All 32 column ADC's of the single monolithic pixel detector were measured. Their DNL is held within 0.5 LSB and -0.75 LSB and INL are held within 1 LSB and -1 LSB. The results of one column ADC in figure 18, figure 19 and figure 20 are shown because nonlinearities from other column ADC's are also held at the same range. This indicates a low process variability of the proposed solution. Comparing simulated and measured results show that the proposed design works as expected, however, at the limited range.

The overall power consumption for all 32 SAR ADC's including ADC drivers, is 3.1 mA from 1.8 V power supply. One SAR ADC with a ADC driver consumes around 180 µW from 1.8 V at 10 frames per second readout speed. A sampling frequency has been set at 1 MSPS for double column conversion. It means that within 1 µs voltages has been sampled from odd and even columns.

A basic comparison with other column ADC's [9, 10] and [1] in the table 1 has been provided. This work shows better power consumption at the expense of lower speed, in comparison with [9]. A single-ended solution can achieve better power consumption but has the disadvantage of lower accuracy and lower noise, interference immunity.

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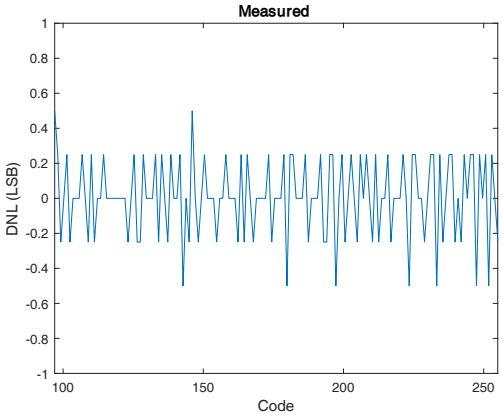

Figure 18. Measured DNL.

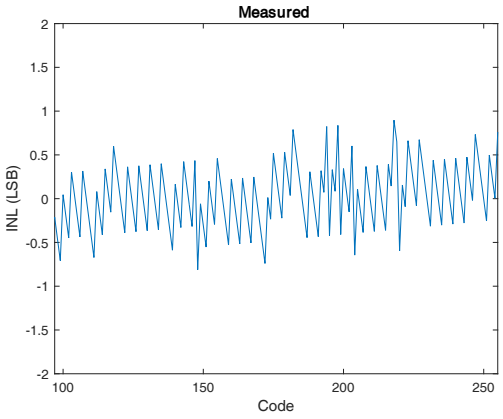

Figure 19. Measured INL.

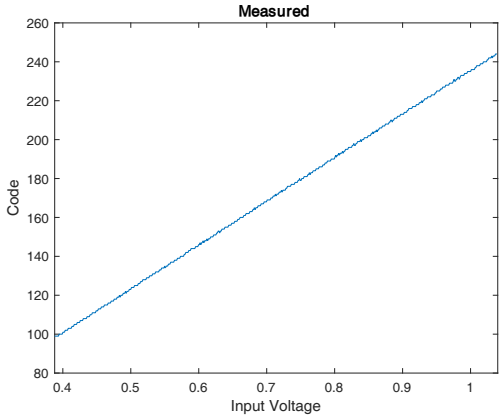

Figure 20. Measured transfer function.

Table 1. Comparison of the proposed design with other column SAR ADC's.

	Dasgupta 2014 [9]	Culurciello 2006 [10]	Havranek 2019 [1]	This work
Architecture	differential	single-ended	single-ended	differential
Bit	10	8	10	8
Speed (MS/s)	20	1.23	0.25	4
INL (LSB)	-	0.87	1.5	1
DNL (LSB)	-	0.18	1	0.75
Power (µW)	900	770	150	200
Area (μm^2)	310×190	450×315	57.5×480	115×445

4 Conclusion

In this work, the column SAR ADC for a monolithic pixel detector was presented. This challenge is specific, with regard to layout, power consumption, process variability, and the integration of fully differential SAR ADC with ADC driver. Furthermore, it is important to maintain high speed. Power consumption of the proposed circuits is less than 200 µW at 10 frames per second from 1.8 V power supply. The maximum driver and SAR ADC speed is 4 MHz. A new MoM capacitor layout with capacitance 4.5 fF was proposed. A single column ADC is shared by two columns to save power and area. The measurements of the implemented prototype have proven that the circuit is working according to simulation. Differential and integral nonlinearities, for all 32 column ADC's placed at the same chip, are held within 0.5 LSB, -0.75 LSB and 1 LSB, -1 LSB respectively. It indicates a low process variability of the proposed solution. The limited range is caused by the incorrect layout of the PMOS voltage divider. The PMOS voltage divider is not part of the presented design, therefore the relevancy of the work presented has been maintained.

Acknowledgments

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