Flexible and Printed Electronics

OPEN ACCESS

RECEIVED
1 October 2019

REVISED
3 December 2019

ACCEPTED FOR PUBLICATION
30 January 2020

PUBLISHED
18 February 2020

PAPER

Megahertz operation of vertical organic transistors for ultra-high resolution active-matrix display

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Keywords: vertical organic transistors, high-frequency operation, active-matrix display

Abstract

Organic field-effect transistors (OFETs) are the technology of choice for flexible electronic devices such as active-matrix (AM) displays. However, despite the continuous improvement of charge carrier mobility in organic semiconductors, the performance of conventional OFETs is too poor for demanding electronic applications. Furthermore, hero-devices reported in literature often make use of processes (shadow mask fabrication, large channel width devices) which cannot be adapted in production lines, e.g. for AM displays. Here we present an OFET with a novel vertical device structure. It has static and dynamic transistor performance superior over conventional lateral organic transistors with regard to application in AM displays. We show that these vertical transistors can be integrated using processes well-established in the micro-electronic industry and thus offer seamless transfer into production lines. We discuss that these transistors obey scaling laws for footprint and capacitance which make them superior over other planar transistor devices. In combination with excellent device stability and uniformity, vertical OFET might enable ultra-high resolution flexible displays of the future.

1. Introduction

High resolution displays with brilliant colors have become daily companions to all of us during the last years. In fact, such devices are being seen today as a commodity product and hence the global flat panel display industry is seeking for innovation and reduction in manufacturing costs in order to retain profitability. One of the leading development trends which has been identified in this regard are flexible displays. Beyond their appealing flexibility offering many new and fascinating applications, they might also enable a significant reduction in production costs due to the use of low-cost flexible substrates and low-temperature processing. However, the transition from rigid to flexible substrates requires the development of new transistors technologies which are compatible with low temperature processing (ideally $\leqslant$150 °C). Moreover, any new transistor technology needs to provide an electrical performance which allows for a high display resolution (2 k and beyond) in order to fulfill the costumer's expectation.

Low temperature poly-crystalline silicon (LTPS) is currently the leading backplane technology for ultra-high resolution active-matrix liquid crystal (AMLCD) and organic light-emitting diode (AMOLED) displays because of its superior electrical performance and operational stability. However, the future potential of LTPS is limited by its process complexity. In particular, the necessity for a high temperature annealing step (usually at $\geqslant$350 °C) does not allow for LTPS backplane manufacturing on large substrates ($\geqslant$GEN6 glass) and on low-cost flexible substrates.

As an alternative to LTPS, transparent metal oxide thin-film transistors (MO-FET) have been developed in order to reduce process temperature and complexity. First products are already available on the market based on amorphous indium gallium tin oxide (a-IGZO). However, the electrical performance of MO-based FETs is still inferior to LTPS and their operational stability under illumination remains a concern [1, 2]. In particular, for a process temperature $\leqslant$250 °C, the MO-FET performance is severely deteriorated by a reduction of charge carrier mobility,

instability under bias and illumination stress, as well as an unacceptable degree of non-uniformity in comparison to the standard processing procedure. Even sophisticated photo-annealing techniques do not allow for stable device operation for process temperatures below 250 °C [3]. Hence, MO-FETs are an interesting alternative to LTPS when it comes to the reduction of fabrication costs, however, besides first display prototypes [4], they are most likely not the technology which is going to enable truly flexible display backplanes.

Organic semiconductors based either on conjugated polymers or so-called small molecules offer superior mechanical flexibility due to the weak van der Waals (vdW) interaction between their constituents. Hence, organic field-effect transistors (OFETs) are considered to be the ideal technology for truly flexible devices [5]. Unfortunately, the weak vdW interaction also gives rise to the fact that the inherent charge carrier mobility of organic semiconductors (OSCs) is low compared to transparent metal oxides or LTPS (best values for organic thin films are in excess of 10 $cm^2 V^{-1} s^{-1}$ [6]) which puts a big question mark behind the usability of OFETs for high resolution displays. Furthermore, most OFET hero-devices [6, 7] claiming cutoff frequency records make use of transistor designs and fabrication processes which cannot be adapted in a display backplane process (e.g. large channel width of $\geqslant$500 μm [7], high resolution shadow masks [8], etc).

Vertical organic transistors [9–15] have been developed in order to circumvent the shortcomings of conventional planar OFETs. The target of the vertical transistor development is to increase the on-current level compared to conventional transistors by means of an ultra-short vertical channel while even reducing the active device capacitance resulting in faster devices. In comparison to their horizontal counterparts, the channel length in vertical transistors is not defined by patterning steps, such as photolithography or printing, but by the thickness of the semiconductor layer which defines the channel area. In this way, a short channel length of $\leqslant$500 nm can be realized easily without employing expensive high resolution lithography. In fact, vertical organic transistors nowadays set the record values for the performance of organic transistors in terms of transition frequency (40 MHz, [16]) and highest current density ($\geqslant$1 kA cm^{-2}, [17]), and can even compete in terms of device stability [18].

In this paper, we focus on vertical organic field-effect transistors (V-OFETs)—a special type of a vertical organic transistor which we have previously pioneered [12, 19]. We report on recent improvements in terms of device integration and performance but most importantly we discuss the potential of this technology to be used in active-matrix (AM) display backplanes. We elucidate the concept and design guidelines for V-OFETs and compare it to the standard planar FET designs. In particular, we show that the device capacitance of V-OFETs is lower compared to planar FETs, providing a substantial benefit in terms of dynamic behavior. We also present the experimental dynamic characteristics of V-OFETs and demonstrate cutoff frequencies of 10 MHz. This is achieved without undue technological effort. We use a 5 μm line width technology, an OSC with relatively low mobility, and an integration process which can be readily adopted in commercial production lines. Superior dynamic behavior along with a high degree of device uniformity, good device stability, and low processing temperatures makes the V-OFET technology competitive with MO-FETs for ultra-high resolution displays.

2. V-OFET concept and design paradigms

V-OFET concept—In this paper we present a vertical organic transistor in bottom gate configuration as shown in figure 1. The current flow and hence also the transistor channel is composed of a vertical channel perpendicular to the gate insulator surface and a lateral channel depending on the exact shape of the source metal electrode and its alignment to the source–drain insulator (SD insulator) [19]. Thus, strictly speaking these devices are a pseudo-vertical transistor with vertical and lateral contributions to the charge carrier transport. The active channel length of the transistor is defined by this lateral transport and the thickness of the semiconducting layer and in our design the typical channel lengths are expected to be in the range of 300–500 nm (details are given in the section where the fabrication is described). OSCs are particularly suited for such short-channel transistors owing to the low number of interface states due to the lack of dangling bonds and their rather large bandgap ($\geqslant$2 eV). Related to this fact, vertical organic transistors show much better on/off switching compared to their silicon or metal oxide based counterparts [20, 21].

We developed a fabrication procedure for V-OFETs which is fully compatible with state-of-the-art display backplane technologies. In this regard, our work differs substantially from previous reports about vertical organic transistors where sophisticated fabrication methods have been employed which cannot seamlessly be adopted in a production line for high-resolution displays. Such processes are: shadow mask patterning [11], lift-off [12], nm-scale lithography [10, 15], and unconventional electrode or gate insulator materials [9, 13]. We only employ well-established fabrication techniques for large area and high throughput industrial processes, such as conventional photolithography, wet and/or dry etching are employed [22–24]. Scalable processes such as sputtering or CVD can be used for the preparation of the gate insulator. In particular, in this work we use a gate dielectric with a specific capacitance of 50 nF cm^{-2} (hybrid dielectrics composed of 25 nm of Al_2O_3 and 30 nm of the fluoropolymer CYTOP), which is in the

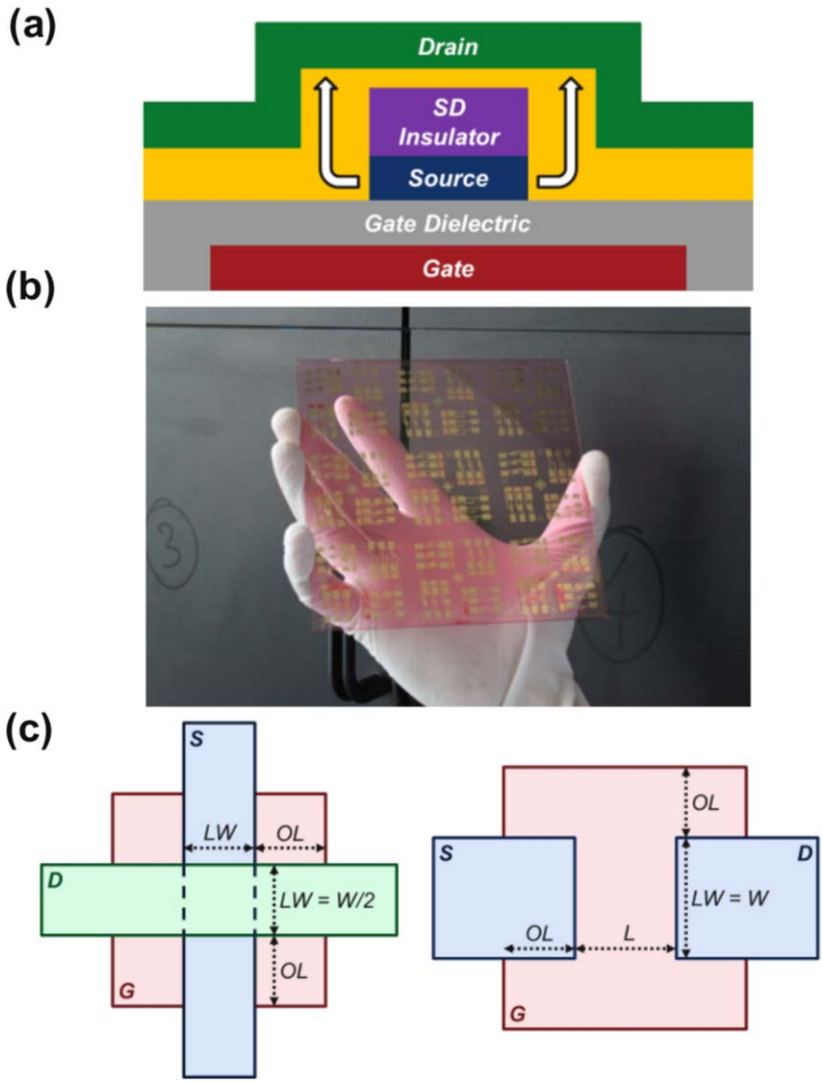

Figure 1. (a) Schematic VOFET cross section, (b) photography of a sample of V-OFETs on a 5 × 5″ substrate, (c) comparison of VOFET and OTFT layouts.

typical range applied in backplane manufacturing. Source and Drain electrodes are composed of Au (thickness of 40 nm) and are patterned by photolithography followed by a wet-etching in KI/I_2 (denoted as standard etchant gold). The gate electrode is made of Al (thickness of 200 nm) and it is patterned by photolithograhy and wet etching. The SD-insulator is a highly cross-linked photoresist (NLOF2020) with a thickness between 400 and 700 nm. The thickness of the semiconductor layer is 25 nm. Finally, the semiconductor film is patterned by reactive ion etching using oxygen [24]. All processing steps are performed under ambient conditions (except the vacuum deposition steps) and at process temperatures $\leqslant$120 °C.

Figure 2(a) shows a typical transfer curve of a V-OFET obtained with a small molecule OSC (2, 6-Diphenylbenzo[1, 2-b:4, 5-b]dithiophene, DPh-DBT) characterized by a nominal mobility of 0.5 $cm^2\,V^{-1}\,s^{-1}$ (measured in a planar OFET design with a channel length of 100 μm using the same hybrid dielectrics). On/off ratios close to 10^7 with on- and off-current densities of ~5 $\mu A\,\mu m^{-1}$ and $\leqslant$1 pA μm^{-1} at $V_{DS} = -10$ V, respectively, are obtained for V-OFETs fabricated as described above. The on-current density is widely independent of the choice of the thickness of the semiconductor materials (evaluated range from 25 to 300 nm) which suggests that the on-current is not limited by the transport through the channel but rather the charge carrier injection, which is consistent to other organic short channel transistor [8].

Besides an outstanding FET performance (on/off-ratio and on-current density) and possibility to process these devices at temperatures $\leqslant$120 °C, V-OFETs show as well excellent device uniformity and stability, demonstrating that this technology is suited for display integration. Focusing on device uniformity, we can report excellent threshold voltage V_{th} and on-current uniformity on a full 5 × 5″ substrate of 0.41 V and 4.3%, respectively (table 1 and figure 2(b)). This high level of uniformity is achieved because only scalable processes such as photolithography and solution-coating are used. Furthermore, we could identify the

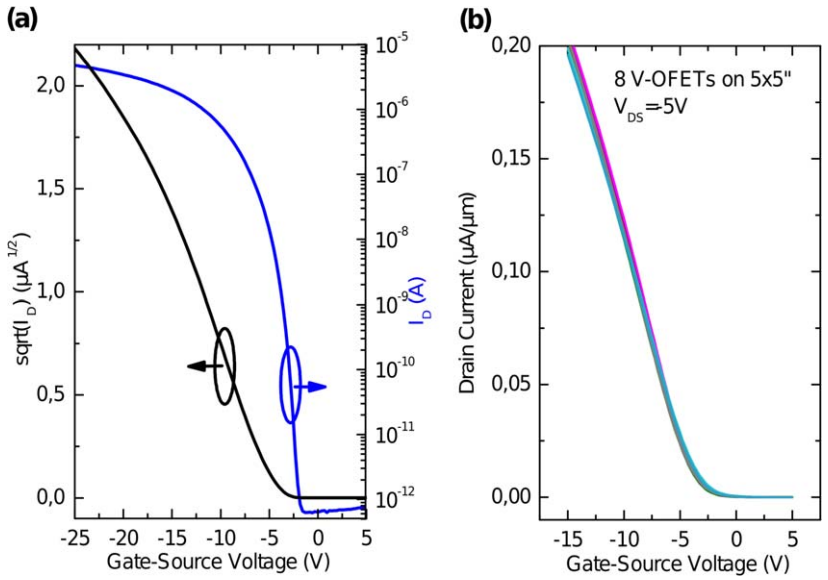

Figure 2. (a) Transfer curve for a V-OFET ($W = 20\ \mu$m) at $V_{DS} = -10$ V approaching the saturation, (b) comparison of the transfer curves in the linear regime of V-OFET devices on a $5 \times 5''$ substrate at $V_{DS} = -5$ V. Different colors represent the transfer curves of the individual transistors.

Table 1. Summary of V-OFET uniformity and stability data. Measurement conditions are: V-OFET (p-type): $V_{DS} = -0.1$ V, $V_{GS} = +/-15$ V, $T = 20$ °C.

	V-OFET
On-current (std. dev.)	4.3% ($5 \times 5''$)
V_{th} (std. dev.)	0.41 V ($5 \times 5''$)
Stability	
Off-state, illuminated	1.5 V at 8000 cd m^{-2}
(ΔV_{th} in V/h)	(white light)
On-state, dark (ΔV_{th} in V/h)	0.1 V

uniformity of the gate insulator thickness and the metal line width as the main uniformity limitation for our process. Hence, it is apparent that V-OFET uniformity will be further improved when transferring the technology to a mass production environment. Finally, we report device stability data in the bottom part of table 1. Especially looking at bias stress stability under illumination, the V-OFET technology provides a clear advantage over a-IGZO due to the low absorption coefficient of the OSC.

V-OFET design paradigms—Due to the vertical stacking of gate, source and drain electrodes, V-OFETs obey different scaling laws than their planar counterparts. The knowledge on the transistor scaling behavior is of utmost importance for high-resolution displays for two reasons: first, the limited area for the transistors due to the demand on the storage capacitor or the aspect ratio of the pixel, and second, the transistor capacitance which is strongly affecting the dynamic properties of each pixel in a display. The existence of the gate-drain capacitance of the switch transistor in an AM backplane, gives rise to the so-called voltage-kick-back effect [25]—a rapid discharging of the storage capacitor when the transistor is switched off—being one of the biggest issues for high-resolution displays. As we will see, V-OFETs offer both, a reduced transistor footprint and a smaller gate-drain overlap capacitance, which in turn makes the V-OFET technology interesting for ultra-high resolution display applications.

To provide a comparison relevant for AM backplanes, we assume a channel width W of 4–10 μm and discuss the ratio of total gate area and capacitance for planar and vertical devices for varying layout parameters. These are defined on the schematic layouts shown in figure 1(c): channel length L, channel width W, minimum metal line width LW, and mask overlay OL. Figure 3(a) shows the total gate area of V-OFETs and planar FETs versus metal line width LW for various values of overlay accuracy. The channel length of the planar FETs is set to $L = 5\ \mu$m. The values chosen for the overlay, channel width and metal line width are typical for high-resolution display. For example, in a 400 ppi AMOLED display each pixel, with a size in the range of 65 μm $\times$ 65 μm, contains at least two transistors, one storage capacitor, the OLED, metal lines, and through-holes for interconnection. Consequently, the available space e.g. for the switching transistor is very limited and challenging design rules for the overlay and metal line width need to be adopted.

From figure 3(a) it is apparent that vertical FETs have always a lower total gate area than planar FETs for the considered parameters. For typical display parameters $OL = LW = 3.5\ \mu$m, the gate area of the V-OFET is only 66% of the gate area for the horizontal FET, corresponding to a reduction in gate capacitance of one third. The area ratio can be further reduced to 35% in case of a more aggressive design with $OL = 2\ \mu$m and $LW = 1\ \mu$m. In figure 3(b), the total

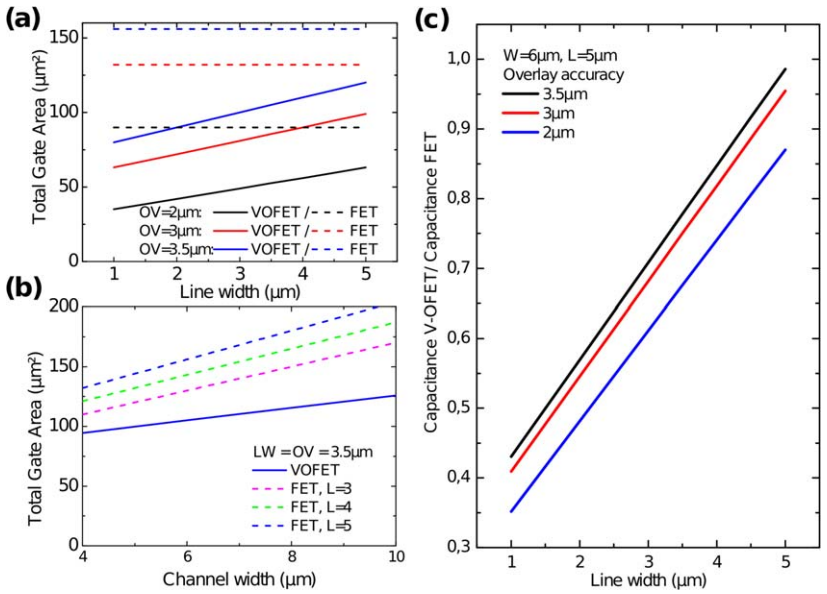

Figure 3. Total gate area for a V-OFET and for a planar FET ($W/L = 6/5$) versus metal line width (a) and channel width (b). (c) V-OFET and OFET capacitance ($W/L = 6/5$) versus metal line width for various overlay accuracies.

gate area of V-OFETs and of planar FETs with different channel lengths L ($OL = LW = 3.5\ \mu$m) is shown as function of the channel width W. As it can be seen, even when scaling the channel length down to 3 μm, the area ratio remains lower than 80%. This reduction of gate area for V-OFETs is related to the vertical channel configuration as well as to the fact that all edges of the source electrode contribute to the channel width.

So far we compared the total gate area for vertical and horizontal FETs. However, this does not directly translate into a gate capacitance gain since only the overlap area between gate and source/drain electrodes contribute the FET capacitance. In figure 3(c), we show the ratio of the device capacitance of vertical and horizontal FETs for a typical value of $W = 6\ \mu$m and a channel length $L = 5\ \mu$m for the planar FET. As it can be seen, the ratio between the vertical and the horizontal FET strongly depends on the line width and to a lesser extent on the overlay accuracy. In particular, there is no advantage of the vertical configuration for $LW \geqslant 6\ \mu$m and $OL \geqslant 4\ \mu$m. However, this case is not relevant for high-resolution displays which require small line width and overlay. For application-relevant dimensions such as $LW \leqslant 4\ \mu$m and $OL \leqslant 4\ \mu$m, the V-OFET provides a reduction of gate capacitance of at least 20%. This reduction of capacitance becomes increasingly important when LW and OL are scaled down as it is needed for higher display resolutions (⩾4k2k).

We would finally like to give an example of typical values for an AMOLED display backplane considering the two layouts in figure 1(c). These are optimized for a design $OL = LW = 3.5\ \mu$m and characterized by $W = 7\ \mu$m and $L = 5\ \mu$m. Assuming a specific gate capacitance of 20 nF cm^{-2}, the device capacitance would be only 12 fF for the V-OFET to be compared to 17 fF for the corresponding planar FET. Furthermore, the reader should keep in mind that due to its short channel, a V-OFET with $W = 6\ \mu$m provides significantly more on-current density than the corresponding planar OFET [22].

Finally, we would like to highlight the importance of this capacitance reduction for the pixel design and performance of a high resolution display. The capacitance reduction affects the dynamic behavior of the switching transistor in two ways. Firstly, the lower total capacitance leads to a faster response (shorter raise time of current) of the switching transistor during the programming phase of the pixel. However, the capacitance reduction due to smaller overlay does not translate one-to-one into a raise time reduction, since in a real display the raise time is also governed by the metal line resistance and the overlay capacitance of the supply lines. Still, the reduced transistor capacitance reduces the overall capacitive load of the supply lines. The second and probably most important effect of the reduced capacitance of the switching transistor concerns the turning-off behavior of the switching transistor at the end of the programming phase. As mentioned above, the gate-drain overlay capacitance leads to a rapid discharging of the storage capacitor and hence a loss of the brightness information programmed onto the storage capacitor when the switching transistor is abruptly switched off. This effect is known as voltage-kick-back effect [25] and it is determined by the ratio of the storage capacitance to the gate-drain capacitance. In fact, the suppression of this kick-back effect is vital for the fabrication of high resolution displays and it is one of the main reasons why self-aligned transistor architectures are preferred for such display. In this context, a reduction of the transistor capacitance by more than 40% enabled by the

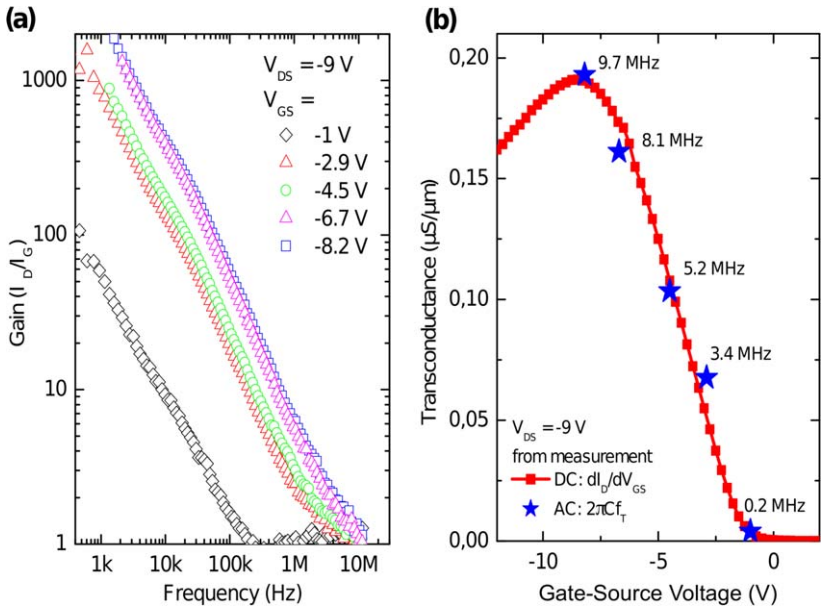

Figure 4. (a) Current Gain $|I_D|/|I_G|$ obtained from AC-measurements (sinusoidal input voltage with varying amplitude at the gate and constant drain-source voltage) and extraction of the unity gain cutoff frequency $f_T = f(|I_D|/|I_G| = 1)$. (b) Transconductance derived from DC measurements (red curve) and transconductance calculated from AC values (f_T, C) for different gate-source voltages showing the consistency of AC and DC measurements.

vertical configuration is essential in order to effectively suppress the kick-back effect.

3. V-OFET dynamic performance

In the following, the scaling behavior and the dynamic properties of V-OFETs are studied for different device dimensions in order to experimentally validate the impact of the device capacitances. In our experiments, the metal line width of the source is varied from 5 to 10 μm while we keep a constant overlay of 5 μm, which is the limitation of our alignment tool. We discuss the dynamic properties, in particular unity gain and cutoff frequency, exemplarily for a V-OFET device with $OL = LW = 5$ μm. Following the definition of the unity current gain $|I_D|/|I_G| = 1$, we adopt the measuring instruction for the cutoff frequency f_T as $f_T = f(|I_D|/|I_G| = 1)$.

In figure 4(a), the measured V-OFET gain $|I_D|/|I_G|$ is shown versus the AC frequency for different drain-source voltages, leading to the values of f_T highlighted in figure 4(b). For the device under analysis, we achieve a cutoff frequency of 10 MHz for driving voltages $\leqslant$10 V. This value is remarkable considering the relatively relaxed design dimensions ($OL = LW = 5$ μm) and the fact that only a moderate mobility semiconductor material ($\mu = 0.5\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) was used in this experiment. In figure 4(b), we also show the transconductance g_m as derived from the DC transfer curve. From the V-OFET layout, we predict and measure a device capacitance of 5 fF $\mu\mathrm{m}^{-1}$ for a specific gate capacitance of 51 nF cm^{-2}. By dividing the measured f_T by the measured device capacitance, we can extract an AC transconductance value which is highlighted in figure 4(b). As it can be seen, the g_m values from DC measurements well agree with the values calculated based on f_T. This proves that the V-OFET gain is scaling with g_m according to the well-known law $f_T = g_m/(2\pi C)$.

In summary, the measured cutoff frequency for V-OFETs with different device dimensions driven at a constant g_m is shown in figure 5 to further prove the scaling of f_T with the FET capacitance. These results confirm that f_T obeys the general law $f_T = g_m/(2\pi C)$ providing an important learning for the design of AM backplanes based on the V-OFET technology. Furthermore, it enables us drawing a very simple equivalent circuit model (see inset in figure 5) which shows that the V-OFET is equivalent to an ultra-short channel horizontal FET in terms of cutoff frequency. Figure 5 finally demonstrates the promising performance of V-OFETs in terms of applications. A measured cutoff frequency of 10 MHz achieved for driving voltages $\leqslant$10 V would satisfy the requirements for a switching transistor in an AMOLED display with a 4k2k resolution (2T1C pixel design) [4]. Moreover, we can predict from our investigations on device scaling that cutoff frequencies beyond 30 MHz and low device capacitances (1.8 fF $\mu\mathrm{m}^{-1}$ for 20 nF cm^{-2}) can be achieved by targeting a process with application-relevant dimensions such as $OL = LW = 3.5$ μm.

4. Discussion and conclusions

The development of backplane technologies with improved performance and simplified manufacturing

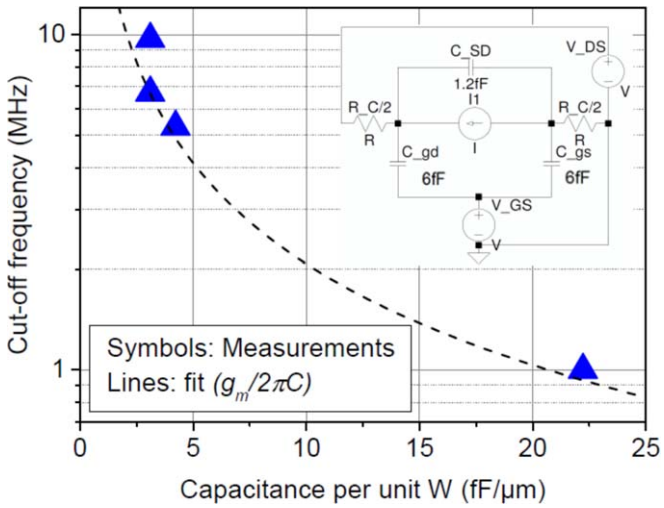

Figure 5. Cutoff frequency versus device capacitance for $g_m = 0.13\ \mu S\ \mu m^{-1}$ measured for V-OFETs with different metal line widths (capacitance/channel width). The inset shows an equivalent circuit model of the V-OFET for device dimensions of $OL = LW = 3.5\ \mu m$, $W = 7\ \mu m$. Mistakenly, the V-OFET with the smallest capacitance as been measured at higher voltage leading to a higher transconductance of $0.19\ \mu S\ \mu m^{-1}$.

processes is mandatory to satisfy customer requirements for next generation flat panel displays. We have demonstrated in this work that vertical organic FETs have the potential to meet the requirements for ultra-high resolution displays. In particular, we have shown that our vertical organic FET technology gives excellent static device performance, namely 10^7 on/off ratio and a on-current density of $\sim 5\ \mu A\ \mu m^{-1}$, which are on par to alternative vertical organic transistor concepts [17, 26] and leading edge, short channel horizontal organic transistors [7, 8]. The 10 MHz cutoff frequency of the V-OFETs presented in this paper is still below the record of best horizontal (27.7 MHz) and vertical organic transistors (40 MHz) [7, 16]. These records though, have been demonstrated for large area devices and fabrication processes such as shadow mask patterning which are difficult to adapt in a production process. The V-OFETs presented in this work, however, possess a size which is relevant for display applications and they have been fabricated using fully scalable processes which can be performed at temperatures lower than 120 °C. Additionally, we have demonstrated that our vertical FET configuration has further advantages in terms of device capacitance when scaling down FET dimensions as required for ultra-high resolution displays. The combination of high electrical performance and low temperature processing typical for organic transistors [5, 27] is the key advantage of V-OFETs when compared to today's mainstream backplane technologies, such as LTPS or MO, which require high-temperature deposition or annealing. This makes the V-OFET an ideal backplane solution for the fabrication of displays on high-flexibility substrates with no penalty on display quality. Although the achievements in this work are important milestones towards the application of V-OFET in the display industry, further work shall address the full pixel integration of our devices and further enhancement of FET performance. By implementation of state-of-the-art OSCs with high carrier mobility, we expect that the performance level of V-OFETs will reach the benchmark of the best MO-FETs while keeping its advantages in terms of technology cost and reduced processing temperature. Furthermore, it remains an active field of development for us to transfer this vertical transistor processes to flexible substrates. The biggest concern in this regard is the undesired thermal expansion of the substrate which renders the fabrication of such small devices very challenging.

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References

[1] Mativenga M, Geng D and Jang J 2014 *SID Symp. Digest of Technical Papers* vol 45, p 1
[2] Kiazadeh A, Gomes H L, Barquinha P, Martins J, Rovisco A, Pinto J V, Martins R and Fortunato E 2016 *Appl. Phys. Lett.* **109** 051606
[3] Kim Y-H, Heo J-S, Kim T-H, Park S, Yoon M-H, Kim J, Oh M S, Yi G-R, Noh Y-Y and Park S K 2012 *Nature* **489** 128
[4] Yoon J *et al* 2015 *SID Symp. Digest of Technical Papers* vol 46, p 962
[5] Sekitani T, Zschieschang U, Klauk H and Someya T 2010 *Nat. Mater.* **9** 1015
[6] Yamamura A, Watanabe S, Uno M, Mitani M, Mitsui C, Tsurumi J, Isahaya N, Kanaoka Y, Okamoto T and Takeya J 2018 *Sci. Adv.* **4** eaao5758
[7] Kitamura M and Arakawa Y 2011 *Japan. J. Appl. Phys.* **50** 01BC01
[8] Borchert J W, Peng B, Letzkus F, Burghartz J N, Chan P K L, Zojer K, Ludwigs S and Klauk H 2019 *Nat. Commun.* **10** 1119
[9] Ma L and Yang Y 2004 *Appl. Phys. Lett.* **85** 5084

[10] Stutzmann N, Friend R H and Sirringhaus H 2003 *Science* **299** 1881
[11] Fischer A, Siebeneicher P, Kleemann H, Leo K and Lüssem B 2012 *J. Appl. Phys.* **111** 044507
[12] Kleemann H, Günther A A, Leo K and Lüssem B 2013 *Small* **9** 3670
[13] McCarthy M A, Liu B and Rinzler A G 2010 *Nano Lett.* **10** 3467
[14] Lüssem B, Günther A, Fischer A, Kasemann D and Leo K 2015 *J. Phys.: Condens. Matter* **27** 443003
[15] Ben-Sasson A J, Chen Z, Facchetti A and Tessler N 2012 *Appl. Phys. Lett.* **100** 263306
[16] Kheradmand-Boroujeni B, Klinger M P, Fischer A, Kleemann H, Leo K and Ellinger F 2018 *Sci. Rep.* **8** 7643
[17] Klinger M P, Fischer A, Kaschura F, Widmer J, Kheradmand-Boroujeni B, Ellinger F and Leo K 2017 *Sci. Rep.* **7** 44713
[18] Dollinger F, Iseke H, Guo E, Fischer A, Kleemann H and Leo K 2019 *Adv. Electron. Mater.* **5** 1900576
[19] Sawatzki F M, Doan D H, Kleemann H, Liero M, Glitzky A, Koprucki T and Leo K 2018 *Phys. Rev. Appl.* **10** 034069
[20] Chan I and Nathan A 2005 *Appl. Phys. Lett.* **86** 253501
[21] Petti L, Frutiger A, Münzenrieder N, Salvatore G A, Büthe L, Vogt C, Cantarella G and Tröster G 2015 *IEEE Electron Device Lett.* **36** 475
[22] Furno M, Kleemann H, Schwartz G and Blochwitz-Nimoth J 2015 *SID Symp. Digest of Technical Papers* vol 46, p 597
[23] Kleemann H, Zakhidov A A, Anderson M, Menke T, Leo K and Lüssem B 2012 *Org. Electron.* **13** 506
[24] Höppner M, Kneppe D, Kleemann H and Leo K 2020 *Org. Electron.* **76** 105357
[25] Kwon J Y and Jeong J K 2015 *Semicond. Sci. Technol.* **30** 024002
[26] Uno M, Cha B-S, Kanaoka Y and Takeya J 2015 *Org. Electron.* **20** 119
[27] Harrison C W M, Garden D K and Horne I P 2014 *SID Symp. Digest of Technical Papers* vol 45, p 256