

# Negative bias-induced threshold voltage instability and zener/interface trapping mechanism in GaN-based MIS-HEMTs\*

Qing Zhu(朱青)<sup>1,2</sup>, Xiao-Hua Ma(马晓华)<sup>2,†</sup>, Yi-Lin Chen(陈怡霖)<sup>1,2</sup>, Bin Hou(侯斌)<sup>2</sup>,  
Jie-Jie Zhu(祝杰杰)<sup>1,2</sup>, Meng Zhang(张濛)<sup>2</sup>, Mei Wu(武玫)<sup>2</sup>, Ling Yang(杨凌)<sup>1,2</sup>, and Yue Hao(郝跃)<sup>2</sup>

<sup>1</sup>School of Advanced Materials and Nanotechnology, Xidian University, Xi'an 710071, China

<sup>2</sup>State Key Discipline Laboratory of Wide Bandgap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, China

(Received 7 February 2020; revised manuscript received 14 February 2020; accepted manuscript online 20 February 2020)

We investigate the instability of threshold voltage in D-mode MIS-HEMT with *in-situ* SiN as gate dielectric under different negative gate stresses. The complex non-monotonic evolution of threshold voltage under the negative stress and during the recovery process is induced by the combination effect of two mechanisms. The effect of trapping behavior of interface state at SiN/AlGaN interface and the effect of zener traps in AlGaN barrier layer on the threshold voltage instability are opposite to each other. The threshold voltage shifts negatively under the negative stress due to the detrapping of the electrons at SiN/AlGaN interface, and shifts positively due to zener trapping in AlGaN barrier layer. As the stress is removed, the threshold voltage shifts positively for the retrapping of interface states and negatively for the thermal detrapping in AlGaN. However, it is the trapping behavior in the AlGaN rather than the interface state that results in the change of transconductance in the D-mode MIS-HEMT.

**Keywords:** threshold voltage instability, interface state, zener trap, MIS-HEMT

**PACS:** 73.61.Ey, 73.40.Kp, 73.50.Gr, 73.20.-r

**DOI:** 10.1088/1674-1056/ab7809

## 1. Introduction

The GaN-based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) have been extensively studied for high power switching application, mainly due to greatly suppressed gate leakage and enlarged gate swing compared with the conventional Schottky-gate HEMTs.<sup>[1,2]</sup> However, introducing an insulating layer would bring in additional defects and trap states which can lead to severe device instabilities.<sup>[3,4]</sup> Even state-of-the-art devices suffer threshold voltage ( $V_{th}$ ) drift introduced by positive or negative gate bias stress.<sup>[5,6]</sup> Typically, the  $V_{th}$  would move positively under positive gate bias stress and negatively under negative gate stress, due to the trapping and detrapping of electrons at the insulator/AlGaN interface or in the insulating layer, respectively.<sup>[7-9]</sup> Both processes are recoverable with different kinetics.<sup>[9]</sup>

The conclusions for positive  $V_{th}$  instability were similar in Refs. [10–13]. A broad distribution of capture and emission time constant have been reported under positive gate stress and recovery conditions, respectively,<sup>[14]</sup> for a distribution of energy and capture cross section of traps at or near the interface, and additional lateral trapping at the dielectric/III-N interface plane due to carrier hopping and thus a transport mechanism between the interface/border states.<sup>[15,16]</sup> The instability of  $V_{th}$  under negative gate stress is a serious concern for depletion-mode devices when they need to be turned off and during off-state. However, there are different views of the mechanisms

behind the negative bias-induced  $V_{th}$  instability. The recoverable negative drift of  $V_{th}$  due to electrons' emission from interface states and border traps has been reported.<sup>[7,17–19]</sup> There is non-recoverable negative drift of  $V_{th}$  in the harsh stress condition due to the formation of interface states as a result of broken H bonds at oxide/semiconductor interface.<sup>[20]</sup> The mechanism of negative  $V_{th}$  drift was also introduced by the accumulation of holes under gate, and the holes were suggested to be generated by impact ionization or inter-band tunneling in the high electric field region.<sup>[21]</sup> However, in the hole-barrier-free E-mode SiN/GaN MIS-FET, the holes, generated in high reverse-bias condition, could not accumulate at the interface and would flow through the gate dielectric, which accelerated the generation of new defects in the gate dielectric and resulted in the large positive  $V_{th}$  shifting.<sup>[22,23]</sup> The positive  $V_{th}$  drift in fully recessed enhancement mode metal-insulator-semiconductor field-effect transistor (MOSFET) under negative gate stress has been reported to be due to the gate-injection and the following trapping in the dielectric layer and the inductively coupled plasma (ICP) recessed GaN channel layer.<sup>[24]</sup>

In this paper, we study the instability of  $V_{th}$  in D-mode MIS-HEMT, with *in situ* SiN as gate dielectric under negative gate stress. It is observed that the drift of  $V_{th}$  is non-monotonic whether in the negative stress condition or after the stress. This is inconsistent with what has been reported. A physical model, based on the combination of the effect of interface states at SiN/AlGaN and the effect of the zener trap in the AlGaN barrier, is proposed for the  $V_{th}$  behavior in the D-mode

\*Project supported by the National Key Research and Development Program of China (Grant No. 2018YFB1802100), the Science Challenge Project, China (Grant No. TZ2018004), and the National Natural Science Foundation of China (Grant Nos. 61534007 and 11690042).

†Corresponding author. E-mail: [xhma@xidian.edu.cn](mailto:xhma@xidian.edu.cn)

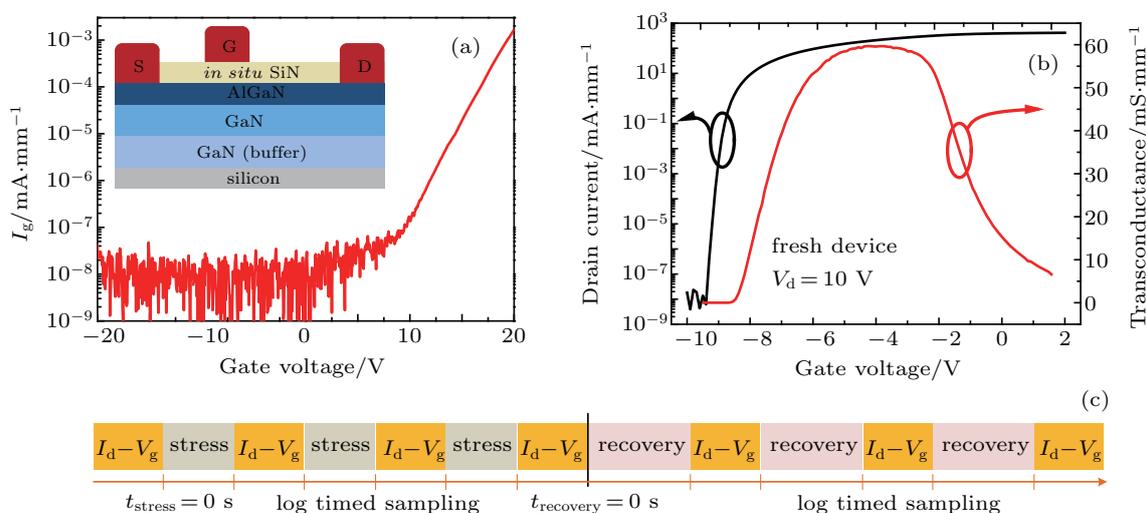
MIS-HEMT. The results in this work provide a comprehensive insight into the instability of  $V_{th}$  in the D-mode MIS-HEMT.

## 2. Devices and experiments

The study was carried out on D-mode MIS-HEMT grown on a Si substrate. The epilayers, from bottom to top, consisted of a GaN buffer intentionally doped with C, an undoped GaN channel, an  $Al_{0.22}Ga_{0.78}N$  barrier, and 30-nm *in situ* SiN as gate dielectric and passivation layer. The cross section of the device is sketched in the inset of Fig. 1(a) (not scaled). The gate length and gate-source distance of the device under test are both 3  $\mu m$ , and gate-drain distance is 20  $\mu m$ . Figure 1(a) exhibits great effects on suppressing gate leakage current at

both reverse and forward bias. The transfer and transconductance characteristics are shown in Fig. 1(b). The fresh device shows that  $I_{d,max}$  is 414 mA/mm,  $V_{th}$  is  $-9.05$  V, and  $G_{m,max}$  is 60 mS/mm.

In order to avoid the influence of drain voltage on the experiment and focus on the region under gate, the drain voltage was set to be 0 V during the stress and the transfer measurements were carried out at  $V_d = 0.1$  V in the intermediate monitoring process. Meanwhile, the gate voltage was swept from  $-10$  V to  $-7$  V in order to exclude the influence of the positive gate voltage. The  $V_{th}$  was defined as the gate voltage corresponding to the drain current of 1  $\mu A/mm$ . The detail of experimental process is shown as Fig. 1(c).



**Fig. 1.** (a) The  $I_{gs}-V_{gs}$  characteristics of MIS-HEMTs with inset showing schematic cross section view of MIS-HEMT. (b) Transfer and transconductance characteristics at  $V_{ds} = 10$  V. (c) Schematic diagram of experimental procedure.

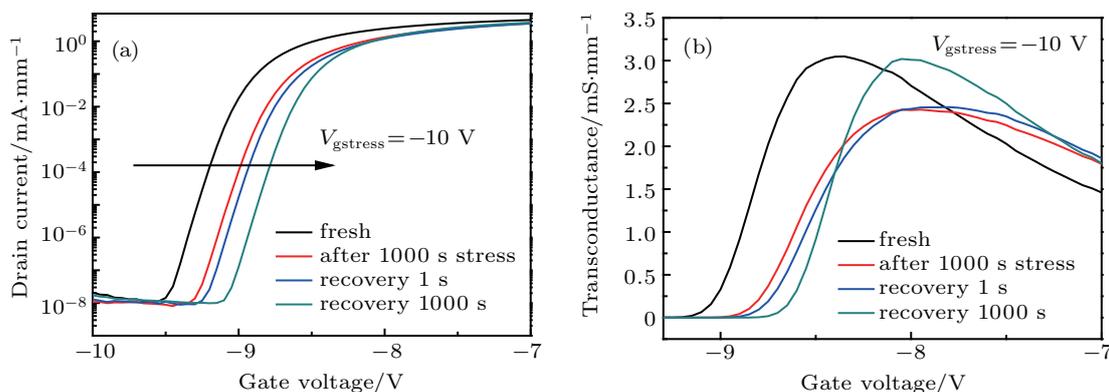
## 3. Results and discussion

As shown in Fig. 2(a), when the negative gate stress of  $V_g = -10$  V is applied, the  $V_{th}$  shifts positively. It is unusual that the  $V_{th}$  continues shifting positively even after the stress has been removed. In addition, the maximum of transconductance ( $G_{m,max}$ ) decreases during the negative stress and increases in the recovery process as shown in Fig. 2(b).

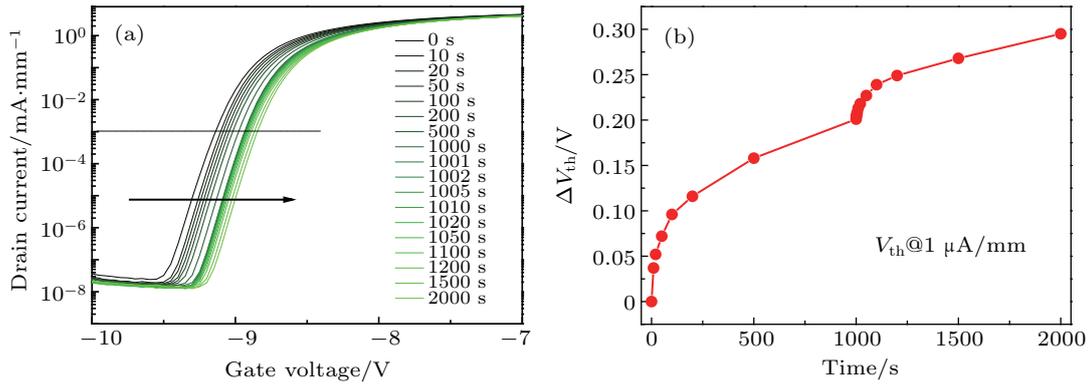
To exclude the influence of the monitoring tests, the transfer measurements without any stress at certain time as men-

tioned above are conducted, and the results are shown in Fig. 3(a). Figure 3(b) shows that the  $V_{th}$  shifts positively at all times.

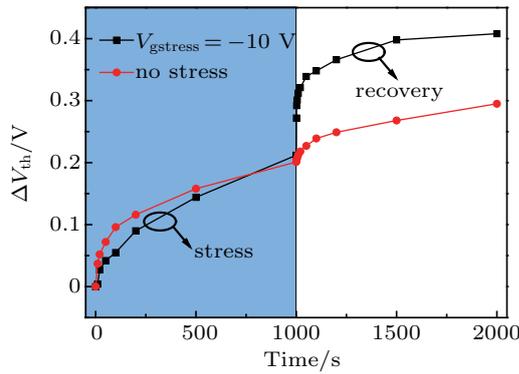
Figure 4 shows the difference between  $V_{th}$  under  $V_g = -10$  V negative stress and that under  $V_g = 0$  V (no stress). The amount of  $V_{th}$  drift with no stress is larger than that under stress ( $0 s < time < 500 s$ ). However, when  $1000 s < time \leq 2000 s$ , the  $V_{th}$  shifts more positively after exerting stress than that under no stress.



**Fig. 2.** (a) Transfer and (b) transconductance curves of GaN-based MIS-HEMTs at different time.



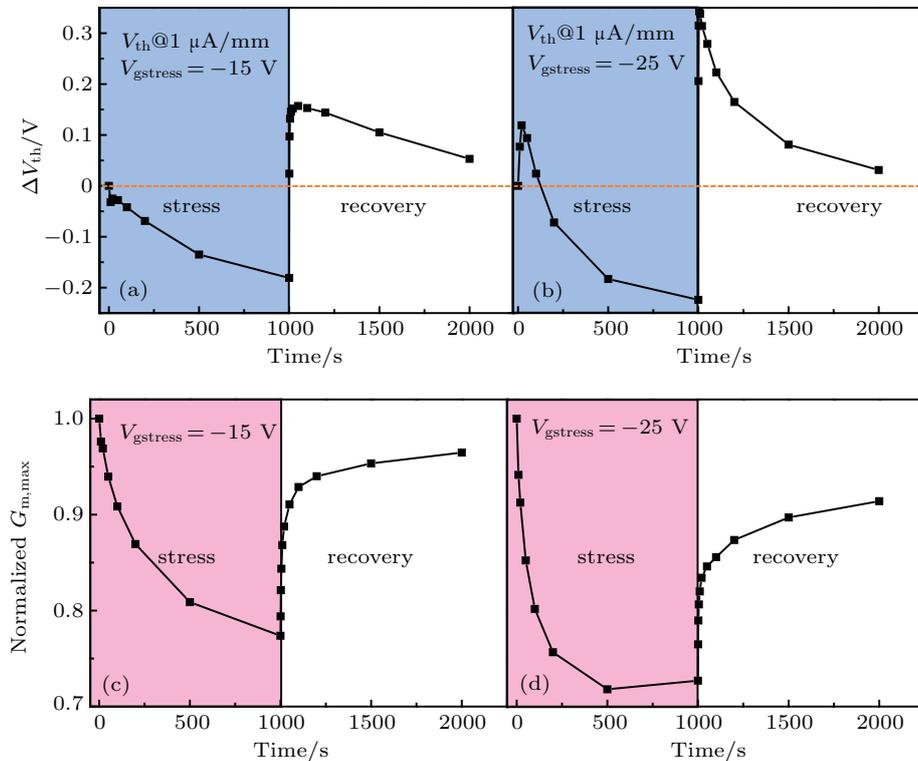
**Fig. 3.** (a) Transfer characteristics measured in 2000 s without any stress, and (b) the variations of threshold voltage with time during the experiments in panel (a).



**Fig. 4.** Drift of  $V_{th}$  versus sampling time with and without negative biased stress.

To further investigate the mechanisms of  $V_{th}$  drift, variations of  $\Delta V_{th}$  with stress time under the negative stresses of

$V_{gstress} = -15$  V and  $-25$  V excluding the influence of the monitoring tests are shown respectively in Figs. 5(a) and 5(b), where  $\Delta V_{th}$  is the difference between the  $V_{th}$  drift under stress and the  $V_{th}$  drift (the degradation of  $G_{m,max}$ ) under no stress. The  $V_{th}$  shifts negatively when  $V_{gstress} = -15$  V. After the stress is removed, the  $V_{th}$  shifts first positively and then negatively. As shown in Fig. 5(c), the  $G_{m,max}$  decreases to 77.37% under  $-15$  V stress and recovers to 96.46% as the recovery time reaches to 1000 s. For  $V_{gstress} = -25$  V, the  $V_{th}$  shifts first positively and then negatively during the stress. As the stress is removed, the  $V_{th}$  shifts first positively and then negatively. As shown in Fig. 5(d), the  $G_{m,max}$  decreases to 71.79% under  $-25$  V stress and recovers to 91.40% as the recovery time reaches to 1000 s.



**Fig. 5.** Plots of  $\Delta V_{th}$  versus stress time and recovery time under stress voltage of (a)  $-15$  V and (b)  $-25$  V. Plots of normalized  $G_{m,max}$  versus stress time and recovery time under stress voltage of (c)  $-15$  V and (d)  $-25$  V.

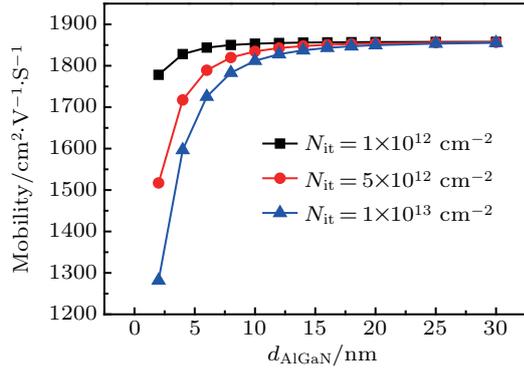


Fig. 6. Plots of calculated mobility versus thickness of AlGaN barrier for different SiN/AlGaN interface charge densities.

Before analyzing the drift of the  $V_{th}$ , the change of the  $G_{m,max}$  should be investigated first. In general, the traps in the SiN insulator and at SiN/AlGaN interface have effects on the electron mobility, acting as remote impurity scattering, thus  $G_{m,max}$  decreases.<sup>[25]</sup> Experimental results and theoretical calculations indicate that the remote scattering rate decreases exponentially as the distance increases between the charges and the channel, which could be simplified as the thickness of AlGaN barrier layer.<sup>[26,27]</sup> In this work, the thickness of AlGaN in MIS-HEMT is 20 nm. The remote impurity scattering could be neglected for the 20 nm AlGaN layer, which is shown in Fig. 6. As a result, the electrons trapping and detrapping at SiN/AlGaN interface and in the SiN insulator can induce the  $V_{th}$  drift but have little influence on  $G_{m,max}$ . However, the

$G_{m,max}$  decreases under the negative stress and increases in the recovery process, indicating that there is trapping behavior in the place closer to the channel, which is in the barrier here.

In the above analysis, the location where the trapping- and detrapping-behaviors occur is identified, and the mechanisms for the drift of  $V_{th}$  can be proposed in the following. Under the negative stress, a strong electric field exists in the barrier layer under the gate, especially at the edges of the gate on the source side and drain side. Electrons can be trapped in the AlGaN barrier, which can take place under high reverse electric field, when electrons tunnel from the valence band to the trap states in the AlGaN barrier in a process, which is sometimes referred to as zener trapping.<sup>[20,28]</sup> The trapped electrons induce the  $V_{th}$  to positively drift and the  $G_{m,max}$  to decrease under the negative stress. This mechanism runs in parallel with the detrapping behavior of interface states at SiN/AlGaN, which induces the  $V_{th}$  to negatively drift and has little influence on transconductance. The effect of zener trap is strongest at the edge of gate, where the highest electric field exists. Trapped electrons lift the bands up as shown in Fig. 7(b). When the negative stress is removed, the  $V_{th}$  shifts negatively for electrons escaped from the trap in the barrier by thermal activation. On the contrary, as the stress is removed, the interface state at SiN/AlGaN falls again below the Fermi level, and is filled with electrons, which induces the  $V_{th}$  to positively drift. The evolution of  $V_{th}$  in the stress and recovery process under the two mechanisms are shown in Fig. 8.

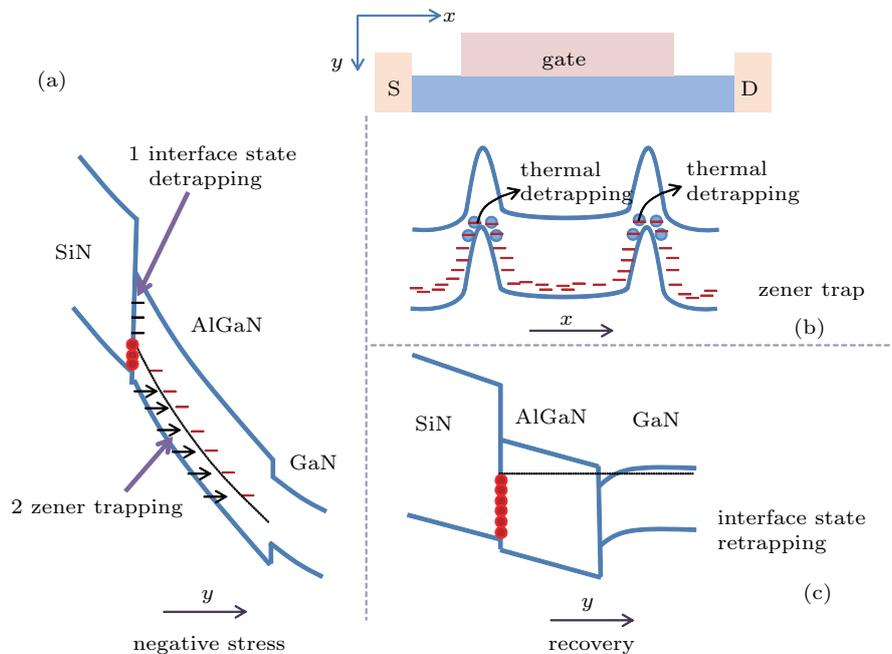
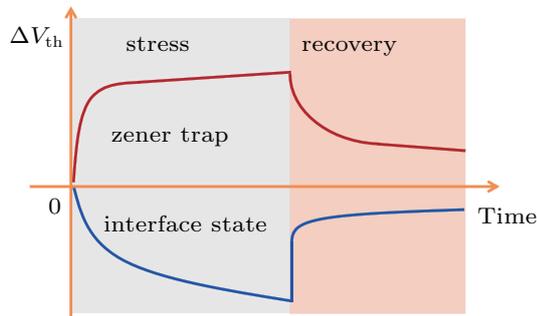


Fig. 7. (a) Two mechanisms under negative stress. Behaviors of (b) zener traps and (c) interface states in recovery process.

Considering the two mechanisms, figure 4 should be further analyzed. When no stress is applied, zener trapping dominates in the monitoring process. And it is hard for the thermal

detrapping because bands lift up slightly with  $V_g = -10$  V. As a result, the  $V_{th}$  shifts positively at all times under no stress. For  $V_{gstress} = -10$  V, the detrapping of the interface states

induces the  $V_{th}$  to less positively drift under negative stress ( $0 \text{ s} < \text{time} < 500 \text{ s}$ ). And the retrapping of the interface states results in the more positive drift of  $V_{th}$  as the stress is just removed.



**Fig. 8.** Plot of variation of  $V_{th}$  with time, induced by zener traps and interface states in negative stress and recovery process.

As shown in Fig. 5(a), for  $V_{g\text{stress}} = -15 \text{ V}$ , the detrapping of interface states dominates the negative drift of  $V_{th}$ . As the  $-15 \text{ V}$  stress is removed, the interface states, especially those with low energy level, can be retrapped rapidly, which results in a sharply positive drift of  $V_{th}$  in 2 s. The electrons are trapped in the AlGaIn barrier due to the zener trapping under  $-15 \text{ V}$  stress, which results in a relatively small positive drift, and then electrons in the AlGaIn barrier can be detrapped through thermal process, resulting in the negative drift of  $V_{th}$ . On account of the relatively deep level, the electrons' thermal detrapping dominates as the time goes on in the recovery process. Because the transconductance is mostly associated with zener traps in the AlGaIn, the variation of  $G_{m,\text{max}}$  is relatively simple as shown in Fig. 5(c). The trapped electrons in the AlGaIn enhance the scattering, indicating the decrease of  $G_{m,\text{max}}$ . And the thermal detrapping in the recovery process causes  $G_{m,\text{max}}$  to increase.

As shown in Fig. 5(b), when  $V_{g\text{stress}} = -25 \text{ V}$  is applied, both the trap effect of interface states at SiN/AlGaIn and the zener trap effect in the AlGaIn barrier are enhanced. The zener trap is based on the tunneling process, whose time constant is on the order of picoseconds. As a result, zener trap effect dominates at the beginning of stress for the higher electric field under a stress of  $-25 \text{ V}$ . As the time increases, the interface states dominate instead. The  $V_{th}$  shifts first positively and then negatively. When the stress is removed, the variation of  $V_{th}$  under stress of  $V_g = -25 \text{ V}$  is similar to that under  $-15 \text{ V}$  stress. It is noted that the negative drift of  $V_{th}$  is faster under  $-25 \text{ V}$  stress. More electrons trapped in the AlGaIn lift the energy bands higher, making thermal emission take place more easily. As the number of trapped electrons decreases, the energy band's lifting up becomes low again and the thermal emission is weakened. As a result, the negative drift of  $V_{th}$  slows down.

## 4. Conclusions

In conclusion, the instabilities of  $V_{th}$  in D-mode MIS-HEMT, with *in situ* SiN as gate dielectric under different negative gate stresses are investigated. The effect of interface state at SiN/AlGaIn and the effect of zener trap in AlGaIn barrier layer are opposite to each other both under negative stress and in recovery process (no stress). The  $V_{th}$  negatively shifts under the stress due to the detrapping of the electrons at SiN/AlGaIn interface, and positively shifts due to zener trapping in AlGaIn. As the stress is removed,  $V_{th}$  positively shifts for the retrapping of interface states and negatively for the thermal detrapping in AlGaIn. The complex non-monotonic evolution of  $V_{th}$  is induced by the two mechanisms together. However, it is the trap behavior in the AlGaIn rather than the interface states that gives rise to the change of transconductance in the D-mode MIS-HEMT.

## References

- [1] Yatabe Z, Hori Y, Ma W C, Asubar J T, Akazawa M, Sato T and Hashizume T 2014 *Jpn. J. Appl. Phys.* **53** 100213
- [2] Zhang Z, Yu G, Zhang X, Deng X, Li S, Fan Y, Sun S, Song L, Tan S, Wu D, Li W, Huang W, Fu K, Cai Y, Sun Q and Zhang B 2016 *IEEE Trans. Electron Dev.* **63** 731
- [3] Fiorenza P, Greco G, Iucolano F, Patti A and Roccaforte F 2015 *Appl. Phys. Lett.* **106** 142903
- [4] Lu X, Yu K, Jiang H, Zhang A and Lau K M 2017 *IEEE Trans. Electron Dev.* **64** 824
- [5] Ostermaier C, Lagger P, Reiner M and Pogany D 2018 *Microelectron. Reliab.* **62** 83
- [6] Blaho M, Gregušová D, Haščík Š, Ťapajna M, Fröhlich K, Šatka A and Kuzmík J 2017 *Appl. Phys. Lett.* **111** 033506
- [7] Yang S, Liu S, Liu C, Tang Z, Lu Y and Chen K J 2014 *IEEE International Electron Devices Meeting, December 15–17, 2014, San Francisco, California, USA*, p. 17.2.1
- [8] Lagger P, Steinschifter P, Reiner M, Stadtmüller M, Denifl G, Naumann A, Müller J, Wilde L, Sundqvist J, Pogany D and Ostermaier C 2014 *Appl. Phys. Lett.* **105** 033512
- [9] Meneghesso G, Meneghini M, De C, Ruzzarin M and Zanoni E 2018 *Microelectron. Reliab.* **80** 257
- [10] Lansbergen G P, Wong K Y, Lin Y S, Yu J L, Yang F J, Tsai C L and Oates A S 2014 *IEEE International Reliability Physics Symposium, June 1–5, 2014, Hilton Waikoloa Village, Hilo, USA*, p. 6C.4.1
- [11] Yang S, Lu Y, Liu S, Wang H, Liu C and Chen K J 2016 *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), June 12–16, 2013, Prague, Czech Republic*, p. 263
- [12] Acurio E, Crupi F, Magnone P, Trojman L, Meneghesso G and Iucolano F 2017 *Solid State Electron.* **132** 49
- [13] Lagger P, Ostermaier C, Pobegen G and Pogany D 2012 *International Electron Devices Meeting, December 10–12, 2012, San Francisco, California, USA*, p. 13.1.1
- [14] Lagger P, Reiner M, Pogany D and Ostermaier C 2014 *IEEE Trans. Electron Dev.* **61** 1022
- [15] Zhang K, Wu M, Lei X Y, Chen W W, Zheng X F, Ma X H and Hao Y 2014 *Semicond. Sci. Technol.* **29** 075019
- [16] Guo A and Alamo J A 2017 *IEEE Trans. Electron Dev.* **64** 2142
- [17] Meneghini M, Rossetto I, Bisi D, Ruzzarin M, Hove M V, Stoffels S, Wu T, Marcon D, Decoutere S, Meneghesso G and Zanoni E 2016 *IEEE Electron Dev. Lett.* **37** 474
- [18] Dalcanale S, Meneghini M, Tajalli A, Rossetto I, Ruzzarin M, Zanoni E, Meneghesso G, Moens P, Banerjee A and Vandeweghe S 2017 *IEEE International Reliability Physics Symposium (IRPS), April 2–6, 2017, Monterey, CA, USA*, p. 4B

- [19] Meneghesso G, Silvestri R, Meneghini M, Cester A, Zanoni E, Verzellesi G, Pozzovivo G, Lavanga S, Detzel T, Häberlen O and Curatola G 2014 *IEEE International Reliability Physics Symposium (IRPS)*, June 1–5, 2014, Hilton Waikoloa Village, Hilo, USA, p. 6C.2.1
- [20] Guo A and del Alamo J A 2016 *IEEE International Reliability Physics Symposium (IRPS)*, April 17–21, 2016, Pasadena, CA, USA, p. 4A
- [21] Bahl S R, Hove M V, Kang X, Marcon D, Zahid M and Decoutere S 2013 *25th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, p. 419
- [22] Hua M, Wei J, Bao Q, He J, Zhang Z, Zheng Z, Lei J and Chen K J 2017 *IEEE International Electron Devices Meeting (IEDM)*, December 2–6, 2017, San Francisco, California, USA, p. 33.2.1
- [23] Hua M, Wei J, Bao Q, Zheng Z, Zhang Z, He J and Chen K J 2018 *IEEE Trans. Electron Dev.* **65** 3831
- [24] Sang F, Wang M J, Zhang C, Tao M, Xie B, Wen C P, Wang J Y, Hao Y L, Wu W G and Shen B 2015 *Jpn. J. Appl. Phys.* **54** 044101
- [25] Liu Z H, Ng G I, Arulkumaran S, Maung Y K, Teo K L, Foo S C and Sahnuganathan V 2009 *Appl. Phys. Lett.* **95** 223501
- [26] Hung T H, Esposto M and Rajan S 2011 *Appl. Phys. Lett.* **99** 162104
- [27] Ji D, Liu B, Lu Y, Liu G, Zhu Q and Wang Z 2012 *Appl. Phys. Lett.* **100** 132105
- [28] Jin D, Joh J, Krishnan S, Tipirneni N, Pendharkar S and Alamo J A D 2013 *IEEE International Electron Devices Meeting*, December 6–13, 2013, Washington, USA, p. 6.2.1