In-situ SiN combined with etch-stop barrier structure for high-frequency AlGaN/GaN HEMT*

Min-Han Mi(宓珉瀚)[1,†], Sheng Wu(武盛)[1], Ling Yang(杨凌)[2], Yun-Long He(何云龙)[1], Bin Hou(侯斌)[1], Meng Zhang(张濛)[1], Li-Xin Guo(郭立新)[3], Xiao-Hua Ma(马晓华)[1], and Yue Hao(郝跃)[1]

[1] *Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071, *China*
[2] *School of Advanced Materials and Nanotechnology, Xidian University, Xi'an* 710071, *China*
[3] *School of Physics and Optoelectronic Engineering, Xidian University, Xi'an* 710071, *China*

(Received 4 February 2020; revised manuscript received 14 February 2020; accepted manuscript online 18 February 2020)

The etch-stop structure including the *in-situ* SiN and AlGaN/GaN barrier is proposed for high frequency applications. The etch-stop process is realized by placing an *in-situ* SiN layer on the top of the thin AlGaN barrier. F-based etching can be self-terminated after removing SiN, leaving the AlGaN barrier in the gate region. With this *in-situ* SiN and thin barrier etch-stop structure, the short channel effect can be suppressed, meanwhile achieving highly precisely controlled and low damage etching process. The device shows a maximum drain current of 1022 mA/mm, a peak transconductance of 459 mS/mm, and a maximum oscillation frequency (f_{max}) of 248 GHz.

Keywords: AlGaN/GaN, *in-situ* SiN, etch-stop barrier

PACS: 71.55.Eq, 73.20.–r, 73.50.–h **DOI:** 10.1088/1674-1056/ab7746

1. Introduction

Due to GaN-based materials possessing superior properties, such as high mobility and high electron saturation velocity, GaN-based high electron mobility transistor (HEMT) has great potential applications in high frequency range.[1–4] For high frequency devices, it is important to reduce the gate length to improve the current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}).[5,6] However, as the gate length decreases to a certain value, the lower aspect ratio L_g/T_{bar} results in short channel effect, thus inhibiting further improvement of frequency characteristics.[7] In general, aspect ratio needs to be larger than 5 to suppress short channel effect.[8] High Al mole fraction barrier combined with thin barrier structure or recessed gate configuration is most commonly used in AlGaN/GaN heterostructure to achieve high aspect ratio. However, for high Al mole fraction barrier structure, it is difficult to form ohmic contact by using conventional annealing process,[9] which restricts the improvement of frequency performance. For the recessed gate configuration, the Cl-based plasma etching creates the high density of trap states and degrades the carrier transport characteristics in the recessing gate region.[10] In addition, it is also difficult to precisely control the recessing depth, which gives rise to poor repeatability and lowers the fabrication yield rate.[11,12] Therefore, it is necessary to propose a new structure that can not only avoid the larger contact resistance caused by high Al fraction barrier, but also eleiminate the negative influence caused by recessing gate process.

In the present research, we propose a 20-nm *in-situ* SiN layer formed by metal–organic chemical vapor deposition (MOCVD) on the top of 6-nm-thick $Al_{0.2}Ga_{0.8}N$ barrier. The benefits of introducing 20-nm *in-situ* SiN lie in two aspects. On the one hand, the 20-nm *in-situ* SiN layer is thick enough to act as a passivation layer, which can reduce barrier thinning induced large access resistance and suppress current collapse. On the other hand, due to the fact that the F-based etching has a highly selective etching ratio between AlGaN and *in-situ* SiN, the F-based recessing process is automatically stopped at the surface of AlGaN barrier as shown in Fig. 1(b), thus the etching depth can be controlled precisely and etching damage can be avoided. Therefore, the proposed structure has good compatibility with the mass production of GaN-HEMTs. For the reported etch-stop, its structure is generally composed of AlN/GaN bi-layer[13,14] to achieve normally-off device that is different from what is to be discussed in this paper.[15] With this newly proposed self-terminated structure, we can obtain the precise control of etching depth and suppress carrier transport degradation. The fabricated devices demonstrate that their effective channel mobility values slightly decrease from 1558 $cm^2 \cdot V^{-1} \cdot s^{-1}$ to 1425 $cm^2 \cdot V^{-1} \cdot s^{-1}$ after recessing their gate, a maximum drain current of higher than 1 A/mm, an extrinsic maximum transconductance of 459 mS/mm, a negligible current collapse, and an f_T/f_{max} of 90 GHz/248 GHz.

*Project supported by the China Postdoctoral Science Foundation (Grant No. 2018M640957), the Fundamental Research Funds for the Central Universities, China (Grant No. 20101196761), the National Natural Science Foundation of China (Grant No. 61904135), and the National Defense Pre-Research Foundation of China (Grant No. 31513020307).

†Corresponding author. E-mail: miminhan@qq.com

2. Device structure and fabrication

The cross section of AlGaN/GaN HEMT is schematically shown in Fig. 1, where the *in-situ* SiN HEMT and the SiN recessing HEMT were fabricated on the same wafer. The epilayer was grown on a sapphire substrate by the metal–organic chemical vapor deposition (MOCVD), which consisted of a 1.2-μm-thick GaN buffer, 6-nm-thick AlGaN barrier layer, and a 20-nm-thick *in-situ* SiN layer. Prior to the formation of the source/drain ohmic contact consisting of Ti/Al/Ni/Au (22/140/55/45 nm) metals that had been treated by the electron beam evaporation and annealing at 880 °C for 30 s in nitrogen ambient, the 20-nm-thick *in-situ* SiN located at source/drain region was removed by F-based etching. Then the device isolation was achieved by using nitrogen ion implantation. The electron-beam lithography was used to define T-shaped gate through using a double layer resist. After that, the F-based etching performed by inductive coupled plasma (ICP) etching system was used to remove the *in-situ* SiN for SiN recessing HEMT as shown in Fig. 1(b). The ICP coil power and radio frequency (RF) power were 80 W and 10 W, respectively, with a CF_4 flow rate of 25 sccm. The Ni/Au/Ni gate metal was deposited by electron beam evaporation after the gate head had been lithography treated. The gate length was 0.1 μm, the source–drain distance was 2 μm, the gate–source was 0.9 μm, and the gate width of 100 μm.

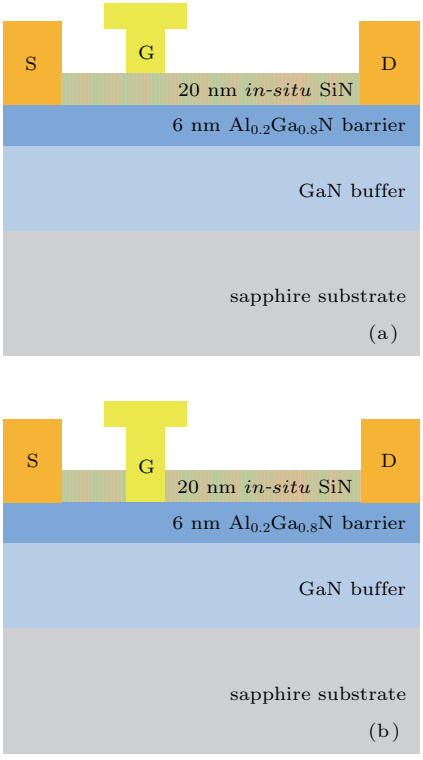

Fig. 1. Schematic diagram of (a) *in-situ* SiN HEMT and (b) recessed SiN HEMT.

To investigate the effect of *in-situ* SiN self-terminated recessing etching on the surface morphology, AFM measurement was carried out on the controlled samples, which had been cut from the wafer on which the devices had been fabricated. The etching process applied to the SiN recessing sample was the same as that used on the SiN recessing HEMT. Figure 2 shows the 5 μm×5 μm surface morphologies of the *in-situ* SiN and SiN recessing sample, respectively. The root-mean-square-surface (RMS) roughness for *in-situ* SiN sample and recessed SiN samples are 0.277 nm and 0.302 nm, respectively, indicating that the *in-situ* SiN etch-stop structure can suppress the negative influence of recessing etching process on the surface roughness.

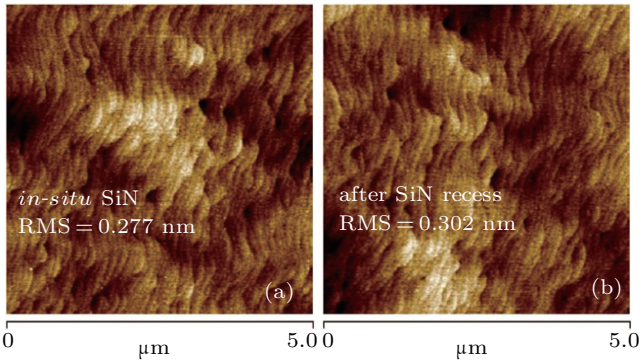

Fig. 2. The 5 μm×5 μm surface morphology of (a) the *in-situ* SiN sample and (b) after SiN recessing sample.

3. Results and discussion

Figure 3 shows the *C*–*V* characteristics of two kinds of capacitors. The turn-on voltage of the SiN recessing capacitor shifts from −8.5 V to −0.8 V compared with that of the *in-situ* SiN capacitor. The depth profile of carrier concentration extracted from *C*–*V* curve shows that the peak concentration of two-dimensional electron gas (2DEG) for the *in-situ* SiN sample is higher than that for the SiN recessing one, and the distance between gate and channel decreases from 26 nm to 6 nm. The results show that 20-nm *in-situ* SiN layer can suppress barrier thinning induced surface-related depletion and maintain 2DEG density with scaling down the barrier thickness, which can maintain low access resistance. The SiN recessing capacitor shows small frequency dispersion between 50 kHz and 1 MHz and small hysteresis under bidirectional measurement as shown in Fig. 3(c), which indicates that this etch-stop structure can eliminate the surface damage in the recessing etching process and obtain low surface trap density.

Figure 4(a) shows the transfer characteristics of two kinds of HEMTs at $V_d = 10$ V. The threshold voltage of *in-situ* SiN HEMT and SiN recessing HEMT is −8.5 V and −0.8 V, respectively, and this trend is consistent with *C*–*V* measurement. The maximum drain current of *in-situ* SiN and SiN recessing HEMT is 1165 mA/mm and 1022 mA/mm, respectively. The decreasing of drain current is due to the increasing of channel resistance, which is caused by removing the *in-situ* SiN in the gate region. The peak transconductance is 207 mS/mm and 459 mS/mm for the *in-situ* SiN and recessed SiN HEMT,

respectively. The increase of transconductance is partly attributed to the reduction in the distance between gate and channel, thus improving the ability to control gate. To ensure that the etching process is self-terminated at AlGaN barrier layer, a 100-s etch is used with 40-s over-etch as shown in Fig. 4(b). Based on the etching rate calculation, the 20-nm *in-situ* SiN can be completely removed in 60 s, and then we continue to perform the etching process for 40 s. After that the threshold voltage and maximum drain current of the sample are almost the same as those for the 60-s-etched sample. This result indicates that the etching process is automatically stopped, which can effectively avoid the effect of etching condition fluctuation on the etching depth. Figure 4(c) shows Schottky characteristics of recessed SiN HEMT and previously reported HEMT, which had the same barrier thickness of 6 nm. The previously reported HEMT adopted conventional Cl-based gate recessing process to etch down the barrier to 6 nm in the gate region. The reverse leakage at $V_g = -10$ V and forward leakage at $V_g = 2$ V of recessed SiN HEMT are 1.8×10^{-5} mA/mm and 1.2×10^{-1} mA/mm, respectively. It is observed that the gate leakage of recessed SiN HEMT is at least two orders of magnitude lower than that of previous Cl-based gate recessing HEMT, even though the recessed SiN HEMT has the same barrier thickness as the previous one. The result shows that the introduction of etch-stop structure can avoid the conventional Cl-based etching damage induced gate leakage increase.[17]

Pulsed *I–V* characteristics of SiN recessing HEMT are shown in Fig. 5(a). The quiescent bias points are chosen at (V_{GSQ}, V_{DSQ} = 0 V, 0 V), and (V_{GSQ}, V_{DSQ} = −8 V, 30 V). The pulse width is 500 ns and the pulse period is 10 μs. The result shows a negligible current collapse (∼ 2%) and knee voltage walkout. It implies that the *in-situ* SiN alone in the gate–source and gate–drain region is sufficient to suppress current collapse, and the passivation effect is comparable to that when using the conventional PECVD SiN.[18] In addition, although the *in-situ* SiN technology was adopted in Ref. [9], the thickness was only 5 nm and needs to combine with PECVD SiN together to suppress current collapse. The channel effective mobility μ_e values of two HEMTs can be extracted from $\mu_e = 1/(qN_{sh}R_{ch})$, where N_{sh} is calculated from

$$N_{sh} = \frac{1}{q}\int_{-\infty}^{V_{GS}} C\,dV,$$

R_{ch} is extracted from the on-resistance which is calculated from the linear region of output curves. Figure 5(b) shows the extracted channel effective mobility of *in-situ* SiN and SiN recessing HEMT. The peak mobility of SiN recessing HEMT is 1425 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is only slightly lower than the 1558 $cm^2 \cdot V^{-1} \cdot s^{-1}$ of peak mobility in *in-situ* SiN HEMT. As far as we know, the value of mobility after the gate has been recessed typically decreases by more than 20%.[14,19] These results indicate the etch-stop structure suppresses etching induced damage and surface roughness increase, which is responsible for the slight mobility degradation. The slight mobility degradation partly contributes to the transconductance improvement after removing *in-situ* SiN in the gate region.

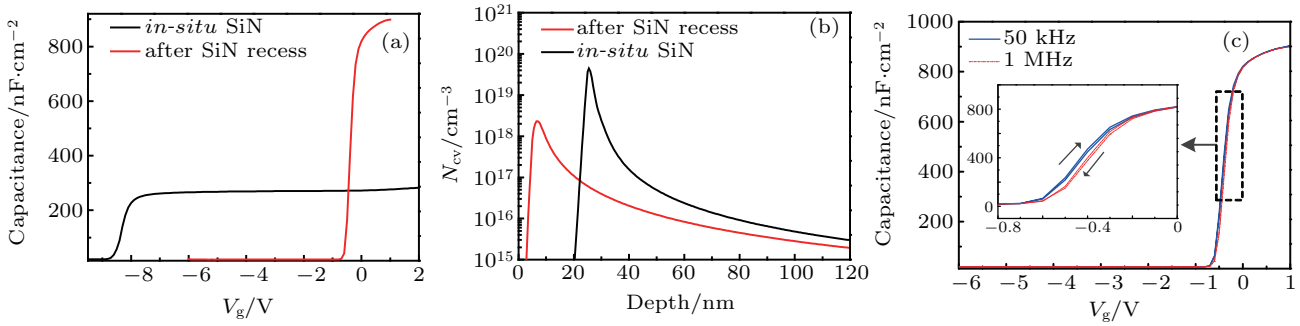

Fig. 3. (a) The *C–V* characteristics of *in-situ* SiN capacitor and SiN recessing capacitor, (b) depth profiles of carrier concentration of two kinds of capacitors, and (c) *C–V* characteristics of SiN recessing capacitor measured at different frequencies.

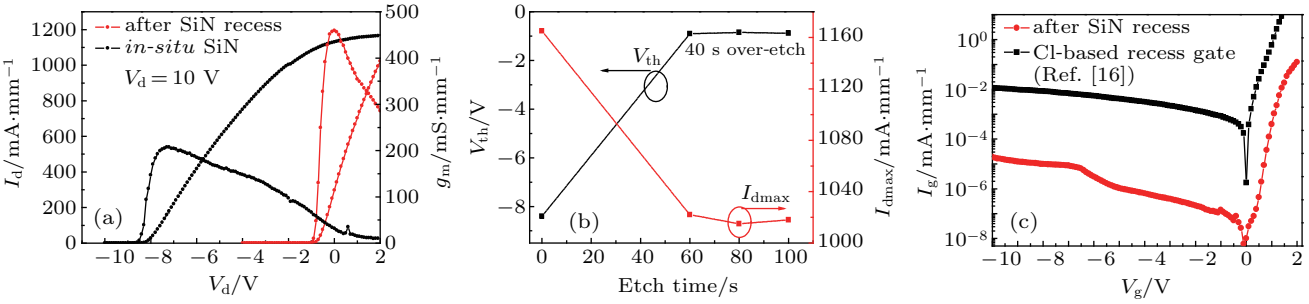

Fig. 4. (a) Transfer characteristics of *in-situ* SiN and SiN recessing HEMTs, (b) threshold voltage and maximum drain current as a function of etch time, and (c) Schottky characteristics of SiN recessing HEMT and previously reported HEMT with recessed gate of $d_{AlGaN} = 6$ nm.[16]

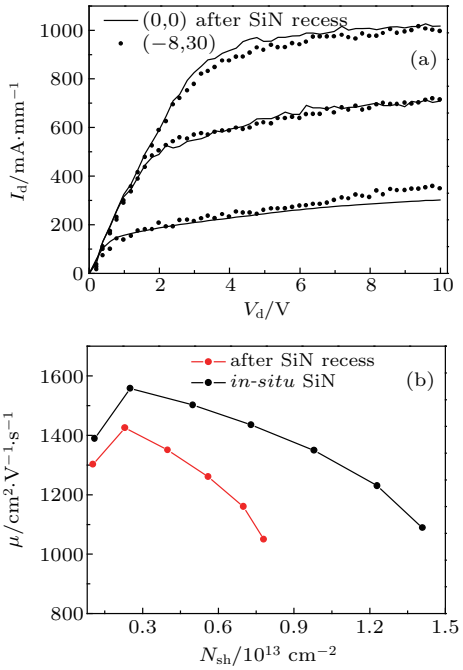

Fig. 5. (a) Pulsed *I*–*V* characteristics of SiN recessing HEMT, and (b) plots of channel effective mobility *versus* N_{sh} of *in-situ* SiN and SiN recessing HEMTs.

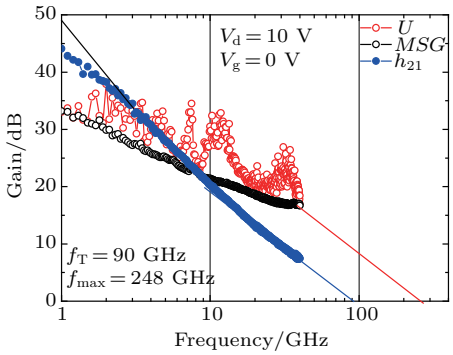

Fig. 6. Small signal characteristics of SiN recessing HEMT.

The small signal characteristics of SiN recessing HEMTs is measured in the frequency from 1 GHz to 40 GHz using Agilent 8363B network analyzer calibrated with a short-open-load-through calibration standard. The measured data were de-embedded by using on-wafer open and short devices. Figure 6 shows the current gain (h_{21}), unilateral gain (U), and maximum stable gain (MSG) of SiN recessing HEMT at $V_g = 0$ V and $V_d = 10$ V. By extrapolating of h_{21} and U curves through using −20 dB/decade slope, the values of f_T and f_{max} are 90 GHz and 248 GHz, respectively. The value of f_{max} is at a relative advanced level among the 100-nm gate length GaN-based HEMTs,[20–22] indicating that this structure has an obvious advantage in the usage of high frequency devices. If the source–drain distance and gate length are further reduced, the f_{max} can be further increased.

4. Conclusions

An *in-situ* SiN with a 6-nm $Al_{0.2}Ga_{0.8}N$/GaN etch-stop barrier is demonstrated. The etch-stop structure can not only realize automatically stopping at AlGaN barrier to eliminate etching damage, but also obtain precise etching depth and high robustness of etching process. Measurements show that the fabricated HEMT exhibits well suppressed gate leakage and current collapse, a slightly reduced effective mobility of 1425 cm^2·V^{-1}·s^{-1} after recessing *in-situ* SiN in the gate region, a maximum drain current of 1022 mA/mm, a transconductance of 459 mS/mm, and an f_{max} of 248 GHz, indicating the availability of this structure for high frequency AlGaN/GaN HEMTs.

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