Characteristics of AlGaN/GaN high electron mobility transistors on metallic substrate*

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We have successfully prepared GaN based high electron mobility transistors (HEMTs) on metallic substrates transferred from silicon substrates by electroplating technique. GaN HEMTs on Cu substrates are demonstrated to basically have the same good electric characteristics as the chips on Si substrates. Furthermore, the better heat dissipation of HEMTs on Cu substrates compared to HEMTs on Si substrates is clearly observed by thermoreflectance imaging, showing the promising potential for very high-power and high-temperature operation. This work shows the outstanding ability of HEMT chips on Cu substrates for solving the self-heating effect with the advantages of process simplicity, high yield, and low production requirement.

Keywords: GaN high electron mobility transistor (HEMT), electric characteristics, electroplating, heat dissipation

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1. Introduction

In the past few decades, GaN high electron mobility transistors (HEMTs) have become the domestic and foreign major research focus because of the great research significance and application prospect in the new generation of high-efficiency, small-size power conversion and management systems, electric locomotives, and new energy vehicles.[1–5] At present, owing to the sophisticated production process and high cost of GaN, most of the mature GaN HEMTs on the market are grown heteroepitaxially on sapphire and SiC due to their relatively small difference in lattice parameters and thermal expansion coefficient.[6–10] By comparison, Si substrates have the advantages of low cost, high crystal quality, large size, and relatively mature process conditions, which makes them more and more competitive.[11–13] However, a large amount of heat is generated and accumulated while outputting high power,[14,15] accompanied by the rapid deterioration of the output power density and efficiency, and even the transistor failure, remaining a significant issue in reliability.[16–20] A significant example is the reduction in drain current as the drain bias increases.[16] Therefore, GaN HEMTs' theoretically high output capacity is far from being realized for now.[21] It is the inefficient heat dissipation that has bottlenecked the further application of GaN microwave power devices. The most direct method to solve this problem is growing GaN based thin films on substrates with high heat dissipation capacity, such as diamond.[22,23] But there is no easy growth technique available now. Consequently, the substrate transfer has been taken into consideration.[24,25] Many researchers substituted diamond with high thermal conductivity for Si substrate by metallic bonding under high temperature and pressure conditions,[26–28] where the harsh process requirements led to low product rates. As a result, The GaN HEMTs with high heat dissipation capacity that are fabricated by simple and reliable process are urgently needed.

In this work, a GaN HEMT on a metallic substrate with high heat dissipation was successfully fabricated by the electroplating technique[29] after the removal of the Si substrate. AFM scanning and Raman measurement were conducted to characterize the surface morphology and stress status of the devices. The electric characteristics of two HEMT chips were also studied. Moreover, the thermoreflectance imaging was presented to represent the heat dissipation capacity clearly. The proposed GaN HEMTs on metallic substrates by electroplating at normal temperature and pressure have the advantages of the simplicity and stability of fabrication process, facility of component separation, and free from the polishing damage, which will play a significant role in achieving the maximum performance edge of high-temperature and high-

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power operation and thus the industrial application.

2. Device fabrication

The schematic cross-sectional views of GaN HEMTs' structures are shown in Fig. 1. All epitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD) on a 6-in (111) Si substrate as shown in Fig. 1(a). First, a 200 nm AlN nucleation layer was deposited, and a 1.5 μm-thick $Al_xGa_{1-x}N$ layer with gradual Al gradient was grown, followed by a 3 μm-thick GaN buffer layer, 200 nm GaN channel layer, and 1 nm AlN intercalation layer thereon. The barrier layer consisted of a 17 nm AlGaN barrier and 2 nm GaN cap. The epitaxial material was cut into 2.5 cm×2.5 cm small samples by laser. The device fabrication process started with mesa isolation using $BCl_3/Cl_2/Ar$ plasma in an inductively coupled plasma (ICP) system. The ohmic contacts pads were patterned by using ultraviolet lithography. The source and drain ohmic contacts were formed with Ti/Al/Ni/Au (20 nm/120 nm/60 nm/100 nm) annealed at 850 ℃ for 30 s in N_2 ambient. Ni/Au (30 nm/100 nm) was evaporated for a gate of 2 μm length and 100 μm width. The source-to-drain spacing was 8 μm and the gate was at the center of the source and drain. The wafer surface was passivated with 150 nm SiN_x by plasma enhanced chemical vapor deposition (PECVD). Finally, Ti/Au (50 nm/200 nm) overlay pads were deposited. The GaN HEMTs on Cu substrates were fabricated as follows. The device was firstly bonded to the sapphire by wax, and the silicon substrate was completely removed by wet etching. The etching solution was a mixture of hydrofluoric, nitric acid, and glacial acetic acid. The etching time was 40 min. After that, a Ti/Au (20 nm/60 nm) layer was deposited as a base metal on the side of the original silicon substrate, and then the device was transferred to a Cu substrate by electroplating technique.

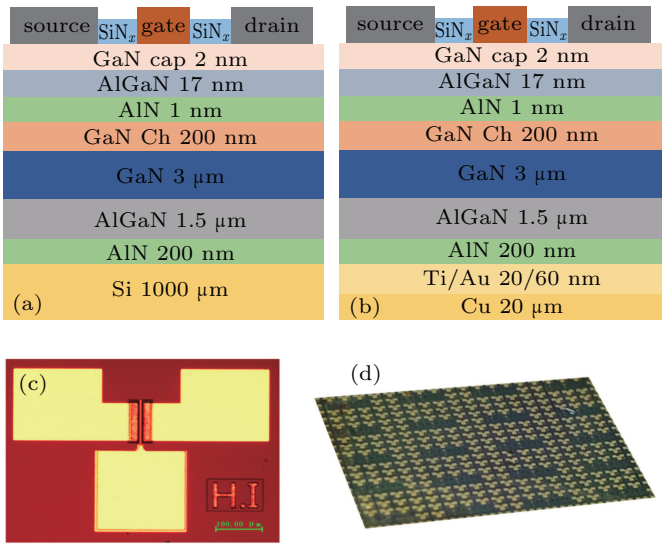

Fig. 1. Schematic cross-sectional views of GaN HEMTs (a) on Si substrate and (b) on Cu substrate. (c) The device front image and (d) photograph of the HEMT chip.

The schematic structures of the HEMTs on Cu substrates are shown in Fig. 1(b), and the device front image and photograph of the HEMT chip are shown in Figs. 1(c) and 1(d).

3. Results and discussion

Figures 2(a) and 2(b) show AFM images of AlGaN/GaN HEMTs on Si substrates and Cu substrates transferred by electroplating technology. The root-mean-square roughnesses of the two devices were measured to be 0.315 nm and 0.593 nm, respectively, which shows that negligible damage was introduced in HEMTs on Cu substrates during the process of substrate transfer by electroplating. The Raman spectra were also measured to characterize the internal stress status of the two devices as shown in Fig. 2(c). As is seen, an obvious blue shift of peak occurs in the spectrum of the HEMT on Cu substrate compared to the HEMTs on Si substrates. As we know, the lattice mismatch as high as 17% between GaN and Si leads to a tensile stress inside the GaN epitaxial layers. The peak blue shift in the Raman spectrum of the HEMTs on Cu substrates was caused by the reduction of tensile stress in the GaN materials due to the removal of the silicon substrates, which avoids the long-time working of devices under large stress.

The electrical characteristics of the two HEMT devices are shown in Fig. 3. All DC measurements were performed by Keithley 4200. All tested devices had a gate length of 2 μm, a gate width of 100 μm, and a source–drain spacing of 8 μm. Figure 3(a) shows the three-terminal I_d–V_{GS} characteristics of the two devices. The gate was biased from 1 V to −3 V in steps of 0.5 V. The current drop in the HEMTs on Cu substrates with voltage increasing, which was associated with the self-heating effect, was observed to be almost the same as that in the HEMTs on Si substrates. A full-channel current of 550 mA/mm was recorded at $V_{GS} = +1$ V for the HEMTs on Si substrates, while the maximum current for the HEMTs on Cu substrates was 532 mA/mm under the same condition. When $V_{DS} = 15$ V, the currents in the HEMTs on silicon substrates and Cu substrates were 465 mA/mm and 453 mA/mm, respectively, with 15.45% and 14.85% attenuation. Figure 3(b) shows the DC transfer characteristics of the two devices at $V_{DS} = 10$ V. The maximum trans-conductance was 143 mS/mm and 136 mS/mm for the two HEMT devices, respectively. As can be seen from Fig. 3(c), the almost negligible increment of the gate leakage current was obtained for the GaN HEMTs on Cu substrates. It is demonstrated that the output characteristics of the HEMTs on Cu substrates were almost unaffected although nearly no heat dissipation improvement was achieved under higher chip temperature using no heat sink, which will be discussed in Fig. 4 in detail. Once the heat sink is provided and the transfer process is optimized, the GaN HEMTs on Cu substrates would have much better electric performance than those on Si substrates.

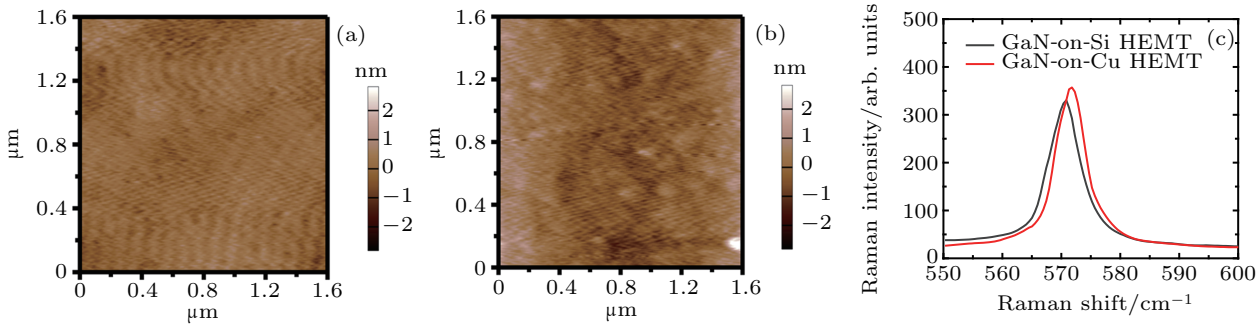

Fig. 2. AFM scanning images of GaN HEMTs (a) on Si substrate and (b) on Cu substrate. (c) The Raman spectra of the two HEMT chips.

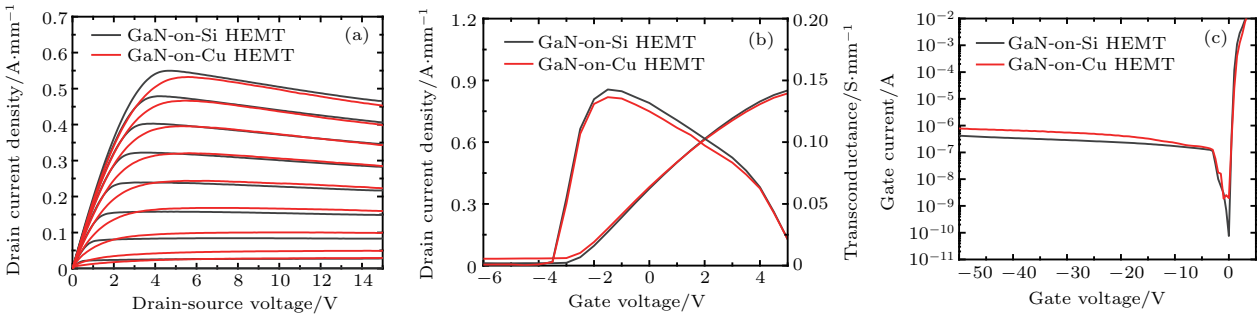

Fig. 3. (a) The *I*–*V* characteristics, (b) transfer characteristics, and (c) gate leakage current as a function of gate voltage for GaN HEMTs on Si and Cu substrates.

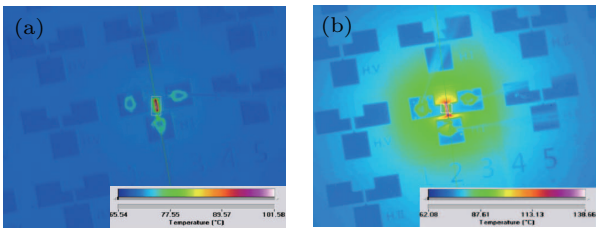

Fig. 4. Thermoreflectance imaging of (a) GaN-on-Si HEMT and (b) GaN-on-Cu HEMT at $V_{DS} = 12$ V.

Table 1. Thermal conductivity coefficients of different materials.

Material	GaN	AlN	Si	Cu	Au	Ti
Coefficient/W·m^{-1}·K^{-1}	130	270	150	401	317	21.9

In order to observe the heat distribution on HEMTs intuitively, the thermoreflectance imaging was measured to provide two-dimensional maps of surface temperature distribution of the devices in Fig. 4. The GaN-on-Cu HEMT chip was bonded to a Cu module with thermal conductive adhesive for better heat dissipation. The Cu module was placed on a stage set at 70 ℃. The surface temperature images when the drain bias voltage was 12 V were taken as example. From Fig. 4(a), we can see that the heat was generated and mainly concentrated in the gate's regulatory region with tiny dispersion for the HEMTs on Si substrates. Differing from that, heat generated in active GaN HEMTs on Cu substrates was clearly revealed to spread out in all directions radially as shown in Fig. 4(b). The difference in heat dissipation pattern of the two devices was closely related to the thermal properties of the substrates. As shown in Table 1, Cu's thermal conductive coefficient is much larger than that of Si and GaN. We suppose that the multilayer composite material is composed of different materials with thermal conductivities of k_1, k_2, …, k_n, thicknesses of h_1, h_2, …, h_n, and cross-section areas of S. The total thickness H and equivalent thermal conductivity K are given as[30]

$$H = h_1 + h_2 + \cdots + h_n,$$
$$K = H/(h_1/k_1 + h_2/k_2 + \cdots + h_n/k_n).$$

From Fig. 1(b), the equivalent thermal conductivity of the Cu based material is calculated as

$$\begin{aligned} K_1 &= 20.32 \times 10^{-6}/(200 \times 10^{-9}/270 + 20 \times 10^{-9}/21.9 \\ &\quad + 100 \times 10^{-9}/317 + 20 \times 10^{-6}/401) \\ &= 391.94\ \mathrm{W \cdot m^{-1} \cdot K^{-1}}. \end{aligned}$$

Assuming that the silicon substrate has the same thickness as the Cu substrate, according to Fig. 1(a), the equivalent thermal conductivity of the Si based material can be obtained as

$$\begin{aligned} K_2 &= 20.2 \times 10^{-6}/(200 \times 10^{-9}/270 + 20 \times 10^{-6}/150) \\ &= 150.66\ \mathrm{W \cdot m^{-1} \cdot K^{-1}}. \end{aligned}$$

Therefore, the equivalent thermal conductivity of the device on Cu substrates was much better than that on silicon substrates. As a result, the HEMTs on Cu substrates have better heat dissipation capacity in comparison to the HEMTs on Si. As soon as the heat sink is installed, heat will disperse through the Cu substrate over a large area to the heat sink much more rapidly. However, the real-time surface temperature of the HEMT chip on Cu substrates was a little higher than that on Si substrates unexpectedly. There are probably two reasons for this. Firstly, compared to the HEMT chip on Si substrates, the lacking of effective heat sink because of unoptimized preparing technique

for the chip on Cu substrates makes the heat dissipation downward across the transistor to the Cu module mainly blocked. In addition, despite of the larger thermal conductive coefficient of Cu, the thermal capacity of the Cu film with 20 μm thickness is believed to be much less than the Si substrate with 1 mm thickness. For the same thickness, the thermal diffusion of copper is undoubtedly better. In order to explore Cu' advantage in heat dissipation, HEMTs on Cu substrates with different thicknesses were fabricated and transient thermoreflectance measurements were conducted. Table 2 shows the surface temperature of HEMTs on Cu substrates with different thicknesses at different powers. As we can see, HEMTs on 35 μm-thickness Cu substrate had a higher working power at the same voltage compared to HEMTs on 28 μm-thickness Cu substrate. However, the surface temperature of the HEMTs on 35 μm-thickness Cu substrate was much lower. It is demonstrated that the heat dissipation ability of the Cu substrate becomes stronger and stronger with the thickness increasing, making HEMTs working in higher-temperature surroundings stably. According to this, when the preparing technique is further optimized and the active heat sink is supplied, the heat dissipation of HEMT chips on Cu substrates will be greatly improved.

Table 2. Surface temperature of HEMTs on Cu substrates with different thicknesses at different powers.

Thickness/μm	28		35	
Voltage/V	8	20	8	20
Current/mA	36	30	43	36
Power/mW	288	600	344	720
Temperature/°C	81.2	94.7	77.8	91.2

4. Conclusion and perspectives

In this paper, AlGaN/GaN HEMT chip was successfully transferred from silicon substrate to the Cu substrate by electroplating technology, with the electrical and thermal properties measured carefully. AFM images show that the surface morphology was nearly unaffected during the substrate transfer process. Raman measurement reveals that there is no large mismatch stress existing in the HEMT on Cu substrate. Also, the output, transfer, and leakage current characteristics of the GaN HEMTs on Cu substrates nearly as good as those of GaN HEMTs on Si substrates were achieved in the absence of active heat sink. Moreover, much better heat dissipation was clearly observed in thermoreflectance imaging of the HEMT chip on Si substrates. The proposed GaN HEMTs on Cu substrates by electroplating at normal temperature and pressure have the advantages of the simplicity and stability of fabrication process, facility of component separation, and free from the polishing damage, which have great potential in achieving the extreme performance of GaN power electronic devices in high-temperature and high-power operation.

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