Jinst

Published by IOP Publishing for Sissa Medialab

Received: *September 30, 2019*
Revised: *December 4, 2019*
Accepted: *December 11, 2019*
Published: *January 22, 2020*

21st International Workshop on Radiation Imaging Detectors
7–12 July 2019
Crete, Greece

Development of a pixel readout ASIC for CZT detectors for spectral X-ray photon-counting imaging applications

X. Wang,[1] **Z. Deng,**[1] **W. Liu and Y. Liu**

Department of Engineering Physics, Tsinghua University, Beijing, China
Key laboratory of Particle & Radiation Imaging, Ministry of Education, Beijing, China

E-mail: dengz@mail.tsinghua.edu.cn, wang-xz18@mails.tsinghua.edu.cn

Abstract: This paper presents the development of a prototype pixel readout ASIC for CZT detectors fabricated in a 180 nm CMOS process. It consists of a 32×32 array of pixels in 100 μm pitch and the EOC (end-of column) circuit for control and data readout. Each pixel integrates a charge sensitive preamplifier, a CR-RC shaper, two discriminators, two 12-bit counters and registers, allowing us to acquire and readout images simultaneously. A local 6-bit register has also been integrated for each pixel for calibration enable and threshold fine tuning, which can be programmed through a SPI slow control interface.

A dedicated chip evaluation system was developed and the initial test results showed that the chip worked well. The power consumption was measured to be 38.9 μW per pixel, which could be adjusted by the master bias unit. The gain of the analog front-end was approximately 77.3 mV/fC and the ENC was less than 100 electrons for different shaping times and the input capacitance of about 100 fF. The results were in good agreement with our design specifications. More detailed design and test results will be discussed in this paper.

Keywords: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

[1]Corresponding author.

https://doi.org/10.1088/1748-0221/15/01/C01030

Contents

2020 JINST 15 C01030

1 Introduction

Spectroscopic imaging with photon-counting detectors is a promising technique for X-ray imaging applications. The contrast resolution, as well as capability of material separation can be potentially improved by providing more spectral information [1]. However, it requires energy resolving power of X-ray detectors at high counting-rates. Room temperature semiconductor detectors such as Cadmium zinc telluride (CZT) and CdTe can directly convert X-ray photons and hence can achieve high energy resolution. Their atomic numbers and densities are high, resulting in good stopping power for hard X-rays and gamma-rays, which makes them suitable for such applications [2]. Dedicated pixel readout ASICs have also been developed for photon-counting spectral X-ray imaging during the past few decades [3–9]. In order to meet various requirements in a broad range of applications, these chips were optimized in pixel size, counting rate capability, noise and the number of energy windows.

A photon-counting pixel ASIC is under development for CZT or CdTe detectors for X-ray imaging applications. In this paper we present the design of our first prototype chip. It integrates 32×32 pixels with the pixel pitch of 100 µm and each pixel consists of the analog front-end and two comparators and counters. The chip was fabricated in a 180 nm CMOS process. The detailed circuit design and the test results will be introduced in the following sections.

2 Architecture and specifications

The overall architecture of the ASIC is shown in figure 1(a) and the corresponding layout of the ASIC is shown in figure 1(b). The chip consists of two parts: the pixel part and the EOC (End-Of-Column) part.

The 32×32 pixel array takes the majority area of the ASIC and each pixel consists of a charge sensitive preamplifer, a CR-RC shaper and the two discriminators and counters. The charge collected by each pixel is amplified and then compared with two adjustable thresholds. Each discriminator directly drives a 12-bit counter. The counter data can be stored in the corresponding register before transmitted out of the chip. No dead time exists during data transimission.

The EOC circuit is placed on the bottom of the chip, which integrates the bias module, control logics and data readout.

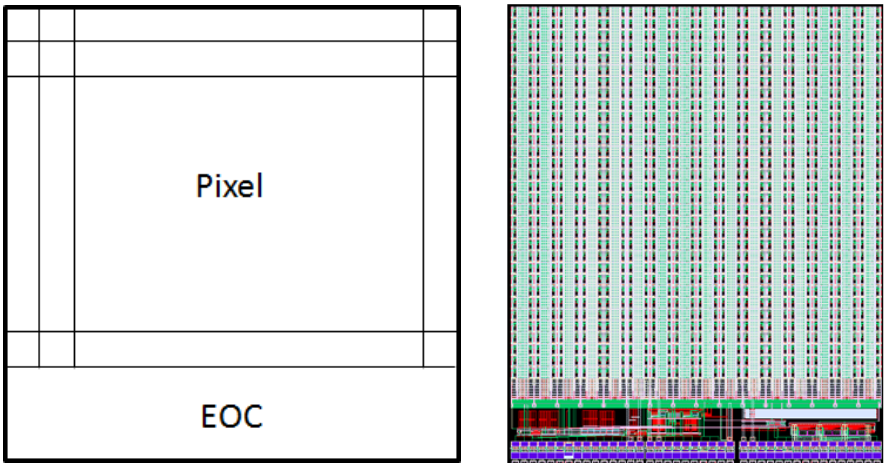

Figure 1. The chip architecture and the layout of the ASIC.

The main design specifications are listed in table 1. The whole pixel array consists of 1024 pixels with 100 µm pitch. The power consumption needs to be less than 100 µW per pixel to meet the heat dissipation requirements. The gain is designed to be 70 mV/fC with a dynamic range of 10 fC to cover high energy X-rays in CdZnTe detectors. The ENC is less than 100 electrons with 100 fF input capacitance. The pulse width can be adjusted with a minimum width of 200 ns. Two 12-bit energy windows are integrated in one pixel. The readout frame rate of 1 kHz can be achieved with 32 MHz readout clock.

Table 1. Main design specifications of the ASIC.

Design specification	Value
Pixel size	100 µm × 100 µm
Array	32×32
Power consumption	< 100 µW/pixel
Gain	70 mV/fC
Dynamic range	10 fC
ENC	< 100 electron @C_{in} = 100 fF
Pulse width	200 ns
Energy window	2
Counter	12 bit
Readout frame rate	1 kHz

3 Circuit design

3.1 The pixel circuits

Each pixel consists of a low-noise charge sensitive preamplifier, a CR-RC shaper, two discriminators, two 12-bit counters and registers, as shown in figure 2. Each energy threshold is set by a 8-bit global threshold and a 2-bit local threshold for fine tuning. The global thresholds are generated by two 8-bit global DACs and are common to all the pixels. The local thresholds are generated by two 2-bit DACs in each pixel. All the DAC values can be programmed through the SPI (Serial Peripheral Interface) slow control bus. The counter data can be latched into the corresponding registers at the end of the frame time and then is reset for the next frame. The register data will be shifted out driven by the readout clock. Each pixel also integrates a number of control registers for local threshold adjustment for each discriminator, enabling calibration signal injection and mask of the discriminator output in case of noisy channel. They can be accessed through the SPI bus as well.

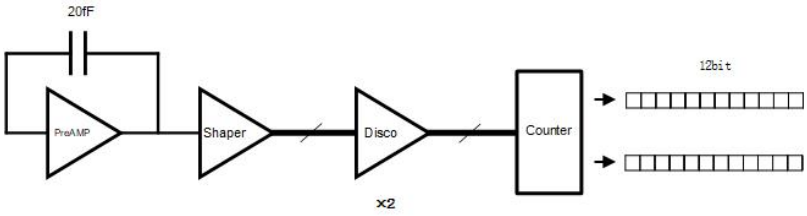

Figure 2. The circuit diagram of one pixel.

The layout of the pixel circuit is shown in figure 3. The analog circuits and the digital circuits are separated by the slow control registers to avoid the interference to the sensitive analog frontend.

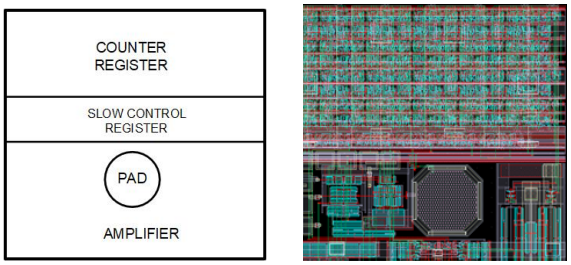

Figure 3. The layout of one pixel.

3.2 The EOC circuits

The EOC parts includes the bias module, the control logics and the data readout. All the analog bias voltages for the amplifiers are generated by the bias module. The master bias current can be adjusted through an external resistor. The control logics consist of the fast and SPI slow control parts. The fast contol logics generates internal control signals for the counter value latching and resetting with the external clock and CONV signals. The slow control includes two 8-bit global DACs together with their registers. The data readout is driven by the readout clock. The register data for each column will be shifted out to the bottom register firstly and then all 32 registers at the bottom of the columns will be serialized and sent out of the chip.

2020 JINST 15 C01030

4 Experimental results

4.1 The test setup

A dedicated test system was developed to evaluate the ASIC performance. It consist of the ASIC evaluation board and the AX512 FPGA evaluation board, as shown in figure 4. A QT monitor program was also devleoped for configuration and data aquisition. The signal generator (Agilent 33120A) was used to inject signal into the calibration inputs of the corresponding pixels with the calibration register enabled. The analog shaper output of the most left bottom pixel can be monitored and captured by the oscilloscope (Lecroy WP404HD). The counter data were aquired firstly to the FPGA and then sent to PC through the Ethernet.

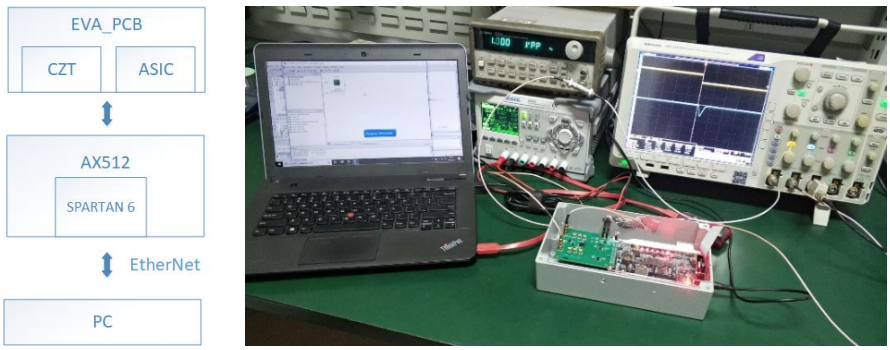

Figure 4. The ASIC evaluation system.

4.2 The power consumption

The currents of the power supply were measured for different main bias currents, as shown in figure 5. The power consumed by the ASIC was assumed to be proportional to the main bias current. The power consumption was then estimated to be 39.8 µW per pixel at 50 µA bias current.

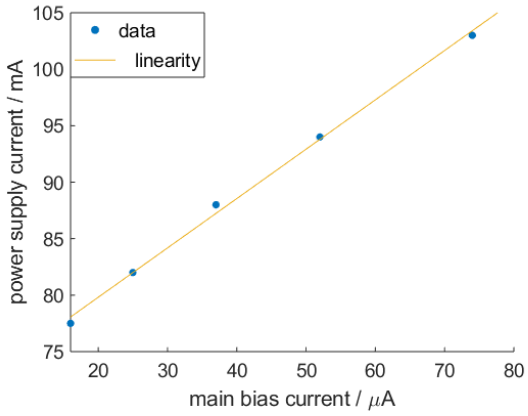

Figure 5. The power supply current vs. the main bias current. All the bias currents in the ASIC are proportional to the main bias current as well as the power consumption. The rest of the supply current is assumed to be consumed by other circuits on the print circuit board.

2020 JINST 15 C01030

4.3 The linearity and noise performance

The linearity and noise performance were measured by injecting signals with different amplitudes and capturing the waveforms of the analog monitor output. The averaged waveform for a certain signal amplitude is shown in figure 6. The pulse width was adjusted to be about 200 ns.

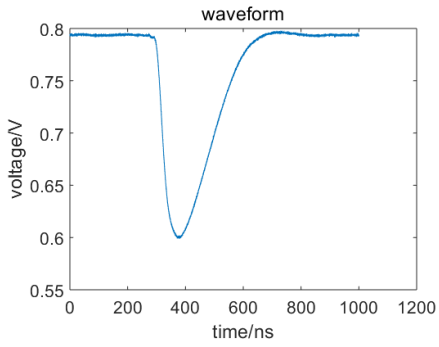

Figure 6. The average waveform of the analog monitor output.

As shown in figure 7, the gain is estimated to be 77.3 mV/fC assuming the calibration capacitance of 2.65 fF. The maximum INL (Integrated Non-Linearity) was about 1.2%. The ENCs were measured with different pulse width from 200 ns to 4900 ns, as shown in figure 8. Spikes can be seen from the analog output due to the inteference from the readout clock. With the readout clock off,

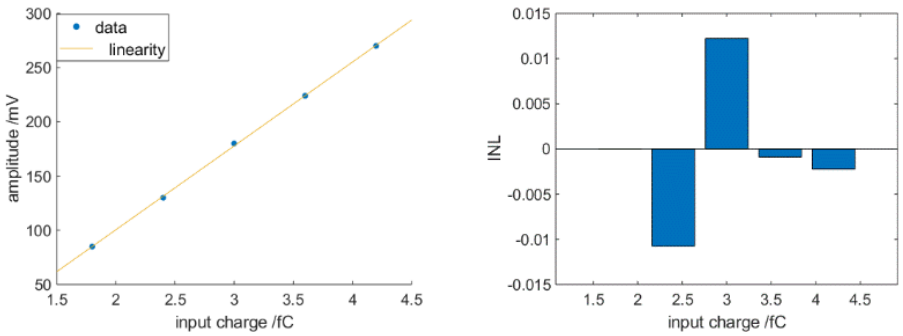

Figure 7. The linearity of the analog frontend. The gain is estimated by fitting the scatter data with linear functions.

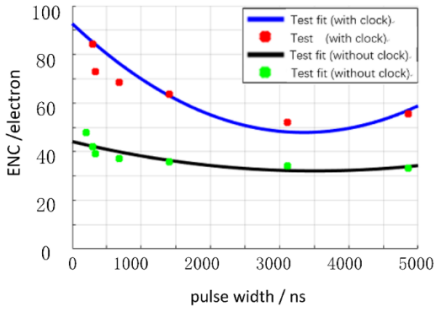

Figure 8. The ENC vs. pulse width.

2020 JINST 15 C01030

the ENCs were less than 50 electrons for all different pulse widths. And the ENCs were increased by 20–35 electrons when the readout clock turned on. These results are in good agreement with the design specifications.

4.4 The S-curve measurements

The linearity and noise performance of all pixels were evaluated using the so-called S-curve method [10]. The S-curve of the pixel corresponding to the analog monitor output is shown in figure 9, which was measured by acquiring the count values for different thresholds. The analog output amplitude and noise were then estimated from the transition edge fitted with the normalized Gaussian cumulative distribution function and the result is shown in figure 10. The gain was measured to be 88 mV/fC, which is larger than the result in the previous subsection and this is probably because of the buffer of the monitor output in the chip. The noise is still less than 100 electrons, but variations of tens of electrons can be noticed, which is probably caused by the readout clock mentioned above.

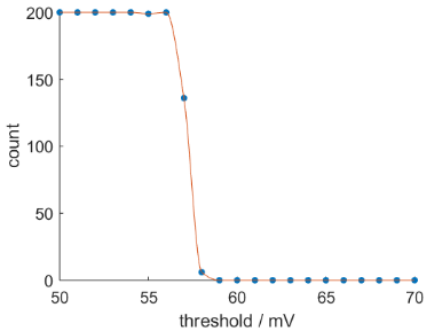

Figure 9. A typical S-curve.

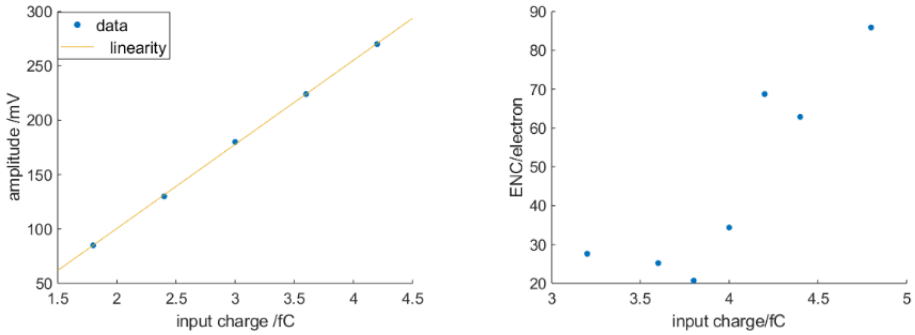

Figure 10. Amplitude and noise vs. input charge.

The amplitudes and noises of all the pixels can be extracted simultaneously, as shown in figure 11. The standard deviations of the distributions of the estimated amplitude and noise with 3.2 fC charge injected are 41.7 mV and 24 electrons, and similar results are obtained under other conditions. The mean values of the two distributions are 114.1 mV and 43 electrons respectively.

2020 JINST 15 C01030

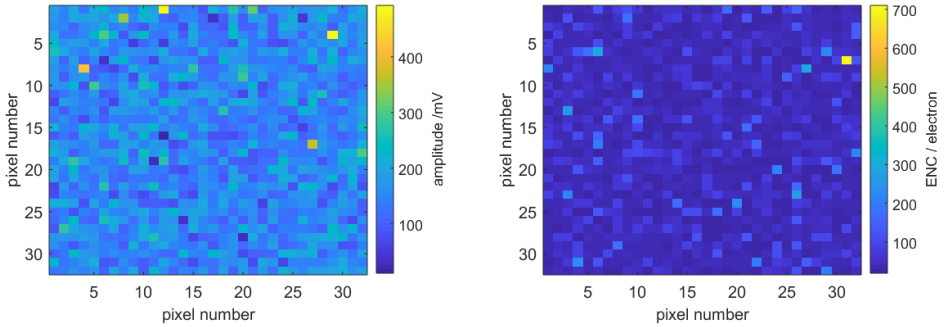

Figure 11. The estimated amplitude and noise (with 3.2 fC charge injected) vs. pixel position.

S-curves with different amounts of injection charge were measured and for each S-curve the amplitude and noise can be estimated. The gains and the pedestals of the analog outputs were then obtained by linear fitting and the results are shown in figure 12 and figure 13. The average gain is 73.3 mV/fC and the standard deviation is 9.4 mV/fC. The average pedestal is −123.5 mV and the standard deviation is 36.6 mV, which indicates that the nonuniformity can be well compensated by a 7-bit DAC with an LSB of 2 mV.

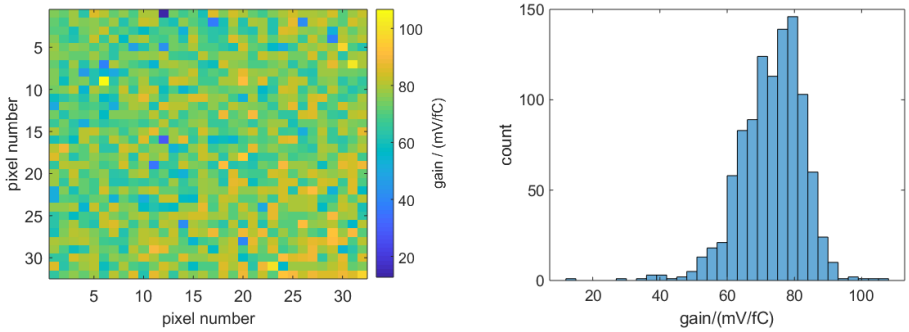

Figure 12. The gain vs. pixel position and the gain distribution.

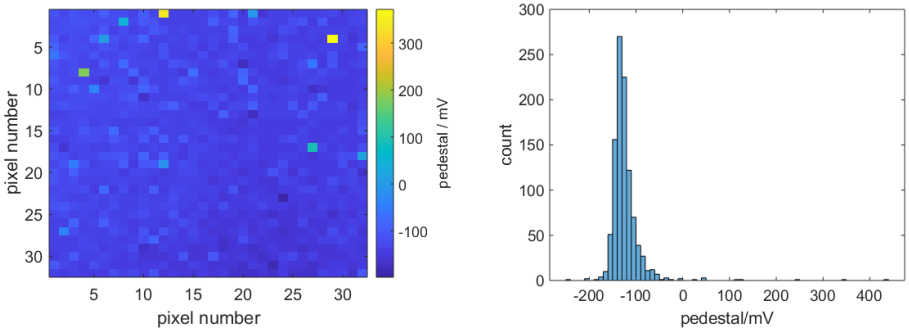

Figure 13. The pedestal vs. pixel position and the pedestal distribution.

2020 JINST 15 C01030

5 Summary

The prototype of a pixelated photon-counting ASIC has been developed for spectral photon-counting X-ray imaging. The chip was fabricated in a 180 nm CMOS process and the test results shows the chip was fully functional and the performance were in good agreement with the design specification. The power consumption was measured to be 38.9 μW per pixel. The gain of the analog front-end was approximately 79 mV/fC and the ENC was less than 100 electrons with the minimum pulse width of 200 ns and input capacitance of about 100 fF. Our prototype ASIC achieves a good noise performance among other ASICs for X-ray spectral imaging applications mentioned above.

The second version pixel chip with larger array are under development and the test with CZT or CdTe detectors will also be carried on in the near future.

Acknowledgments

The work is supported by the National Key Research and Development Program (under grant no. 2016YFF0101302).

References

[1] P.M. Shikhaliev and S.G. Fritz, *Photon counting spectral CT versus conventional CT: comparative evaluation for breast imaging application*, *Phys. Med. Biol.* **56** (2011) 1905.

[2] T. Schlesinger, J. Toney, H. Yoon, E. Lee, B. Brunett, L. Franks et al., *Cadmium zinc telluride and its use as a nuclear radiation detector material*, *Mat. Sci. Eng.* **R 32** (2001) 103.

[3] P. Pangaud, S. Basolo, N. Boudet, J.-F. Berar, B. Chantepie, P. Delpierre et al., *XPAD3: A new photon counting chip for X-ray CT-scanner*, *Nucl. Instrum. Meth.* **A 571** (2007) 321.

[4] R. Steadman, C. Herrmann, O. Mülhens, D.G. Maeding, J. Colley, T. Firlit et al., *ChromAIX: A high-rate energy-resolving photon-counting ASIC for spectal computed tomography*, *Proc. SPIE* **7622** (2010) 762220.

[5] T. Loeliger, C. Brönnimann, T. Donath, M. Dchneebeli, R. Schnyder and P. Trüb, *The new PILATUS3 ASIC with instant retrigger capability*, in proceedings of *IEEE Nuclear Science Symposium and Medical Imaging Conference*, Anaheim, CA, U.S.A., 27 Occtober – 3 November 2012, pp. 610–615.

[6] R. Ballabriga, M. Campbell, E. H. M. Heijne, X. Llopart and L. Tlustos, *The Medipix3 prototype, a pixel readout chip working in single photon counting mode with improved spectrometric performance*, *IEEE Trans. Nucl. Sci.* **54** (2007) 1824.

[7] R. Bellazzini, A. Brez, G. Spandre, M. Minuti, M. Pinchera, P. Delogu et al., *PIXIE III: a very large area photon-counting CMOS pixel ASIC for sharp X-ray spectral imaging*, 2015 *JINST* **10** C01032.

[8] C. Ullberg, M. Urech, N. Weber, A. Engman, A. Redz and F. Henckel, *Measurements of a dual-energy fast photon counting CdTe detector with integrated charge sharing correction*, *Proc. SPIE* **8668** (2013) 86680P.

[9] R. Dinapoli, A. Bergamaschi, B. Henrich, R. Horisberger, I. Johnson, A. Mozzanica et al., *EIGER: Next generation single photon counting detector for x-ray applications*, *Nucl. Instrum. Meth.* **A 650** (2011) 79.

[10] RD-19 collaboration, *A 1006 element hybrid silicon pixel detector with strobed binary output*, *IEEE Trans. Nucl. Sci.* **39** (1992) 654.

2020 JINST 15 C01030