New Topology Multilevel Inverter Type Diode Clamped Five Level Single Phase

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Abstract. Multilevel inverter is a converter that converts DC power sources into AC power sources with the voltage output higher than two levels. Conventional multilevel inverter topology for five levels that is currently developing generally uses eight components of power switches. In this paper, a five-level multilevel inverter topology is proposed by reducing the power switch component to four and aided with two pin diodes and capacitors as voltage couplings. The simulation with MATLAB that has been done shows various advantages of this topology compared to conventional multilevel inverter topologies. Results and discussion This topology compare the switching techniques used between Pulse Width Modulation (PWM) and Sinus Pulse Width Modulation (SPWM) for five-level multilevel inverter. Cohesiveness in switching techniques topology is proposed and validated by using passive filter. The harmonic analysis performed by the proposed topology could reduce the output voltage with the low harmonics.

1. Introduction

Developments of power electronics allows it to produce the generation, the processing and the use of electrical energy and economic efficiency. Power electronics is defined as an electronic application that focuses on regulating electrical equipment by making changes to electrical parameters (current, voltage, frequency and electrical power). Today multilevel inverter has attracted great interest in the high usage power industry with numerous advantages. The power electronics equipment is widely applied such as utilization of DC resources, uninterruptible power supplies, direct voltage power transmission (HVDC), variable frequency drive systems, air conditioners and others [1].

Multilevel inverter (MLI) is a converter that converts DC power sources into AC power sources where the output voltage forms are more than two levels where there are three levels, five levels, seven levels and so on. Those numerous output levels can be adjusted by the number of semiconductor switches power circuit. Multilevel inverters that are currently developing can be recognized based on their architecture (topology) such as diode clamped, flying capacitor and cascade H-bridge. Those are the three multilevel inverter structures known in industrial applications with separate DC sources. The advantage of diode clamped, and flying capacitor is to use a voltage balancer using a capacitor so that for many voltage levels on DC sources could be minimized

Conventional five-level multilevel inverter requires eight switches to enumerate the two DC sources separately while the next topology is proposed using six switches and two DC sources apart from being given with two diode clamped and two capacitors as a voltage balancers that have the form of cascade

waves with smaller harmonic distortions compared to the conventional multilevel inverters [2]. Then the topology is then reduced by six switches and two separate DC sources without using clamped and capacitor diodes as a voltage balancer where the wave cascade forms with harmonic distortion reduced compared to the previous topology [3].

By analysing the advantages and disadvantages of existing topologies, a new topology is proposed in reducing multilevel inverter switches using four switches to count two DC sources for positive polarity and negative polarity assisted by two pin diodes and capacitors as voltage couplings. Results and discussion This topology compare the switching techniques used in Pulse Width Modulation (PWM) and Sinus Pulse Width Modulation (SPWM) to analyse the resulting harmonics [4]. The discussion would be on overcoming the weaknesses of the existing topology.

2. Multilevel inverter five levels type diode clamped

Conventional topology in the clamped multilevel inverter was first proposed in 1981 then also known as the neutral point. Many studies were then published that discussed on the advantages and disadvantages. Modified sinusoidal waveforms in a five-level multilevel inverter are shown in Figure 1. Unlike the cascaded H-bridge inverters, this topology requires diodes to be used as clamping devices. This DC voltage is further divided through the capacitor coupling. The components which needed by the multilevel inverter topology diode type clamped for *n* levels are listed as below [4].

- number of switches = 2 (*n*-1),
- number of diodes = (*n*-1) (n-2),
- number of capacitors = (*n*-1)

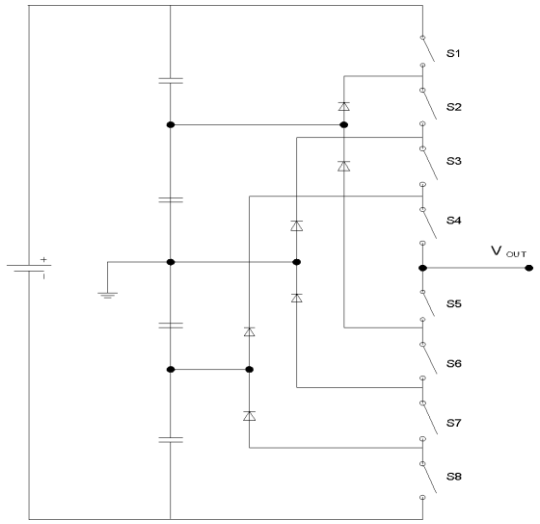

Figure 1. MLI five levels of type diodes clamped

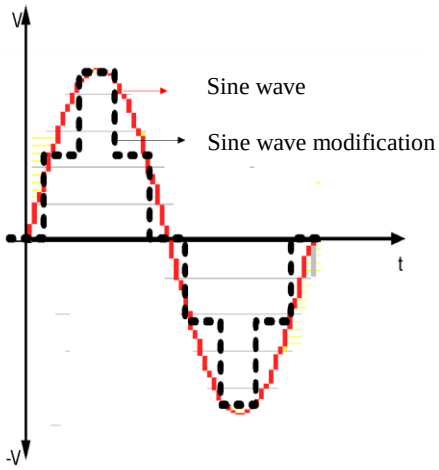

Figure 2. Sinusoidal wave modifications the five-level multilevel inverter

2.1. Proposed Topology

Topology proposed in a five-level multilevel inverter is built using two DC sources, four switches, four diodes and two capacitors, in this topology is to show in the reduction of the number of switches used in conventional topologies, validation of the output of the proposed topology can be formed five-level output voltage, as for the proposed topology shown in Figure 3.

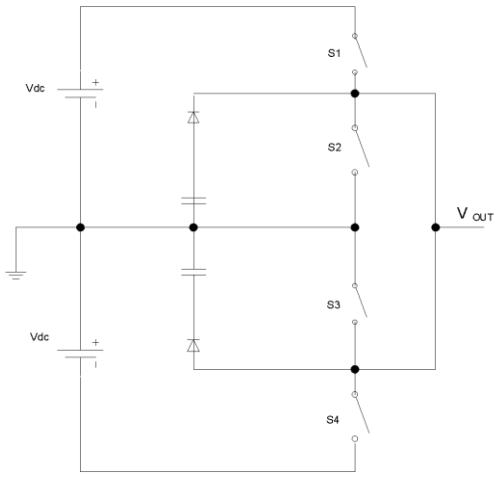

Figure 3. Multilevel inverter five topology the proposed level

From Figure 3 above can be explained the work of the proposed topology where there are two DC sources namely at the upper limit and at the lower limit, the upper DC source is used for positive cycle polarity while the lower limit DC source is used for negative cycle polarity, two capacitors used as a coupling at the voltage level of a large DC source while the two diodes are used as clamps from each DC source. The switching topology of the four switches is shown in Table 1.

Table 1. MLI Switching Topology Five Levels Using Four Switches

No	Condition Switch				Output (Vdc)
	S1	S2	S3	S4	
1	1	0	1	0	0.5
2	1	0	0	0	0.0
3	1	1	0	0	0.5
4	0	1	0	0	0.0
5	0	1	0	1	-0.5
6	0	0	0	1	-0.5
7	0	0	1	1	-0.5
8	0	0	1	0	0.0

2.2. Pulse Width Modulation (PWM)

The basic principle of a PWM switching technique is to compare a triangular wave ($V_{carrier}$) with a sine wave ($V_{reference}$) which is called a modulation technique, this process produces a pulse wave at the basic frequency of a sine wave. This PWM wave is in the form of a box with a certain frequency in the ratio of the width of the high and low pulses that are different

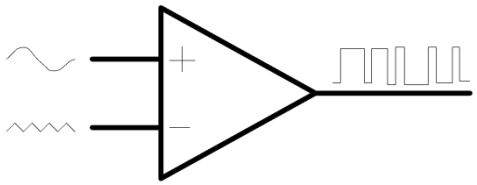

Figure 4. Processed PWM

From the above description the PWM duty cycle can be explained in the following equation (1) and (2) [4].

$$\frac{V_{reference}}{V_{carrier}} = \frac{t_{on}}{(t_{on} + t_{off})} \tag{1}$$

$$D = \frac{t_{on}}{(t_{on} + t_{off})} \tag{2}$$

Where;
D = duty cycle

2.3. Total Harmonic Distortion (THD)
Research on Multilevel Inverter technology to get the output voltage is more than two levels has been developed by various researchers. The important technology in developing multilevel inverters is how to modify the shape of the output level nearing sinusoidal waves. With Fourier series, the square wave can be expressed as the sum of harmonic components and expressed in the following equation

$$V_o(\omega t) = V_o + \sum_{n=1}^{\infty} (a_n \sin n\,\omega t) + \sum_{n=1}^{\infty} (b_n \cos n\,\omega t) V_o(\omega t) = V_o + \sum_{n=1}^{\infty} (a_n \sin n\,\omega t) + \sum_{n=1}^{\infty} (b_n \cos n\,\omega t) \tag{3}$$

THD states the amount of distortion or deviation of a wave containing harmonics expressed in percent (%) formulated as follows:

$$THD = \frac{\sqrt{V^2{}_2(rms) + V^2{}_3(rms) + V^2{}_4(rms) + \cdots + V^2{}_n(rms)}}{V_1(rms)} \tag{4}$$

Where:
$V_{1\,(rms)}$ = effective basic harmonic voltage
$V_{n\,(rms)}$ = harmonic effective voltage to n

3. Results and analysis

The simulation conducted is intended to show that for the harmonic level of output voltage generated from topology multilevel inverter five conventional levels using eight switches (MOSFETs) compared to the proposed topology.

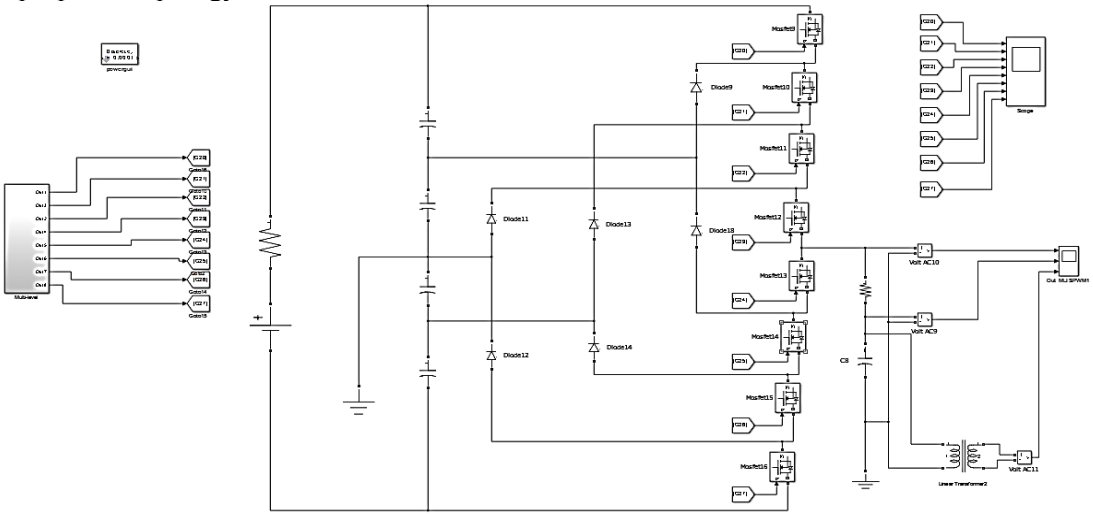

Figure 5. Simulation of conventional multilevel five-level inverter model

Simulation carried out from Figure 5 above use a 24 Volt DC source, five-level multilevel inverter voltage output shown in Figure 5, to reduce harmonic magnitude from multilevel voltage output passive filter R = 15 Ohm and C = 25mF, for the purpose of increasing the voltage, a step up transformer with a ratio of 1:34 is given, that the output voltage is shown in Figure 6. The harmonic voltage of each output uses analysis of Fast Fourier Transform (FFT) at the fundamental frequency of 50 Hz as in Figure 8 and 9.

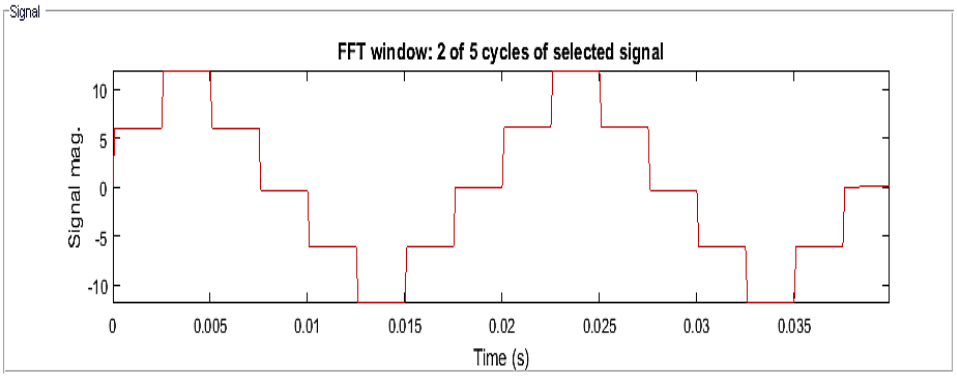

Figure 6. MLI five-level conventional MLI five level conventional

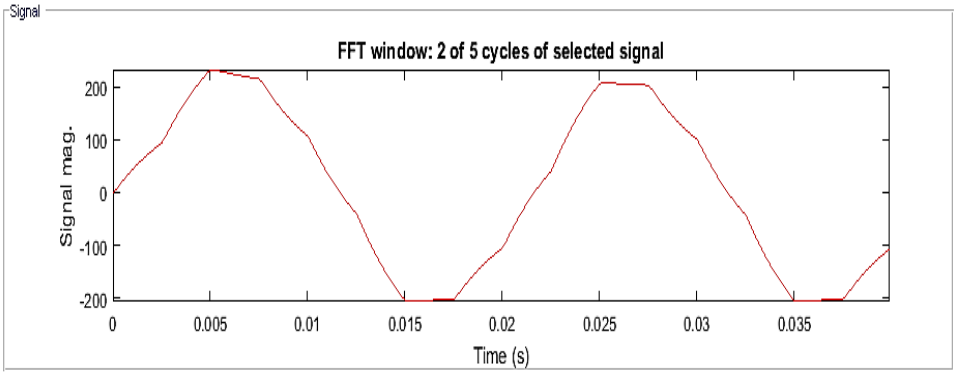

Figure 7. Step up MLI five level conventional mode

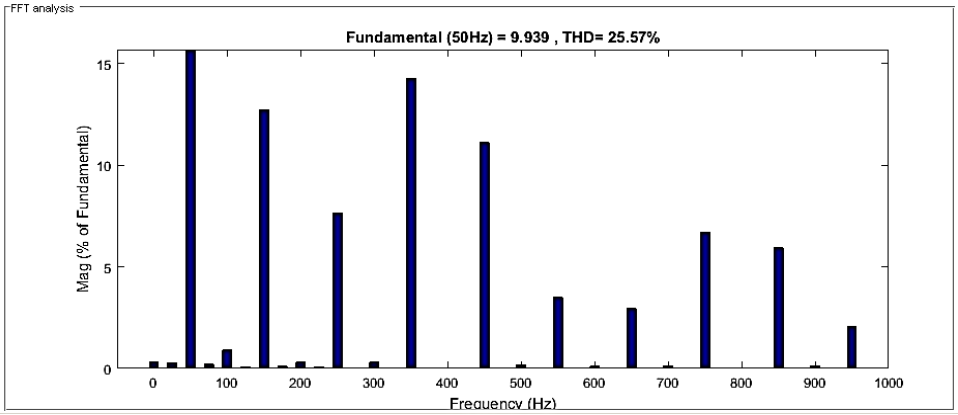

Figure 8. Conventional five-level MLI FFT

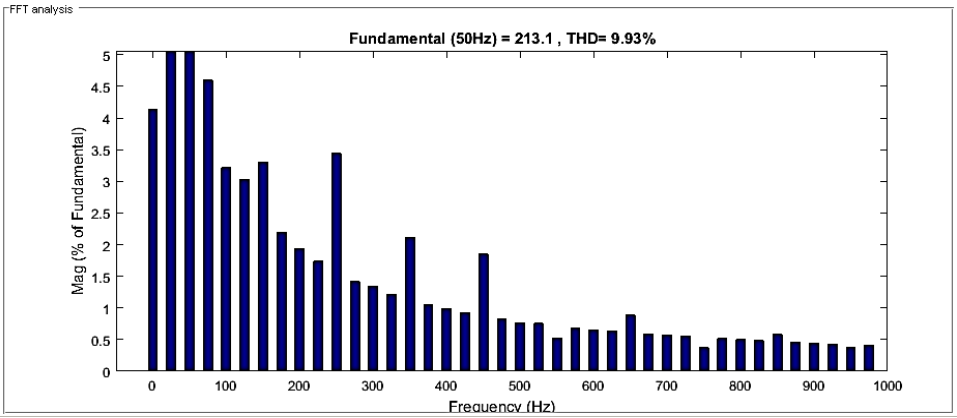

Figure 9. Step up MLI five level conventional mode

Figure 7 shows the output voltage harmonic of large MLI that uses FFT the level obtained is 25.57% while Figure 8 uses passive filter and the large harmonic step up mode MLI output voltage obtained is 9.93%. From the conventional simulation, the topology is proposed by reducing the number of switches by validation using the PWM and SPWM techniques, to obtain the optimum efficiency.

3.1. The Five Level MLI Simulation Model proposed by the PWM Technique

Proposed as a comparison discussed by using the PWM technique. Figure 9 below shows the proposed five-level multilevel inverter simulation model which uses four switches (MOSFETs). And consists of two DC sources.

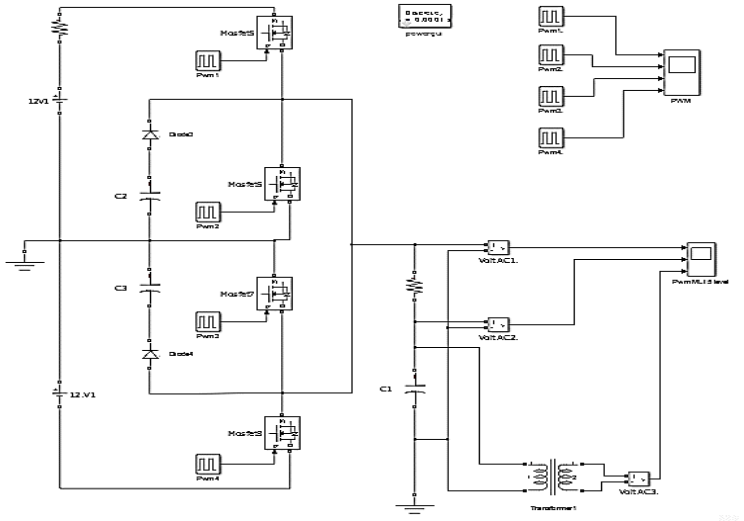

Figure 10. Five-level multilevel inverter simulation model with PWM technique

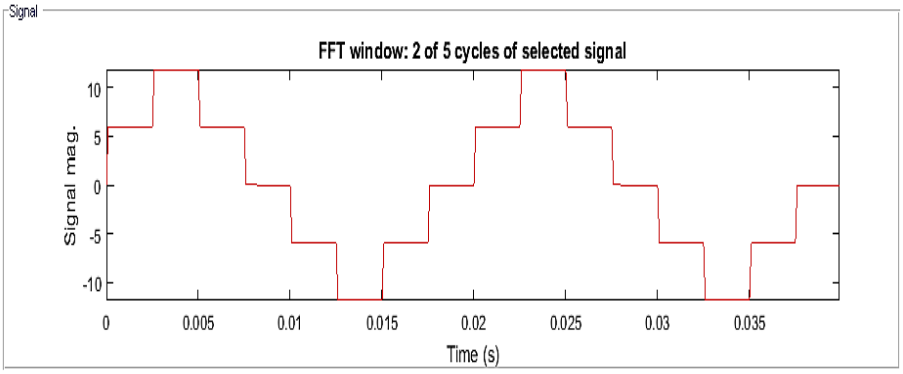

Figure 11. MLI proposed five levels with PWM

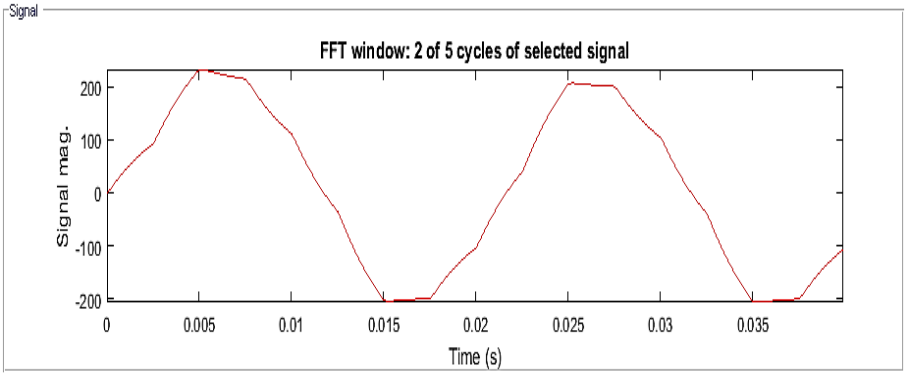

Figure 12. Proposed step up mode for five-level MLI with PWM

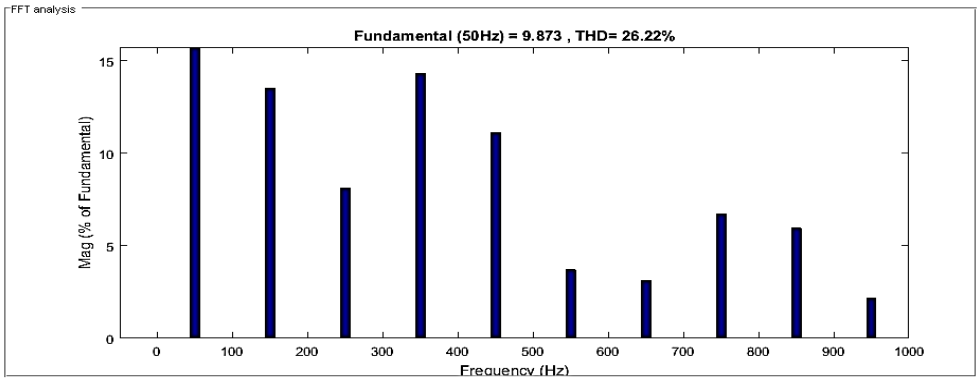

Figure 13. Proposed five-level MLI FFT with PWM

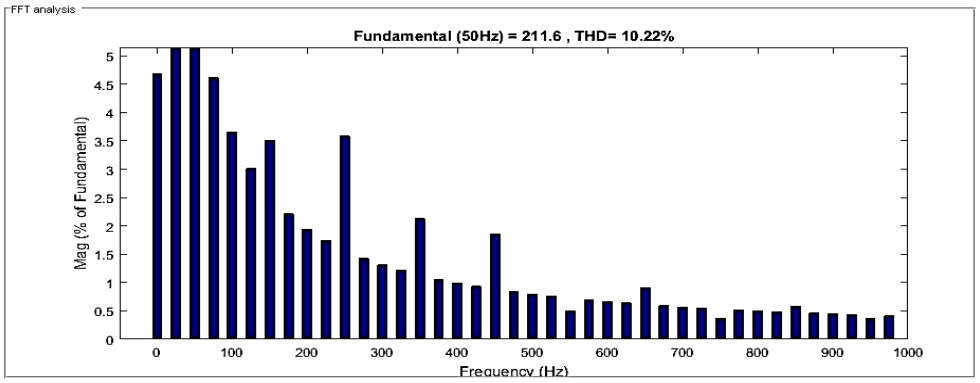

Figure 14. Proposed step up mode five level MLI FFT with PWM

As shown in Figure 13 that use the PWM technique, the harmonic output of the MLI output using FFT is 26.22%, while from Figure 14, it uses a passive filter and a large step-up harmonic mode. The output voltage is 10.22%.

The proposed topology simulation results show that to multilevel the five-level inverter by reducing the number of switches can be done, then to reduce the proposed Topology harmonic voltage, the SPWM technique is one of the first steps in multilevel inverter devices to produce low harmonics.

3.2. The Five Level MLI Simulation Model proposed by the SPWM Technique

Modulation of the PWM signal pulse width generated is a reference voltage reference (sine wave) and carrier voltage (triangle wave), in this paper the voltage frequency used is 50 Hz and 1.125 kHz respectively. The simulation model shown is shown in Figure 15 below.

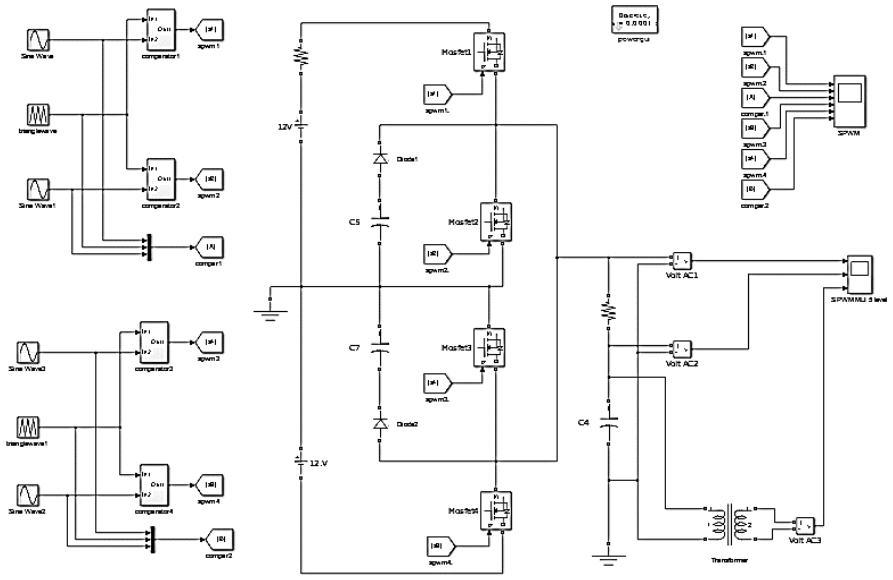

Figure 15. Simulink five-level model of proposed SPWM technic multilevel inverter

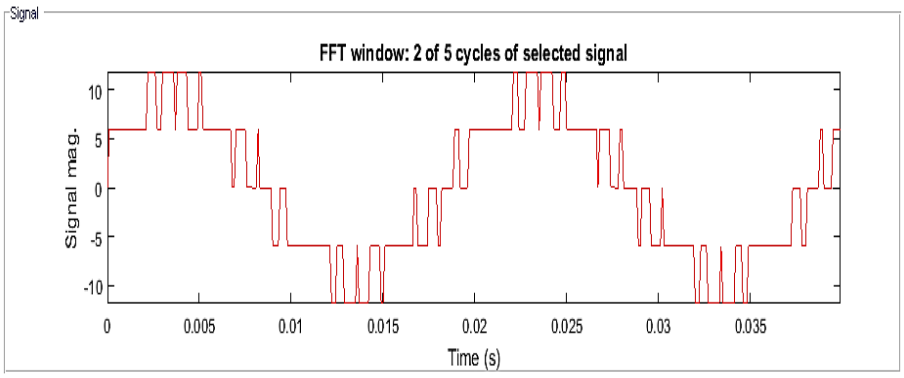

Figure 16. MLI proposed five levels with SPWM

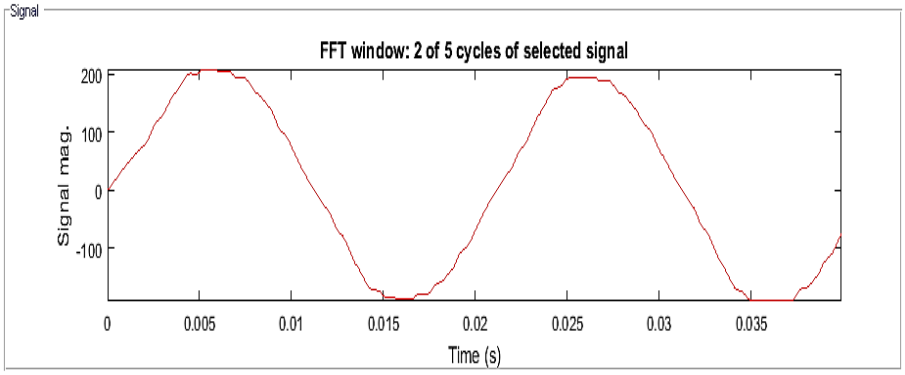

Figure 17. Proposed step up mode MLI five levels with SPWM

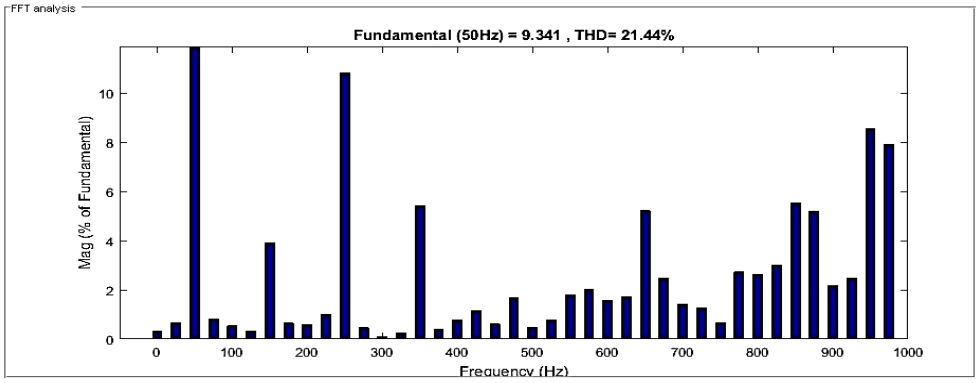

Figure 18. Proposed MLI FFT five levels with SPWM

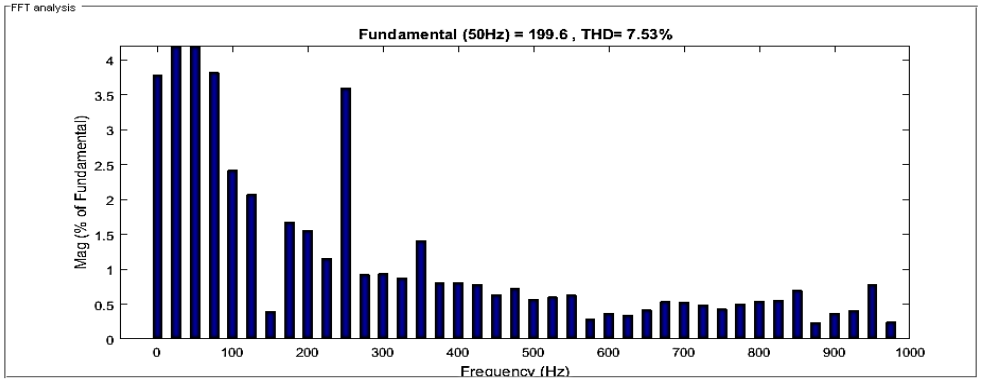

Figure 19. Proposed step up mode MLI FFT five levels with SPWM

As shown in Figure 17 the harmonic output voltage of MLI using FFT is 21.55%, while from Figure 19 that uses a passive filter and a large step-up harmonic mode the output voltage is 7.53%.

3.3. THD Comparison

Table 2 shows the comparison values of the THD

Table 2. Comparison values of THD

Harmonic mode	Conventional PWM		Proposed PWM		Proposed SPWM	
Voltage of five levels (V)	MLI 26.22	Filter 9.93	MLI 25.75	Filter 10.22	MLI 21.55	Filter 7.53

4.0 Conclusion

The proposed topology has been able to redirect component switches on a five-level multilevel inverter. MATLAB simulations performed on the conventional five-level multilevel inverters in reducing harmonic magnitude can be obtained using the topology that uses only four switch components (MOSFETs) in PWM and SPWM switching modes, the magnitude of the output voltage harmonics is 27.75% in PWM mode and 21.55% in SPWM mode A better THD using a passive filter provides a harmonic reduction in output voltage of 9.93% in PWM mode and 7.53% in SPWM mode. Thus, the proposed topology can overcome the disadvantages of conventional topology in the cost of using switch components. The implementation of hardware can also be made so that it is applied in various aspects of industrial needs.

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