Designing a new data acquisition circuit for SiPM-based detection systems — MexSiC

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Abstract: Silicon Photomultipliers (SiPM) are currently an excellent option to replace the traditional photomultiplier tubes (PMT) due to the fact that they require much lower operational voltages than the PMTs with photon detection efficiencies (PDE) higher than 40% at peak wavelengths (in the blue-green visible part of the spectra), do not require the electromechanical complexity related with PMT based solutions, and are insensitive to magnetic fields. However, one disadvantage of SiPMs, if used in applications where huge detection areas are required, is their respectively small photoactive area (of few square millimeters). Modular approaches based on arrays of SiPMs are normally used in such cases. In order to use SiPM arrays, the modular data acquisition (DAQ) systems must be capable of reading multiple channels in parallel, synchronizing the times of arrival of all SiPM output pulses, processing these pulses, discriminating between events, and generating resulting digital output signals that can be stored on an external memory unit. An application specific integrated circuit (MexSIC) to be fabricated in the 180 nm CMOS technology has been designed as a core unit of such a DAQ system. It contains a transimpedance amplifier (TIA) as its input stage, a triggering logic unit (TLU) used to discriminate the input signals, a phase locked loop (PLL) used to generate a clock reference for the time-to-digital converter (TDC) and an additional charge-to-digital converter (QDC), used for discrimination of detected events based on the amount

of charge generated within each individual SiPM on the one side, and the duration of each event on the other, as well as a Delta-Sigma (Δ-Σ) analog-to-digital converter (ADC). An additional field-programmable gate array (FPGA), the *Xilinx Kintex 7*, is used for signal processing and system controlling. We present the concept of the proposed DAQ system.

Contents

1 Introduction

This work describes the concept and the first simulation results for a data acquisition (DAQ) system designed to process and digitize signals delivered by clusters of *On-Semiconductor SensL J-Series 30035* [1] SiPMs. The core part of the system is the MexSIC chip, currently under development in a 180 nm commercial CMOS technology, aimed at acquiring nine input SiPM current pulse signals in parallel, discriminating the detected events of interest using a Triggering Logic Unit (TLU), defining their exact time of arrival using an internal 2 GHz digital oscillator that forms the core part of both, the time-to-digital converter (TDC) and the charge-to-digital converter (QDC). The TDC unit calculates the signal time-over-threshold (ToT) values triggered by the TLU, and the DAQ system finally delivers 12-bit digitized signals and the integral of each individual current pulse, i.e. its charge content. Additionally, a Delta-Sigma ($\Delta\Sigma$) ADC and an external FPGA module process the signals from the transimpedance amplifier (TIA) to assist the data conversion.

2 SiPM characterization

The *On-Semiconductor SensL J-Series 30035* SiPM is a 3×3 mm^2 photoactive area detector, capable of detecting input radiation bursts containing a small amount of individual photons in the visible part of the spectra (with a peak wavelength at 420 nm) during short emission times, ranging between 1 ns and 20 ns. According to the datasheet [1], it needs 24.2 V of biasing to induce a breakdown voltage. If a high amplification is needed, a recommended overvoltage is of about 2.5V and it is added to the breakdown voltage, which produces a gain factor of 3×10^6.

2.1 Experimental setup

Figure 1 shows a schematic diagram of the experimental setup used in the characterization of the SiPM. In the first step, a FPGA based pulse generator controls a Light Emission Diode (LED) emitting blue light. Applying different durations in the pulse width, the LED illumination emits

different optical intensities. The SiPM datasheet [1] shows that the typical electrical output pulse duration expected from these SiPMs is of about 250 ns if the standard (anode-cathode) output is used, and of 5 ns if the so-called "fast output" is used yielding nevertheless only approximately 10% of the output charge in the process. In this work, the standard output will be used. For device characterization, pulse durations of the LED illumination are varied while the separation between the light pulses is always kept at 300 ns. The SiPMs under test were introduced into a black box to avoid any stray light and ensure it only captures the illumination from the LED alone. Following, the SiPMs (biased at 27 V) send the generated electrical outputs caused by the LED illumination bursts to a TIA circuit. The signal is amplified, and the output is digitalized via Digital Signal Analyzer (DSA) that runs at 8 GHz and takes 80 Gs/s.
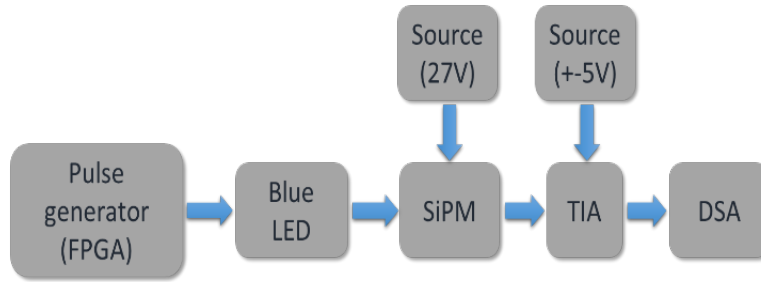

Figure 1. Experimental setup to characterize the SiPM.

According to the user manual [1] of *On-Semiconductor SensL J-Series* SiPM detectors, the recommended TIA is the OPA656 [2], a standard high-speed amplifier capable of supporting the SiPM outputs with a high amplification. In this characterization, different outputs from the SiPM were obtained, as shown in figure 2. The SiPM outputs obtained without amplification are shown in figure 2 (a). These responses were obtained using a larger pulse duration emitted by the LED and they don't need an amplification of their amplitude to analyze them. However, the proposed system must be able to process all possible cases, including the smaller signals.
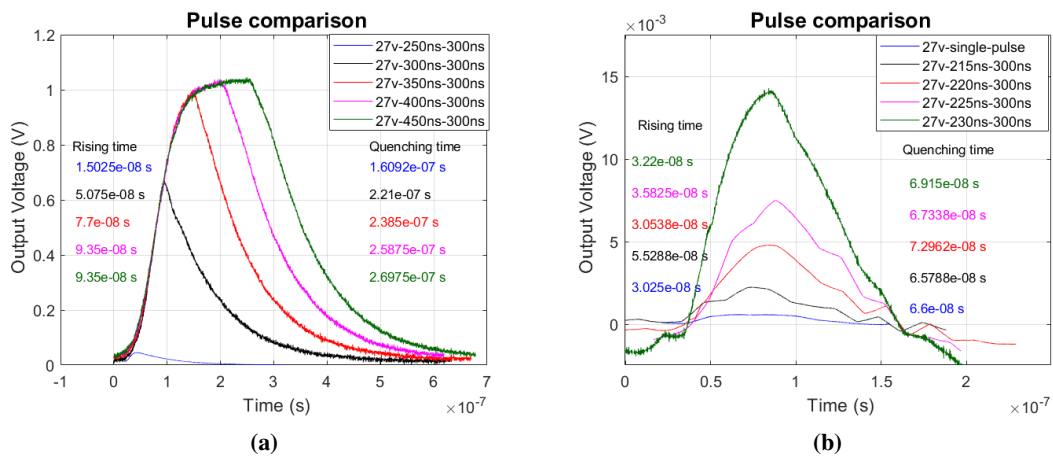

Figure 2. SiPM output applying different Led pulses: (a) with TIA circuit, (b) without using TIA circuit.

When a short pulse duration from the LED is applied, the SiPM output is a low amplitude charge. In order to analyze the low output amplitude from the SiPM, a TIA circuit is used. Figure 2 (b) shows the SiPM output when a TIA circuit amplifies the smaller signals. Further it is noted that the amplified signals are nosier than the signals without amplification, but the most important in this case is the obtained amplitude. On the other hand, figure 2 (b) shows a single count (blue signal) acquired from the SiPM. This signal is obtained when the noise is analyzed, and the source illumination (LED) is off. This condition generates dark counts that can be acquired with the DSA. Figure 3 (a) (blue signal) shows that some peaks contained on the signal have a considerable higher amplitude and they may be candidates for single counts. It occurs when a single avalanche event is triggered. When a wavelet transform filter [3] is applied to this signal, then the black signal in figure 3 (b) is obtained. It was decided to analyze the signal inside the red rectangle, because this region contains peaks with a low amplitude. When a zoom (figure 3 (b)) is applied (between -3 and $-2\,\mu s$) the single count is obtained.
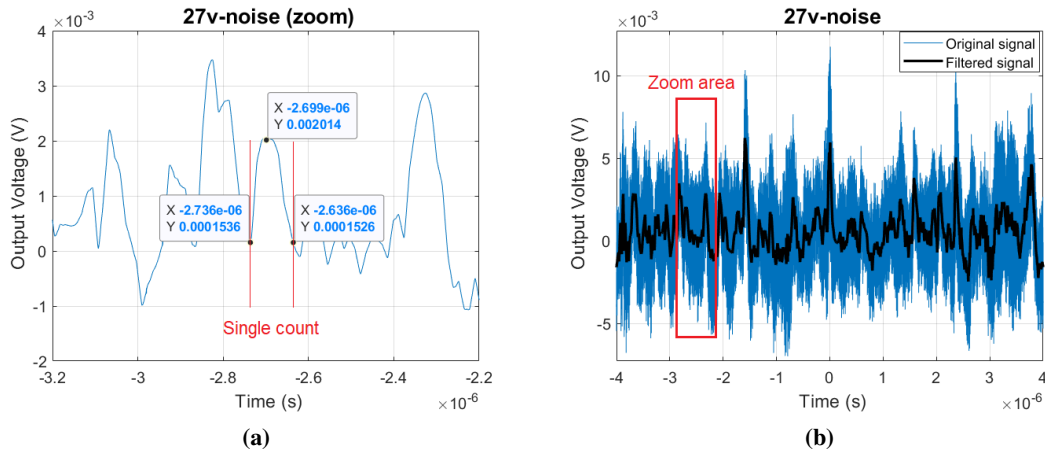

Figure 3. Output noise analyzed with a wavelet transform filter: (a) original and filtered signal comparison, (b) single count obtained.
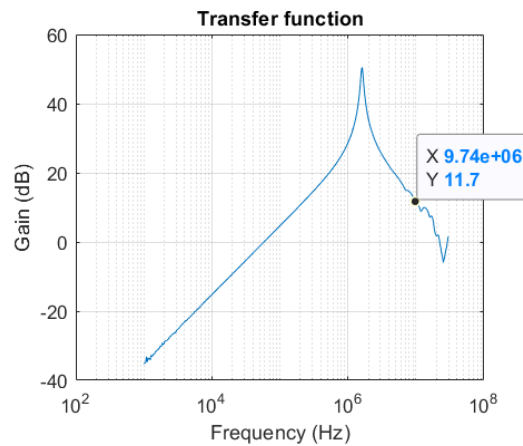

Figure 4. Transfer function of TIA circuit.

The single count has a voltage of about 2.7 mV with amplification. Figure 4 shows the TIA transfer function and the amplification value corresponding to the single count (11.7 dB). The original amplitude of the single count is: $Gain = 10^{\frac{11.7}{20}} \approx 3.55$. When the 2.7 mV is divided by the amplification, 563.38 μV is obtained as the original voltage amplitude. Table 1 shows the SiPM output characteristics. The maximum voltage obtained was 1.03 V or 20.8 mA with a time duration of 363.25 ns. The single count represents the minimal voltage with 563.38 μV of amplitude and 100 ns of time duration. The system must be capable to process this minimal time duration. Using the data previously obtained, the dynamic range is:

$$\text{Dynamic Range}_{dB} = 20 \cdot \log \left(\frac{V_{\max}}{V_{\min}} \right) = 20 \cdot \log \left(\frac{1.04\,\text{V}}{563.38\,\mu V} \right) \approx 65.32\,\text{dB}$$

Table 1. Pulse characteristics from SiPM.

LED pulse	Amplitude (V)	Amplitude (A)	Rising time (s)	Quenching time (s)	Pulse duration (s)
0ns-0ns (noise)	5.74×10^{-4}	1.149×10^{-5}	3.025×10^{-8}	6.6×10^{-8}	100.9×10^{-9}
215ns-300ns	2.23×10^{-3}	4.463×10^{-5}	5.528×10^{-8}	6.578×10^{-8}	125.23×10^{-9}
220ns-300ns	4.77×10^{-3}	9.55×10^{-5}	3.05×10^{-8}	7.29×10^{-8}	132.14×10^{-9}
225ns-300ns	7.48×10^{-3}	1.4×10^{-4}	3.582×10^{-8}	6.733×10^{-8}	127.99×10^{-9}
230ns-300ns	14.2×10^{-3}	2.85×10^{-4}	3.22×10^{-8}	6.915×10^{-8}	130.29×10^{-9}
250ns-300ns	45.93×10^{-3}	9.186×10^{-4}	1.5025×10^{-8}	1.6092×10^{-7}	175.95×10^{-9}
300ns-300ns	0.671	13.42×10^{-3}	5.075×10^{-8}	2.21×10^{-7}	271.75×10^{-9}
350ns-300ns	1	20×10^{-3}	7.7×10^{-7}	2.385×10^{-7}	315.5×10^{-9}
400ns-300ns	1.038	20.76×10^{-3}	9.35×10^{-8}	2.5875×10^{-7}	352.25×10^{-9}
450ns-300ns	1.039	20.8×10^{-3}	9.35×10^{-8}	2.6975×10^{-7}	363.25×10^{-9}

3 Methodology

The operational diagram of the proposed system is shown in figure 5. In this proposed design, the SiPM is placed off-chip whilst the rest of the components, excluding the FPGA, will be placed on-chip. When the SiPM is illuminated, the output is sent to the TIA as the input stage used to convert the current signals into voltage and additionally, amplify them. To discriminate the SiPM signals, a TLU is used to compare the SiPM output signals with the desired programmable threshold levels adjusted to the background illumination (including the dark count rate, DCR). When the input signal is validated with the TLU unit, it is delivered from the TIA to the QDC and TDC processing units, as depicted in figure 3. The main idea consists in using the PLL generated oscillations running at 2 GHz and count the amount of cycles the signal remains above the TLU defined threshold levels (with a timing resolution of 500 ps) using a 10-bit digital counter. On the other hand, in parallel, the signals undergo a 12-bit analog-to-digital conversion at a Delta-Sigma ($\Delta\Sigma$) ADC [4]. The system delivers the digitized original signals and performs a 12-bit resolution integration of these signals in the digital domain to obtain the amount of charge contained in each validated SiPM output signal.

As explained below, the decimation of the 1-bit modulated output signals of the Delta-Sigma ($\Delta\Sigma$) ADC modulation core unit as well as the integration of the obtained digital signals is performed off-chip using the FPGA unit present on each DAQ unit board.
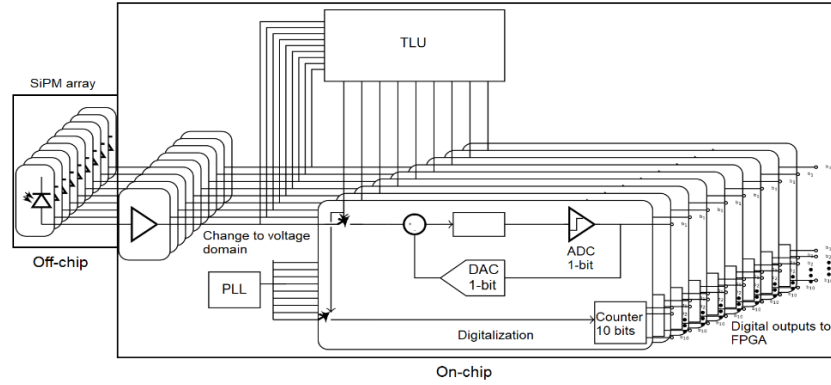

Figure 5. Operational diagram of the proposed DAQ system.

As mentioned above, a $\Delta\Sigma$ which contains integrators performs feed-forward summation. The $\Delta\Sigma$ modulator finally sends an output 1-bit pulse train at 2 GHz of oscillation frequency to the on-board FPGA unit, ensuring that the pulse width is proportional to the signal slope at rise-time. Following, the FPGA receives the pulse train and starts a decimation process [5]. During this decimation process the signal is demodulated, and a digital signal is finally obtained. Figure 4 shows a schematic representation of this simple decimation process, as it was implemented in the FPGA. Basically, the decimation process is started using a digital integrator (Z^{-1} is a simple digital integrator) and followed by a down sampling process (it removes parts of the signal generated by the oversampling of $\Delta\Sigma$) and finally, a comb filter (Z^{-d} where d is the time to delay the signal) delivering the digital signal. This proposed system is capable of delivering the digitized signals considering the input dynamic range of up to 70 dB and 12-bit of resolution.
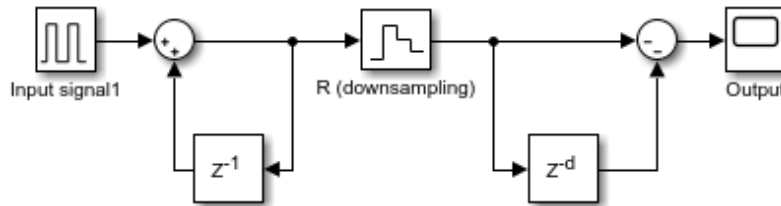

Figure 6. Decimator implemented on FPGA.

In parallel, the time-to-digital conversion of the input signals is taking place. This process starts once the LTU unit has validated an input signals as it surpasses the defined threshold voltage considered for the background radiation. The PLL unit is generating a 2 GHz oscillations, and the TDC unit starts counting, using an on-chip implemented 10-bit digital counter for this task, the amount of 500 ps time-cycles counted represents the time of the signal above the threshold voltage (monitored the entire time by the LTU unit). Once the signal drops below this threshold value, the counter stops and delivers the 10-bit TDC information to the FPGA unit off-chip. As shown in

figure 5, the final idea is to create a multichannel DAQ system with a single master clock (one PLL unit for each nine channels) that will able to work in parallel with synchronous signals.
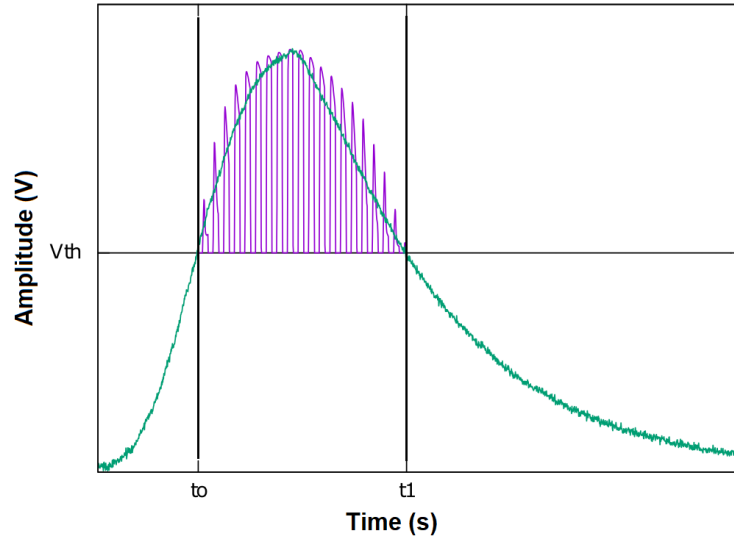

Figure 7. TDC output.

4   Preliminary results for the ΔΣ modulator

Figure 8 shows the simulation results obtained using a VHDL description of the explained logical units of the DAQ system proposed. The on-chip functionality was simulated using the Verilog tool contained in CADENCE software. The blue signal represents the ΔΣ modulator 1-bit coded output from the MexSIC chip.
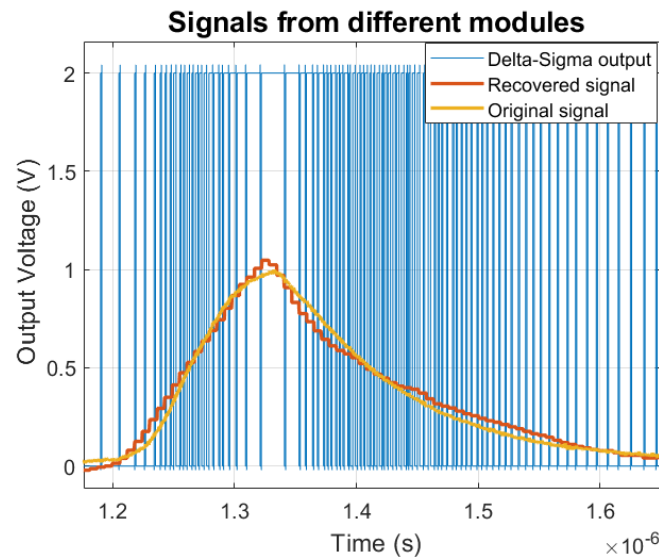

Figure 8. Simulation output of the DAQ system.

The $\Delta\Sigma$ modulator output shows that the width of the pulse train is short when the analog input signal shows steep slopes and become wider when the signal remains unaltered over longer periods of time. The yellow signal represents the original signal from the SiPM introduced to the TIA amplification unit and afterwards to $\Delta\Sigma$ modulation stage. The orange signal represents the digital output of the SiPM signals generated at the FPGA after the decimation process is applied. The recovered signal is very similar to the real input with a standard deviation about 0.28 V.

5 Conclusions

The analog SiPM DAQ system conceived for several parallel SiPM generated input signals is featured by the application specific integrated circuit MexSIC, designed to be fabricated in a 180 nm commercial CMOS technology as its core element. The MexSIC, with 9 input channels working in parallel, was conceived and simulated to run at 2 GHz frequency, yielding event triggering times with 500 ps time-resolution, 10-bit event time-over-threshold information, 12-bit $\Delta\Sigma$ ADC digital reconstruction of the SiPM input signals, as well as 12-bit digital event charge information. The first design of the proposed MexSIC chip is currently in fabrication and the first performance results will be reported in the first half of 2020.

Acknowledgments

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