

High efficiency superconducting field effect devices for oxide electronic applications

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Abstract

We present a study of the efficiency of $\text{LaAlO}_3/\text{SrTiO}_3$ nanoscale field effect devices realized in the side gate configuration. We show that a change in the resistance of more than four orders of magnitude and a voltage gain of up to 50 can be obtained with the application of a gate voltage smaller than 1V. At dilution temperatures, the nanodevices become superconducting and we demonstrate the possibility to obtain a superconductor to insulator transition by applying only 200 mV. These results are discussed in the view of applications for quantum electronics.

Keywords: oxide interfaces, field effect transistors, oxide nanodevices, superconducting field effect device

(Some figures may appear in colour only in the online journal)

1. Introduction

Two dimensional electron systems (2DES) at the interface between oxide materials hold great potential for electronic applications, thanks to their wide range of properties [1, 2]. One of the most celebrated oxide 2DES is the $\text{LaAlO}_3/\text{SrTiO}_3$ (LAO/STO) heterostructure, which shows, among other properties, a superconducting ground state [3] coexisting with Rashba spin-orbit coupling [4], both of which are tunable using the electric field effect. The latter is, on one hand, one of the most important tools to study the interactions between several degrees of freedom in these systems [5–7]. On the other hand, it can also be exploited to realize oxide-based electronic devices. The possibility to realize complex circuits using uniquely LAO/STO-based building blocks has been recently demonstrated by Jany *et al* [8], who realized and tested n-type metal-oxide-semiconductor (NMOS) ring-oscillators composed of field effect transistors, resistors and interconnects. The transistors, in particular, were realized in the top gate configuration and operated at room temperature with a gate voltage in the order of a few volts.

Another possible application of high efficiency field effect oxide devices is in the field of quantum electronics, similarly to what is being pursued for graphene and other 2D

systems [9]. Currently, for instance, the electronic interface for the control of a quantum computer works at room temperature. As the number of qubits increases, approaching that required for the implementation of practical algorithms, this architecture becomes inadequate and new designs, with optimized performances at cryogenic temperatures, are needed [10, 11].

In this work we test LAO/STO field effect nanodevices realized in the side gate configuration and discuss their efficiency at cryogenic temperatures. We demonstrate that it is possible to tune the 2DES from the superconducting to the insulating phase and control the superconductivity with a gate voltage in the range of hundreds of millivolts or less. We finally discuss the possibilities offered by these devices and the perspectives for application in quantum electronics.

2. Samples design

The devices studied in this work were realized following the side gate layout described in [12] (see the sketch in figure 1(a)). This configuration exploits the LAO/STO 2DES as both active channel and gate electrode and the high dielectric constant STO substrate as gate dielectric [13, 14].

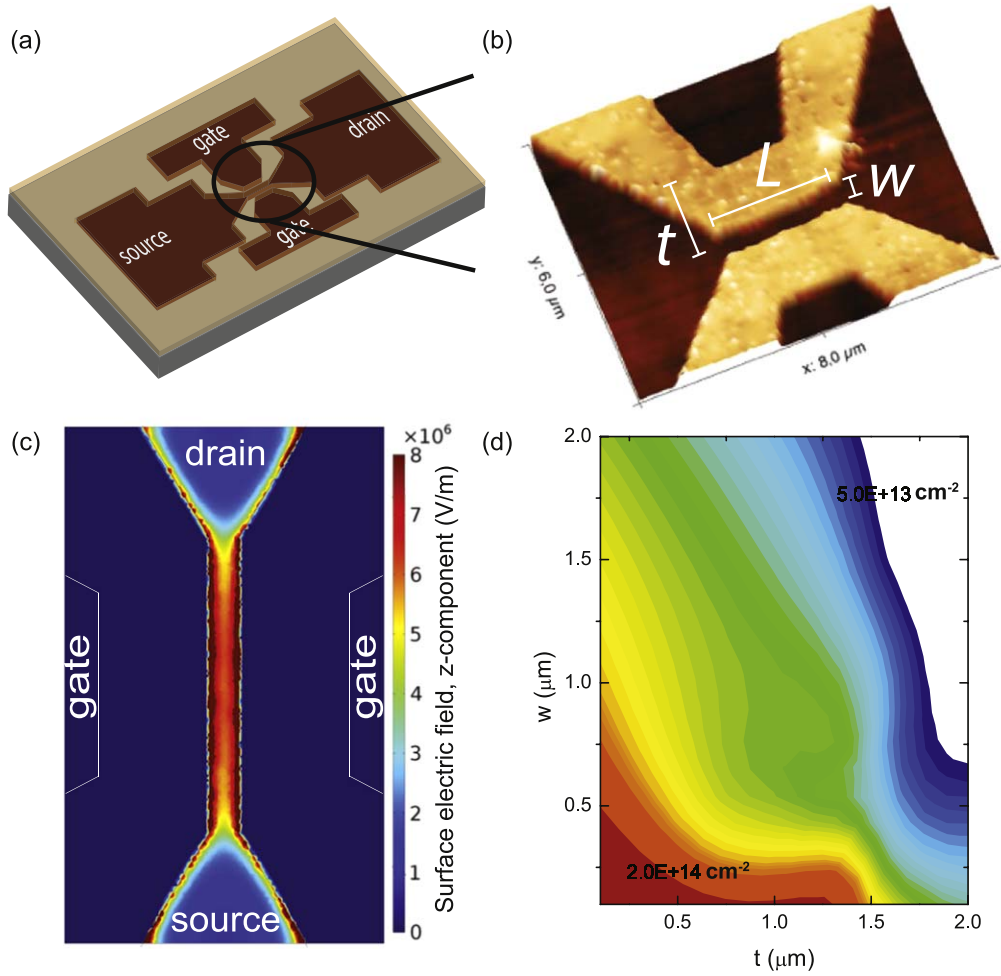


Figure 1. Panel (a) shows the sketch of side-gate field effect devices. The nanochannel area is shown in detail in the atomic force microscope image of panel (b). Here w is the channel width, L its length and t is the distance between the gate electrodes and the middle of the channel. Panel (c) shows a finite elements simulation of the electric field in the z direction induced by a gate voltage $V_G = 0.5\text{V}$ in a device having $w = 0.4 \mu\text{m}$, $t = 1.7 \mu\text{m}$ and $L = 4 \mu\text{m}$. Panel (d) shows the simulated change in carrier concentration for the applied voltage as a function of w and t .

Electron beam lithography is used to define a PMMA mask on a TiO_2 terminated STO substrate; an amorphous STO layer (10 nm thin) is then deposited on the sample and the mask is transferred to it via lift-off [15]. Subsequently, after cleaning in oxygen plasma to ensure the complete removal of the PMMA resist, a 10 unit cell thick LAO film is deposited via reflection high-energy electron diffraction assisted pulsed laser deposition. This film grows epitaxial on the exposed substrate areas and amorphous/polycrystalline on the areas covered by the amorphous STO. In figure 1(b) we show an atomic force microscope image of a typical device. The amorphous/polycrystalline LAO areas have a yellow color, while the epitaxial LAO ones, under which the 2DES develops, are shown in brown. We point out that, using this fabrication process, the LAO/STO nanochannel and two gates, one at each side of it, are created in a single lithography step, thereby limiting the number of lithography processes the sample undergoes. For operations, the same gate voltage is applied to both gate electrodes while the channel is current or voltage biased.

For a more efficient design of these devices, we simulated their electrical transport behavior using the COMSOL MULTIPHYSICS software. In a previous report [12], we verified that in the side gate configuration, the field effect is comparable to a back gate action (with an electrode placed on the back of the STO single crystal substrate [5]): the field lines departing from the side gate electrodes penetrate into the high dielectric permittivity STO substrate and close below the 2DES channel. In figure 1(c) we show the simulation of the electric field induced by the side gates in a device having width $w = 0.4 \mu\text{m}$ and length $L = 4 \mu\text{m}$. The distance between the gate electrodes and middle of the channel is $t = 1.7 \mu\text{m}$ (see sketch in figure 1(b)). Panel (d) shows the simulated change in carrier concentration for the applied voltage as a function of w and t . By reducing both parameters, a change in the carrier concentration in the center of the channel up to $2 \times 10^{14} \text{ cm}^{-2}$ can be obtained applying a gate voltage of only one volt. This change is up to three orders of magnitude larger than what can be obtained in conventional back-gate LAO/STO field effect devices applying several tens of volts, one order of magnitude larger than what is

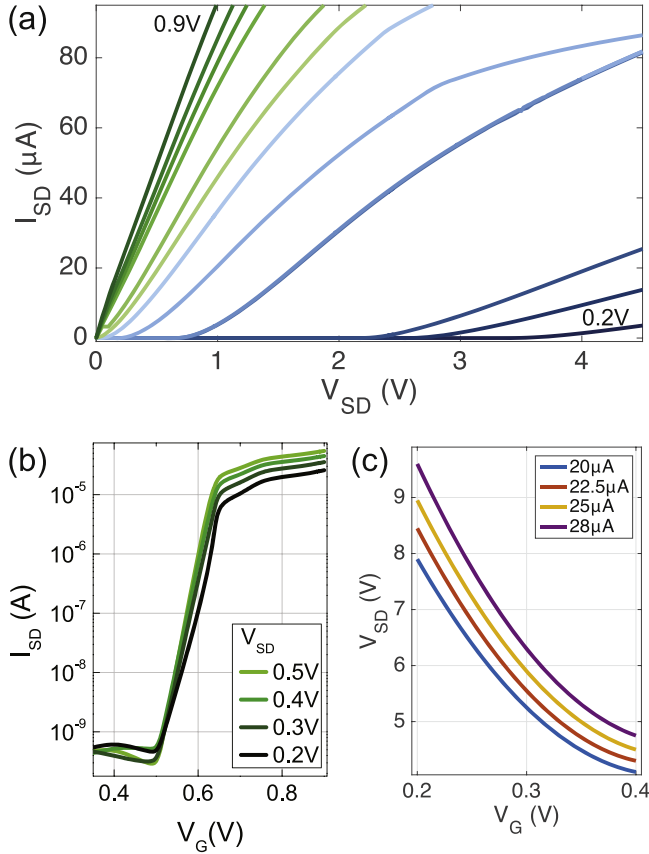


Figure 2. Panel (a) shows the output characteristic of device A. Panel (b) shows the I_{SD} vs V_G transfer characteristic of device A for several values of the source-drain voltage V_{SD} . Panel (c) shows the change of the output voltage V_{SD} as a function of gate voltage V_G for several values of I_{SD} . All the data were measured at $T = 1.5$ K.

obtained in top gate devices [16, 17] and more than twice that obtained using ionic liquid top gating [18].

In the next section, we demonstrate that side gate devices show a ‘standard’ field effect behavior with extremely high efficiency. Moreover, when cooled down to dilution temperatures, an insulator to superconductor transition can be obtained with only a few hundreds of millivolts.

3. Transport properties as a function of the temperature

We studied the field effect tuned electrical transport as a function of the temperature for device A, with $w = 0.4$ μm , $t = 1.7$ μm and $L = 4$ μm , and device B, with $w = 0.25$ μm , $t = 0.7$ μm and $L = 2$ μm . These dimensions were chosen to obtain a reproducible fabrication procedure and an efficient field effect modulation [12]. All the measurements shown below were performed after a ‘forming process’ of the 2DES, which is an initial positive sweep of the gate voltage needed to obtain a reversible R versus V_G curve [17, 19]. The output characteristic of device A, measured at $T = 1.5$ K, is shown in figure 2(a). The curves show a non-saturating behavior and

an upturn at large V_{SD} . Similar behavior was found in LAO/STO top gate field effect devices [20, 21] and ascribed to short channel effects. Our measurements, realized on a different gate configuration, reinforce the conclusion that LAO/STO field effect transistors have, in this respect, a behavior comparable to that of standard semiconducting devices.

Figure 2(b) shows the transfer characteristic of device A. Although the device channel width is in the sub-micron range, off currents are very low (in the order of 4×10^{-10} A) and the on-off ratio is about 10^5 . These good performances could be further improved by optimizing the device design. As it can be seen from the simulation of figure 1(c), the gate induced field is slightly weaker at the edges of the nano-channel, therefore these areas act as a series resistance. By extending the side gate electrodes, making them of the same length of the channel, this effect could be greatly reduced. A similar issue has been found in top gate geometry devices where, for technical reasons, the gate electrode can cover only a part of the channel [20].

Finally, in order to evaluate the voltage gain $G = \Delta V_{SD} / \Delta V_G$, we show the high voltage response of device A for several values of the current I_{SD} in figure 2(c). This plot shows that a gain of up to 50 can be obtained, using for instance $I_{SD} = 28$ μA and $V_G = 0.2$ V [22].

Figure 3(a) shows the field effect modulation of the resistance of device B, where the channel width and the distance between the channel and the gate electrodes were reduced compared to device A. Device B was biased with a current $I_{SD} = 100$ nA and the resistance measured with a lock-in technique. The data sets were acquired during different cool-down runs, and their consistency confirm the stability of these devices. While at 100 K the gate voltage needed to tune the device resistance is in the range of tens of volts, by decreasing the temperature the tuning can be accomplished with only a few hundreds of millivolts. Indeed, the value of the gate voltage needed to change the ratio R/R_{max} from 0.1 to 1 (i.e. change the resistance of one order of magnitude) decreases from 250 mV to 37 mV upon reducing the temperature from 100 K to 1.5 K. This behavior reflects the increasing of STO dielectric constant upon decreasing the temperature. The field effect is even more striking when operating the device at dilution temperature, as we will show in the next section.

4. Superconductivity

Figure 3(b) shows measurements of the resistance as a function of gate voltage of device B at $T = 30$ mK. These data were acquired using a dilution refrigerator equipped with magnetic screens and copper powder filters for low noise measurements [23, 24]. In order to reveal the superconducting transition in our devices, we reduced the bias current to 5 nA. At dilution temperatures, the R versus V_G tuning is steeper compared to data shown in panel 3(a), with a change of more than three orders of magnitude with a ΔV of just 170 mV. The

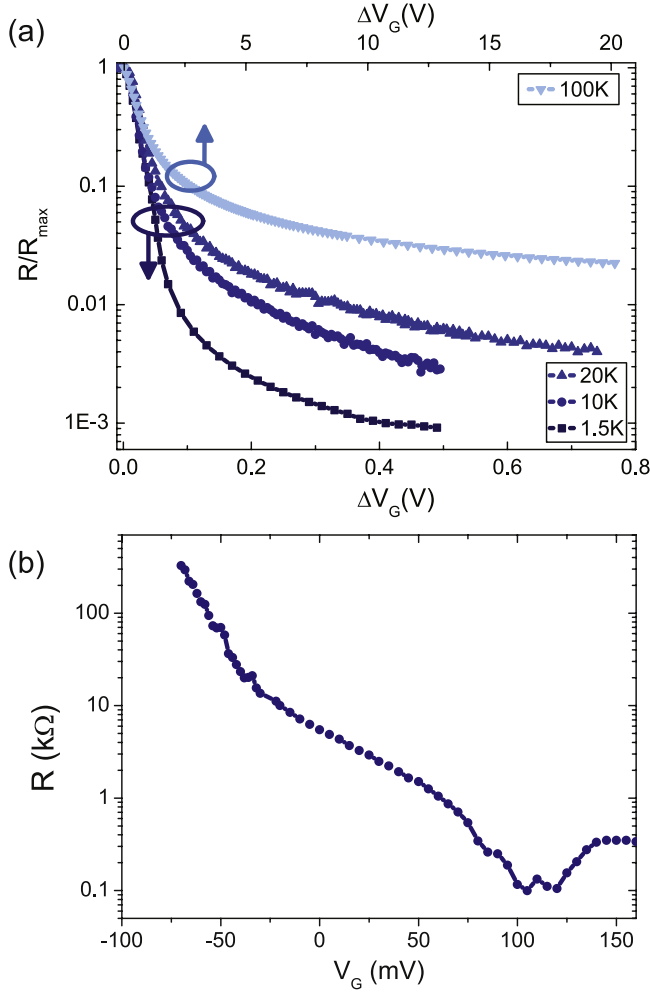


Figure 3. Panel (a) shows the normalized resistance R/R_{\max} versus normalized gate voltage $\Delta V = V_G/V_G(R_{\max})$ of device B measured at several temperatures. Panel (b) shows the resistance versus gate voltage at dilution temperature (30 mK).

plot shows a non monotonic R versus V_G behavior, with a minimum of the resistance for $V_G = 100$ mV, followed by a slight increase. This behavior mimics that of the critical current. The minimum of the resistance coincides indeed with the maximum of the critical current I_c (see inset of figure 4(b)), then is followed by an increase, corresponding to the decrease of I_c in the over-doped part of the phase diagram (where, in turn, the critical temperature decreases). The complete R versus T and current versus voltage ($I - V$) curves are shown in figure 4. The R versus T data of panel (a), acquired changing the field effect voltage across the superconductor to insulator transition, show several steps. This behavior is typical of a superconducting channel with non uniform doping and different local critical temperatures [25]. A first sharper kink, indicated by the gray dashed line, is visible at 200 mK for all the gate voltage values. We attribute this feature to the superconducting transition of those parts of the device which are not affected by the side gates (ex. large pads). The other steps, as for instance that marked with the dashed green line, change position with the gate voltage and are therefore related to the field effect-tuned superconducting

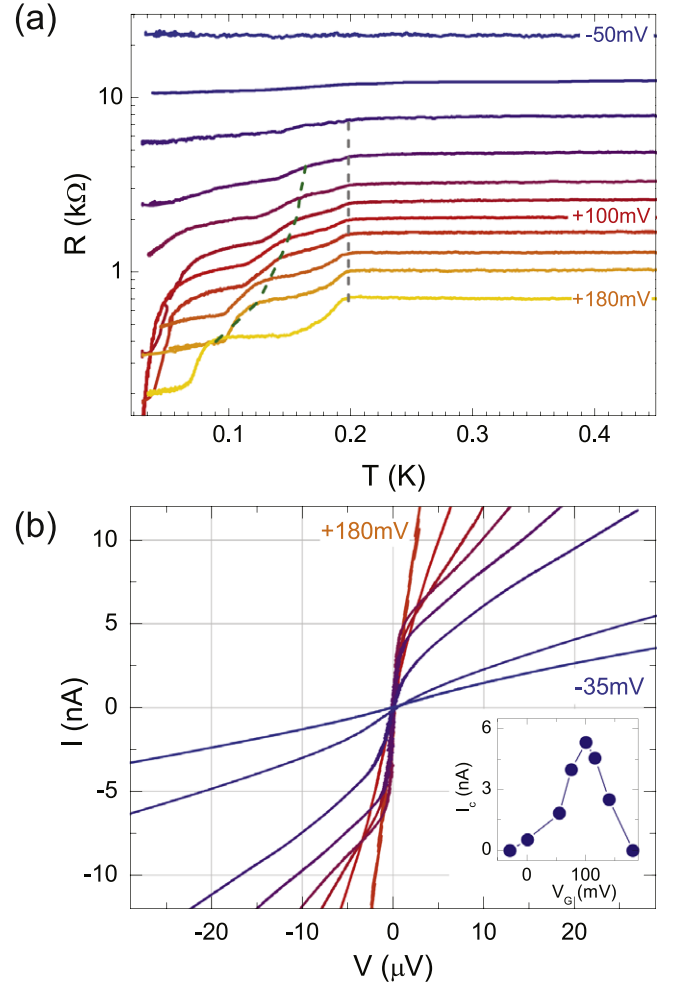


Figure 4. Panel (a) shows selected R versus T curves of device B. The data show multiple steps as discussed in the text. Panel (b) shows $I - V$ curves measured for device B at $T = 30$ mK. The maximum critical current of 5 nA is reached at $V_G = 100$ mV. In the inset, the modulation of the critical current as a function of the gate voltage is reported. The I_c was extracted using a $V = 1.5 \mu V$ criterion.

transition of the nanochannel. The presence of multiple transitions can be understood looking at the finite elements simulation picture of figure 1(c). As mentioned in the previous section, the gate-induced electric field is larger in the central part of the channel than in the ends, bringing a modulation of the carrier concentration, thus of the critical temperature, along the length of the nanowire. Finally, in figure 4(b) we show selected $I - V$ curves measured at $T = 30$ mK changing the gate voltage⁴. A maximum critical current $I_c = 5$ nA is reached for $V_G = 100$ mV, corresponding to a critical current density of $200 \mu A cm^{-1}$, in agreement with previous works on micron and sub-micron size LAO/STO devices [15, 26]. The tuning of the critical current (inset of panel (b)) mimics the ‘dome’ of the superconducting phase diagram of LAO/STO, showing complete

⁴ The low voltage rounding of the $I - V$ curves, more pronounced as the critical current decreases, is due to the occurrence of thermally activated phase slip events. Those are commonly found in superconducting nanostructures.

suppression of the I_c both in depletion and in accumulation mode.

5. Discussion

In this work we demonstrate that very high efficiency can be reached in LAO/STO field effect devices in the side gate configuration. These devices can be operated down to 30 mK where a gate voltage of just 200 mV is needed to perform a complete superconductor to insulator transition, making them perfect candidates for superconducting field-effect electronics [27].

Another possible application of these devices could be in the field of rapid single-flux quantum-based circuits. For this application, the ability to switch using (i) a voltage pulse of a few millivolts at (ii) a working frequency in the order of GHz are needed. Finite element simulations indicate that the first requirement could be reached with a further reduction of the size, realizing nanochannels of 100 nm in width, which is feasible with the electron beam lithography technique used and by improving the side gate electrodes design. As regards the frequency response of LAO/STO channels, promising results have been recently obtained by Liu *et al* [28], who measured LAO/STO field effect devices in the top gate configuration, with a gate length of several microns, and estimated a cut-off frequency at room temperature in the order of tens of MHz. This value is primarily determined by the low room temperature effective mobility of the 2DES, in the range of $4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. However, the mobility is expected to increase up to two orders of magnitude with decreasing temperature [29]. Therefore, we estimate that cut-off frequencies in the GHz range could be reached at millikelvin temperatures.

In conclusion, the performances shown in this work, added to the presence of sizable spin-orbit coupling in LAO/STO [6] and to the possibility to induce ferromagnetism by delta doping (as recently demonstrated in [7, 30]) suggest that oxide 2DES are promising systems for electronic applications, both in combination with existing platforms and for the creation of new ones based on the interplay between charge and spin degrees of freedom [31, 32].

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