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Development of Silicon Photomultiplier sensors using a 180 nm custom CMOS process technology

A. Topkar,[1] **A. Singh, B. Aggarwal, S. Chakraborty and A. Kumar**

Electronics Division, Bhabha Atomic Research Centre,
Trombay, Mumbai, 400085, India

E-mail: anita@barc.gov.in

Abstract: Silicon Photomultiplier (SiPM) sensors with different pixel sizes and active areas were designed. The fabrication technology was developed using a 8″ silicon wafer foundry supporting 180 nm CMOS process technology. A simulation study using process and device simulators was carried out to study the effect of critical process parameters on the device characteristics. A custom process based on CMOS process flow was developed by optimizing critical process parameters for the fabrication of SiPMs. The sensors were characterized using various techniques for the measurement of dark current, breakdown voltage, dark count rate and cross talk, response to external light at different operating voltages and light intensities. The SiPMs were demonstrated to have desired performance in terms of dark current, geometric efficiency, and dark count rate. The developed SiPMs have low dark currents (<5 nA/cm^2) and breakdown voltage of 22 V. Initial measurements with LED light shows good linearity of SiPM response with light intensity.

Keywords: Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs, CMOS imagers, etc); Solid state detectors

[1]Corresponding author.

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1 Introduction

Silicon photomuliplier (SiPM) is a multi-pixel photodiode in which a number of pixels fabricated on a common substrate are connected in parallel through quenching resistors [1, 2]. The pixels are operated in the Geiger mode and provide a high gain for the multiplication of electrons or holes in the avalanche region. Compared to conventional photomultiplier tubes (PMT), SiPMs have excellent characteristics such as higher quantum efficiency, lower operating voltage, compact size, fast timing response (~100 ps), similar gain (~10^6) and insensitivity to magnetic field. Because of these advantages, SiPMs have great potential for applications in the fields of high energy physics experiments [3, 4], astrophysics experiments [5–7], radiation monitoring instrumentation, sensor network and security [8–11], and medicine [12, 13]. Despite widely established applications of SiPMs as photon sensors, these or similar sensors such as MPPC are being commercially produced worldwide only by a few manufacturers such as Hamamatsu Photonics, KETEK GmbH, SensL (now ON Semiconductor), etc.

Realization of a SiPM necessitates the generation of a high electric field avalanche region in the pixel area. Since SiPMs suffer from localized breakdown conditions due to the high electric field at the junction edges, a mechanism is needed to maintain the electric field uniform across the whole sensitive area. This has been achieved by either a slightly lower doped guard ring at the junction edges or using a virtual guard ring. Several reports have been published for the development of single photon avalanche photodiodes (SPAD) using standard CMOS technologies of various feature sizes [14–19]. Device structures to increase the edge breakdown voltage above the photodiode breakdown voltage have been discussed in these papers. A SiPM has several avalanche photodiode pixels connected in parallel through quench resistors. Hence the device structures and fabrication technology are derived from SPAD design/process. Various types of device structures have been implemented for the realization of SiPMs [20–23]. CMOS foundries could be used for SiPM fabrication if the SiPMs could be realized using a CMOS process flow. The integration of the SiPM with front end electronics would be also possible using such technology. A CMOS process line with lower feature size results in minimization of dead areas and hence improvement in

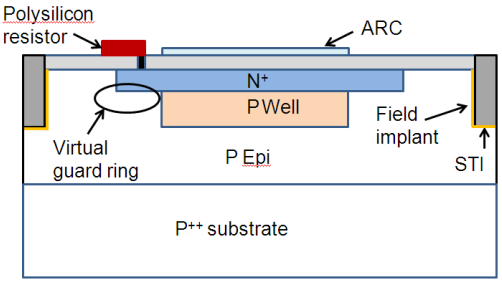

Figure 1 (a). Schematic representation of the cross section of the SiPM pixel with STI isolation.

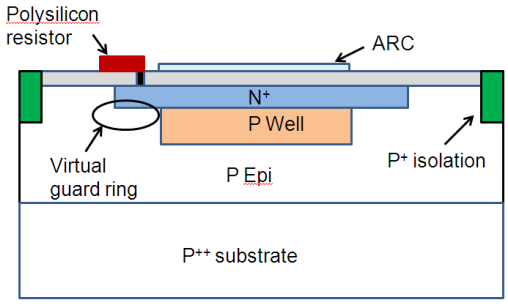

Figure 1 (b). Schematic representation of the cross section of the SiPM pixel with junction isolation.

the geometric efficiency. However, adapting the standard CMOS technology for SiPM fabrication is not straightforward. For example, the doping parameters used for source/drain and well, and inadequate spacing of the Shallow Trench Isolation (STI) region to the pixel active region would result in much lower breakdown voltage and unacceptable high dark count rate. The high resistance polysilicon module is not available in the CMOS process and needs to be developed to implement the quenching resistors which are in series with each pixel. Hence it is necessary to adapt the process parameters and design rules of standard CMOS process to achieve acceptable performance parameters for the SiPMs.

We have developed SiPMs in India using the 180 nm CMOS foundry. A considerable effort was devoted to the device design and development of a custom fabrication process. The details of SiPM device design, device and process simulation studies, fabrication process development and performance results of fabricated SiPMs are presented in this paper.

2 SiPM device design

A dedicated Process Engineering Vehicle (PEV) incorporating about twenty design variants was designed for the development and optimization of SiPM fabrication process. The PEV consisted of SiPMs of different pixel sizes (10 µm × 10 µm and 50 µm × 50 µm), and geometric sizes (1.5 mm × 1.5 mm and 3 mm × 3 mm). Additionally, other processes and device test structures were included in the PEV for process diagnosis and monitoring. The N^+/P-well diode with virtual guard ring architecture was adopted for the pixel. The inter-pixel isolation was based on implant isolation or STI. Figure 1(a) and figure 1(b) show the schematic cross sections of the SiPM pixels with these two types of isolations. As depicted in these figures, each pixel is composed of a N^+/ P-well junction in series with a polysilicon quenching resistance (R_{poly}). All pixels are connected in parallel through the aluminum (Al) layer on the photo-sensitive side and the substrate on the other side. The polysilicon line forming the quench resistor and metal lines connecting the pixels are routed over the inter pixel isolation area itself so as to reduce the dead area between the pixels. Since the metal lines, polysilicon resistor line, etc., contribute to the inactive area of the SiPM, the footprint of these lines was minimized in the design.

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The active area of pixels is covered by an anti-reflection coating which was tuned for the wavelength of 500 nm. As shown in figure 1(a), STI is used for isolating electrically the neighbouring pixels. For junction isolation, the N^+ regions of two pixels are electrically isolated by a P^+ layer (Figure 1(b)). The geometric efficiencies for 10 µm × 10 µm and 50 µm × 50 µm pixel size SiPMs were about 20% and 75% respectively. The fill factor for the SiPM was lower by about 12% in the junction isolation case compared to the STI isolation case due to increased spacing between the isolation implant and pixel N^+ edge. Depending on the pixel size and geometric area, the total number of pixels in the SiPMs varied from a few hundred to several thousands. The design rules for the mask design of SiPM were adapted from the critical process parameters and capability of process equipment. The full process flow was implemented using an eleven mask process the details of which are presented in the next section.

3 SiPM fabrication process development

SiPMs were fabricated on a P^{++} doped wafer with a P-type epitaxial layer. A custom process sequence based on the 180 nm CMOS process flow was designed for the fabrication of SiPMs. The process flow typically consisted of about 100 process steps with 20 inline metrological and inspection steps for process control. Silicon wafers of diameter of 8″ and with a 4 µm P-type epitaxial layer (8–10 Ω-cm) were used as starting wafers for the process development.

The key target parameters for the SiPM devices were breakdown voltage (V_{BD}) of the SiPM and the quenching resistance, the latter determining the recovery time of the output response. The fabrication of the SiPMs was carried out using a complex process sequence involving the following main process steps:

i. Oxidation cycles for field oxidation, screen oxidation.

ii. Diode P-well implant and drive-in.

iii. STI formation in the case of STI-isolation.

iv. Polysilicon deposition and implant for polysilicon resistors.

v. N^+ and P^+ implantation and activation anneal for diode and poly contacts.

vi. Dielectric deposition for laying the Al metal lines.

vii. Al deposition for connecting lines and contacts.

viii. Passivation for the complete SiPM chip.

ix. ARC window etch over active area of pixels and ARC deposition.

x. Pad etch and alloying.

All the steps mentioned above involved subsequent photolithography cycles for patterning various layers. By maintaining the same thermal budget, the process sequence was designed in such a way that the photodiode pixels and high-resistance polysilicon modules exhibited the same electrical parameters (V_{bd} and R_{poly}) in the integrated process employing junction and STI isolation. Though the fill factor for the SiPM with junction isolation case was lower, the process of junction isolation

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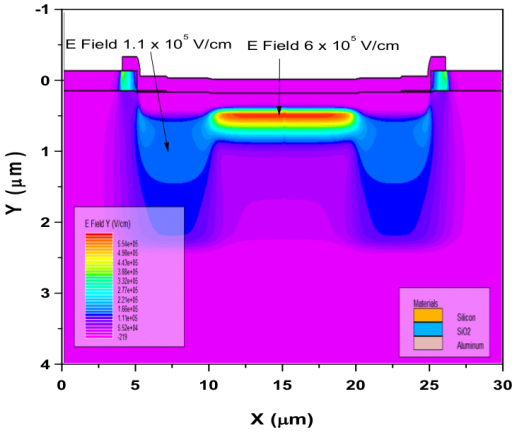

Figure 2 (a). Two dimensional cross section of the SiPM pixel showing high electric field avalanche region in the centre.

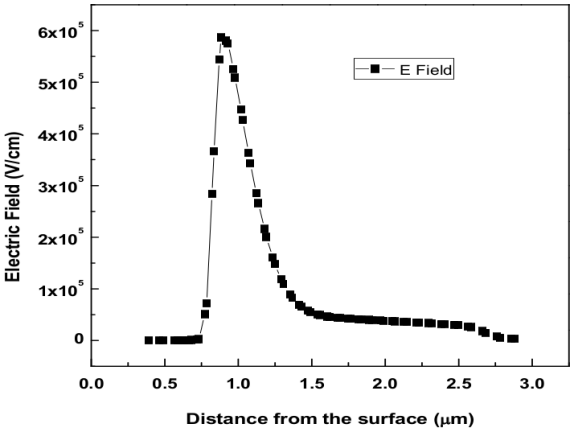

Figure 2 (b). Electric field profile in the avalanche region. The peak electric field in the centre of the pixel is about 6×10^6 V/cm.

was simpler than the STI isolation. Hence the tuning of main photodiode region was initially done using the design with junction isolation. After the optimization of the main diode region, the process flow for STI isolation was implemented.

Technology Computer Aided Design (TCAD) tools were used for device and process simulations so as to finalize the initial process parameters, particularly for the optimization of implant process conditions which were used for the P-well and pixel isolation. The typical device cross section generated using device simulation is shown in figure 2(a). This device cross section was generated using a process simulator in which all the steps were virtually executed. The high electric field avalanche region can be observed under the N^+/P-well diode without a corner breakdown due to the virtual guard ring region (figure 2(b)). The process was simulated for different N^+ and P-well implants and drive in parameters for optimization of the process. Figure 3 presents the simulated I-V characteristics for the pixel. The I-V characteristics indicates breakdown at ~21 V. By tuning the implant parameters for the N^+ and P-well regions, the desired V_{BD} can be realized. The targeted value of 300–500 kΩ for R_{poly} was achieved through ex-situ doping of polysilicon using boron implant. The implant dose was optimized through various short loop experiments, first on blanket wafers, followed by further fine tuning of implant dose as required for the narrow line width (0.5 µm) used in the design. It was found that, for small widths of poly (< 2 µm), the dose required is significantly higher than that required for wider polysilicon lines. Various P-well implant conditions (dose and energy) were implemented during the process engineering loops for the analysis and for final selection of P-well process parameters.

The edge breakdown of the N^+/P-epi junction was simulated to estimate the corner breakdown voltage as it was required to have a sufficient margin between edge breakdown and centre pixel breakdown voltage. The simulated edge breakdown voltages for different isolation (channel stop) implant conditions are presented in figure 4.

It was observed that for lower spacing, the edge breakdown voltage critically depends on the dose, and also the spacing of the channel stop implants from N^+ edge of the pixel. Separate diode test structures with layout splits in guard ring spacing (N^+ to P-well), as well as to adjacent field

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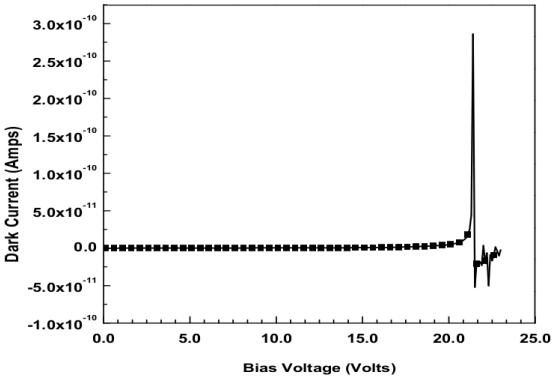

Figure 3. Simulated I-V characteristics of a pixel showing breakdown at about 21 V.

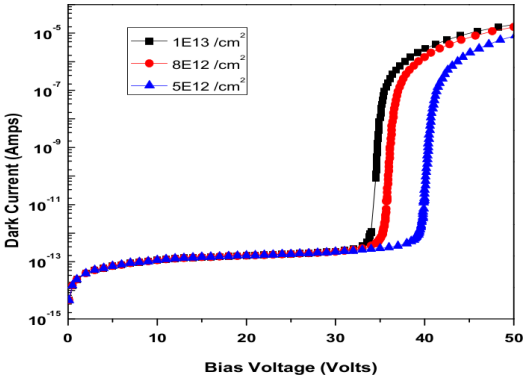

Figure 4. Simulated edge breakdown characteristics of N^+/P-epi junction showing breakdown at different voltages depending upon the channel stop implant parameters.

implant for channel stop (boron) were analyzed to study the breakdown characteristics of edge diode present in the pixel (N^+/P-epi junction). Edge breakdown voltage of N^+/P-epi junction was sensitive to dose and spacing of channel-stop implants in case of STI isolation case. Premature breakdown of edge diode affecting the functionality of SiPM was noticed during the initial device lots of STI-SiPMs. A novel implementation of channel-stop implants was used to avoid the premature breakdown of the device. Instead of selective implantation through a dedicated photo masking step after active area oxide-CMP, quad-implant (tilt = 7, rotation = 0, 90, 180, 275) was done in the trench regions through pad oxide/SiN as a hard mask. The self-alignment of this implant to trench increases effective space margin to N^+, and hence the edge breakdown voltage.

SiPMs fabricated using the above approach yielded 27 V edge breakdown with 5 V margin to the centre breakdown voltage. Using the final process with tuned process parameters, SiPMs with low dark currents and V_{BD} of about 22 V were realized. The SiPMs from the final process lot were packaged on Lead-Less Chip Carriers (LCC) for characterization. The photograph of the SiPM chip with 50 µm × 50 µm pixel size is shown in figure 5. Figure 6(a) and (b) show packaged SiPMs of 3 mm × 3 mm and 1.5 mm × 1.5 mm active areas. After Al wire bonding, the SiPM chips were covered with an optically transparent epoxy which allowed mechanical protection without preventing the external photons to reach the SiPM front surface.

4 Performance of SiPMs

The fabricated SiPMs were first tested using I-V characteristics for the measurement of dark current and breakdown voltage. An automated setup comprising a picoammeter with a programmable voltage source was used for these measurements. The SiPM was housed in a dark box to prevent the generation of charge carriers due to external light. The breakdown voltages were independent of isolation technique used as they were mainly decided by the doping of N^+/P-well region which was the same in both devices. Typical reverse characteristics of the SiPMs are presented for pixel size of 50 µm × 50 µm in figure 7 for SiPMs with STI isolation. As can be seen from figure 7, the

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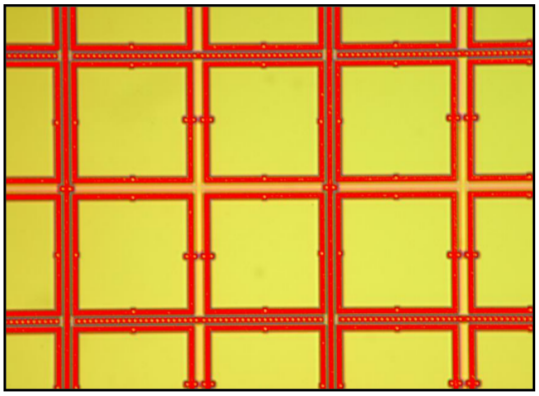
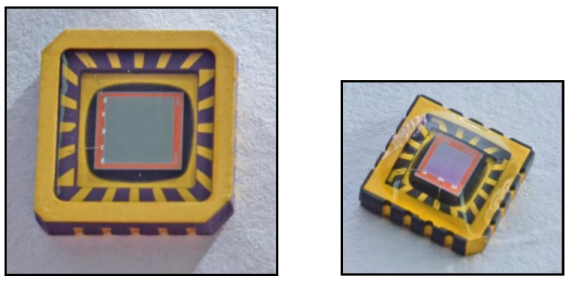


Figure 5. Photograph of fabricated SiPM chip taken with an optical microscope.



(a) **(b)**

Figure 6. Packaged SiPMs; (a) 3 mm × 3 mm active area, (b) 1.5 mm × 1.5 mm active area.

dark currents are very low and the breakdown is at about 22.0 V. The dark current is also observed to be proportional to the active area of the SiPM. Considering the active areas, the dark current of the SiPM with 3 mm × 3 mm active area is expected to be higher by a factor of 4 than the dark current of SiPM with active area of 1.5 mm × 1.5 mm. The measured factor from the data plotted in figure 7 is 4.72. The R_{poly} value has been measured to be about 500 kΩ.

The measurement of breakdown voltages, dark currents and polysilicon resistors showed very good uniformity for SiPMs across the wafer. For several applications, SiPMs are operated at temperatures lower than the room temperatures. Also, for field applications such as radiation monitoring instruments, SiPMs are subjected to temperatures higher than room temperatures. Hence, the variation of V_{BD} with temperature was studied in a temperature range of −30°C to +60°C. The dark currents measured at different bias voltages and temperatures are plotted in figure 8. Due to electronic noise, the background current in the system was about 5×10^{-15} amperes. Hence, the dark current could be correctly measured only when the SiPM current exceeded this background current. Therefore at −30°C, the dark current data is plotted only for bias voltages above 18 V. As expected, V_{BD} decreases with decrease of temperature with a linear dependence. The linear fit to the plot of V_{BD} with temperature exhibits a slope of 2×10^{-2} V/°C with the coefficient of determination $R^2 = 1$.

The pulses in the absence of external photons (i.e. dark counts) were obtained using a fast amplifier of rise time of about 1 ns. The output pulses were stored in a digital oscilloscope of bandwidth of 2 GHz. Depending on the active area, number of pixels and over voltage, the dark counts varied from a MHz to few hundred kHz i.e. dark count rate is higher for high over voltages and pixel numbers. The typical dark counts observed for a 1.5 mm × 1.5 mm SiPM (676 pixels, pixel size of 50 µm × 50 µm) are shown in figure 9. At an overvoltage of 2 V, the dark count rate is about 60 kHz/mm^2. Based on the dark count rate at 0.5 p.e. and 1.5 p.e., the cross talk was measured as < 5%. The gain of the SiPM was measured as 2×10^6 at 1 V overvoltage. The SiPM response to light was verified using an external pulsed light source. The SiPM test system from CAEN was used for these measurements [24]. The SiPM was housed in a dark box and its response

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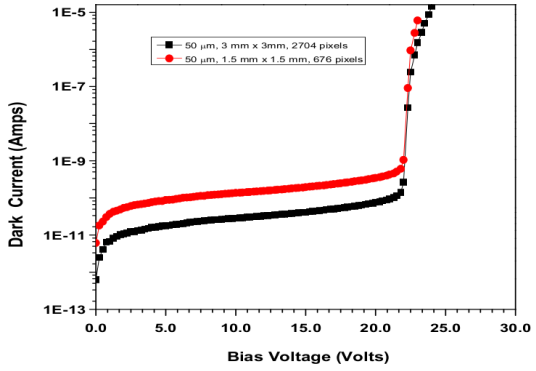

Figure 7. Dark current characteristics of SiPMs with STI isolation, pixel size — 50 µm × 50 µm, and active areas of 3 mm × 3 mm, 1.5 mm ×1.5 mm.

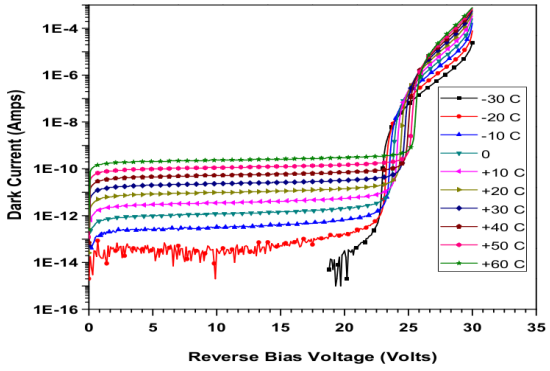

Figure 8. Variation of $V_{BD}$with temperature. As expected, V_{BD} decreases with temperature.

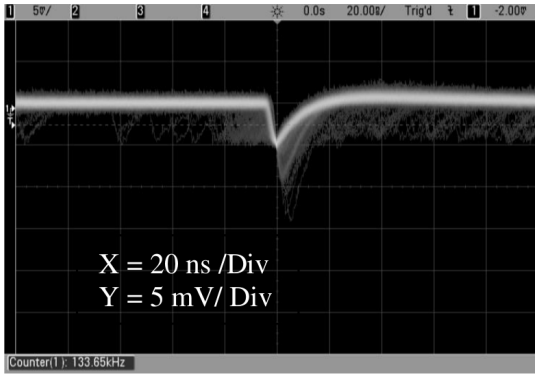

Figure 9. Dark counts observed on a DSO for a SiPM of active area 1.5 mm × 1.5 mm (676 pixels, pixel size of 50 µm × 50 µm). At 0.5 p. e., the dark count rate is about 133 kHz.

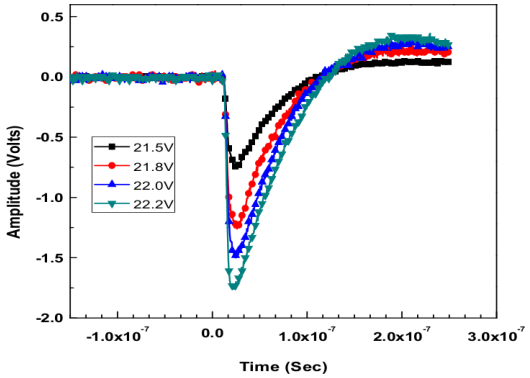

Figure 10. Response of a SiPM to external light photons at different bias voltages. The SiPM pulse width is about 100 ns. The amplitude of output pulse increases with bias voltage.

to external light was measured with an ultrafast LED driver (SP5601). The output of the SiPM was amplified using a fast amplifier. The LED light was guided very close to the SiPM surface using an optical fiber. The measured output pulse in synchronous with the LED trigger at different bias voltages, but for a fixed light intensity are plotted in figure 10 for a 3 mm × 3 mm SiPM with 50 µm pixel size. The output of the amplifier was AC coupled resulting in the overshoot of a pulse which is more pronounced at higher pulse heights. It can be observed that the SiPM pulse width is about 100 ns. As expected, the magnitude of output pulse increases with bias voltage. Higher bias voltage results in higher electric field in the avalanche region causing increase in the avalanche gain.

The SiPM output response was also studied for a fixed bias voltage, but different light intensities with the same system. The LED driver (SP5601) provided linear increase of light intensity using the light intensity setting. The SiPM pulses were amplified using the CAEN power supply-amplification unit (SP5600). The amplifier output pulses were digital processed for charge to digital conversion with 250 MS/s digitizer ((DT5720A). The histogram of number of counts vs ADC channel number

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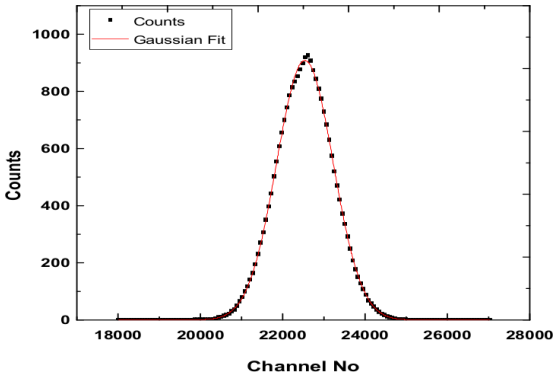

Figure 11 (a). Histogram of counts with ADC Channel No (equivalent to charge) obtained at a fixed light intensity (setting 7). SiPM area 3.0 mm × 3.0 mm, pixel size of 50 µm × 50 µm. The operating voltage was 22.5 V.

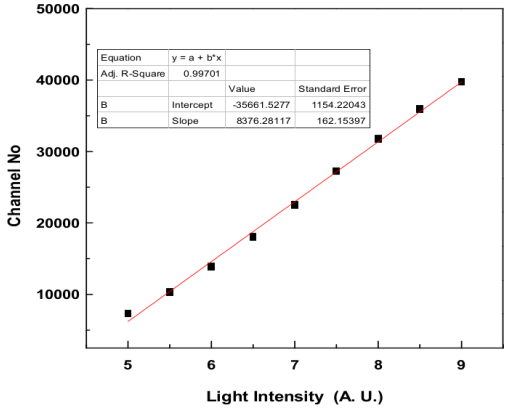

Figure 11 (b). The plot showing linearity of SiPM response with light intensity. The peak channel No of histograms obtained with different light intensities (as shown in figure 11(a)) are plotted at different settings of the LED driver.

(representing the integrated charge) was obtained for each light intensity. Each acquired spectrum (counts vs ADC channel No) was fitted to the Gaussian function for obtaining the peak channel number (figure 11(a)). The peak channel numbers are plotted with light intensities in figure 11(b). As can be seen, the SiPM response shows very good linearity with light intensity, i.e. the estimated coefficient of determination R^2 is 0.997.

Based on test results presented in this paper, a comparison of various parameters of developed SiPMs with commercially available SiPMs from M/S ON Semiconductor (previously known as SensL) is presented in table 1. It is to be noted that the C-Series SiPMs are specifically manufactured for low dark-count rate combined with a high PDE [25].

5 Conclusions and outlook

A generic technology for SiPMs has been developed using a 180 nm CMOS process line in India. With a lower feature size of 180 nm, very narrow widths of about 0.5 µm can be used for various layers. This allows to reduce the inactive area of the SiPM. The fabrication process was optimized by targeting the critical process parameters which decide the operating voltage and dark current. The SiPMs demonstrated to have the desired performance in terms of dark current, geometric efficiency, gain, dark count rate and cross talk. Initial measurements with LED light shows good linearity of SiPM response with light intensity. Other parameters such as photon detection efficiency, response to different wavelengths of light, etc., will be further studied. As the main aim of this work was technology development, some of the design rules used for designing the SiPMs were not very tight. Based on the present technology, the next version of SiPMs will be made by exploiting the tighter design rules of modules such as contact and metallization to achieve the best possible geometric efficiency. Since SiPMs are very suitable for compact handheld radiation monitoring instruments, SiPM response will be further investigated with different types of scintillators.

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Table 1. Comparison of various parameters of developed SiPMs with commercial SiPMs from ON Semiconductor.

S No	Sensitive area — 3 mm × 3 mm, Pixel size — 50 µm × 50 µm		
		On Semiconductor C-Series 30050	Present work
1	Breakdown voltage	24.2 V	22.0 V
2	No of pixels	2668	2704
3	Fill factor	72%	75%
5	Gain	6×10^6 @ V_{BD} +2.5 V	$\sim 2 \times 10^6$ @ V_{BD} +1.0 V
6	Temperature dependence of V_{BD}	21.5 mV/°C	20.0 mV/°C
7	Capacitance (cathode - anode)	920 pF	1000 pF
8	Dark count rate	@ V_{BD} +2.5 V Typ. 300 kHz	@ V_{BD} +2.0 V Typ. 500 kHz (at 0.5 p.e.)
9	Crosstalk	@ V_{BD} +2.5 V 10%	@ V_{BD} +2.0 V < 5%

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